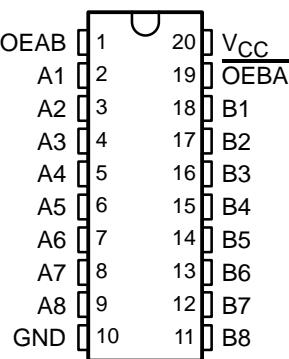
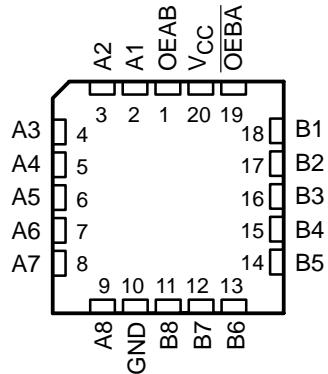


- Operating Voltage Range of 4.5 V to 5.5 V
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical $t_{pd} = 11$ ns
- ± 6 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- Inputs Are TTL-Voltage Compatible
- Lock Bus-Latch Capability
- True Logic
- High-Current 3-State Outputs Can Drive Up To 15 LSTTL Loads

SN54HCT623 . . . J OR W PACKAGE
SN74HCT623 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HCT623 . . . FK PACKAGE
(TOP VIEW)



description/ordering information

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation allows for maximum flexibility in timing.

The 'HCT623 devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the output-enable (OEAB and \overline{OEBA}) inputs.

The output-enable inputs disable the device so that the buses are effectively isolated. The dual-enable configuration gives the transceivers the capability to store data by simultaneously enabling OEAB and \overline{OEBA} . Each output reinforces its input in this transceiver configuration. When both OEAB and \overline{OEBA} are enabled and all other data sources to the two sets of bus lines are in the high-impedance state, both sets of bus lines (16 total) remain at their last states. The 8-bit codes appearing on the two sets of buses are identical.

To ensure the high-impedance state during power up or power down, \overline{OEBA} should be tied to V_{CC} through a pullup resistor and OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

ORDERING INFORMATION

TA	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube	SN74HCT623N	SN74HCT623N
	SOIC – DW	Tube	SN74HCT623DW	HCT623
-55°C to 125°C	CDIP – J	Tube	SNJ54HCT623J	SNJ54HCT623J
	CFP – W	Tube	SNJ54HCT623W	SNJ54HCT623W
	LCCC – FK	Tube	SNJ54HCT623FK	SNJ54HCT623FK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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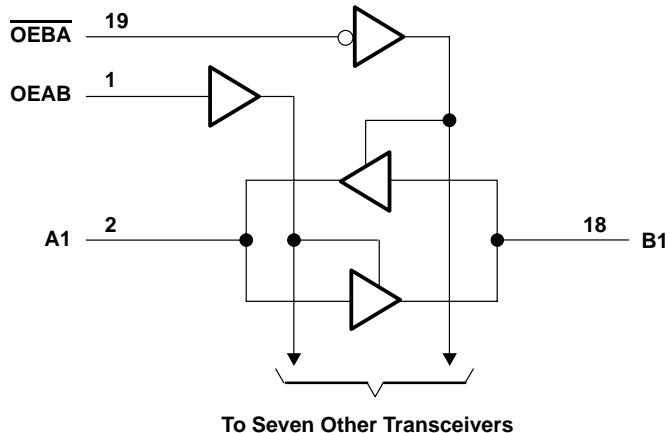
SN54HCT623, SN74HCT623 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCLS016C – MARCH 1984 – REVISED MARCH 2003

FUNCTION TABLE

INPUTS		OPERATION
OEBA	OEAB	
L	L	B data to A bus
H	H	A data to B bus
H	L	Isolation
L	H	B data to A bus, A data to B bus

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 35 mA
Continuous current through V_{CC} or GND	± 70 mA
Package thermal impedance, θ_{JA} (see Note 2): DW package	58°C/W
N package	69°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			SN54HCT623			SN74HCT623			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 4.5 V to 5.5 V	2			2			V
V _{IL}	Low-level input voltage	V _{CC} = 4.5 V to 5.5 V			0.8			0.8	V
V _I	Input voltage		0	V _{CC}		0	V _{CC}		V
V _O	Output voltage		0	V _{CC}		0	V _{CC}		V
t _t	Input transition (rise and fall) time				500			500	ns
T _A	Operating free-air temperature		-55	125		-40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	T _A = 25°C			SN54HCT623		SN74HCT623		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -20 μA	4.5 V	4.4	4.499		4.4		4.4		V
		I _{OH} = -6 mA		3.98	4.3		3.7		3.84		
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
		I _{OL} = 6 mA			0.17	0.26		0.4		0.33	
I _I	OEAB or OEBA	V _I = V _{CC} or 0	5.5 V		±0.1	±100		±1000		±1000	nA
I _{OZ}	A or B	V _O = V _{CC} or GND	5.5 V		±0.01	±0.5		±10		±5	μA
I _{CC}		V _I = V _{CC} or 0, I _O = 0	5.5 V			8		160		80	μA
ΔI _{CC} [†]		One input at 0.5 V or 2.4 V, Other inputs at 0 or V _{CC}	5.5 V		1.4	2.4		3		2.9	mA
C _i	OEAB or OEBA		4.5 V to 5.5 V		3	10		10		10	pF

[†]This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HCT623		SN74HCT623		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	B or A	4.5 V		15	22		33		28	ns
			5.5 V		13	20		30		25	
t _{en}	OEBA	A	4.5 V		30	42		63		53	ns
			5.5 V		23	38		57		48	
t _{dis}	OEBA	A	4.5 V		18	30		45		38	ns
			5.5 V		16	28		42		35	
t _{en}	OEAB	B	4.5 V		30	42		63		53	ns
			5.5 V		23	38		57		48	
t _{dis}	OEAB	B	4.5 V		18	30		45		38	ns
			5.5 V		16	28		42		35	
t _t		A or B	4.5 V		9	12		18		15	ns
			5.5 V		8	11		16		14	

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



**SN54HCT623, SN74HCT623
OCTAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS**

SCLS016C – MARCH 1984 – REVISED MARCH 2003

switching characteristics over recommended operating free-air temperature range, $C_L = 150 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HCT623	SN74HCT623	UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	B or A	4.5 V	18	38	58	47	42	ns
			5.5 V	11	34	52	47	42	
t_{en}	OEBA	A	4.5 V	36	59	89	74	67	ns
			5.5 V	30	53	80	74	67	
	OEAB	B	4.5 V	36	59	89	74	67	ns
			5.5 V	30	53	80	74	67	
t_t		A or B	4.5 V	17	42	63	53	48	ns
			5.5 V	14	38	57	48	42	

operating characteristics, $T_A = 25^\circ\text{C}$

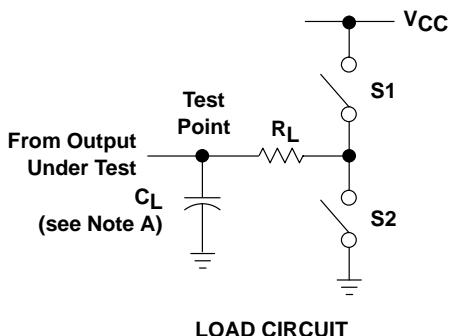
PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per transceiver	No load	40	pF

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

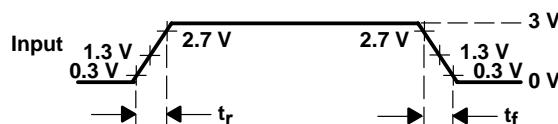


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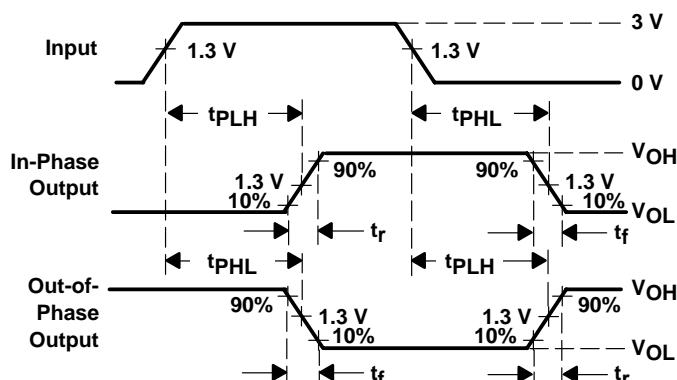
PARAMETER MEASUREMENT INFORMATION



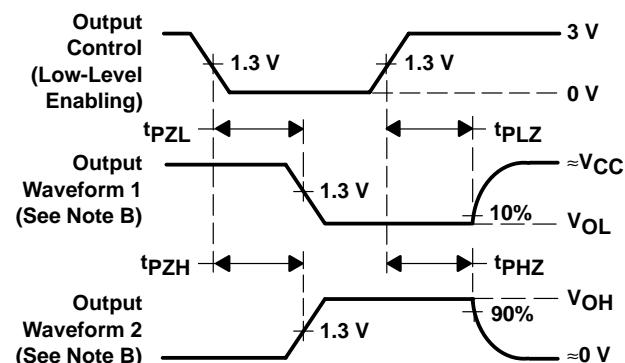
PARAMETER	R_L	C_L	S1	S2
t_{en}	1 k Ω	50 pF or 150 pF	Open	Closed
			Closed	Open
t_{dis}	1 k Ω	50 pF	Open	Closed
			Closed	Open
t_{pd} or t_t	—	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 D. The outputs are measured one at a time with one input transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74HCT623N	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HCT623N
SN74HCT623N.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HCT623N

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

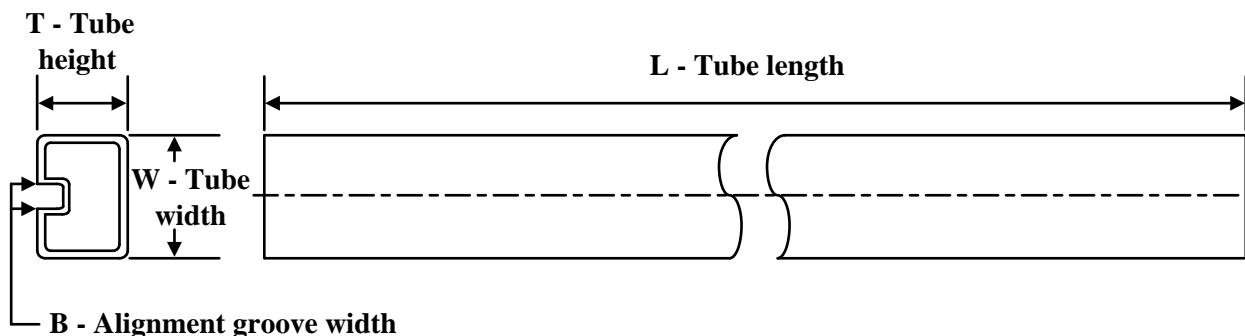
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TUBE


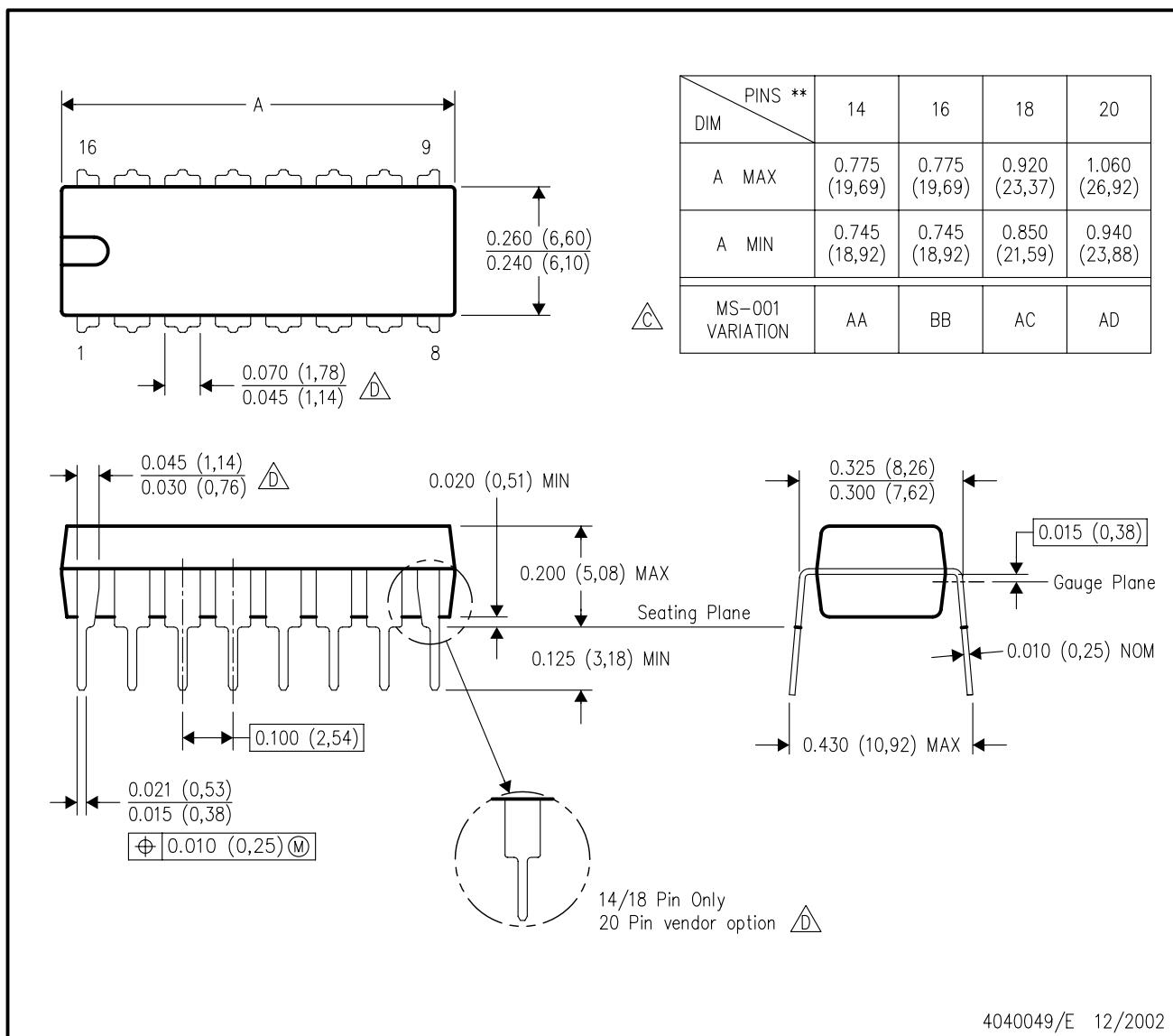
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μ m)	B (mm)
SN74HCT623N	N	PDIP	20	20	506	13.97	11230	4.32
SN74HCT623N.A	N	PDIP	20	20	506	13.97	11230	4.32

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

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