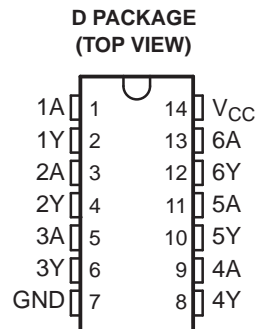


FEATURES

- **Controlled Baseline**
 - One Assembly Site
 - One Test Site
 - One Fabrication Site
- **Extended Temperature Performance of -55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product Change Notification**
- **Qualification Pedigree ⁽¹⁾**
- **Operates From 1.65 V to 3.6 V**
- **Inputs and Open Drain Outputs Accept Voltages up to 5.5 V**
- **Max t_{pd} of 3.7 ns at 3.3 V**
- **I_{off} Supports Partial Power Down Mode Operation**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.



DESCRIPTION/ORDERING INFORMATION

The SN74LVC06A is a hex inverter buffer/driver that is designed for 1.65-V to 3.6-V V_{CC} operation.

The outputs of the SN74LVC06A device are open drain and can be connected to other open-drain outputs to implement active low wired OR or active high wired AND functions. The maximum sink current is 24 mA.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V system environment.

This device is fully specified for partial power down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

**FUNCTION TABLE
(EACH INVERTER)**

INPUT A	OUTPUT Y
H	L
L	H

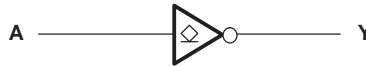


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SN74LVC06A-EP HEX INVERTER BUFFER/DRIVER WITH OPEN DRAIN OUTPUTS

SCAS832A–APRIL 2007–REVISED MAY 2007

LOGIC DIAGRAM, EACH INVERTER (POSITIVE LOGIC)



ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-55°C to 125°C	SOIC – D	Reel of 2500	SN74LVC06AMDREP	LVC06AM

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
- (2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
V _{CC}	Supply voltage range	-0.5	6.5	V	
V _I	Input voltage range ⁽²⁾	-0.5	6.5	V	
V _O	Output voltage range	-0.5	6.5	V	
I _{IK}	Input clamp current	V _I < 0 V		-50	mA
I _{OK}	Output clamp current	V _O < 0 V		-50	mA
I _O	Continuous output current			±50	mA
Continuous current through V _{CC} or GND				±100	mA
θ _{JA}	Package thermal impedance ⁽³⁾			86	°C/W
T _{stg}	Storage temperature range	-65	150	°C	
P _{tot}	Power dissipation ⁽⁴⁾	T _A = -55°C to 125°C		500	mW

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.
- (4) Above 70°C the value of P_{tot} derates linearly with 8 mW/K.

Recommended Operating Conditions⁽¹⁾

		T _A = 25°C		-55°C to 125°C		UNIT	
		MIN	MAX	MIN	MAX		
V _{CC}	Supply voltage	Operating	1.65	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		1.7		
		V _{CC} = 2.7 V to 3.6 V	2		2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}		0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	0.7		0.7		
		V _{CC} = 2.7 V to 3.6 V	0.8		0.8		
V _I	Input voltage	0	5.5	0	5.5	V	
V _O	Output voltage	0	5.5	0	5.5	V	

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Recommended Operating Conditions (continued)

		$T_A = 25^\circ\text{C}$		$-55^\circ\text{C to } 125^\circ\text{C}$		UNIT
		MIN	MAX	MIN	MAX	
I_{OL}	Low-level output current	$V_{CC} = 1.65\text{ V}$		4		4
		$V_{CC} = 2.3\text{ V}$		8		8
		$V_{CC} = 2.7\text{ V}$		12		12
		$V_{CC} = 3\text{ V}$		24		24

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			$-55^\circ\text{C to } 125^\circ\text{C}$		UNIT
			MIN	TYP	MAX	MIN	MAX	
V_{OL}	$I_{OL} = 100\ \mu\text{A}$	1.65 V to 3.6 V			0.1		0.3	V
	$I_{OL} = 4\text{ mA}$	1.65 V			0.24		0.6	
	$I_{OL} = 8\text{ mA}$	2.3 V			0.3		0.75	
	$I_{OL} = 12\text{ mA}$	2.7 V			0.4		0.6	
	$I_{OL} = 24\text{ mA}$	3 V			0.55		0.8	
I_I	$V_I = 5.5\text{ V or GND}$	3.6 V			± 1		± 20	μA
I_{off}	V_I or $V_O = 5.5\text{ V}$	0 V			± 1		± 20	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			1		40	μA
ΔI_{CC}	One input at $V_{CC} - 0.6\text{ V}$, Other inputs at V_{CC} or GND	2.7 V to 3.6 V			500		5000	μA
C_I	$V_I = V_{CC}$ or GND	3.3 V		5				pF

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

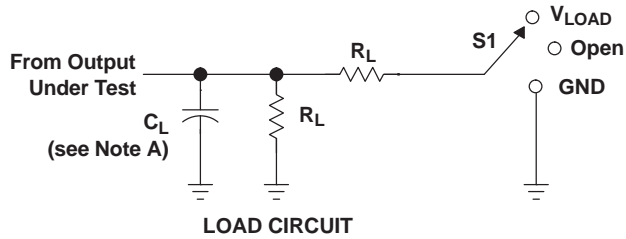
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$-55^\circ\text{C to } 125^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	$1.8\text{ V} \pm 0.15\text{ V}$	1.4	3	5.1	1.4	7.6	ns
			$2.5\text{ V} \pm 0.2\text{ V}$	1	1.9	2.8	1	4	
			2.7 V	1	2.4	3.7	1	5	
			$3.3\text{ V} \pm 0.3\text{ V}$	1	2.2	3.5	1	5	

Operating Characteristics

$T_A = 25^\circ\text{C}$

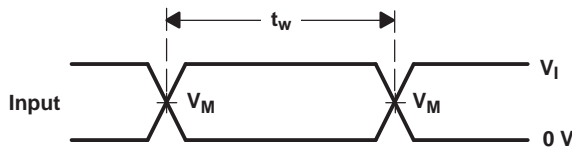
PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer/driver	f = 10 MHz	1.8 V	2.1	pF
			2.5 V	2.3	
			3.3 V	2.5	

PARAMETER MEASUREMENT INFORMATION

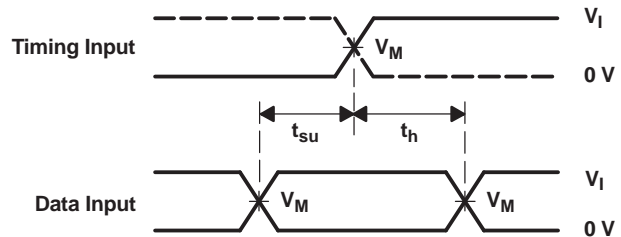


TEST	S1
t_{pZL} (see Notes E and F)	V_{LOAD}
t_{pLZ} (see Notes E and G)	V_{LOAD}
t_{PHZ}/t_{PZH}	V_{LOAD}

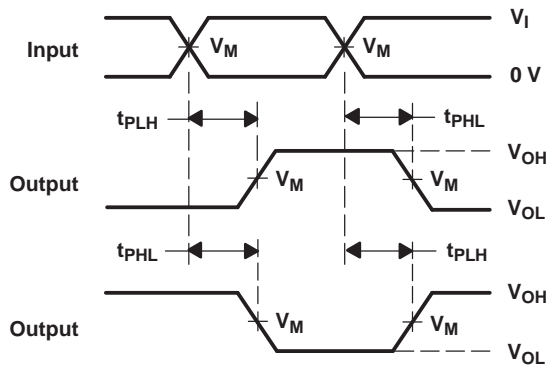
V_{CC}	INPUT		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V



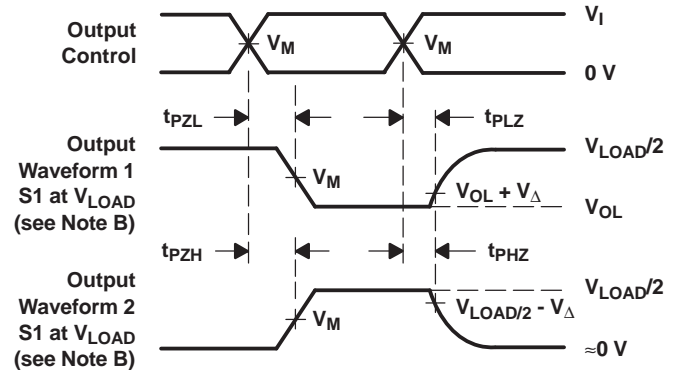
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
D. The outputs are measured one at a time, with one transition per measurement.
E. Since this device has open-drain outputs, t_{pLZ} and t_{pZL} are the same as t_{pD} .
F. t_{pZL} is measured at V_M .
G. t_{pLZ} is measured at $V_{OL} + V_{\Delta}$.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC06AMDREP	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LC06AM
V62/06661-01XE	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LC06AM

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74LVC06A-EP :

- Catalog : [SN74LVC06A](#)

- Automotive : [SN74LVC06A-Q1](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC06AMDREP	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC06AMDREP	SOIC	D	14	2500	353.0	353.0	32.0



D0014A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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