

## SN74LVC1G04 Single Inverter Gate

### 1 Features

- Available in the ultra-small 0.64mm<sup>2</sup> package (DPW) with 0.5mm pitch
- Supports 5V V<sub>CC</sub> operation
- Inputs accept voltages up to 5.5V allowing down translation to V<sub>CC</sub>
- Maximum t<sub>pd</sub> of 3.3ns at 3.3V
- Low power consumption, 10μA maximum I<sub>CC</sub>
- ±24mA output drive at 3.3V
- I<sub>off</sub> supports live-insertion, partial-power-down mode, and back-drive protection
- Latch-up performance exceeds 100mA per JESD 78, Class II
- ESD protection exceeds JESD 22
  - 2000V human-body model (A114-A)
  - 200V machine model (A115-A)
  - 1000V charged-device model (C101)

### 2 Applications

- AV receiver
- Audio dock: portable
- Blu-ray player and home theater
- Embedded PC
- MP3 player/recorder (portable audio)
- Personal Digital Assistant (PDA)
- Power: telecom/server AC/DC supply: single controller: analog and digital
- Solid State Drive (SSD): client and enterprise
- TV: LCD/digital and high-definition (HDTV)
- Tablet: enterprise
- Video analytics: server
- Wireless headset, keyboard, and mouse

### 3 Description

This single inverter gate is designed for 1.65V to 5.5V V<sub>CC</sub> operation.

The SN74LVC1G04 device performs the Boolean function  $Y = \bar{A}$ .

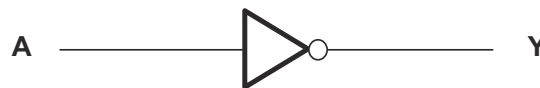
The CMOS device has high output drive while maintaining low static power dissipation over a broad V<sub>CC</sub> operating range.

The SN74LVC1G04 device is available in a variety of packages, including the ultra-small DPW package with a body size of 0.8mm × 0.8mm.

#### Package Information

DEVICE NAME	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>	BODY SIZE (NOM) <sup>(3)</sup>
SN74LVC1G04	DBV (SOT-23, 5)	2.9mm × 2.8mm	2.9mm × 1.6mm
	DCK (SC70, 5)	2.0mm × 2.1mm	2.0mm × 1.25mm
	DPW (X2SON, 5)	0.8mm × 0.8mm	0.8mm × 0.8mm
	DRL (SOT-5X3, 5)	1.6mm × 1.6mm	1.6mm × 1.2mm
	DRY (USON, 6)	1.45mm × 1.0mm	1.45mm × 1.0mm
	DSF (X2SON, 6)	1.0mm × 1.0mm	1.0mm × 1.0mm
	YZP (DSBGA, 5)	1.75mm × 1.75mm	1.75mm × 1.25mm
	YZV (DSBGA, 4)	1.25mm × 1.25mm	1.25mm × 1.25mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) The body size (length × width) is a nominal value and does not include pins.



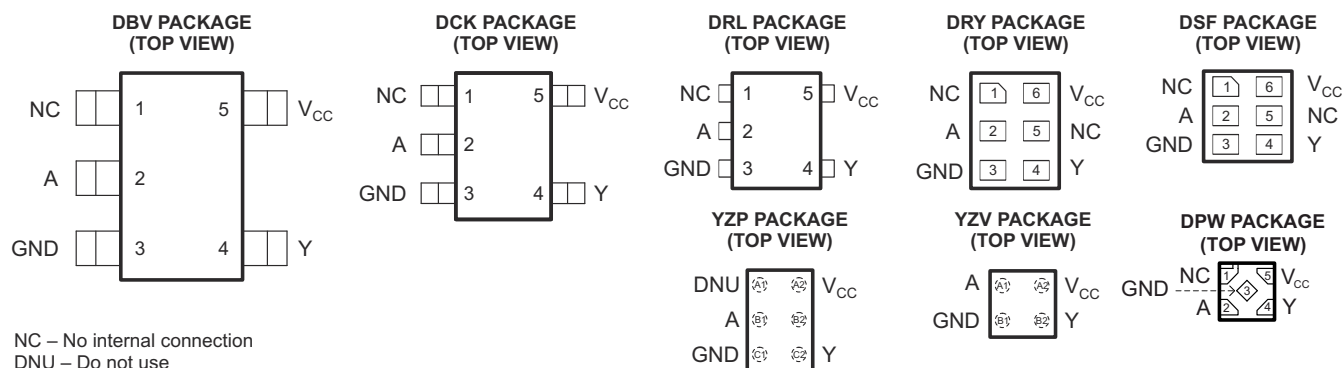
**Simplified Schematic**



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## 4 Pin Configuration and Functions



### Pin Functions

PIN						DESCRIPTION
NAME	DBV, DCK, DRL	DSF, DRY	YZP	YZV	DPW	
NC	1	1, 5	A1, B2	–	1	No connect
A	2	2	B1	A1	2	Input
GND	3	3	C1	B1	3	Ground
Y	4	4	C2	B2	4	Output
V <sub>CC</sub>	5	6	A2	A2	5	Power terminal

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	−0.5	6.5	V
$V_I$	Input voltage range	−0.5	6.5	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	−0.5	6.5	V
$V_O$	Voltage range applied to any output in the high or low state <sup>(2) (3)</sup>	−0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$		−50 mA
$I_{OK}$	Output clamp current	$V_O < 0$		−50 mA
$I_O$	Continuous output current		±50	mA
	Continuous current through $V_{CC}$ or GND		±100	mA
$T_{stg}$	Storage temperature	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of  $V_{CC}$  is provided in the *Recommended Operating Conditions* table.

### 5.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge		
	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

(1)			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65V to 1.95V	0.65 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3V to 2.7V	1.7		
		V <sub>CC</sub> = 3V to 3.6V	2		
		V <sub>CC</sub> = 4.5V to 5.5V	0.7 × V <sub>CC</sub>		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65V to 1.95V		0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3V to 2.7V		0.7	
		V <sub>CC</sub> = 3V to 3.6V		0.8	
		V <sub>CC</sub> = 4.5V to 5.5V		0.3 × V <sub>CC</sub>	
V <sub>I</sub>	Input voltage		0	5.5	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65V		–4	mA
		V <sub>CC</sub> = 2.3V		–8	
		V <sub>CC</sub> = 3V		–16	
				–24	
		V <sub>CC</sub> = 4.5V		–32	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65V		4	mA
		V <sub>CC</sub> = 2.3V		8	
		V <sub>CC</sub> = 3V		16	
				24	
		V <sub>CC</sub> = 4.5V		32	
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 1.8V ± 0.15V, 2.5V ± 0.2V		20	ns/V
		V <sub>CC</sub> = 3.3V ± 0.3V		10	
		V <sub>CC</sub> = 5V ± 0.5V		5	
T <sub>A</sub>	Operating free-air temperature		–40	125	°C

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

### 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74LVC1G04						UNIT
		DBV	DCK	DRL	DRY	YZP	DPW	
		5 PINS	5 PINS	5 PINS	6 PINS	5 PINS	4 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	357.1	371.0	243	439	130	340	°C/W
R <sub>θJCTop</sub>	Junction-to-case (top) thermal resistance	263.7	297.5	78	277	54	215	
R <sub>θJB</sub>	Junction-to-board thermal resistance	264.4	258.6	78	271	51	294	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	195.6	195.6	10	84	1	41	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	262.2	256.2	77	271	50	294	
R <sub>θJBot</sub>	Junction-to-case (bottom) thermal resistance	–	–	–	–	–	250	

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

## 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	–40°C to 85°C			RECOMMENDED –40°C to 125°C			UNIT
				MIN	TYP <sup>(1)</sup>	MAX	MIN	TYP	MAX	
V <sub>OH</sub>		I <sub>OH</sub> = –100μA	1.65V to 5.5V	V <sub>CC</sub> – 0.1			V <sub>CC</sub> – 0.1			V
		I <sub>OH</sub> = –4mA	1.65V	1.2			1.2			
		I <sub>OH</sub> = –8mA	2.3V	1.9			1.9			
		I <sub>OH</sub> = –16mA	3V	2.4			2.4			
		I <sub>OH</sub> = –24mA		2.3			2.3			
		I <sub>OH</sub> = –32mA	4.5V	3.8			3.8			
V <sub>OL</sub>		I <sub>OL</sub> = 100μA	1.65V to 5.5V	0.1			0.1			V
		I <sub>OL</sub> = 4mA	1.65V	0.45			0.45			
		I <sub>OL</sub> = 8mA	2.3V	0.3			0.3			
		I <sub>OL</sub> = 16mA	3V	0.4			0.4			
		I <sub>OL</sub> = 24mA		0.55			0.55			
		I <sub>OL</sub> = 32mA	4.5V	0.55			0.55			
I <sub>I</sub>	A input	V <sub>I</sub> = 5.5V or GND	0 to 5.5V	±5			±5			μA
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 5.5V	0	±10			±10			μA
I <sub>CC</sub>		V <sub>I</sub> = 5.5V or GND      I <sub>O</sub> = 0	1.65V to 5.5V	10			10			μA
ΔI <sub>CC</sub>		One input at V <sub>CC</sub> – 0.6V, Other inputs at V <sub>CC</sub> or GND	3V to 5.5V	500			500			μA
C <sub>i</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	3.3V	3.5			3.50			pF

(1) All typical values are at  $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$ .

## 5.6 Switching Characteristics, $C_L = 15pF$

over recommended operating free-air temperature range,  $C_L = 15pF$  (unless otherwise noted)

(see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−40°C to 85°C								UNIT
			V <sub>CC</sub> = 1.8V ± 0.15V		V <sub>CC</sub> = 2.5V ± 0.2V		V <sub>CC</sub> = 3.3V ± 0.3V		V <sub>CC</sub> = 5V ± 0.5V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	2	6.4	1	4.2	0.7	3.3	0.7	3.1	ns

## 5.7 Switching Characteristics, $C_L = 30pF$ or $50pF$ , –40°C to 85°C

over recommended operating free-air temperature range,  $C_L = 30pF$  or  $50pF$  (unless otherwise noted)

(see Figure 6-2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−40°C to 85°C								UNIT
			V <sub>CC</sub> = 1.8V ± 0.15V		V <sub>CC</sub> = 2.5V ± 0.2V		V <sub>CC</sub> = 3.3V ± 0.3V		V <sub>CC</sub> = 5V ± 0.5V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	3	7.5	1.4	5.2	1	4.2	1	3.7	ns

## 5.8 Switching Characteristics, $C_L = 15\text{pF}$ , $-40^\circ\text{C}$ to $125^\circ\text{C}$

over recommended operating free-air temperature range,  $C_L = 15\text{pF}$  (unless otherwise noted)  
(see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	-40°C to 125°C								UNIT
			V <sub>CC</sub> = 1.8V ± 0.15V		V <sub>CC</sub> = 2.5V ± 0.2V		V <sub>CC</sub> = 3.3V ± 0.3V		V <sub>CC</sub> = 5V ± 0.5V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	2	6.4	1	4.2	0.7	3.3	0.7	3.1	ns

## 5.9 Switching Characteristics, $C_L = 30\text{pF}$ or $50\text{pF}$ , $-40^\circ\text{C}$ to $125^\circ\text{C}$

over recommended operating free-air temperature range,  $C_L = 30\text{pF}$  or  $50\text{pF}$  (unless otherwise noted)  
(see [Figure 6-2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	-40°C to 125°C								UNIT
			V <sub>CC</sub> = 1.8V ± 0.15V		V <sub>CC</sub> = 2.5V ± 0.2V		V <sub>CC</sub> = 3.3V ± 0.3V		V <sub>CC</sub> = 5V ± 0.5V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	3	7.5	1.4	5.2	1	4.2	1	3.7	ns

## 5.10 Operating Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC} = 1.8\text{V}$	$V_{CC} = 2.5\text{V}$	$V_{CC} = 3.3\text{V}$	$V_{CC} = 5.0\text{V}$	UNIT
		TYP	TYP	TYP	TYP	
$C_{pd}$ Power dissipation capacitance	$f = 10\text{MHz}$	16	18	18	20	pF

## 5.11 Typical Characteristics

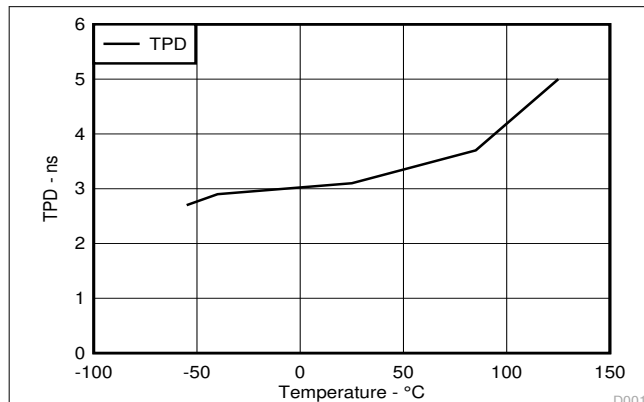


Figure 5-1. TPD Across Temperature at 3.3V  $V_{CC}$

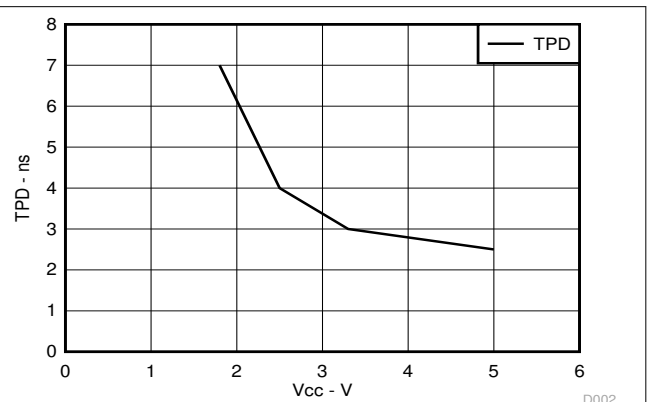
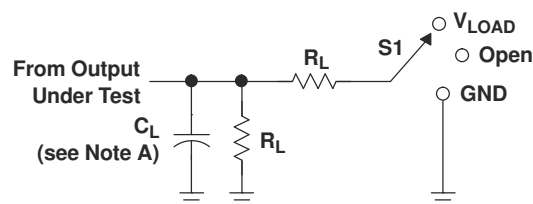


Figure 5-2. TPD Across  $V_{CC}$  at  $25^\circ\text{C}$

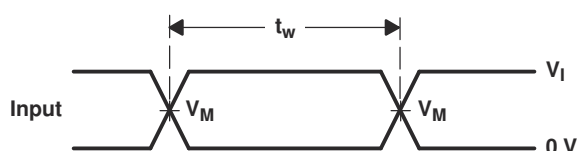
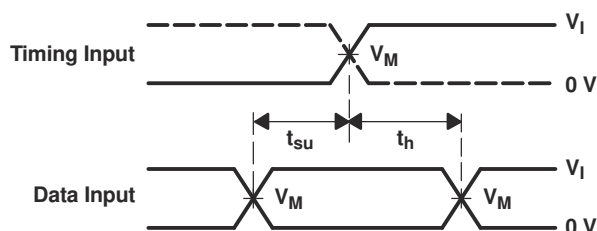
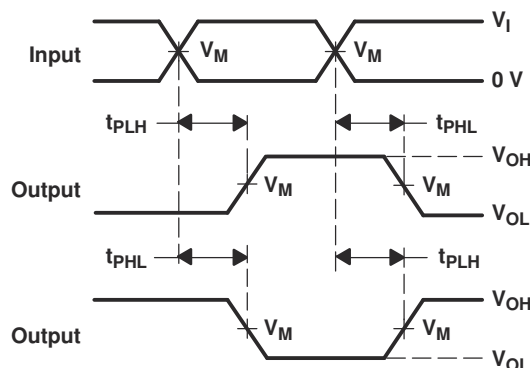
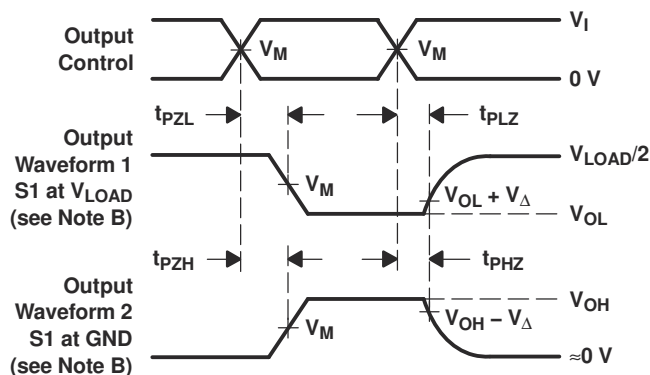
## 6 Parameter Measurement Information



LOAD CIRCUIT

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

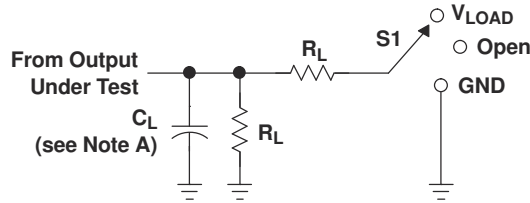
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M $\Omega$	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	15 pF	1 M $\Omega$	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	$V_{CC}$	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M $\Omega$	0.3 V

VOLTAGE WAVEFORMS  
PULSE DURATIONVOLTAGE WAVEFORMS  
SETUP AND HOLD TIMESVOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTSVOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms

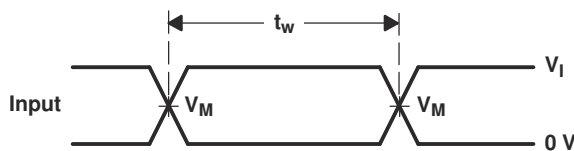




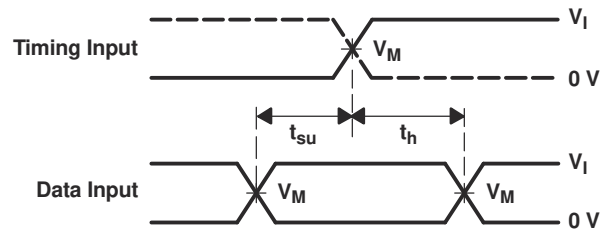
LOAD CIRCUIT

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

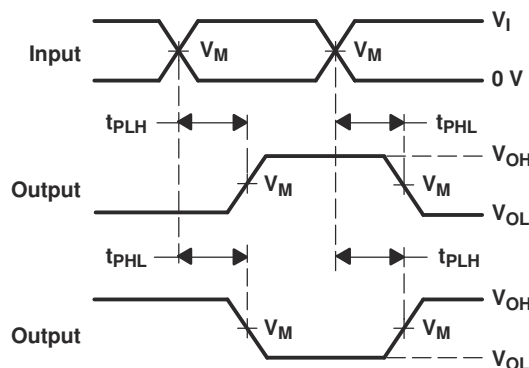
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	$V_{CC}$	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 $\Omega$	0.3 V



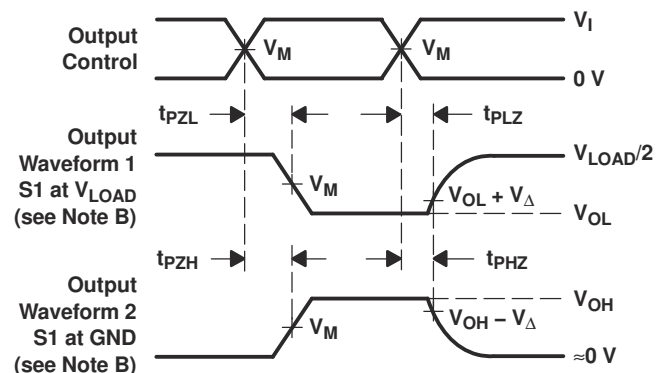
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
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LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\text{ }\Omega$ .  
D. The outputs are measured one at a time, with one transition per measurement.  
E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
H. All parameters and waveforms are not applicable to all devices.

Figure 6-2. Load Circuit and Voltage Waveforms

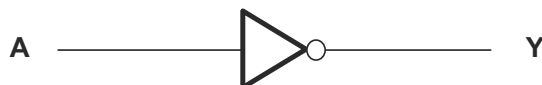
## 7 Detailed Description

### 7.1 Overview

The SN74LVC1G04 device contains inverter gate and performs the Boolean function  $Y = \bar{A}$ . This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The DPW package technology is a major breakthrough in IC packaging. Its tiny 0.64mm square footprint saves significant board space over other package options while still retaining the traditional manufacturing friendly lead pitch of 0.5mm.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

- Wide operating voltage range.
  - Operates from 1.65V to 5.5V.
- Allows down voltage translation.
- Inputs accept voltages to 5.5V.
- $I_{off}$  feature allows voltages on the inputs and outputs, when  $V_{CC}$  is 0V.

### 7.4 Device Functional Modes

Function Table

INPUT A	OUTPUT Y
H	L
L	H

## 8 Application and Implementation

### 8.1 Application Information Disclaimer

#### Note

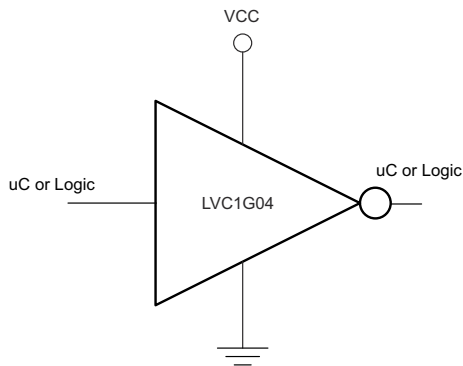
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.2 Application Information

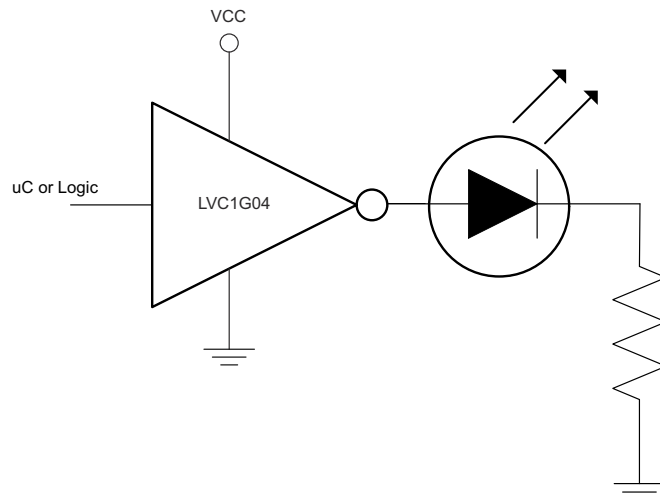
The SN74LVC1G04 is a high drive CMOS device that can be used for implementing inversion logic with a high output drive, such as an LED application. It can produce 24mA of drive current at 3.3V making it ideal for driving multiple outputs and good for high speed applications up to 100MHz. The inputs are 5.5V tolerant allowing it to translate down to  $V_{CC}$ .

### 8.3 Typical Application

Inverter Logic Function



Basic LED Driver



#### 8.3.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

#### 8.3.2 Detailed Design Procedure

##### 1. Recommended Input Conditions

- Rise time and fall time specs: See ( $\Delta t/\Delta V$ ) in the [Recommended Operating Conditions](#) table.
- Specified high and low levels: See ( $V_{IH}$  and  $V_{IL}$ ) in the [Recommended Operating Conditions](#) table.
- Inputs are overvoltage tolerant allowing them to go as high as ( $V_I$  max) in the [Recommended Operating Conditions](#) table at any valid  $V_{CC}$ .

##### 2. Recommend Output Conditions

- Load currents should not exceed ( $I_O$  max) per output and should not exceed total current (continuous current through  $V_{CC}$  or GND) for the part. These limits are located in the [Absolute Maximum Ratings](#) table.
- Outputs should not be pulled above  $V_{CC}$ .

### 8.3.3 Application Curves

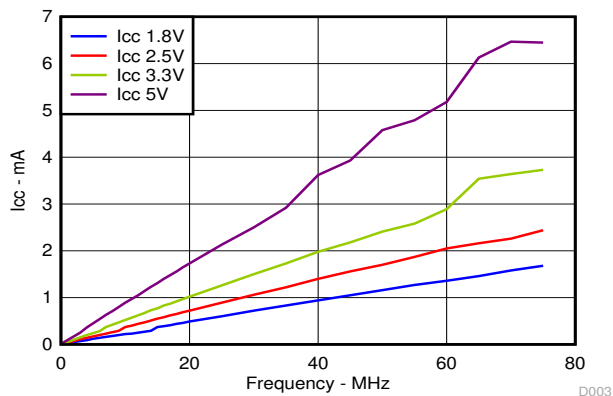


Figure 8-1. I<sub>CC</sub> vs Frequency

## 8.4 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each VCC pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1μF capacitor is recommended. If there are multiple VCC pins, then a 0.01μF or 0.022μF capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1μF and 1μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 8.5 Layout

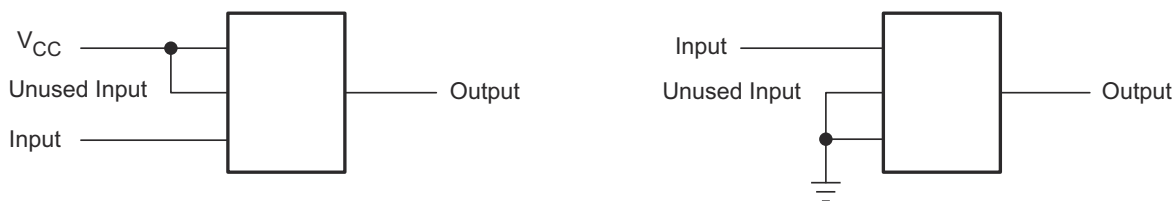
### 8.5.1 Layout Guidelines

When using multiple bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. The rules that must be observed under all circumstances are specified in the next paragraph.

All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or VCC; whichever makes more sense or is more convenient.

### 8.5.2 Layout Example



## 9 Device and Documentation Support

### 9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

### 9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision AE (June 2025) to Revision AF (October 2025)	Page
• Changed Junction-to-ambient thermal resistance value for DCK package from: 229°C/W to: 371.0°C/W .....	5
• Changed Junction-to-case (top) thermal resistance value for DCK package from: 93°C/W to: 297.5°C/W .....	5
• Changed Junction-to-board thermal resistance value for DCK package from: 65°C/W to: 258.6°C/W .....	5
• Changed Junction-to-top characterization value for DCK package from: 2°C/W to: 195.6°C/W .....	5
• Changed Junction-to-board characterization value for DCK package from: 64°C/W to: 256.2°C/W .....	5

Changes from Revision AD (April 2014) to Revision AE (June 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Changed <i>Device Information</i> table to <i>Package Information</i> .....	1
• Moved T <sub>stg</sub> to <i>Absolute Maximum Ratings</i> table.....	4
• Changed Handling Ratings to ESD Ratings.....	4
• Changed Junction-to-ambient thermal resistance value for DBV package from: 278°C/W to: 357.1°C/W .....	5
• Changed Junction-to-case (top) thermal resistance value for DBV package from: 164°C/W to: 263.7°C/W ....	5
• Changed Junction-to-board thermal resistance value for DBV package from: 62°C/W to: 264.4°C/W .....	5
• Changed Junction-to-top characterization value for DBV package from: 44°C/W to: 195.6°C/W .....	5
• Changed Junction-to-board characterization value for DBV package from: 62°C/W to: 262.2°C/W .....	5

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74LVC1G04DBVR</a>	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	(C045, C04F, C04J, C04K, C04R) (C04H, C04P, C04S)
SN74LVC1G04DBVR.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C045, C04F, C04J, C04K, C04R) (C04H, C04P, C04S)
SN74LVC1G04DBVR.B	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C045, C04F, C04J, C04K, C04R) (C04H, C04P, C04S)
SN74LVC1G04DBVRE4	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C04 C04P
SN74LVC1G04DBVRG4.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C04 C04P
SN74LVC1G04DBVRG4.B	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C04 C04P
<a href="#">SN74LVC1G04DBVT</a>	Active	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	(C045, C04F, C04J, C04K, C04R) (C04H, C04P, C04S)
SN74LVC1G04DBVT.B	Active	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(C045, C04F, C04J, C04K, C04R) (C04H, C04P, C04S)
SN74LVC1G04DBVTE4	Active	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C04 C04P
<a href="#">SN74LVC1G04DBVTG4</a>	Active	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C04 C04P
SN74LVC1G04DBVTG4.B	Active	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C04 C04P
<a href="#">SN74LVC1G04DCK3</a>	Last Time Buy	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	SNBI	Level-1-260C-UNLIM	-40 to 125	(CCF, CCZ)

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC1G04DCK3.B	Last Time Buy	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	SNBI	Level-1-260C-UNLIM	-40 to 125	(CCF, CCZ)
<a href="#">SN74LVC1G04DCKR</a>	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	(CC5, CCF, CCJ, CC K, CCR) (CCH, CCP, CCS)
SN74LVC1G04DCKR.A	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CC5, CCF, CCJ, CC K, CCR) (CCH, CCP, CCS)
SN74LVC1G04DCKR.B	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CC5, CCF, CCJ, CC K, CCR) (CCH, CCP, CCS)
SN74LVC1G04DCKRE4	Active	Production	SC70 (DCK)   5	3000   null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CC5, CCF, CCK, CC R) (CCH, CCP, CCS)
SN74LVC1G04DCKRE4.B	Active	Production	SC70 (DCK)   5	3000   null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CC5, CCF, CCK, CC R) (CCH, CCP, CCS)
SN74LVC1G04DCKRG4	Active	Production	SC70 (DCK)   5	3000   null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CC5
SN74LVC1G04DCKRG4.B	Active	Production	SC70 (DCK)   5	3000   null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CC5
<a href="#">SN74LVC1G04DCKT</a>	Active	Production	SC70 (DCK)   5	250   SMALL T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	(CC5, CCF, CCJ, CC R) (CCH, CCP)
SN74LVC1G04DCKT.B	Active	Production	SC70 (DCK)   5	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CC5, CCF, CCJ, CC R) (CCH, CCP)
SN74LVC1G04DCKTE4	Active	Production	SC70 (DCK)   5	250   null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CC5, CCF, CCR) (CCH, CCP)
SN74LVC1G04DCKTE4.B	Active	Production	SC70 (DCK)   5	250   null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CC5, CCF, CCR) (CCH, CCP)
<a href="#">SN74LVC1G04DCKTG4</a>	Active	Production	SC70 (DCK)   5	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CC5, CCF, CCR) (CCH, CCP)
SN74LVC1G04DCKTG4.B	Active	Production	SC70 (DCK)   5	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CC5, CCF, CCR) (CCH, CCP)
<a href="#">SN74LVC1G04DPWR</a>	Active	Production	X2SON (DPW)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	K4
SN74LVC1G04DPWR.B	Active	Production	X2SON (DPW)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	K4
<a href="#">SN74LVC1G04DRLR</a>	Active	Production	SOT-5X3 (DRL)   5	4000   LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(CC7, CCR)



Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC1G04DRLR.B	Active	Production	SOT-5X3 (DRL)   5	4000   LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(CC7, CCR)
<a href="#">SN74LVC1G04DRY2</a>	Active	Production	SON (DRY)   6	5000   LARGE T&R	Yes	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CC
SN74LVC1G04DRY2.B	Active	Production	SON (DRY)   6	5000   LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CC
<a href="#">SN74LVC1G04DRYR</a>	Active	Production	SON (DRY)   6	5000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CC
SN74LVC1G04DRYR.B	Active	Production	SON (DRY)   6	5000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CC
SN74LVC1G04DRYRG4	Active	Production	SON (DRY)   6	5000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CC
<a href="#">SN74LVC1G04DSF2</a>	Active	Production	SON (DSF)   6	5000   LARGE T&R	Yes	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CC
SN74LVC1G04DSF2.B	Active	Production	SON (DSF)   6	5000   LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CC
SN74LVC1G04DSF2G4	Active	Production	SON (DSF)   6	5000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CC
SN74LVC1G04DSF2G4.B	Active	Production	SON (DSF)   6	5000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CC
<a href="#">SN74LVC1G04DSFR</a>	Active	Production	SON (DSF)   6	5000   LARGE T&R	Yes	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CC
SN74LVC1G04DSFR.B	Active	Production	SON (DSF)   6	5000   LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CC
<a href="#">SN74LVC1G04YZPR</a>	Active	Production	DSBGA (YZP)   5	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(CC7, CCN)
SN74LVC1G04YZPR.B	Active	Production	DSBGA (YZP)   5	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(CC7, CCN)
<a href="#">SN74LVC1G04YZVR</a>	Active	Production	DSBGA (YZV)   4	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CC 7
SN74LVC1G04YZVR.B	Active	Production	DSBGA (YZV)   4	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CC 7

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74LVC1G04 :**

- Automotive : [SN74LVC1G04-Q1](#)
- Enhanced Product : [SN74LVC1G04-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G04DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G04DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G04DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G04DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G04DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G04DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G04DCKTG4	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G04DCKTG4	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G04DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q3
SN74LVC1G04DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC1G04DRY2	SON	DRY	6	5000	180.0	9.5	1.6	1.15	0.75	4.0	8.0	Q3
SN74LVC1G04DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1G04DSF2	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q3
SN74LVC1G04DSF2G4	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q3
SN74LVC1G04DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G04YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

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Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G04YZVR	DSBGA	YZV	4	3000	180.0	8.4	1.0	1.0	0.63	2.0	8.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G04DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
SN74LVC1G04DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
SN74LVC1G04DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
SN74LVC1G04DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G04DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G04DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G04DCKTG4	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G04DCKTG4	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G04DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
SN74LVC1G04DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0
SN74LVC1G04DRY2	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G04DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G04DSF2	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G04DSF2G4	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G04DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G04YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0
SN74LVC1G04YZVR	DSBGA	YZV	4	3000	182.0	182.0	20.0

## GENERIC PACKAGE VIEW

**DPW 5**

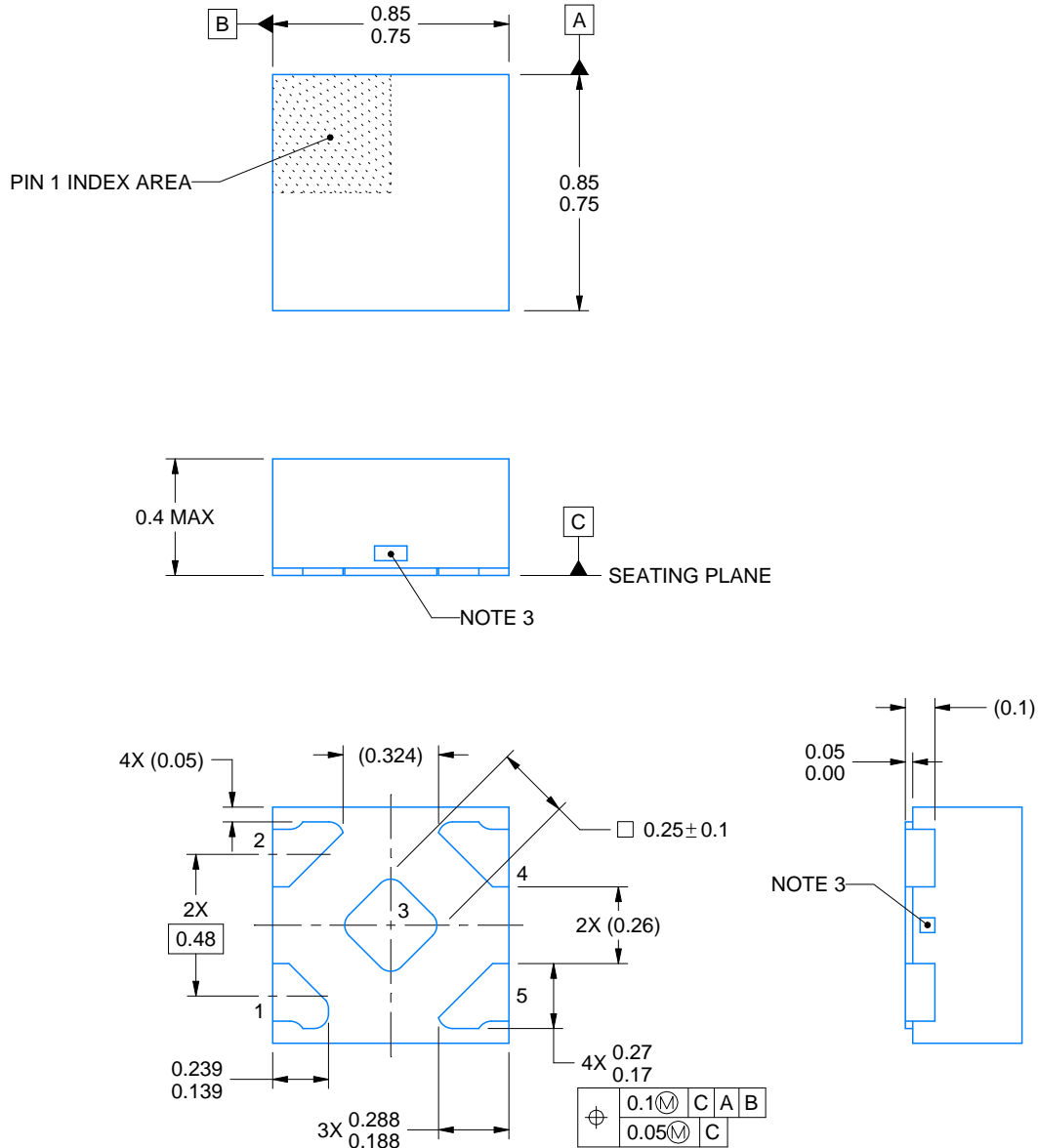
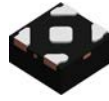
**X2SON - 0.4 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4211218-3/D



4223102/D 03/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

**DPW0005A**

**X2SON - 0.4 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SOLDER MASK DEFINED  
SCALE:60X

4223102/D 03/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).



# EXAMPLE STENCIL DESIGN

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3  
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:100X

4223102/D 03/2022

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

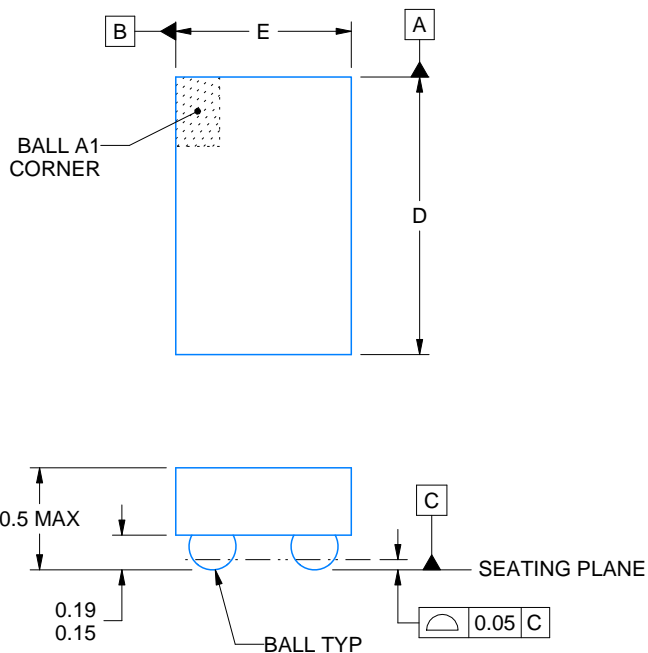
YZP0005



# PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.418 mm, Min = 1.358 mm

E: Max = 0.918 mm, Min = 0.858 mm

4219492/A 05/2017

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

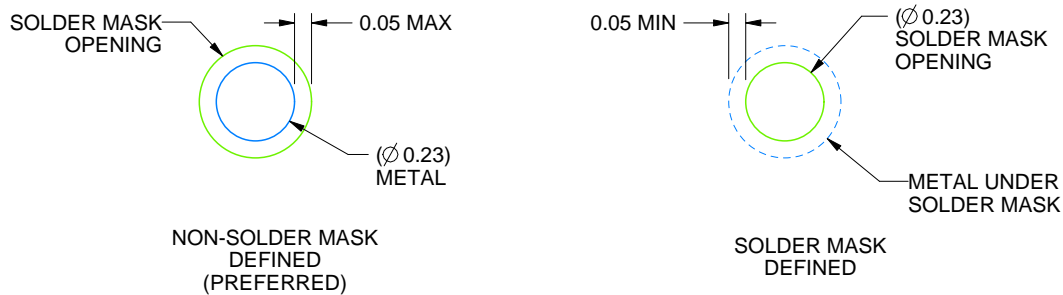
YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:40X



SOLDER MASK DETAILS  
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

## EXAMPLE STENCIL DESIGN

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:40X

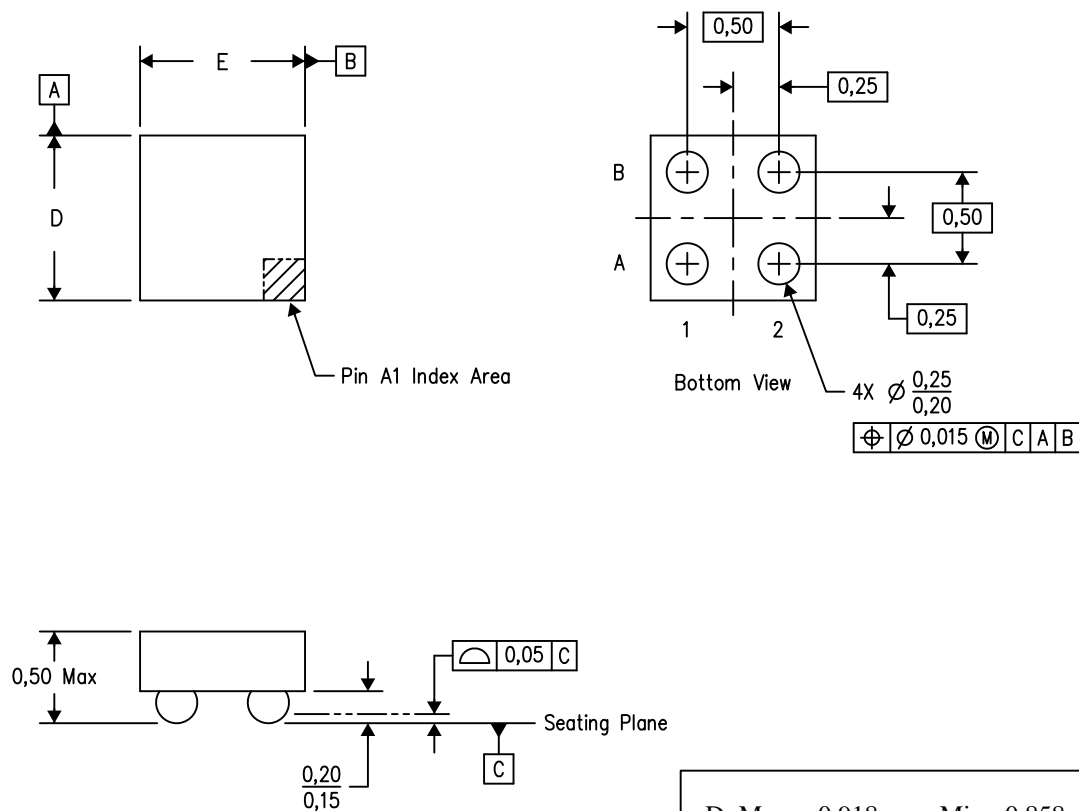
4219492/A 05/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

YZV (S-XBGA-N4)

DIE-SIZE BALL GRID ARRAY



4206083/C 07/13

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

DCK0005A



## PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214834/G 11/2024

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

# EXAMPLE BOARD LAYOUT

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:18X

4214834/G 11/2024

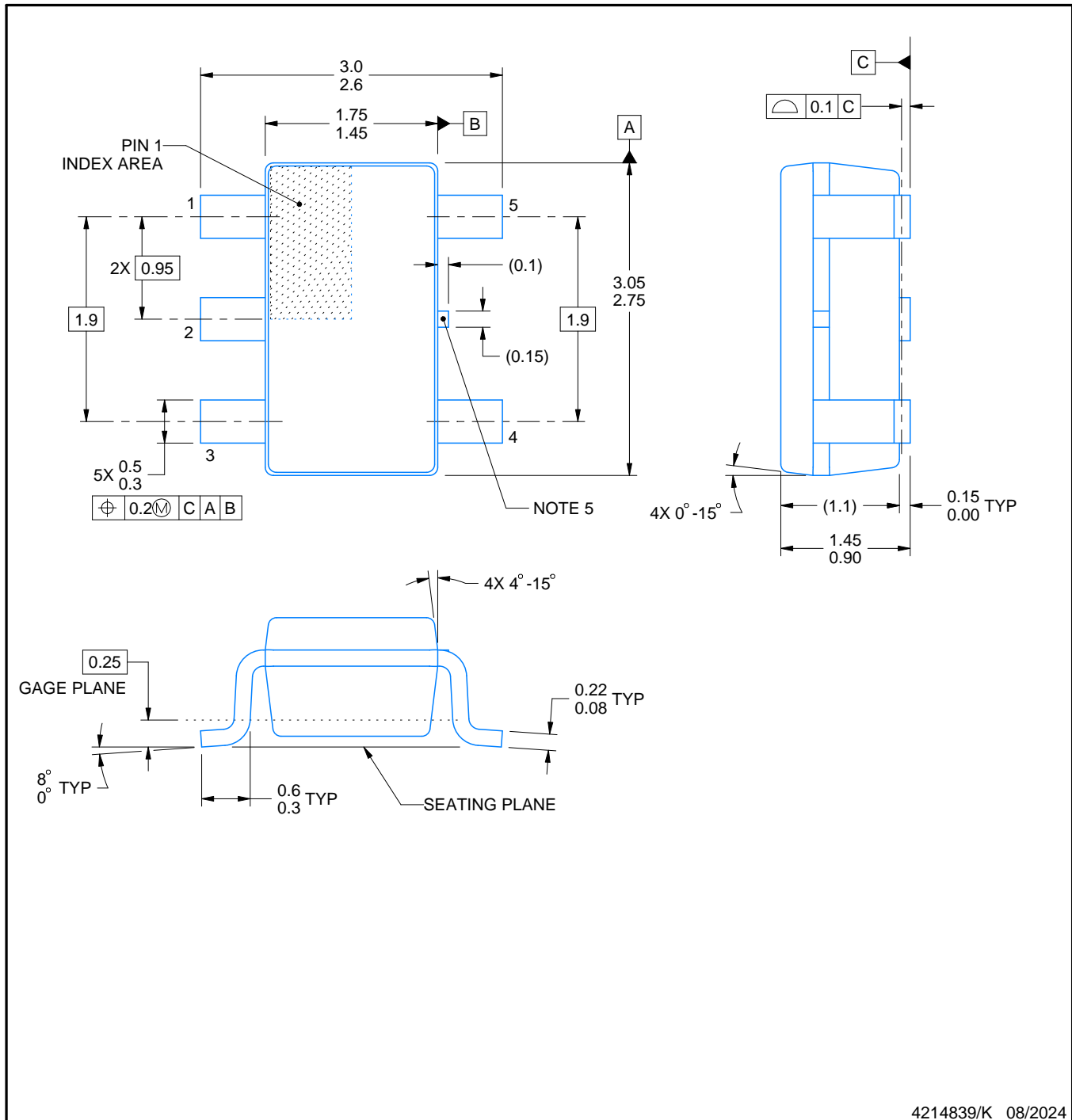
NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.



**DBV0005A****PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR

**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

# EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

**DRY 6**

**USON - 0.6 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4207181/G

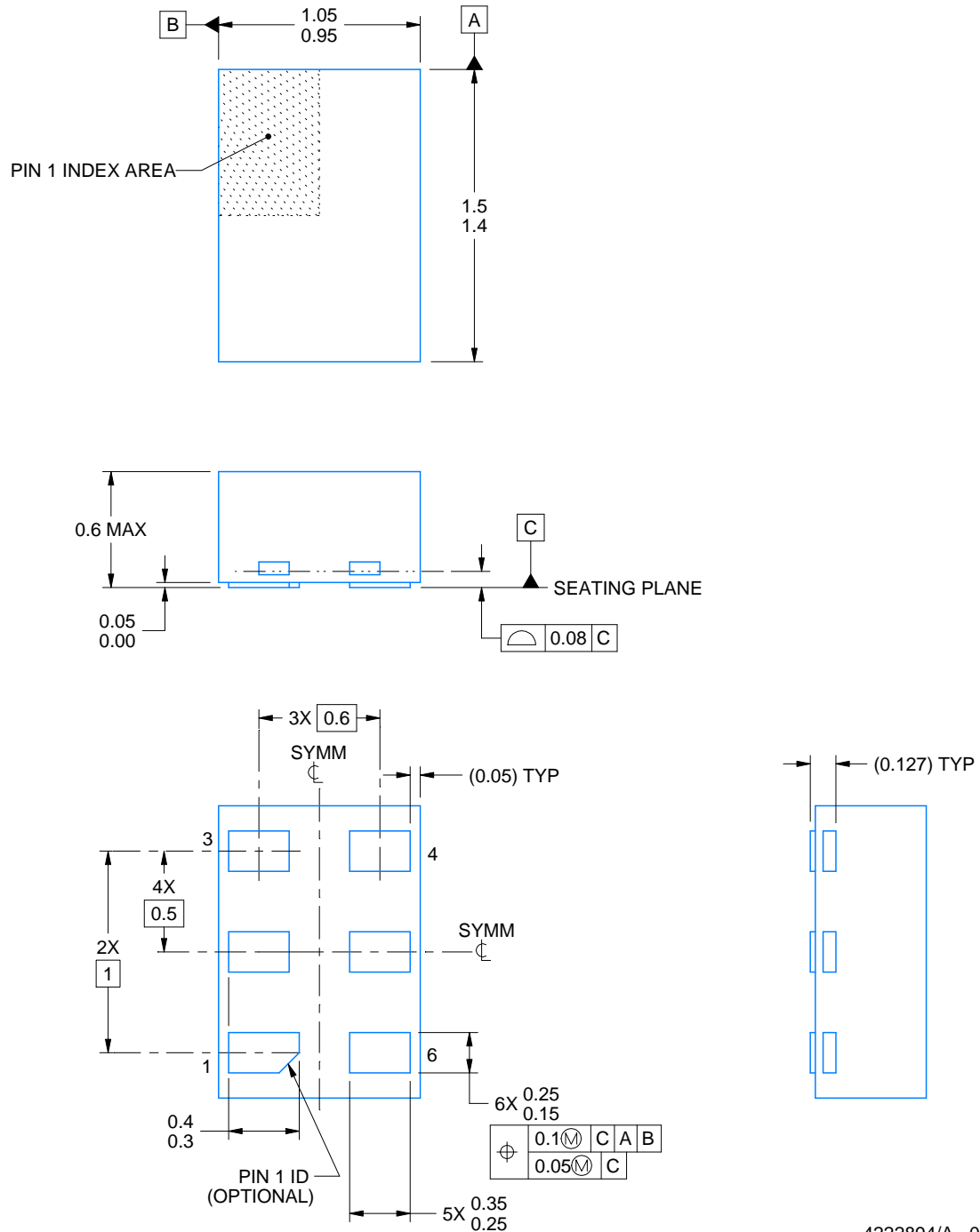
DRY0006A



## PACKAGE OUTLINE

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4222894/A 01/2018

### NOTES:

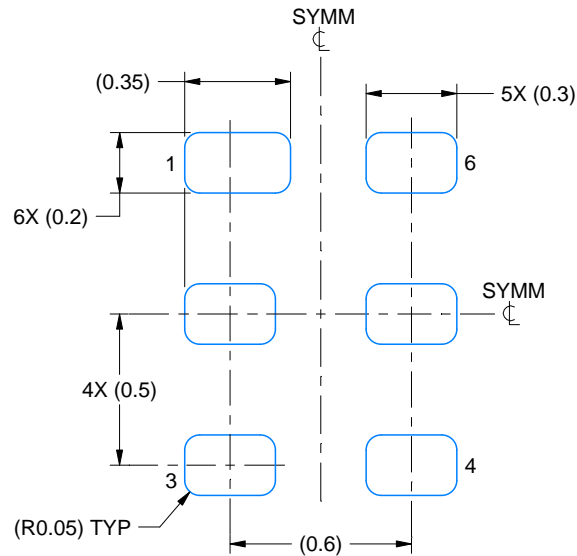
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



**LAND PATTERN EXAMPLE**  
1:1 RATIO WITH PKG SOLDER PADS  
EXPOSED METAL SHOWN  
SCALE:40X



**SOLDER MASK DETAILS**

4222894/A 01/2018

NOTES: (continued)

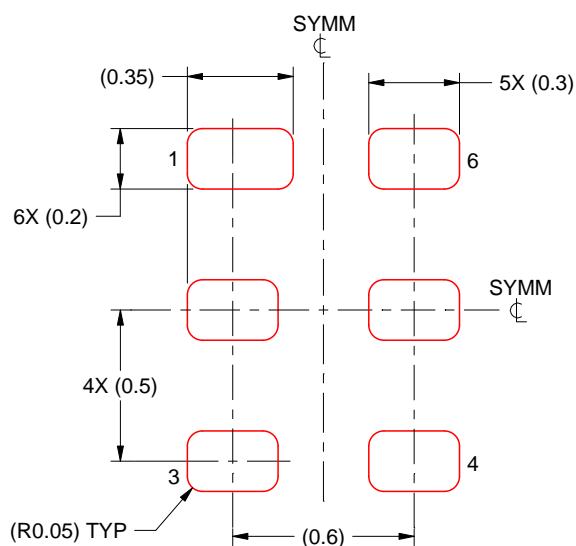
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 ([www.ti.com/lit/slue271](http://www.ti.com/lit/slue271)).

## EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.075 - 0.1 mm THICK STENCIL  
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





# EXAMPLE BOARD LAYOUT

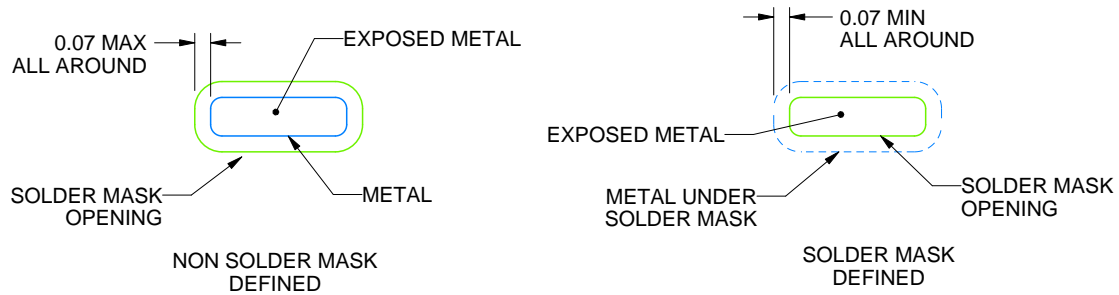
DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:40X



SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slue271](http://www.ti.com/lit/slue271)).

## EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

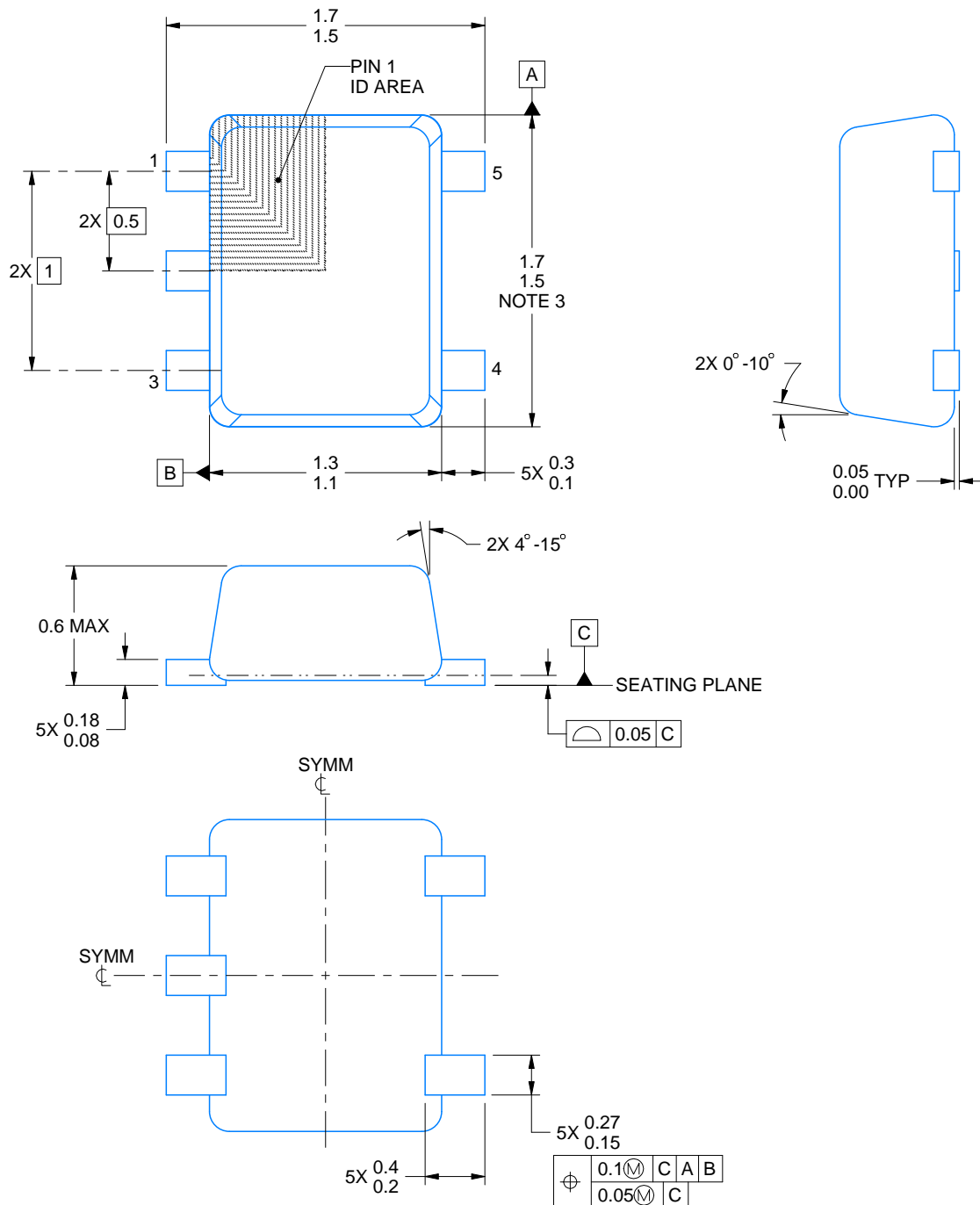
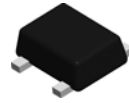


SOLDER PASTE EXAMPLE  
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:40X

4220597/B 06/2022

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4220753/E 11/2024

## NOTES:

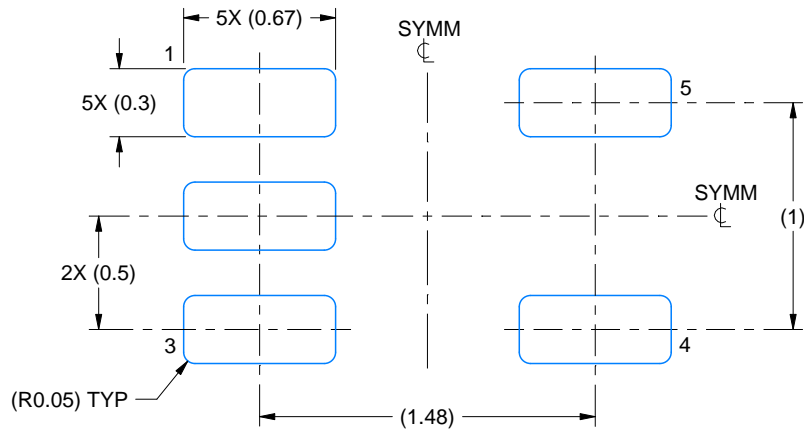
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1

# EXAMPLE BOARD LAYOUT

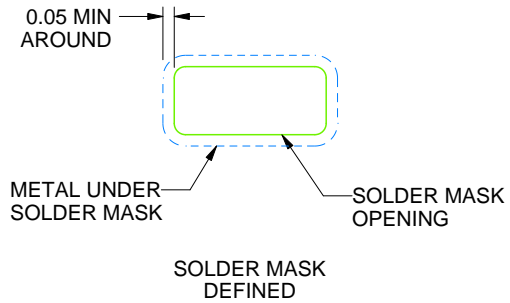
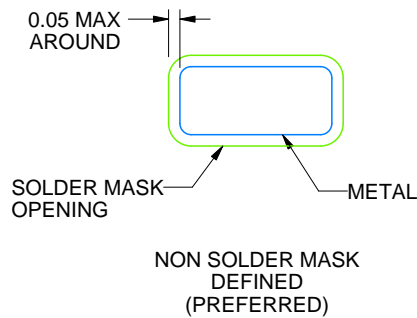
DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:30X



SOLDERMASK DETAILS

4220753/E 11/2024

NOTES: (continued)

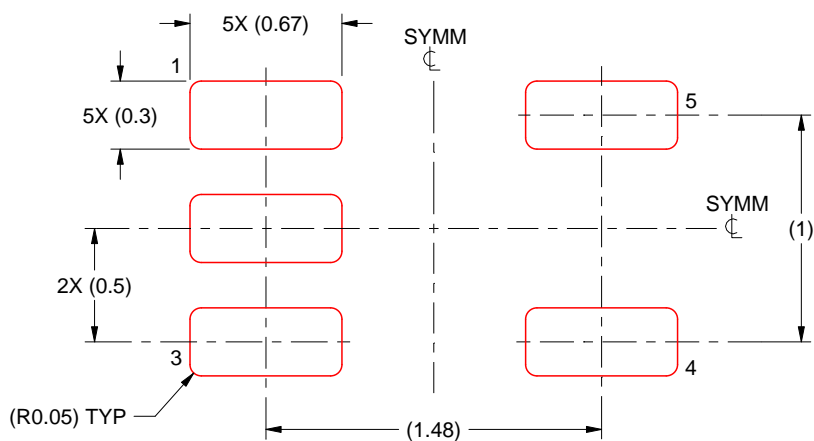
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:30X

4220753/E 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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