

SN74LVC1G80-Q1 Single Positive-Edge-Triggered D-Type Flip-Flop

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
 - $\pm 4000\text{V}$ Human-Body Model (HBM) ESD classification level 3A
 - $\pm 1000\text{V}$ Charged-Device Model (CDM) ESD classification level C5
- Supports $5\text{V } V_{\text{CC}}$ operation
- Inputs accept voltages to 5.5V
- Supports down translation to V_{CC}
- Maximum t_{pd} of 6ns at 3.3V
- Low power consumption, $10\mu\text{A}$ maximum I_{CC}
- $\pm 24\text{mA}$ output drive at 3.3V
- I_{off} supports partial-power-down mode and back-drive protection

2 Applications

- Automotive infotainment
- Automotive cluster
- Automotive ADAS
- Automotive body electronics
- Automotive HEV/EV powertrain

3 Description

The SN74LVC1G80-Q1 device is an automotive AEC-Q100 qualified, single positive-edge-triggered D-type flip-flop that is designed for 1.65V to 5.5V V_{CC} operation.

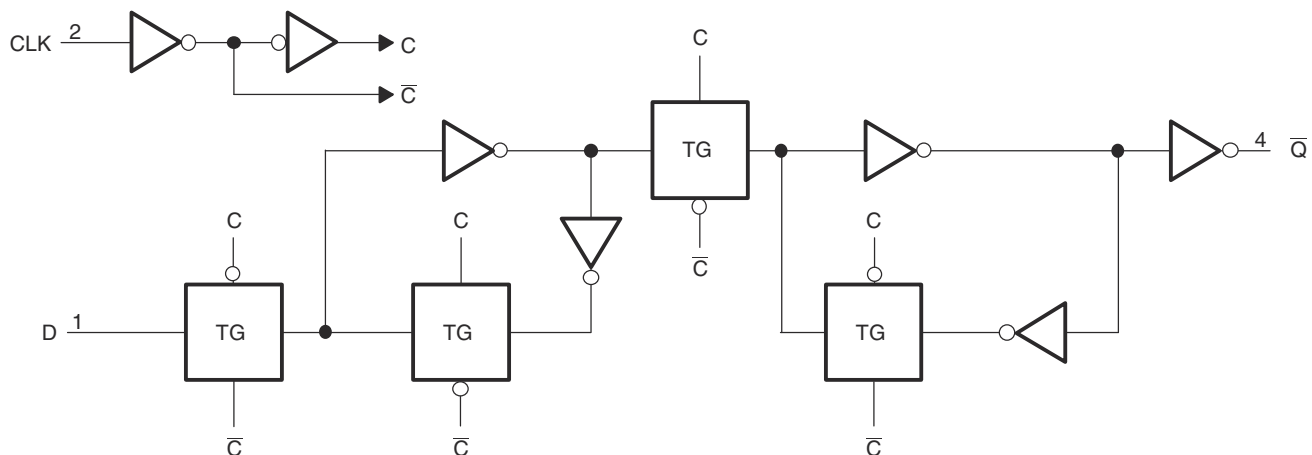
When data at the data (D) input meets the setup time requirement, the data is transferred to the $\bar{Q}$ output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the level at the output.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device which prevents damage to the device.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
SN74LVC1G80-Q1	SC70 (5)	2.00mm × 1.25mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



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A. TG - Transmission Gate

Logic Diagram (Positive Logic)

Table of Contents

1 Features	1	7.1 Overview.....	12
2 Applications	1	7.2 Functional Block Diagram.....	12
3 Description	1	7.3 Feature Description.....	12
4 Pin Configuration and Functions	3	7.4 Device Functional Modes.....	13
5 Specifications	4	8 Application and Implementation	14
5.1 Absolute Maximum Ratings.....	4	8.1 Application Information.....	14
5.2 ESD Ratings.....	4	8.2 Typical Application.....	14
5.3 Recommended Operating Conditions.....	5	9 Power Supply Recommendations	16
5.4 Thermal Information.....	5	10 Layout	17
5.5 Electrical Characteristics.....	6	10.1 Layout Guidelines.....	17
5.6 Timing Requirements: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	6	10.2 Layout Example.....	17
5.7 Timing Requirements: $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	7	11 Device and Documentation Support	18
5.8 Switching Characteristics: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $C_L = 15\text{pF}$	7	11.1 Documentation Support.....	18
5.9 Switching Characteristics: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $C_L = 30\text{pF}$ or 50pF	7	11.2 Receiving Notification of Documentation Updates..	18
5.10 Switching Characteristics: $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $C_L = 30\text{pF}$ or 50pF	8	11.3 Support Resources.....	18
5.11 Operating Characteristics.....	8	11.4 Trademarks.....	18
5.12 Typical Characteristics.....	9	11.5 Electrostatic Discharge Caution.....	18
6 Parameter Measurement Information	10	11.6 Glossary.....	18
7 Detailed Description	12	12 Revision History	18
		13 Mechanical, Packaging, and Orderable Information	18

4 Pin Configuration and Functions

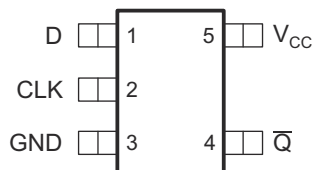


Figure 4-1. DCK Package 5-Pin SC70 Top View

Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
CLK	2	I	Positive-Edge-Triggered Clock input
D	1	I	Data input
GND	3	—	Ground pin
$\bar{Q}$	4	O	Inverted output
V _{CC}	5	—	Positive Supply

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		−0.5	6.5	V
V _I	Input voltage ⁽²⁾		−0.5	6.5	V
V _O	Voltage applied to any output in the high-impedance or power-off state ⁽²⁾		−0.5	6.5	V
V _O	Voltage applied to any output in the high or low state ^{(2) (3)}		−0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		−50	mA
I _{OK}	Output clamp current	V _O < 0		−50	mA
I _O	Continuous output current			±50	mA
	Continuous current through V _{CC} or GND			±100	mA
T _J	Junction temperature			150	°C
T _{stg}	Storage temperature		−65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input negative-voltage and output voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
- (3) The value of V_{CC} is provided in *Recommended Operating Conditions*.

5.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±4000
		Charged-device model (CDM), per AEC Q100-011	±1000

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65V to 1.95V	0.65 × V _{CC}		V
		V _{CC} = 2.3V to 2.7V	1.7		
		V _{CC} = 3V to 3.6V	2		
		V _{CC} = 4.5V to 5.5V	0.7 × V _{CC}		
V _{IL}	Low-level input voltage	V _{CC} = 1.65V to 1.95V		0.35 × V _{CC}	V
		V _{CC} = 2.3V to 2.7V		0.7	
		V _{CC} = 3V to 3.6V		0.8	
		V _{CC} = 4.5V to 5.5V		0.3 × V _{CC}	
V _I	Input voltage		0	5.5	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65V		–4	mA
		V _{CC} = 2.3V		–8	
		V _{CC} = 3V		–16	
		V _{CC} = 4.5V		–24	
I _{OL}	Low-level output current	V _{CC} = 1.65V		4	mA
		V _{CC} = 2.3V		8	
		V _{CC} = 3V		16	
		V _{CC} = 4.5V		24	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 1.8V ± 0.15V, 2.5V ± 0.2V		20	ns/V
		V _{CC} = 3.3V ± 0.3V		10	
		V _{CC} = 5V ± 0.5V		5	
T _A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, [Implications of Slow or Floating CMOS Inputs](#) (SCBA004).

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LVC1G80-Q1	UNIT
		DCK (SC70)	
		5 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	371	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	297.5	°C/W
R _{θJB}	Junction-to-board thermal resistance	258.6	°C/W
ψ _{JT}	Junction-to-top characterization parameter	195.6	°C/W
ψ _{JB}	Junction-to-board characterization parameter	256.2	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN TYP ⁽¹⁾ MAX	UNIT
V _{OH}	I _{OH} = –100μA	1.65V to 5.5V	V _{CC} – 0.1	V
	I _{OH} = –4mA	1.65V	1.2	
	I _{OH} = –8mA	2.3V	1.9	
	I _{OH} = –16mA	3V	2.4	
	I _{OH} = –24mA		2.3	
	I _{OH} = –32mA	4.5V	3.8	
V _{OL}	I _{OL} = 100μA	1.65V to 5.5V	0.1	V
	I _{OL} = 4mA	1.65V	0.45	
	I _{OL} = 8mA	2.3V	0.3	
	I _{OL} = 16mA	3V	0.4	
	I _{OL} = 24mA		0.55	
	I _{OL} = 32mA	4.5V	0.55	
I _I CLK or D inputs	V _I = 5.5V or GND	0 to 5.5V	±10	μA
I _{off}	V _I or V _O = 5.5V	0	±10	μA
I _{CC}	V _I = 5.5V or GND, I _O = 0	1.65V to 5.5V	10	μA
ΔI _{CC}	One input at V _{CC} – 0.6V, Other inputs at V _{CC} or GND	3V to 5.5V	500	μA
C _i	V _I = V _{CC} or GND T _A = –40°C to 85°C	3.3V	3.5	pF

(1) All typical values are at V_{CC} = 3.3V, T_A = 25°C.

5.6 Timing Requirements: T_A = –40°C to +85°C

over recommended operating free-air temperature range, T_A = –40°C to +85°C (unless otherwise noted) (see [Figure 6-1](#))

		V _{CC}	MIN	MAX	UNIT
f _{clock} Clock frequency		V _{CC} = 1.8V ± 0.15V	160		MHz
		V _{CC} = 2.5V ± 0.2V			
		V _{CC} = 3.3V ± 0.3V			
		V _{CC} = 5.5V ± 0.5V			
t _w Pulse duration, CLK high or low		V _{CC} = 1.8V ± 0.15V	2.5		ns
		V _{CC} = 2.5V ± 0.2V			
		V _{CC} = 3.3V ± 0.3V			
		V _{CC} = 5.5V ± 0.5V			
t _{su} Setup time before CLK↑	Data high	V _{CC} = 1.8V ± 0.15V	2.3		ns
		V _{CC} = 2.5V ± 0.2V	1.5		
		V _{CC} = 3.3V ± 0.3V	1.3		
		V _{CC} = 5.5V ± 0.5V	1.1		
	Data low	V _{CC} = 1.8V ± 0.15V	2.5		
		V _{CC} = 2.5V ± 0.2V	1.5		
		V _{CC} = 3.3V ± 0.3V	1.3		
		V _{CC} = 5.5V ± 0.5V	1.1		
t _h Hold time, data after CLK↑		V _{CC} = 1.8V ± 0.15V	0		ns
		V _{CC} = 2.5V ± 0.2V	0.2		
		V _{CC} = 3.3V ± 0.3V	0.9		
		V _{CC} = 5.5V ± 0.5V	0.4		

5.7 Timing Requirements: $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$

over recommended operating free-air temperature range, $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ (unless otherwise noted) (see [Figure 6-1](#))

		V_{CC}	MIN	MAX	UNIT
f_{clock}	Clock frequency	$V_{CC} = 1.8\text{V} \pm 0.15\text{V}$	160		MHz
		$V_{CC} = 2.5\text{V} \pm 0.2\text{V}$			
		$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$			
		$V_{CC} = 5.5\text{V} \pm 0.5\text{V}$			
t_w	Pulse duration, CLK high or low	$V_{CC} = 1.8\text{V} \pm 0.15\text{V}$	2.5		ns
		$V_{CC} = 2.5\text{V} \pm 0.2\text{V}$			
		$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$			
		$V_{CC} = 5.5\text{V} \pm 0.5\text{V}$			
t_{su}	Data high	$V_{CC} = 1.8\text{V} \pm 0.15\text{V}$	2.3		ns
		$V_{CC} = 2.5\text{V} \pm 0.2\text{V}$	1.5		
		$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$	1.3		
		$V_{CC} = 5.5\text{V} \pm 0.5\text{V}$	1.1		
	Data low	$V_{CC} = 1.8\text{V} \pm 0.15\text{V}$	2.5		
		$V_{CC} = 2.5\text{V} \pm 0.2\text{V}$	1.5		
		$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$	1.3		
		$V_{CC} = 5.5\text{V} \pm 0.5\text{V}$	1.1		
t_h	Hold time, data after CLK $\uparrow$	$V_{CC} = 1.8\text{V} \pm 0.15\text{V}$	0		ns
		$V_{CC} = 2.5\text{V} \pm 0.2\text{V}$	0.2		
		$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$	0.9		
		$V_{CC} = 5.5\text{V} \pm 0.5\text{V}$	0.4		

5.8 Switching Characteristics: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $C_L = 15\text{pF}$

over recommended operating free-air temperature range, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $C_L = 15\text{pF}$ (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
f_{max}			$V_{CC} = 1.8\text{V} \pm 0.15\text{V}$	160		MHz
			$V_{CC} = 2.5\text{V} \pm 0.2\text{V}$			
			$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$			
			$V_{CC} = 5\text{V} \pm 0.5\text{V}$			
t_{pd}	CLK	$\bar{Q}$	$V_{CC} = 1.8\text{V} \pm 0.15\text{V}$	3	9.1	ns
			$V_{CC} = 2.5\text{V} \pm 0.2\text{V}$	1.5	6	
			$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$	1.3	4.2	
			$V_{CC} = 5\text{V} \pm 0.5\text{V}$	1.1	3.8	

5.9 Switching Characteristics: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $C_L = 30\text{pF}$ or 50pF

over recommended operating free-air temperature range, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $C_L = 30\text{pF}$ or 50pF (unless otherwise noted) (see [Figure 6-2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
f_{max}			$V_{CC} = 1.8\text{V} \pm 0.15\text{V}$	160		MHz
			$V_{CC} = 2.5\text{V} \pm 0.2\text{V}$			
			$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$			
			$V_{CC} = 5\text{V} \pm 0.5\text{V}$			

over recommended operating free-air temperature range, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $C_L = 30\text{pF}$ or 50pF (unless otherwise noted) (see [Figure 6-2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
t_{pd}	CLK	$\bar{Q}$	$V_{CC} = 1.8\text{V} \pm 0.15\text{V}$	4.4	9.9	ns
			$V_{CC} = 2.5\text{V} \pm 0.2\text{V}$	2.3	7	
			$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$	2	5.2	
			$V_{CC} = 5\text{V} \pm 0.5\text{V}$	1.3	4.5	

5.10 Switching Characteristics: $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $C_L = 30\text{pF}$ or 50pF

over recommended operating free-air temperature range, $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $C_L = 30\text{pF}$ or 50pF (unless otherwise noted) (see [Figure 6-2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
f_{max}			$V_{CC} = 1.8\text{V} \pm 0.15\text{V}$	160		MHz
			$V_{CC} = 2.5\text{V} \pm 0.2\text{V}$			
			$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$			
			$V_{CC} = 5\text{V} \pm 0.5\text{V}$			
t_{pd}	CLK	$\bar{Q}$	$V_{CC} = 1.8\text{V} \pm 0.15\text{V}$	4.4	12.5	ns
			$V_{CC} = 2.5\text{V} \pm 0.2\text{V}$	2.3	8.5	
			$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$	2	6	
			$V_{CC} = 5\text{V} \pm 0.5\text{V}$	1.3	5.5	

5.11 Operating Characteristics

$T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd} Power dissipation capacitance	$f = 10\text{MHz}$	$V_{CC} = 1.8\text{V}$	24	pF
		$V_{CC} = 2.5\text{V}$	24	
		$V_{CC} = 3.3\text{V}$	25	
		$V_{CC} = 5\text{V}$	27	

5.12 Typical Characteristics

This plot shows the different I_{CC} values for various voltages on the data input (D). Voltage sweep on the input is from 0V to 6.5V.

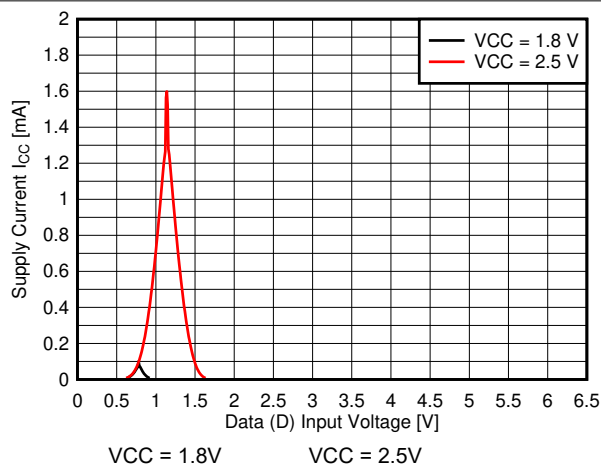


Figure 5-1. Supply Current (I_{CC}) vs Data (D) Input Voltage

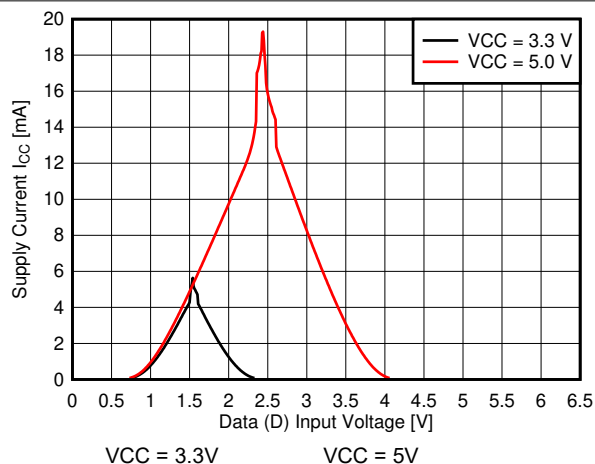
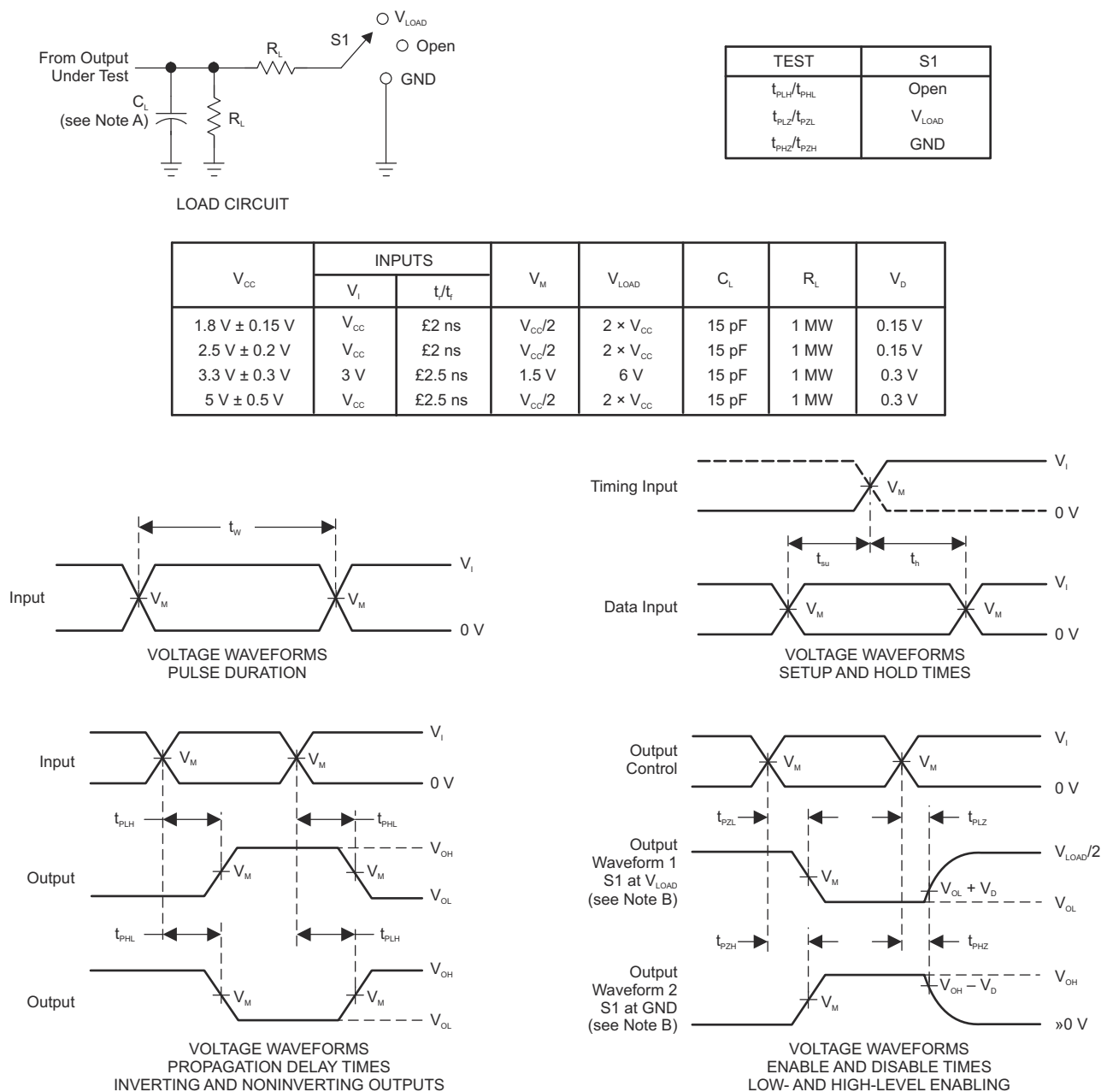


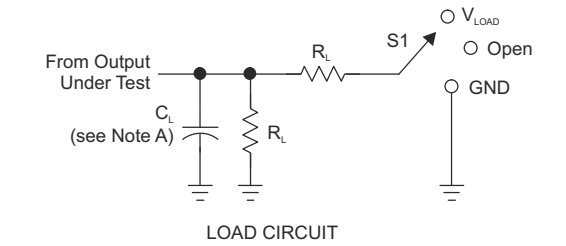
Figure 5-2. Supply Current (I_{CC}) vs Data (D) Input Voltage

6 Parameter Measurement Information



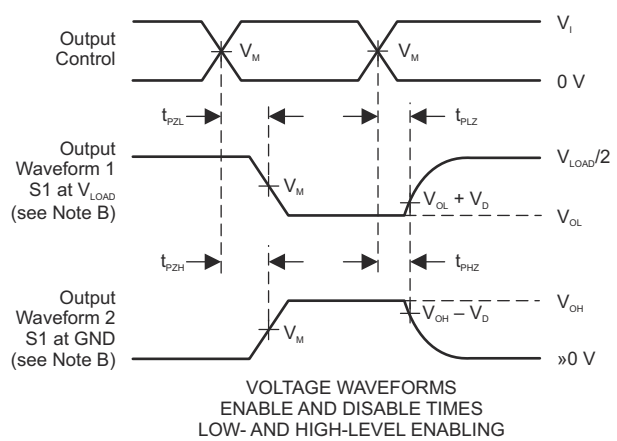
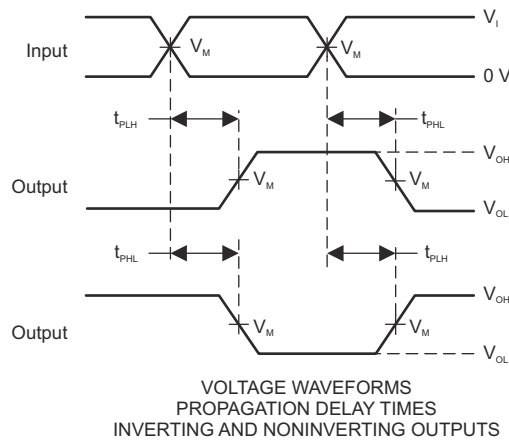
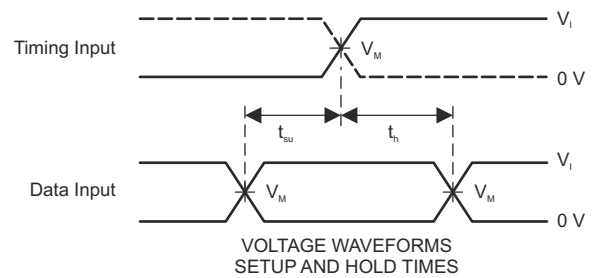
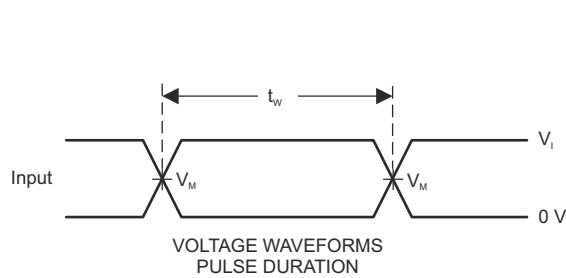
- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_o = 50\text{ }\Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_D
	V_I	t/t_r					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	£2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kW	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	£2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 W	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	£2.5 ns	1.5 V	6 V	50 pF	500 W	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	£2.5 ns	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 W	0.3 V



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR £ 10 MHz, $Z_o = 50\text{ }\Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

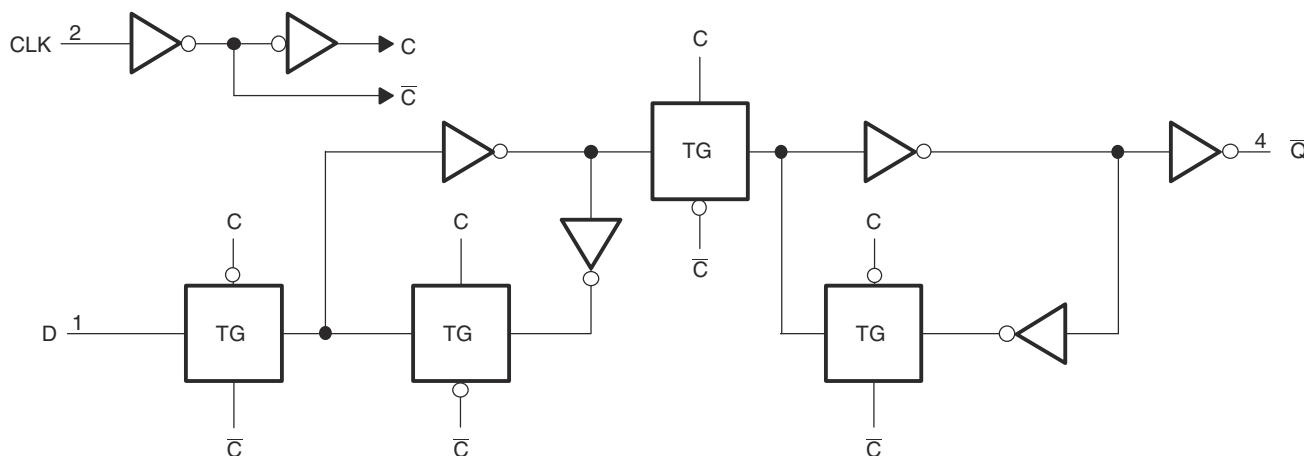
Figure 6-2. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The SN74LVC1G80-Q1 is a single positive-edge-trigger D-type flip-flop and is AEC-Q100 qualified for automotive applications. Data at the input (D) is transferred to the output ($\bar{Q}$) on the positive-going edge of the clock pulse when the setup time requirement is met. Because the clock triggering occurs at a voltage level, it is not directly related to the rise time of the clock pulse. This allows for data at the input to be changed without affecting the level at the output, following the hold-time interval.

7.2 Functional Block Diagram



Logic Diagram (Positive Logic)

7.3 Feature Description

7.3.1 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions must be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. Limit the tower output of the device to avoid thermal runaway and damage due to over-current. The electrical and thermal limits defined the in the [Section 5.1](#) must be followed at all times.

7.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the [Section 5.5](#). The worst case resistance is calculated with the maximum input voltage, given in the [Section 5.3](#), and the maximum input leakage current, given in the [Section 5.5](#), using ohm's law ($R = V \div I$).

Signals applied to the inputs need to have fast edge rates, as defined by $\Delta t/\Delta v$ in [Section 5.3](#) to avoid excessive currents and oscillations. If tolerance to a slow or noisy input signal is required, a device with a Schmitt-trigger input must be used to condition the input signal prior to the standard CMOS input.

7.3.3 Clamp Diodes

The inputs and outputs to this device have negative clamping diodes.

CAUTION

Voltages beyond the values specified in the [Section 5.1](#) table can cause damage to the device. The input negative-voltage and output voltage ratings can be exceeded if the input and output clamp-current ratings are observed.

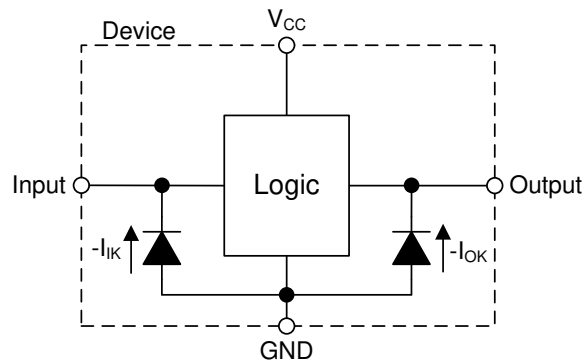


Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

7.3.4 Partial Power Down (I_{off})

The inputs and outputs for this device enter a high impedance state when the supply voltage is 0V. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the [Section 5.5](#).

7.3.5 Over-Voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the [Section 5.1](#).

7.4 Device Functional Modes

[Table 7-1](#) lists the functional modes of the SN74LVC1G80-Q1.

Table 7-1. Function Table

INPUTS		OUTPUT $\bar{Q}$
CLK	D	
↑	H	L
↑	L	H
L	X	Q_0

8 Application and Implementation

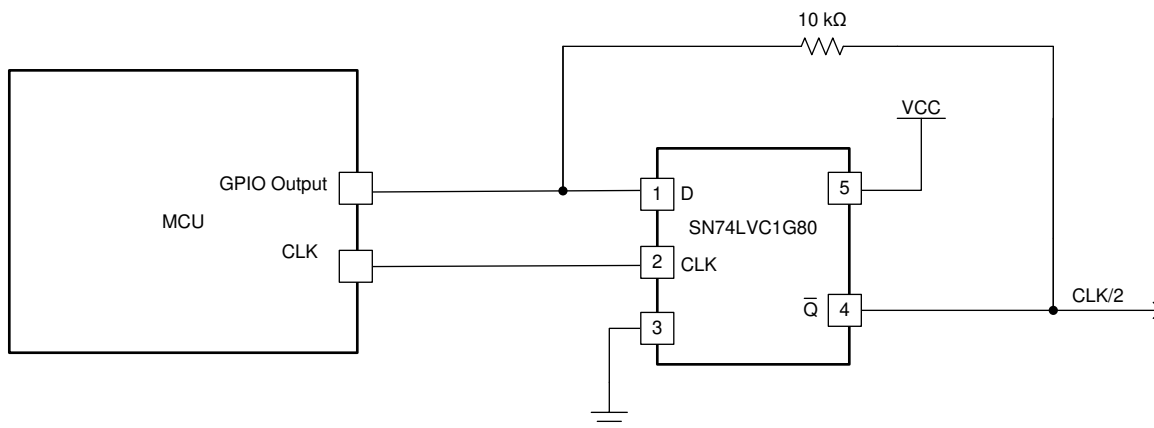
Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

A useful application for the SN74LVC1G80-Q1 is using it as a frequency divider. By feeding back the output ($\bar{Q}$) to the input (D), the output will toggle on every rising edge of the clock waveform. The output goes HIGH once every two clock cycles so essentially the frequency of the clock signal is divided by a factor of two. The SN74LVC1G80-Q1 does not have preset or clear functions so the initial state of the output is unknown. This application implements the use of a microcontroller GPIO pin to initially set the input HIGH, so the output LOW. Initialization is not needed, but can be kept in mind. Post initialization, the GPIO pin is set to a high impedance mode. Depending on the microcontroller, the GPIO pin can be set to an input and used to monitor the clock division.

8.2 Typical Application



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Figure 8-1. Clock Frequency Division

8.2.1 Design Requirements

For this application, a resistor needs to be placed on the feedback line for the initialization voltage from the microcontroller to overpower the signal coming from the output ($\bar{Q}$). Without it the state at the input will be challenged by the GPIO from the microcontroller and from the output of the SN74LVC1G80-Q1.

The SN74LVC1G80-Q1 device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that exceed maximum limits.

8.2.2 Detailed Design Procedure

1. Recommended input conditions:
 - For rise time and fall time specifications, see $\Delta t/\Delta v$ in [Section 5.3](#).
 - For specified high and low levels, see V_{IH} and V_{IL} in [Section 5.3](#).
 - Input voltages are recommended to not go below 0V and not exceed 5.5V for any V_{CC} . See [Section 5.3](#).
2. Recommended output conditions:
 - Load currents must not exceed $\pm 50\text{mA}$. See [Section 5.1](#).
 - Output voltages are recommended to not go below 0V and not exceed the V_{CC} voltage. See [Section 5.3](#).
3. Feedback resistor:
 - A 10k Ω resistor is chosen here to bias the input so the microcontroller GPIO output can initialize the input and output. The resistor value is important because a resistance too high, say at 1M Ω , would cause too much of a voltage drop, causing the output to no longer be able to drive the input. Conversely, a resistor too low, such as a 1 Ω , would not bias enough and might cause current to flow into the microcontroller, possibly damaging the device.

8.2.3 Application Curve

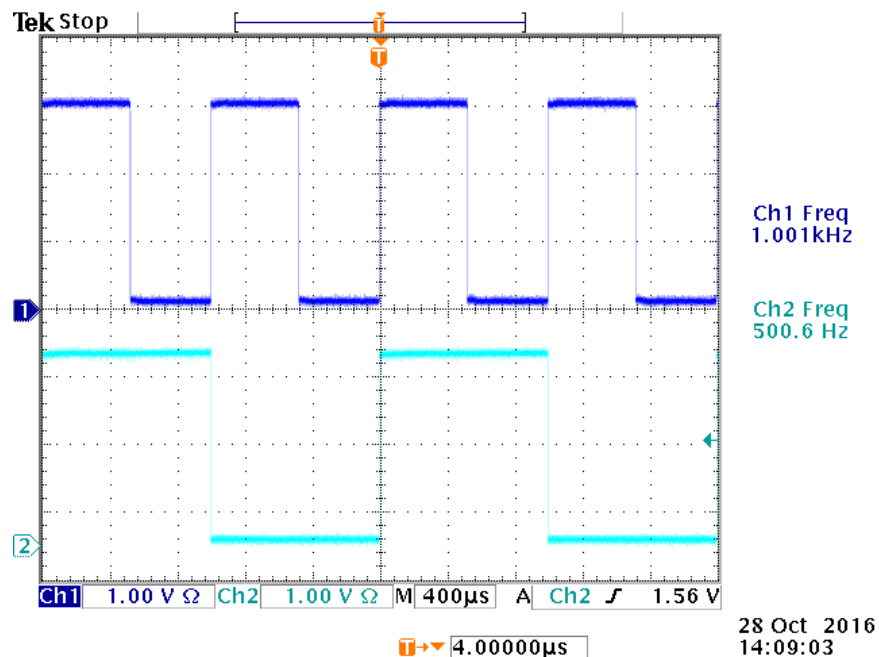


Figure 8-2. Frequency Division

9 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in [Section 5.3](#). A 0.1- μ F bypass capacitor is recommended to be connected from the VCC terminal to GND to prevent power disturbance. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1 μ F and 1 μ F are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results.

10 Layout

10.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. [Figure 10-1](#) shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

10.2 Layout Example

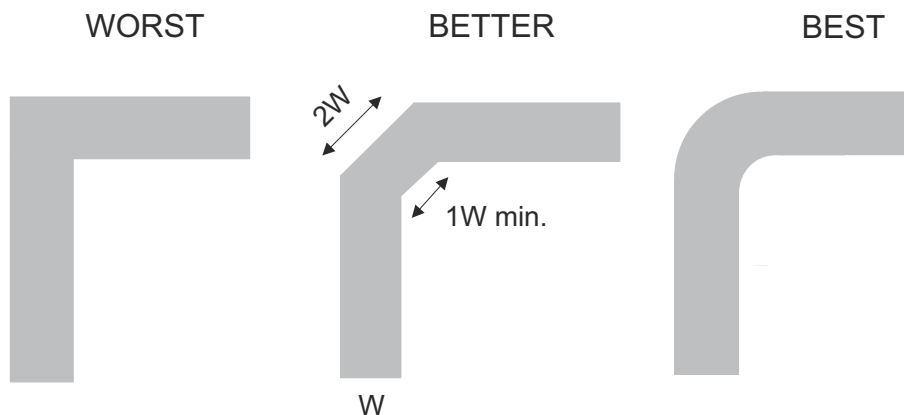


Figure 10-1. Trace Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Implications of Slow or Floating CMOS Inputs](#)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 Trademarks

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11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from April 1, 2017 to August 12, 2026 (from Revision * (April 2017) to Revision A (August 2026))

Page

• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Changed Junction-to-ambient thermal resistance value for DCK package from: 278.9°C/W to: 371°C/W.....	5
• Changed Junction-to-case (top) thermal resistance value for DCK package from: 121.3°C/W to: 297.5°C/W..	5
• Changed Junction-to-board characterization value for DCK package from: 65.6°C/W to: 258.6°C/W.....	5
• Changed Junction-to-top characterization value for DCK package from: 7.5°C/W to: 195.6°C/W.....	5
• Changed Junction-to-board characterization value for DCK package from: 64.9°C/W to: 256.2°C/W.....	5

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC1G80QDCKRQ1	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	17U
SN74LVC1G80QDCKRQ1.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	17U
SN74LVC1G80QDCKRQ1.B	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	17U
SN74LVC1G80QDCKTQ1	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	17U
SN74LVC1G80QDCKTQ1.B	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	17U

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "--" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74LVC1G80-Q1 :

- Catalog : [SN74LVC1G80](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G80QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G80QDCKRQ1	SC70	DCK	5	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC1G80QDCKTQ1	SC70	DCK	5	250	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC1G80QDCKTQ1	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G80QDCKRQ1	SC70	DCK	5	3000	340.0	340.0	38.0
SN74LVC1G80QDCKRQ1	SC70	DCK	5	3000	210.0	185.0	35.0
SN74LVC1G80QDCKTQ1	SC70	DCK	5	250	210.0	185.0	35.0
SN74LVC1G80QDCKTQ1	SC70	DCK	5	250	340.0	340.0	38.0



4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

EXAMPLE BOARD LAYOUT

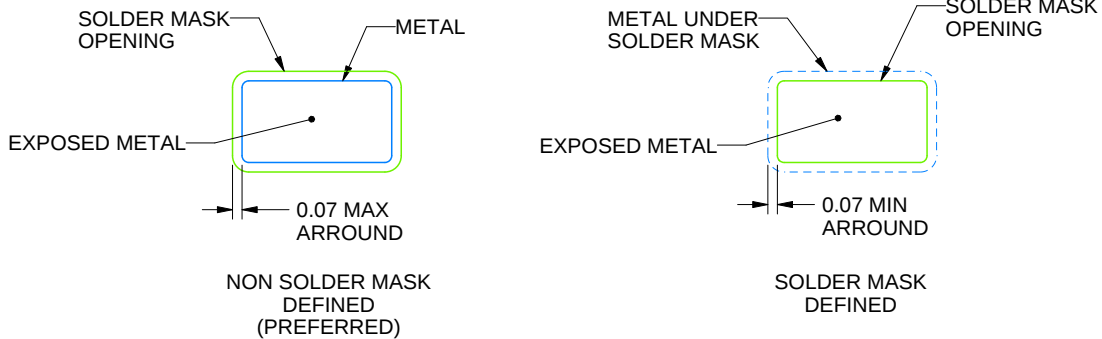
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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