

## SN74LVC2244A Octal Buffer/Driver With 3-State Outputs

### 1 Features

- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 5.5 ns at 3.3 V
- Output Ports Have Equivalent 26- $\Omega$  Series Resistors, So No External Resistors Are Required
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $>2$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V  $V_{CC}$ )
- $I_{off}$  Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

### 2 Applications

- Wearable Health and Fitness Devices
- Network Switches
- Servers
- Tests and Measurements

### 3 Description

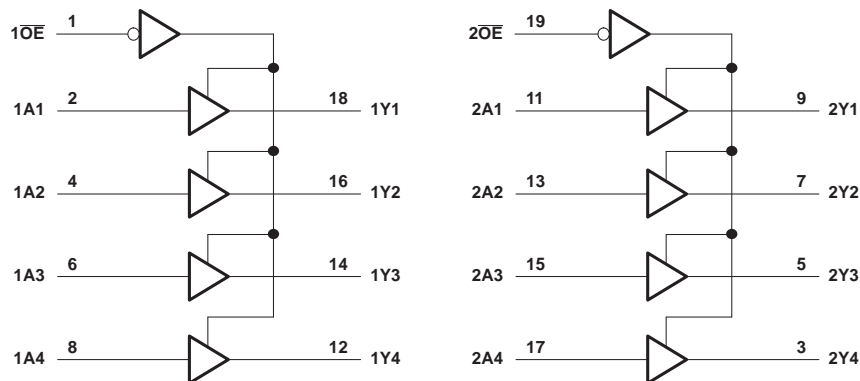
The SN74LVC2244A octal buffer/line driver is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC2244A	SSOP (20)	7.20 mm x 5.30 mm
	SSOP (20)	8.65 mm x 3.90 mm
	TVSOP (20)	5.00 mm x 4.40 mm
	SOIC (20)	12.80 mm x 7.50 mm
	TSSOP (20)	6.50 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### 4 Simplified Schematic



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	<b>9 Detailed Description</b> .....	<b>9</b>
<b>2 Applications</b> .....	<b>1</b>	9.1 Overview .....	9
<b>3 Description</b> .....	<b>1</b>	9.2 Functional Block Diagram .....	9
<b>4 Simplified Schematic</b> .....	<b>1</b>	9.3 Feature Description .....	9
<b>5 Revision History</b> .....	<b>2</b>	9.4 Device Functional Modes .....	9
<b>6 Pin Configuration and Functions</b> .....	<b>3</b>	<b>10 Application and Implementation</b> .....	<b>10</b>
<b>7 Specifications</b> .....	<b>4</b>	10.1 Application Information .....	10
7.1 Absolute Maximum Ratings .....	4	10.2 Typical Application .....	10
7.2 Handling Ratings .....	4	<b>11 Power Supply Recommendations</b> .....	<b>11</b>
7.3 Recommended Operating Conditions .....	5	<b>12 Layout</b> .....	<b>11</b>
7.4 Thermal Information .....	5	12.1 Layout Guidelines .....	11
7.5 Electrical Characteristics .....	6	12.2 Layout Example .....	11
7.6 Switching Characteristics, –40°C to 85°C .....	6	<b>13 Device and Documentation Support</b> .....	<b>12</b>
7.7 Switching Characteristics, –40°C to 125°C .....	6	13.1 Trademarks .....	12
7.8 Operating Characteristics .....	7	13.2 Electrostatic Discharge Caution .....	12
7.9 Typical Characteristics .....	7	13.3 Glossary .....	12
<b>8 Parameter Measurement Information</b> .....	<b>8</b>	<b>14 Mechanical, Packaging, and Orderable Information</b> .....	<b>12</b>

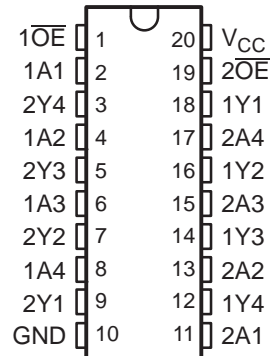
## 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision K (March 2005) to Revision L</b>	<b>Page</b>
• Updated document to new TI data sheet standards. ....	1
• Deleted Ordering Information table. ....	1
• Changed $I_{off}$ bullet in Features list. ....	1
• Added Applications. ....	1
• Added Pin Functions table. ....	3
• Added Handling Ratings table. ....	4
• Changed MAX ambient temperature to 125°C in Recommended Operating Conditions. ....	5
• Added Thermal Information table. ....	5
• Added –40°C to 125°C temperature range in Electrical Characteristics table. ....	6
• Added data to Switching Characteristics, –40°C to 85°C. ....	6
• Added Switching Characteristics table, –40°C to 125°C. ....	6
• Changed Operating Characteristics table. ....	7
• Added Typical Characteristics. ....	7
• Added Detailed Description section. ....	9
• Added Application and Implementation section. ....	10

## 6 Pin Configuration and Functions

DB, DBQ, DGV, DW, NS, OR PW PACKAGE  
(TOP VIEW)



### Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	$\overline{1OE}$	I	Output Enable 1
2	1A1	I	1A1 Input
3	2Y4	O	2Y4 Output
4	1A2	I	1A2 Input
5	2Y3	O	2Y3 Output
6	1A3	I	1A3 Input
7	2Y2	O	2Y2 Output
8	1A4	I	1A4 Input
9	2Y1	O	2Y1 Output
10	GND	—	Ground Pin
11	2A1	I	2A1 Input
12	1Y4	O	1Y4 Output
13	2A2	I	2A2 Input
14	1Y3	O	1Y3 Output
15	2A3	I	2A3 Input
16	1Y2	O	1Y2 Output
17	2A4	I	2A4 Input
18	1Y1	O	1Y1 Output
19	$\overline{2OE}$	I	Output Enable 2
20	VCC	—	Power Pin

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	–0.5	6.5	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	–0.5	6.5	V
V <sub>O</sub>	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	–0.5	6.5	V
V <sub>O</sub>	Voltage range applied to any output in the high or low state <sup>(2)</sup> <sup>(3)</sup>	–0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0	–50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0	–50	mA
I <sub>O</sub>	Continuous output current		±50	mA
	Continuous current through V <sub>CC</sub> or GND		±100	mA

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V<sub>CC</sub> is provided in the *Recommended Operating Conditions* table.

### 7.2 Handling Ratings

		MIN	MAX	UNIT	
T <sub>stg</sub>	Storage temperature range	–65	150	°C	
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	0	1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

 over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.5		
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		
		V <sub>CC</sub> = 2.7 V to 3.6 V	2		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	
		V <sub>CC</sub> = 2.7 V to 3.6 V		0.8	
V <sub>I</sub>	Input voltage	0	5.5	V	
V <sub>O</sub>	Output voltage	High or low state	0	V <sub>CC</sub>	V
		3-state	0	5.5	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V		–2	mA
		V <sub>CC</sub> = 2.3 V		–4	
		V <sub>CC</sub> = 2.7 V		–8	
		V <sub>CC</sub> = 3 V		–12	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V		2	mA
		V <sub>CC</sub> = 2.3 V		4	
		V <sub>CC</sub> = 2.7 V		8	
		V <sub>CC</sub> = 3 V		12	
Δt/Δv	Input transition rise or fall rate			10	ns/V
T <sub>A</sub>	Operating free-air temperature	–40	125		°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs (SCBA004)*.

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	SN74LVC2244A						UNIT	
	DB	DBQ	DGV	DW	NS	PW		
	20 PINS							
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	94.5	94.7	114.7	88.3	74.7	102.5	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	56.2	47.9	29.8	51.1	40.5	35.9	
R <sub>θJB</sub>	Junction-to-board thermal resistance	49.7	45.0	56.2	50.9	42.3	53.5	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	18.1	11.0	0.8	20.0	14.3	2.2	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	49.5	44.6	55.5	50.5	41.9	52.9	
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	n/a	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report ([SPRA953](#)).

## 7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	–40°C to 85°C			–40°C to 125°C			UNIT
			MIN	TYP <sup>(1)</sup>	MAX	MIN	TYP <sup>(1)</sup>	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = –100 μA	1.65 V to 3.6 V	V <sub>CC</sub> – 0.2			V <sub>CC</sub> – 0.2			V
	I <sub>OH</sub> = –2 mA	1.65 V	1.2			1.2			
	I <sub>OH</sub> = –4 mA	2.3 V	1.7			1.7			
		2.7 V	2.2			2.2			
	I <sub>OH</sub> = –6 mA	3 V	2.4			2.4			
	I <sub>OH</sub> = –8 mA	2.7 V	2			2			
I <sub>OH</sub> = –12 mA	3 V	2			2				
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V	0.2			0.2			V
	I <sub>OL</sub> = 2 mA	1.65 V	0.45			0.45			
	I <sub>OL</sub> = 4 mA	2.3 V	0.7			0.7			
		2.7 V	0.4			0.4			
	I <sub>OL</sub> = 6 mA	3 V	0.55			0.55			
	I <sub>OL</sub> = 8 mA	2.7 V	0.6			0.6			
I <sub>OL</sub> = 12 mA	3 V	0.8			0.8				
I <sub>I</sub>	V <sub>I</sub> = 0 to 5.5 V	3.6 V	±5			±5			μA
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0	±10			±10			μA
I <sub>OZ</sub>	V <sub>O</sub> = 0 to 5.5 V	3.6 V	±10			±10			μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	I <sub>O</sub> = 0	10			10			μA
	3.6 V ≤ V <sub>I</sub> ≤ 5.5 V <sup>(2)</sup>		10			10			
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V	500			500			μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	4			4			pF
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V	5.5			5.5			pF

 (1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

(2) This applies in the disabled state only.

## 7.6 Switching Characteristics, –40°C to 85°C

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y		10.9		7.9		6.4	1.5	5.5	ns
t <sub>en</sub>	$\overline{OE}$	Y		12.6		9.6		8.1	1	7.1	ns
t <sub>dis</sub>	$\overline{OE}$	Y		12.1		7.8		7.3	1.5	6.8	ns

## 7.7 Switching Characteristics, –40°C to 125°C

over operating free-air temperature range (unless otherwise noted)

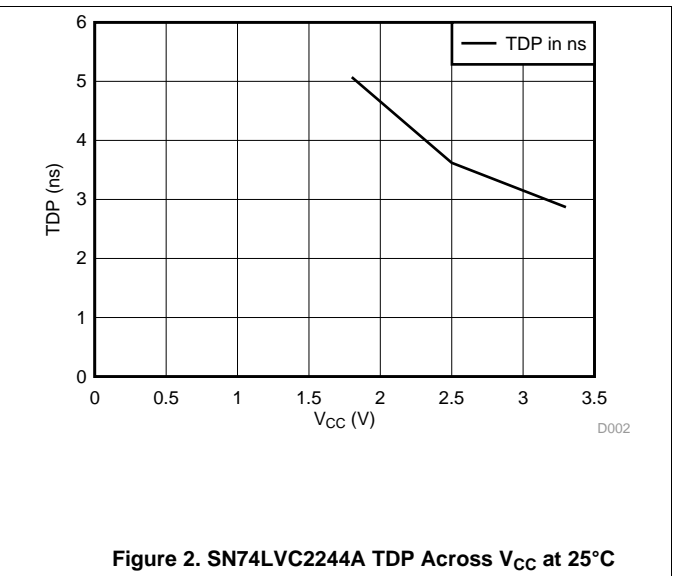
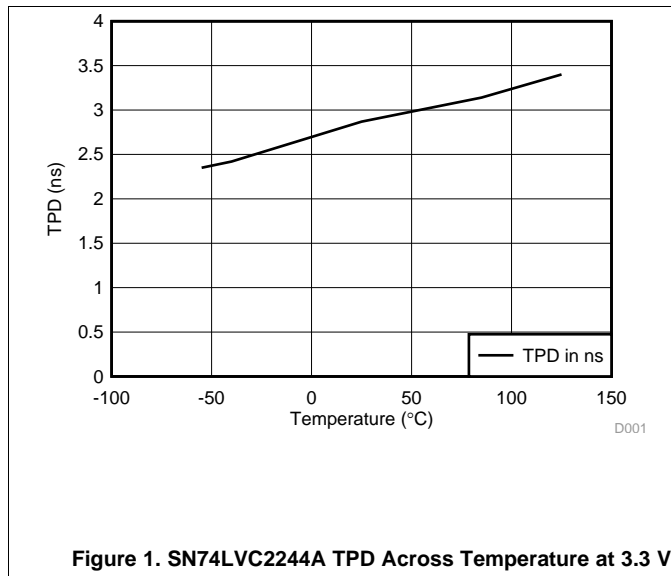
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y		12.4		10		7.1	1.5	6.5	ns
t <sub>en</sub>	$\overline{OE}$	Y		14.1		11.7		8.5	1	7.8	ns
t <sub>dis</sub>	$\overline{OE}$	Y		13.6		9.9		7.8	1.5	7.6	ns

### 7.8 Operating Characteristics

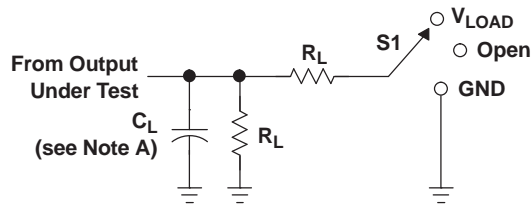
T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	UNIT
			TYP	TYP	TYP	
C <sub>pd</sub>	Power dissipation capacitance per buffer/driver	Outputs enabled	43	43	46	pF
		Outputs disabled	1	1	2	

### 7.9 Typical Characteristics

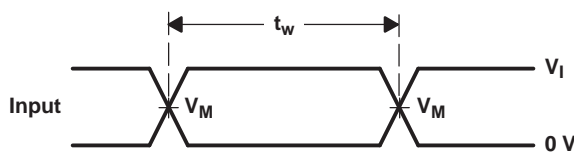
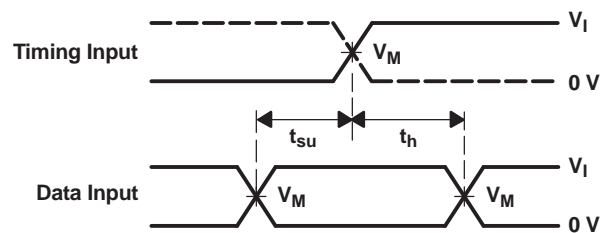
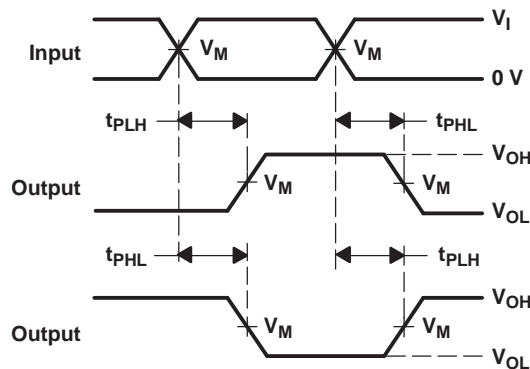
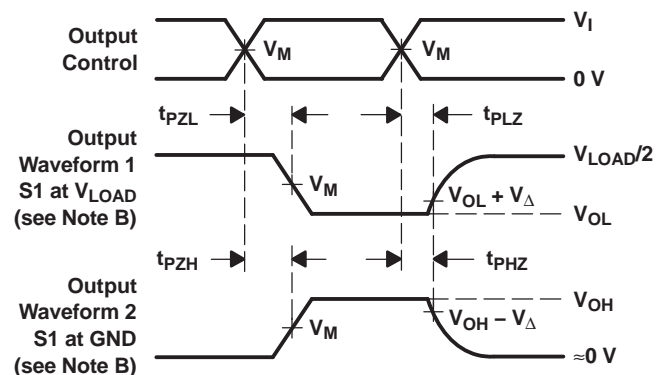


## 8 Parameter Measurement Information


**LOAD CIRCUIT**

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V


**VOLTAGE WAVEFORMS  
PULSE DURATION**

**VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING**

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

**Figure 3. Load Circuit and Voltage Waveforms**

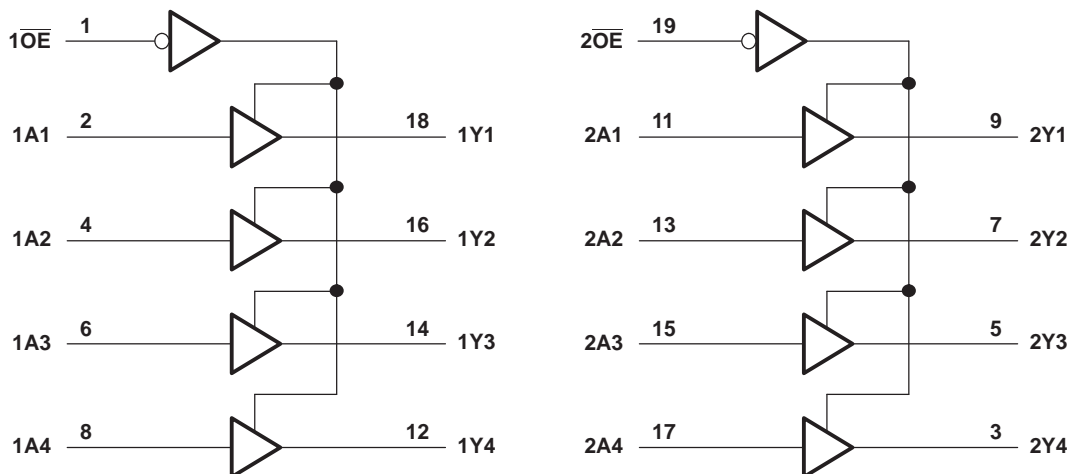


## 9 Detailed Description

### 9.1 Overview

This octal buffer and line driver is designed for 1.65-V to 3.6-V  $V_{CC}$  operation. The SN74LVC2244A device is organized as two 4-bit line drivers with separate output-enable ( $\overline{OE}$ ) inputs. When  $\overline{OE}$  is low, the device passes data from the A inputs to the Y outputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state. The outputs, which are designed to sink up to 12 mA, include equivalent 26-ohm resistors to reduce overshoot and undershoot.

### 9.2 Functional Block Diagram



### 9.3 Feature Description

- Wide operating voltage range
  - Operates from 1.65 V to 3.6 V
- Allows down voltage translation
  - Inputs accept voltages to 5.5 V
- $I_{off}$  Feature
  - Allows voltages on the inputs and outputs when  $V_{CC}$  is 0 V

### 9.4 Device Functional Modes

Table 1. Function Table  
(Each Buffer)

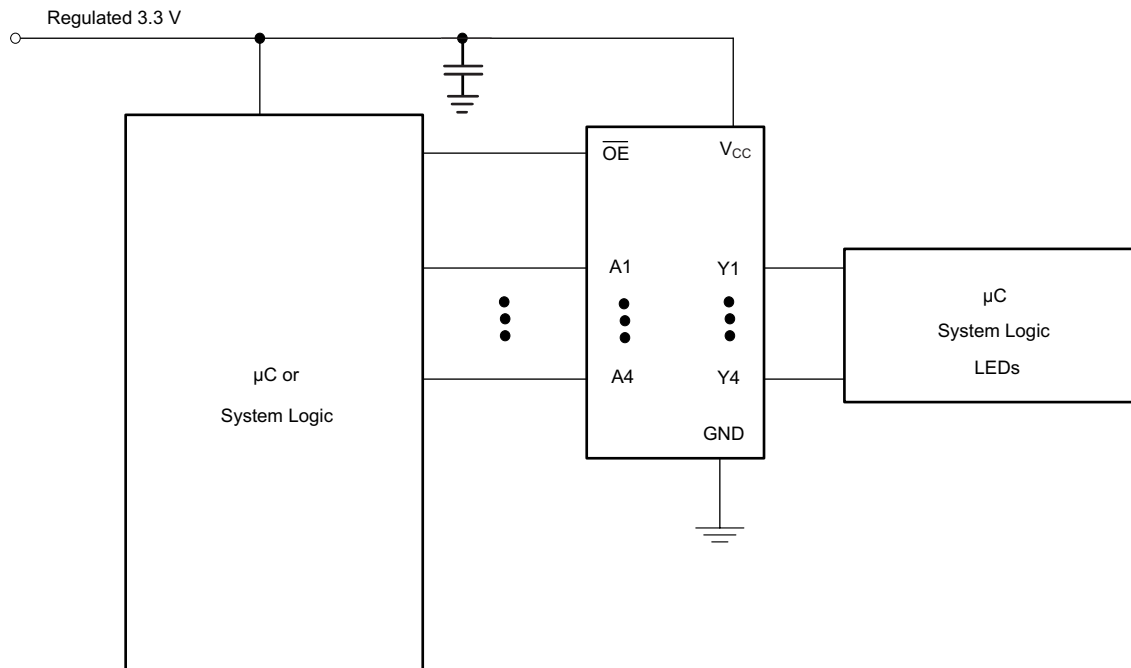
INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

## 10 Application and Implementation

### 10.1 Application Information

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment. This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### 10.2 Typical Application



**Figure 4. Typical Application Diagram**

#### 10.2.1 Design Requirements

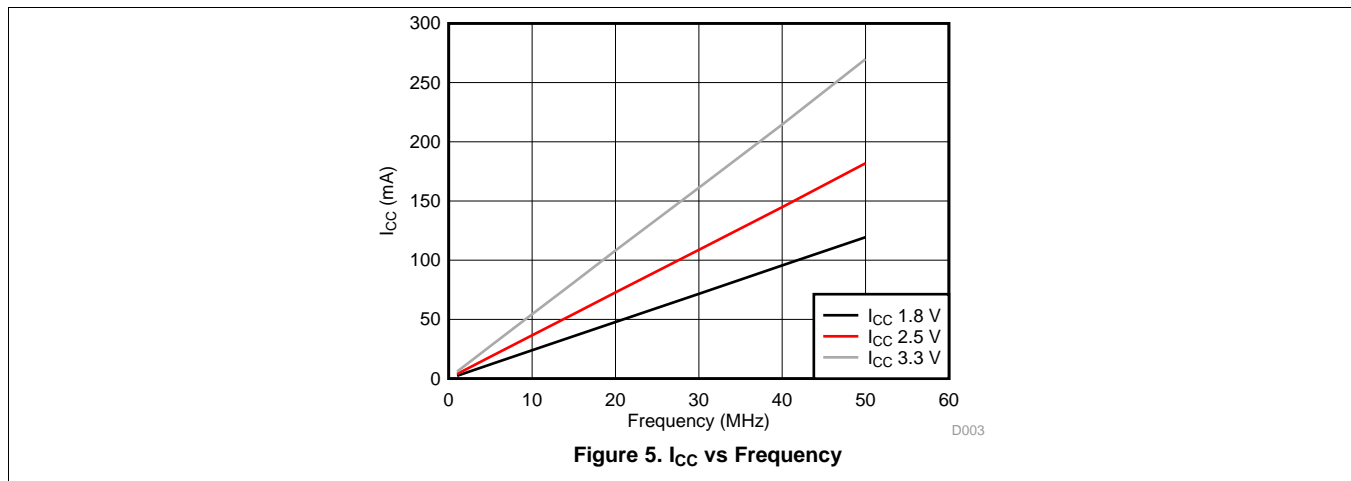
This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

#### 10.2.2 Detailed Design Procedure

1. Recommended Input Conditions
  - Rise time and fall time specs: See  $(\Delta t/\Delta V)$  in the [Recommended Operating Conditions](#) table.
  - Specified high and low levels: See  $(V_{IH}$  and  $V_{IL})$  in the [Recommended Operating Conditions](#) table.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid  $V_{CC}$ .
2. Recommend Output Conditions
  - Load currents should not exceed 25 mA per output and 50 mA total for the part.
  - Outputs should not be pulled above  $V_{CC}$ .

## Typical Application (continued)

### 10.2.3 Application Curves



## 11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu\text{f}$  is recommended; if there are multiple  $V_{CC}$  pins, then 0.01  $\mu\text{f}$  or 0.022  $\mu\text{f}$  is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu\text{f}$  and a 1  $\mu\text{f}$  are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 12 Layout

### 12.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. [Figure 6](#) specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the IOs, so they cannot float when disabled.

### 12.2 Layout Example

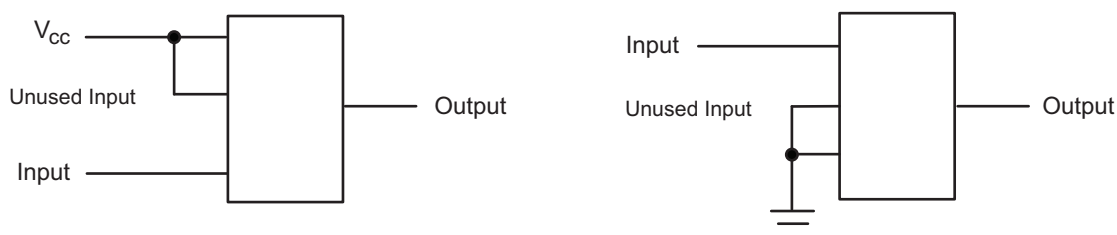


Figure 6. Layout Diagram

## 13 Device and Documentation Support

### 13.1 Trademarks

All trademarks are the property of their respective owners.

### 13.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74LVC2244ADBQR</a>	Active	Production	SSOP (DBQ)   20	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVC2244A
SN74LVC2244ADBQR.B	Active	Production	SSOP (DBQ)   20	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVC2244A
SN74LVC2244ADBQRE4	Active	Production	SSOP (DBQ)   20	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVC2244A
<a href="#">SN74LVC2244ADBR</a>	Active	Production	SSOP (DB)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LE244A
SN74LVC2244ADBR.B	Active	Production	SSOP (DB)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LE244A
SN74LVC2244ADBRG4	Active	Production	SSOP (DB)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LE244A
<a href="#">SN74LVC2244ADGVR</a>	Active	Production	TVSOP (DGV)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LE244A
SN74LVC2244ADGVR.B	Active	Production	TVSOP (DGV)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LE244A
SN74LVC2244ADGVRG4	Active	Production	TVSOP (DGV)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LE244A
SN74LVC2244ADGVRG4.B	Active	Production	TVSOP (DGV)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LE244A
<a href="#">SN74LVC2244ADW</a>	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC2244A
SN74LVC2244ADW.B	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC2244A
<a href="#">SN74LVC2244ADWR</a>	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC2244A
SN74LVC2244ADWR.B	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC2244A
SN74LVC2244ADWRE4	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC2244A
<a href="#">SN74LVC2244ANSR</a>	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC2244A
SN74LVC2244ANSR.B	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC2244A
SN74LVC2244ANSRG4	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC2244A
SN74LVC2244ANSRG4.B	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC2244A
<a href="#">SN74LVC2244APW</a>	Active	Production	TSSOP (PW)   20	70   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LE244A
SN74LVC2244APW.B	Active	Production	TSSOP (PW)   20	70   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LE244A
SN74LVC2244APWG4	Active	Production	TSSOP (PW)   20	70   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LE244A
<a href="#">SN74LVC2244APWR</a>	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LE244A
SN74LVC2244APWR.B	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LE244A
SN74LVC2244APWRE4	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LE244A
SN74LVC2244APWRG4	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LE244A
<a href="#">SN74LVC2244APWT</a>	Active	Production	TSSOP (PW)   20	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LE244A
SN74LVC2244APWT.B	Active	Production	TSSOP (PW)   20	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LE244A

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC2244ADBQR	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC2244ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LVC2244ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC2244ADGVRG4	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC2244ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LVC2244ANSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LVC2244ANSRG4	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LVC2244APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LVC2244APWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC2244ADBQR	SSOP	DBQ	20	2500	353.0	353.0	32.0
SN74LVC2244ADBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74LVC2244ADGVR	TVSOP	DGV	20	2000	353.0	353.0	32.0
SN74LVC2244ADGVRG4	TVSOP	DGV	20	2000	353.0	353.0	32.0
SN74LVC2244ADWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74LVC2244ANSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74LVC2244ANSRG4	SOP	NS	20	2000	356.0	356.0	45.0
SN74LVC2244APWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74LVC2244APWT	TSSOP	PW	20	250	353.0	353.0	32.0



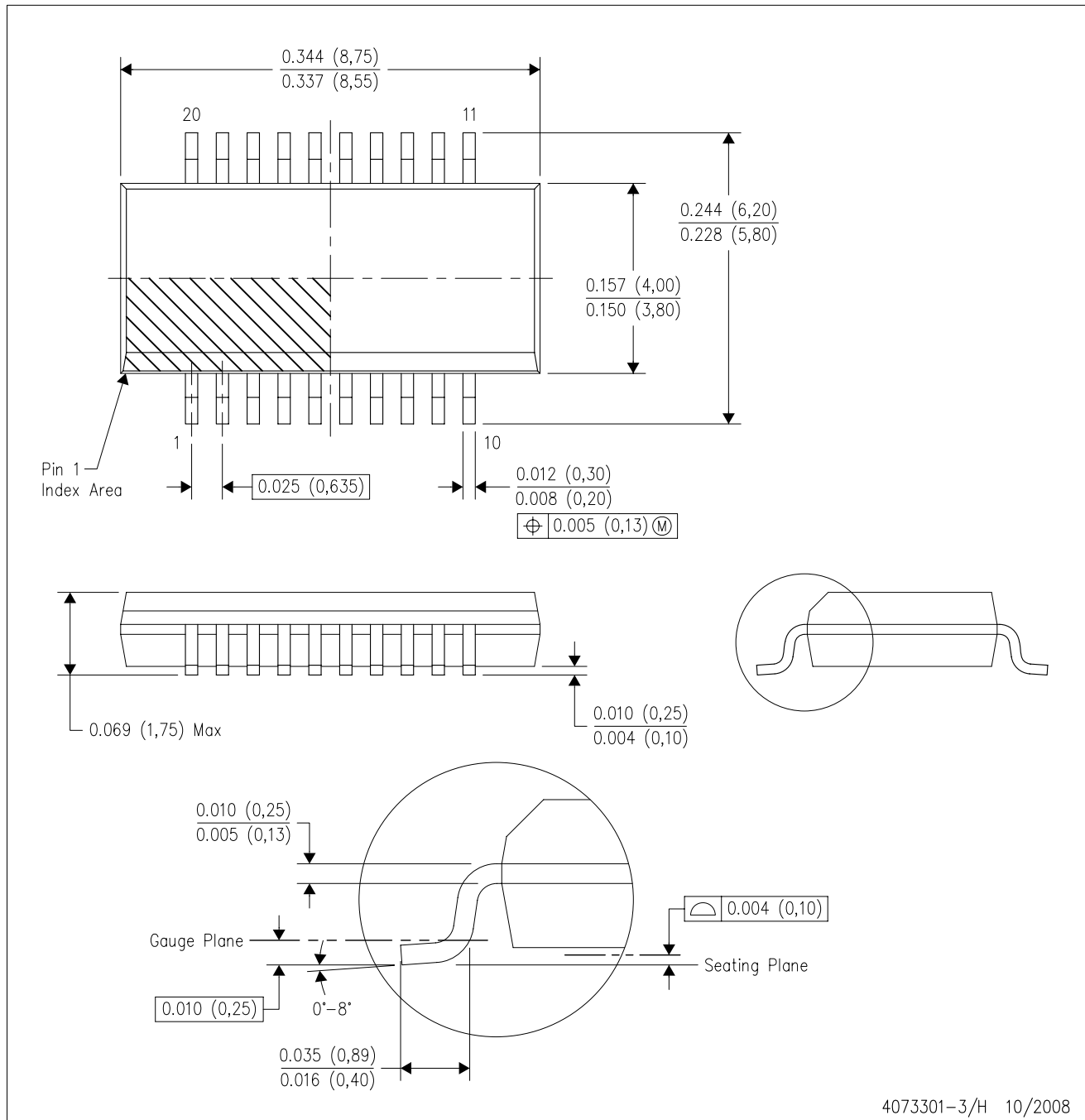
**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LVC2244ADW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LVC2244ADW.B	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LVC2244APW	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74LVC2244APW.B	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74LVC2244APWG4	PW	TSSOP	20	70	530	10.2	3600	3.5

DBQ (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
  - D. Falls within JEDEC MO-137 variation AD.

# DB0020A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

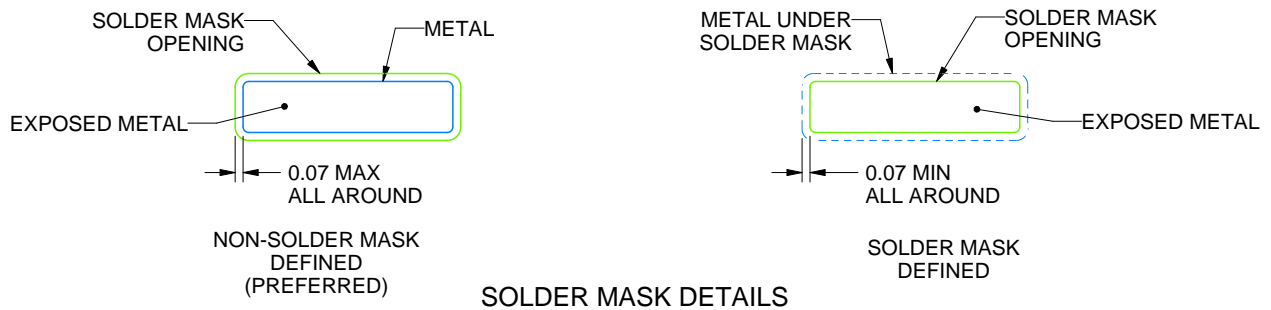
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

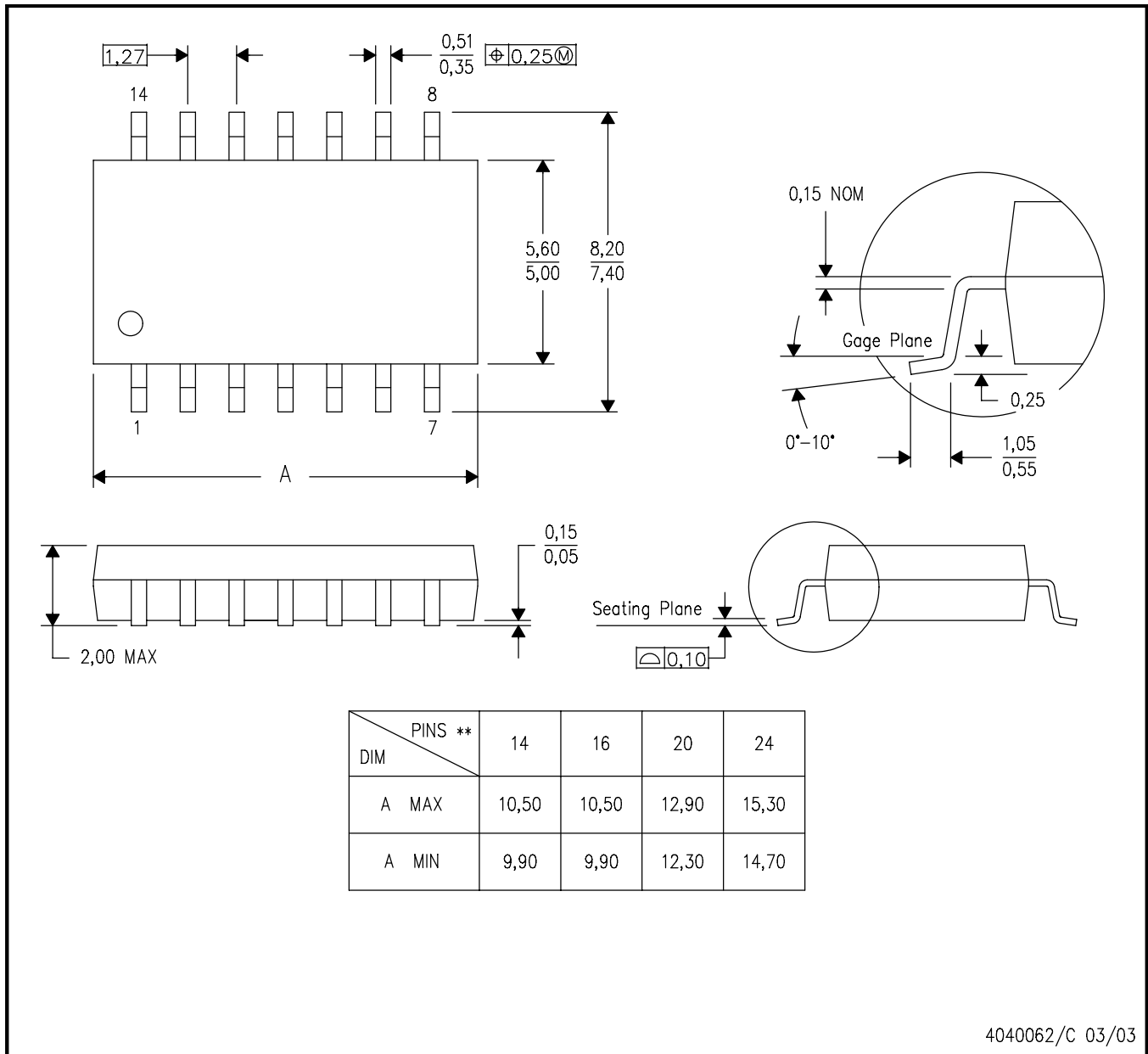
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)   
 14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G\*\*)

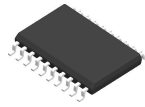
PLASTIC SMALL-OUTLINE

24 PINS SHOWN



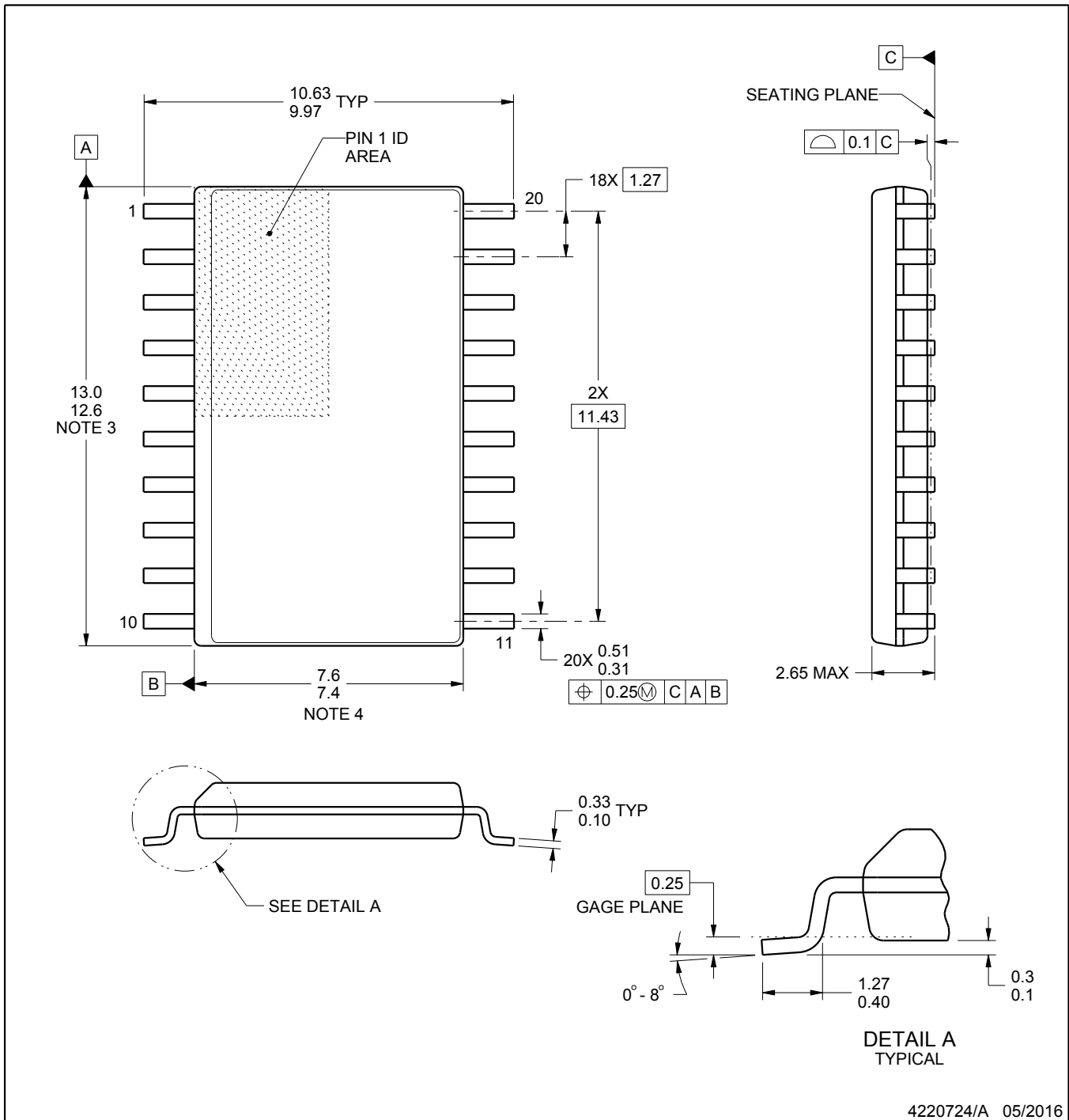
- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

# DW0020A



## PACKAGE OUTLINE SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW0020A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

### NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025