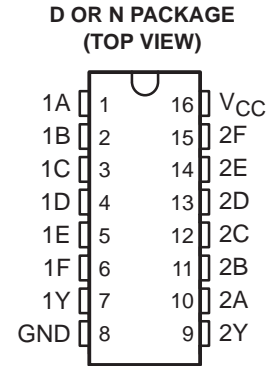


- Meets or Exceeds the Requirements of IBM™ System 360 Input/Output Interface Specification
- Operate From Single 5-V Supply
- TTL Compatible
- 3.11-V Output at $I_{OH} = -59.3 \text{ mA}$
- Uncommitted Emitter-Follower Output Structure for Party-Line Operation
- Short-Circuit Protection
- AND-OR Logic Configuration
- Designed for Use With Triple Line Receiver SN75124
- Designed to Be Interchangeable With N8T13 and N8T23



THE SN751730 IS RECOMMENDED
FOR NEW IBM 360/370 INTERFACE DESIGNS.

description

The SN75123 is a dual line driver specifically designed to meet the input/output interface specifications for IBM System 360. It also is compatible with standard-TTL logic and supply-voltage levels.

The SN75123 low-impedance emitter-follower outputs drive terminated lines such as coaxial cable or twisted pair. Having the outputs uncommitted allows wired-OR logic to be performed in party-line applications. Output short-circuit protection is provided by an internal clamping network that turns on when the output voltage drops below approximately 1.5 V. All the inputs are in conventional TTL configuration, and the gating can be used during power-up and power-down sequences to ensure that no noise is introduced to the line.

The SN75123 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS						OUTPUT Y
A	B	C	D	E	F	
H	H	H	H	X	X	H
X	X	X	X	H	H	H
All other input combinations						L

H = high level, L = low level, X = irrelevant



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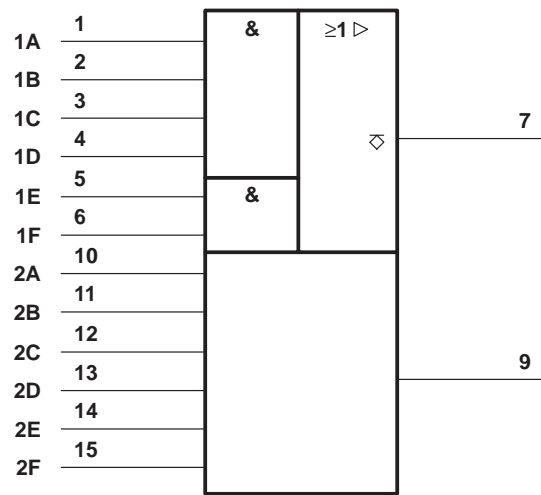
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SN75123
DUAL LINE DRIVER

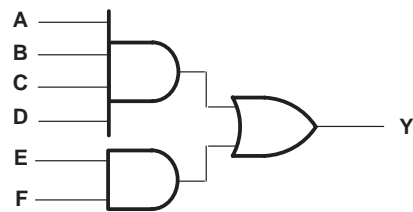
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			-100	mA
Operating free-air temperature, T_A	0		70	°C

SN75123

DUAL LINE DRIVER

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electrical characteristics, $V_{CC} = 4.75 \text{ V to } 5.25 \text{ V}$, $T_A = 0^\circ\text{C to } 70^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT	
V _{IK}	Input clamp voltage	V _{CC} = 5 V, I _I = −12 mA		−1.5		V	
V _{I(BR)}	Input breakdown voltage	V _{CC} = 5 V, I _I = 10 mA		5.5		V	
V _{OH}	High-level output voltage	V _{CC} = 5 V, V _{IH} = 2 V, I _{OH} = −59.3 mA, See Note 3	T _A = 25°C	3.11		V	
			T _A = 0°C to 70°C	2.9			
V _{OL}	Low-level output voltage	V _{IL} = 0.8 V, I _{OL} = −240 μA, See Note 3		0.15		V	
I _{OH}	High-level output current	V _{CC} = 5 V, V _{IH} = 4.5 V, V _{OH} = 2 V, T _A = 25°C, See Note 3			−100	−250	mA
I _{O(off)}	Off-state output current	V _{CC} = 0, V _O = 3 V			40		μA
I _{IH}	High-level input current	V _I = 4.5 V			40		μA
I _{IL}	Low-level input current	V _I = 0.4 V			−0.1	−1.6	mA
I _{OS}	Short-circuit output current†	V _{CC} = 5 V, T _A = 25°C		−30		mA	
I _{CCH}	Supply current, outputs high	V _{CC} = 5.25 V,	All inputs at 2 V,	Outputs open	28		mA
I _{CCL}	Supply current, outputs low	V _{CC} = 5.25 V,	All inputs at 0.8 V,	Outputs open	60		mA

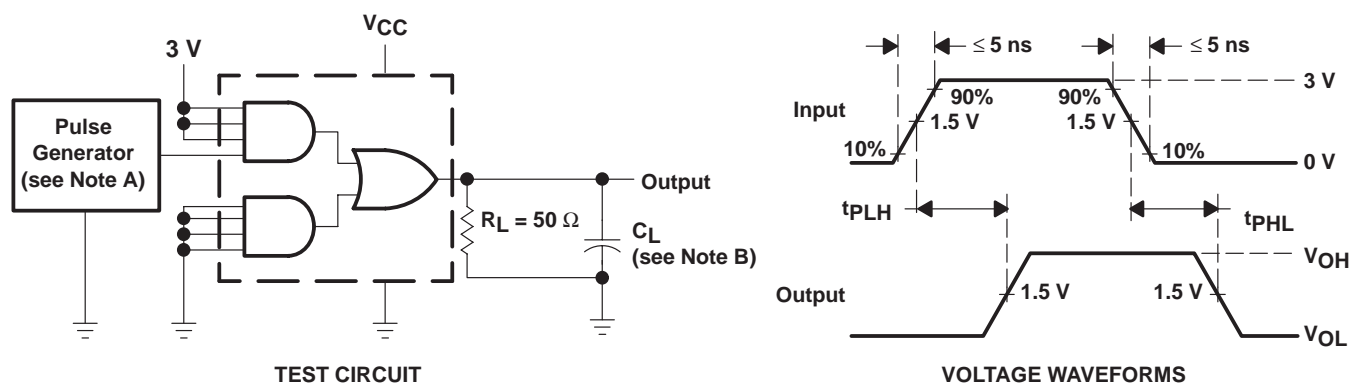
† Not more than one output should be shorted at a time.

NOTE 3: The output voltage and current limits are valid for any appropriate combination of high and low inputs specified by the function table for the desired output.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low- to high-level output	$R_L = 50 \Omega$, $C_L = 15 \text{ pF}$, See Figure 1		12	20	ns
t_{PHL} Propagation delay time, high- to low-level output	$R_L = 50 \Omega$, $C_L = 15 \text{ pF}$, See Figure 1		12	20	ns
t_{PLH} Propagation delay time, low- to high-level output	$R_L = 50 \Omega$, $C_L = 100 \text{ pF}$, See Figure 1		20	35	ns
t_{PHL} Propagation delay time, high- to low-level output	$R_L = 50 \Omega$, $C_L = 100 \text{ pF}$, See Figure 1		15	25	ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, $t_w = 200 \text{ ns}$, duty cycle = 50%.

B. C_L Includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

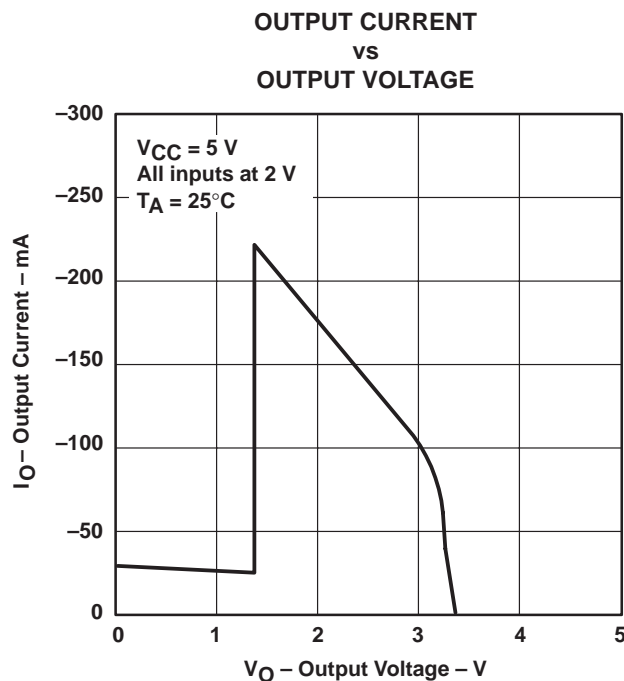


Figure 2

APPLICATION INFORMATION

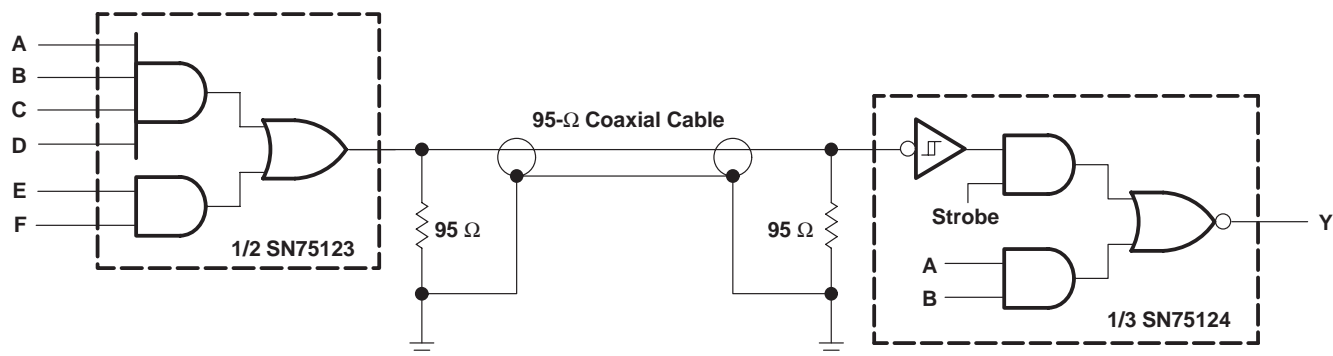


Figure 3. Unbalanced Line Communication Using SN75123 and SN75124

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75123N	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75123N
SN75123N.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75123N

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN75123N	N	PDIP	16	25	506	13.97	11230	4.32
SN75123N.A	N	PDIP	16	25	506	13.97	11230	4.32

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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