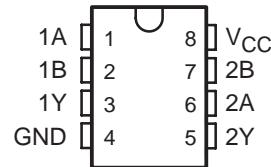


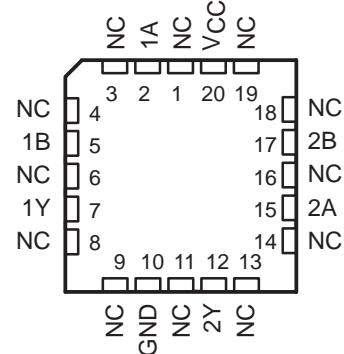
**PERIPHERAL DRIVERS FOR
HIGH-VOLTAGE, HIGH-CURRENT DRIVER
APPLICATIONS**

- Characterized for Use to 300 mA
- High-Voltage Outputs
- No Output Latch-Up at 30 V (After Conducting 300 mA)
- Medium-Speed Switching
- Circuit Flexibility for Varied Applications and Choice of Logic Function
- TTL-Compatible Diode-Clamped Inputs
- Standard Supply Voltages
- Plastic DIP (P) With Copper Lead Frame for Cooler Operation and Improved Reliability
- Package Options Include Plastic Small Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

SN55461, SN55462, SN55463 . . . JG PACKAGE
SN75461, SN75462, SN75463 . . . D OR P PACKAGE
(TOP VIEW)



SN55461, SN55462, SN55463 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

SUMMARY OF SERIES 55461/75461

| DEVICE | LOGIC | PACKAGES |
|---------|-------|----------|
| SN55461 | AND | FK, JG |
| SN55462 | NAND | FK, JG |
| SN55463 | OR | FK, JG |
| SN75461 | AND | D, P |
| SN75462 | NAND | D, P |
| SN75463 | OR | D, P |

description

These dual peripheral drivers are functionally interchangeable with SN55451B through SN55453B and SN75451B through SN75453B peripheral drivers, but are designed for use in systems that require higher breakdown voltages than those devices can provide at the expense of slightly slower switching speeds. Typical applications include logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers.

The SN55461/SN75461, SN55462/SN75462, and SN55463/SN75463 are dual peripheral AND, NAND, and OR drivers respectively (assuming positive logic), with the output of the gates internally connected to the bases of the npn output transistors.

Series SN55461 drivers are characterized for operation over the full military temperature range of -55°C to 125°C . Series SN75461 drivers are characterized for operation from 0°C to 70°C .

SN55461 THRU SN55463

SN75461 THRU SN75463

DUAL PERIPHERAL DRIVERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | SN55' | SN75' | UNIT |
|---|------------------------------|--------------|-------------|
| Supply voltage, V_{CC} (see Note 1) | 7 | 7 | V |
| Input voltage, V_I | 5.5 | 5.5 | V |
| Integrator voltage (see Note 2) | 5.5 | 5.5 | V |
| Off-state output voltage, V_O | 35 | 35 | V |
| Continuous collector or output current (see Note 3) | 400 | 400 | mA |
| Peak collector or output current ($t_W \leq 10$ ms, duty cycle $\leq 50\%$, see Note 4) | 500 | 500 | mA |
| Continuous total power dissipation | See Dissipation Rating Table | | |
| Operating free-air temperature range, T_A | -55 to 125 | 0 to 70 | °C |
| Storage temperature range, T_{STG} | -65 to 150 | -65 to 150 | °C |
| Case temperature for 60 seconds, T_C | FK package | 260 | °C |
| Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds | JG package | 300 | °C |
| Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds | D or P package | 260 | °C |

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network GND unless otherwise specified.

2. This is the voltage between two emitters A and B.

3. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500Ω .

4. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

DISSIPATION RATING TABLE

| PACKAGE | $T_A \leq 25^\circ\text{C}$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 70^\circ\text{C}$ POWER RATING | $T_A = 125^\circ\text{C}$ POWER RATING |
|----------------|--|--|---|--|
| | | | $T_A = 70^\circ\text{C}$ POWER RATING | $T_A = 125^\circ\text{C}$ POWER RATING |
| D | 725 mW | 5.8 mW/°C | 464 mW | - |
| FK | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| JG | 1050 mW | 8.4 mW/°C | 672 mW | 210 mW |
| P | 1000 mW | 8.0 mW/°C | 640 mW | - |

recommended operating conditions

| | SN55' | | | SN75' | | | UNIT |
|---------------------------------------|--------------|------------|------------|--------------|------------|------------|-------------|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, V_{CC} | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level input voltage, V_{IH} | 2 | | | 2 | | | V |
| Low-level input voltage, V_{IL} | | | 0.8 | | | 0.8 | V |
| Operating free-air temperature, T_A | -55 | 125 | | 0 | 70 | | °C |



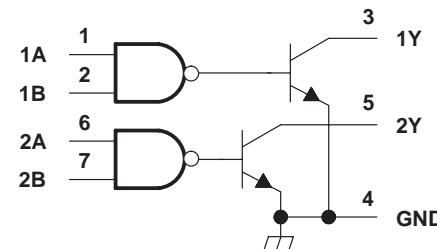
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251-1443

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, JG, and P packages.

logic diagram (positive logic)

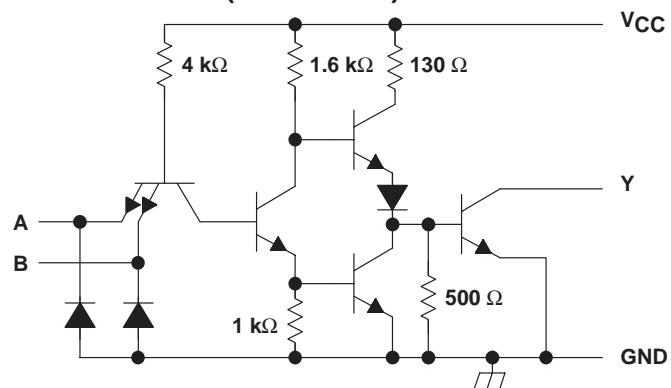


FUNCTION TABLE
(each driver)

| A | B | Y |
|---|---|---------------|
| L | L | L (on state) |
| L | H | L (on state) |
| H | L | L (on state) |
| H | H | H (off state) |

positive logic:
 $Y = AB \text{ or } \bar{A} + \bar{B}$

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

| PARAMETER | TEST CONDITIONS† | SN55461 | | | SN75461 | | | UNIT |
|-----------|--|---------|------|-----|---------|------|-----|---------------|
| | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| V_{IK} | $V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$ | -1.2 | -1.5 | | -1.2 | -1.5 | | V |
| I_{OH} | $V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $V_{OH} = 35 \text{ V}$ | | 300 | | | 100 | | μA |
| V_{OL} | $V_{CC} = \text{MIN}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 100 \text{ mA}$ | | 0.25 | 0.5 | | 0.25 | 0.4 | V |
| | $V_{CC} = \text{MIN}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 300 \text{ mA}$ | | 0.5 | 0.8 | | 0.5 | 0.7 | |
| I_I | $V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$ | | 1 | | | 1 | | mA |
| I_{IH} | $V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$ | | 40 | | | 40 | | μA |
| I_{IL} | $V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$ | -1 | -1.6 | | -1 | -1.6 | | mA |
| I_{CCH} | $V_{CC} = \text{MAX}$, $V_I = 5 \text{ V}$ | 8 | 11 | | 8 | 11 | | mA |
| I_{CCL} | $V_{CC} = \text{MAX}$, $V_I = 0$ | 56 | 76 | | 56 | 76 | | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|---|--|------------|-----|------|
| t_{PLH} | $I_O \approx 200 \text{ mA}$, $C_L = 15 \text{ pF}$, $R_L = 50 \Omega$, See Figure 1 | 30 | 55 | | ns |
| t_{PHL} | | 25 | 40 | | |
| t_{TLH} | | 8 | 20 | | |
| t_{THL} | | 10 | 20 | | |
| V_{OH} | $SN55461$ | $V_S = 30 \text{ V}$, $I_O \approx 300 \text{ mA}$, See Figure 2 | $V_S - 10$ | | mV |
| | $SN75461$ | | $V_S - 10$ | | |

**SN55461 THRU SN55463
SN75461 THRU SN75463
DUAL PERIPHERAL DRIVERS**

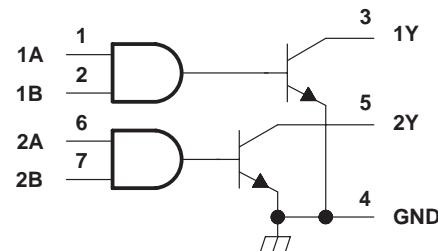
SLRS022A - DECEMBER 1976 - REVISED OCTOBER 1995

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, JG, and P packages.

logic diagram (positive logic)

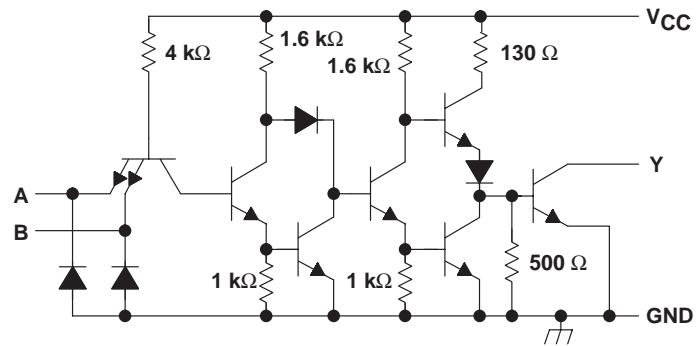


**FUNCTION TABLE
(each driver)**

| A | B | Y |
|---|---|---------------|
| L | L | H (off state) |
| L | H | H (off state) |
| H | L | H (off state) |
| H | H | L (on state) |

positive logic:
 $Y = AB \text{ or } A + B$

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

| PARAMETER | TEST CONDITIONS† | SN55462 | | | SN75462 | | | UNIT |
|-----------|---|---------|------|------|---------|------|------|---------------|
| | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| V_{IK} | $V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$ | | -1.2 | -1.5 | | -1.2 | -1.5 | V |
| I_{OH} | $V_{CC} = \text{MIN}$, $V_{IL} = 0.8 \text{ V}$, $V_{OH} = 35 \text{ V}$ | | 300 | | | 100 | | μA |
| V_{OL} | $V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $I_{OL} = 100 \text{ mA}$ | | 0.25 | 0.5 | | 0.25 | 0.4 | V |
| | $V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $I_{OL} = 300 \text{ mA}$ | | 0.5 | 0.8 | | 0.5 | 0.7 | |
| I_I | $V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$ | | 1 | | | 1 | | mA |
| I_{IH} | $V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$ | | 40 | | | 40 | | μA |
| I_{IL} | $V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$ | -1.1 | -1.6 | | -1.1 | -1.6 | | mA |
| I_{CCH} | $V_{CC} = \text{MAX}$, $V_I = 0$ | 13 | 17 | | 13 | 17 | | mA |
| I_{CLL} | $V_{CC} = \text{MAX}$, $V_I = 5 \text{ V}$ | 61 | 76 | | 61 | 76 | | mA |

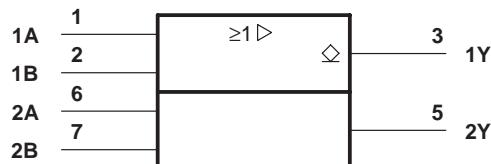
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

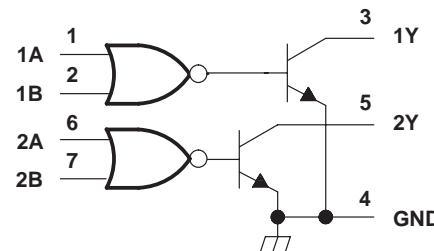
| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|---|---|-----|-----|------|
| t_{PLH} | $I_O \approx 200 \text{ mA}$, $C_L = 15 \text{ pF}$, $R_L = 50 \Omega$, See Figure 1 | | 45 | 65 | ns |
| t_{PHL} | | | 30 | 50 | |
| t_{TLH} | | | 13 | 25 | |
| t_{THL} | | | 10 | 20 | |
| V_{OH} | SN55462 SN75462 | $V_S = 30 \text{ V}$, $I_O \approx 300 \text{ mA}$ | | | mV |
| | | $V_S - 10$ | | | |
| | | $V_S - 10$ | | | |

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, JG, and P packages.

logic diagram (positive logic)

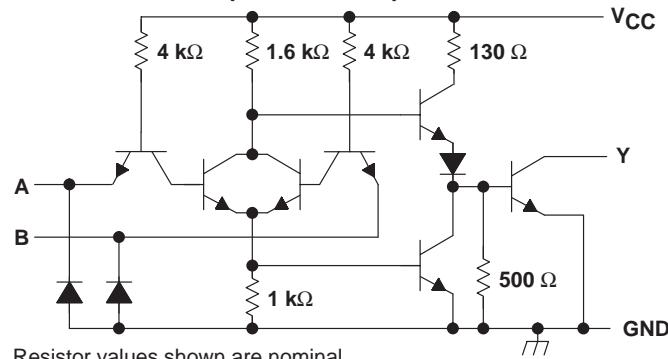


FUNCTION TABLE (each driver)

| A | B | Y |
|---|---|---------------|
| L | L | L (on state) |
| L | H | H (off state) |
| H | L | H (off state) |
| H | H | H (off state) |

positive logic: $Y = A + B$ or $\overline{A} \overline{B}$

schematic (each driver)



electrical characteristics over recommended operating free-air temperature range

| PARAMETER | TEST CONDITIONS [†] | SN55463 | | | SN75463 | | | UNIT | |
|------------------|--|--|------------------|------|---------|------------------|------|------|----|
| | | MIN | TYP [‡] | MAX | MIN | TYP [‡] | MAX | | |
| V _{IK} | Input clamp voltage | V _{CC} = MIN, I _I = -12 mA | | -1.2 | -1.5 | | -1.2 | -1.5 | V |
| I _{OH} | High-level output current | V _{CC} = MIN, V _{IH} = MIN, V _{OH} = 35 V | | 300 | | | 100 | | µA |
| V _{OL} | Low-level output voltage | V _{CC} = MIN, V _{IL} = 0.8 V, I _{OL} = 100 mA | | 0.25 | 0.5 | | 0.25 | 0.4 | V |
| | | V _{CC} = MIN, V _{IL} = 0.8 V, I _{OL} = 300 mA | | 0.5 | 0.8 | | 0.5 | 0.7 | |
| I _I | Input current at maximum input voltage | V _{CC} = MAX, V _I = 5.5 V | | 1 | | | 1 | | mA |
| I _{IH} | High-level input current | V _{CC} = MAX, V _I = 2.4 V | | 40 | | | 40 | | µA |
| I _{IL} | Low-level input current | V _{CC} = MAX, V _I = 0.4 V | | -1 | -1.6 | | -1 | -1.6 | mA |
| I _{CCH} | Supply current, outputs high | V _{CC} = MAX, V _I = 5 V | | 8 | 11 | | 8 | 11 | mA |
| I _{CCL} | Supply current, outputs low | V _{CC} = MAX, V _I = 0 | | 58 | 76 | | 58 | 76 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

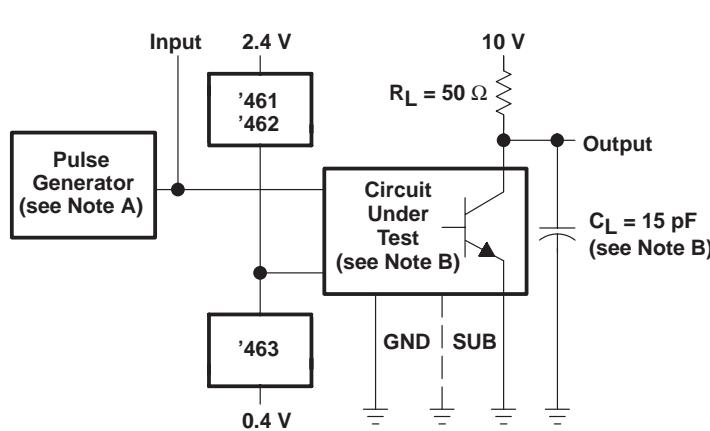
switching characteristics, $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|-----------------|--|--|--|--------------------------------|--------------------|------|----|
| tPLH | Propagation delay time, low-to-high-level output | $I_O \approx 200 \text{ mA}$, $C_L = 15 \text{ pF}$, $R_L = 50 \Omega$, See Figure 1 | 30 | 55 | | ns | |
| tPHL | Propagation delay time, high-to-low-level output | | 25 | 40 | | | |
| tTLH | Transition time, low-to-high-level output | | 8 | 25 | | | |
| tTHL | Transition time, high-to-low-level output | | 10 | 25 | | | |
| V _{OH} | High-level output voltage after switching | SN55463 | $V_S = 30 \text{ V}$, See Figure 2 | $I_O \approx 300 \text{ mA}$, | V _S -10 | | |
| | | SN75463 | | | V _S -10 | | mV |

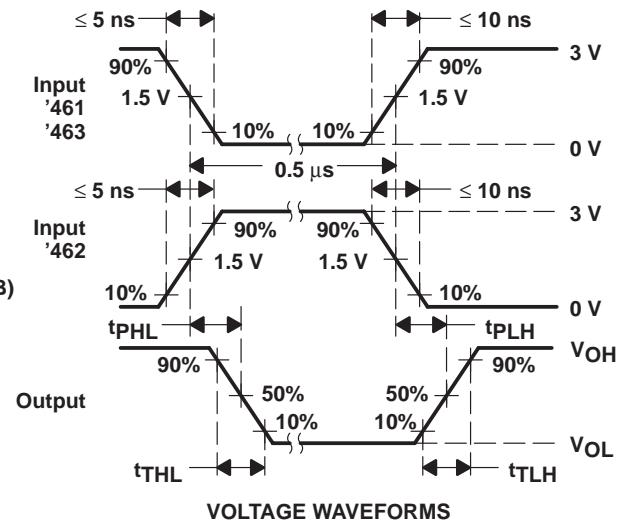
**SN55461 THRU SN55463
SN75461 THRU SN75463
DUAL PERIPHERAL DRIVERS**

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PARAMETER MEASUREMENT INFORMATION

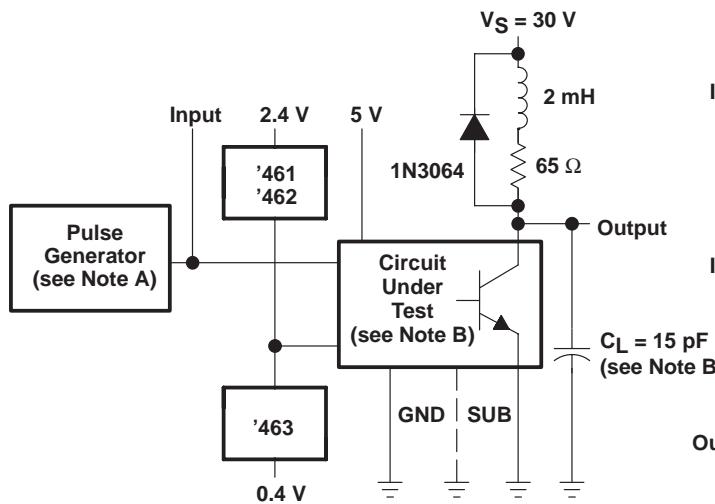


TEST CIRCUIT

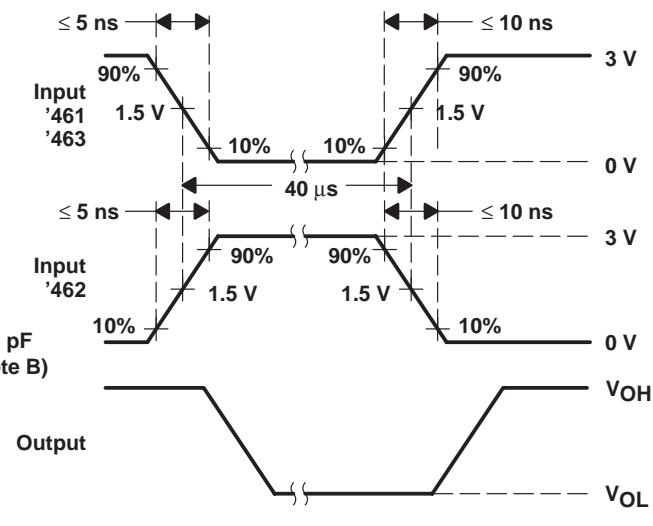


NOTES: A. The pulse generator has the following characteristics: PRR \leq 1 MHz, $Z_O \approx 50 \Omega$.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms for Switching Times



TEST CIRCUIT



NOTES: A. The pulse generator has the following characteristics: PRR \leq 12.5 kHz, $Z_O = 50 \Omega$.
B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit and Voltage Waveforms for Latch-Up Test

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|----------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|----------------------|
| JM38510/12908BPA | Active | Production | CDIP (JG) 8 | 50 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510 /12908BPA |
| JM38510/12908BPA.A | Active | Production | CDIP (JG) 8 | 50 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510 /12908BPA |
| M38510/12908BPA | Active | Production | CDIP (JG) 8 | 50 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510 /12908BPA |
| SN75462D | Active | Production | SOIC (D) 8 | 75 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75462 |
| SN75462D.A | Active | Production | SOIC (D) 8 | 75 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75462 |
| SN75462DR | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75462 |
| SN75462DR.A | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75462 |
| SN75462P | Active | Production | PDIP (P) 8 | 50 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN75462P |
| SN75462P.A | Active | Production | PDIP (P) 8 | 50 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN75462P |
| SN75462PE4 | Active | Production | PDIP (P) 8 | 50 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN75462P |
| SN75463P | Active | Production | PDIP (P) 8 | 50 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN75463P |
| SN75463P.A | Active | Production | PDIP (P) 8 | 50 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN75463P |
| SNJ55462FK | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SNJ55 462FK |
| SNJ55462FK.A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SNJ55 462FK |
| SNJ55462JG | Active | Production | CDIP (JG) 8 | 50 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SNJ55462JG |
| SNJ55462JG.A | Active | Production | CDIP (JG) 8 | 50 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SNJ55462JG |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

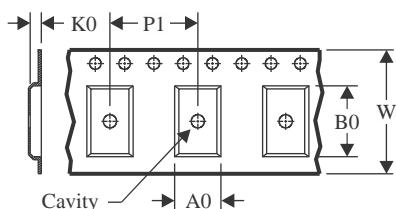
OTHER QUALIFIED VERSIONS OF SN55462, SN75462 :

- Catalog : [SN75462](#)
- Military : [SN55462](#)

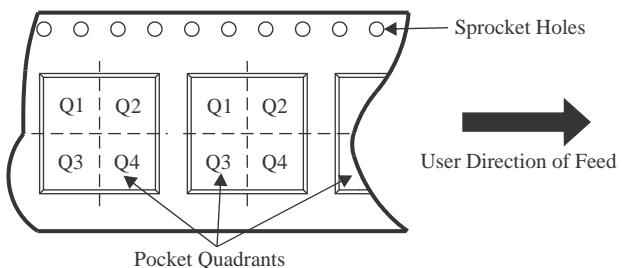
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN75462DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN75462DR | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |

TUBE


*All dimensions are nominal

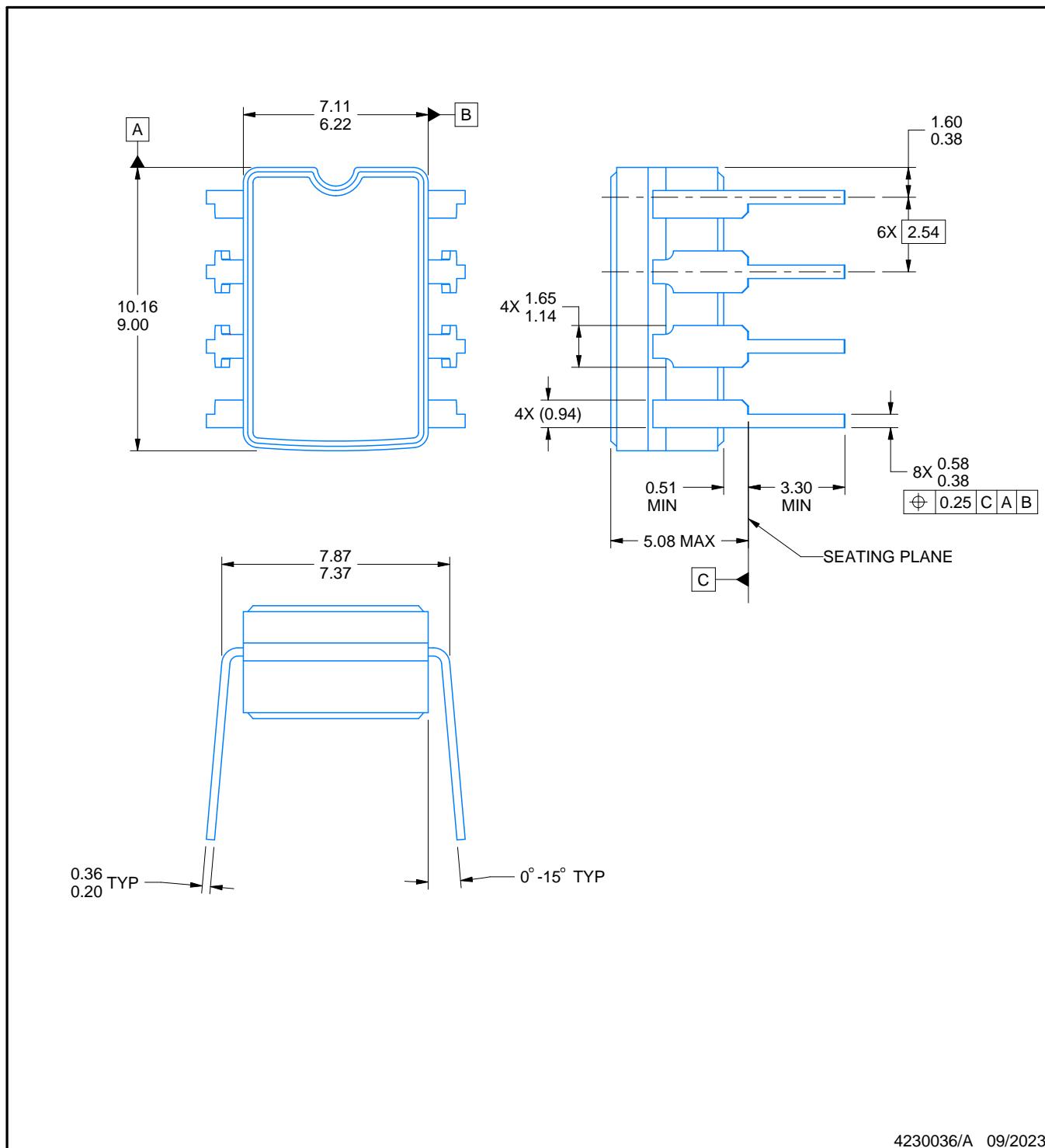
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|--------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN75462D | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| SN75462D.A | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| SN75462P | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| SN75462P.A | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| SN75462PE4 | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| SN75463P | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| SN75463P.A | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| SNJ55462FK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ55462FK.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |

PACKAGE OUTLINE

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



NOTES:

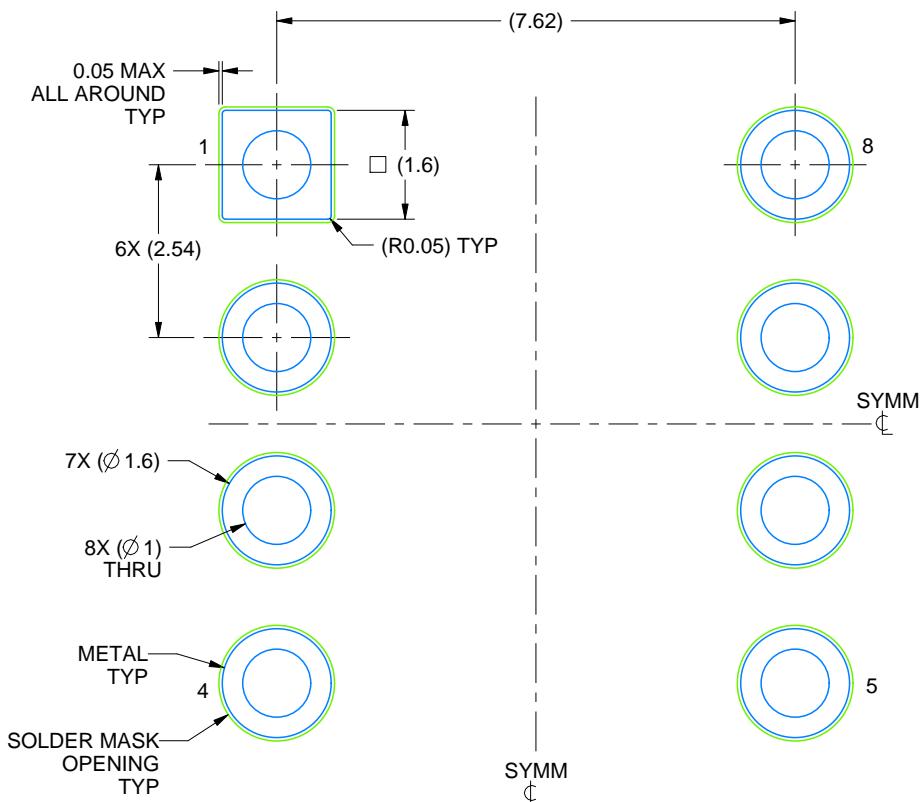
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8

EXAMPLE BOARD LAYOUT

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



LAND PATTERN EXAMPLE
NON SOLDER MASK DEFINED
SCALE: 9X

4230036/A 09/2023

GENERIC PACKAGE VIEW

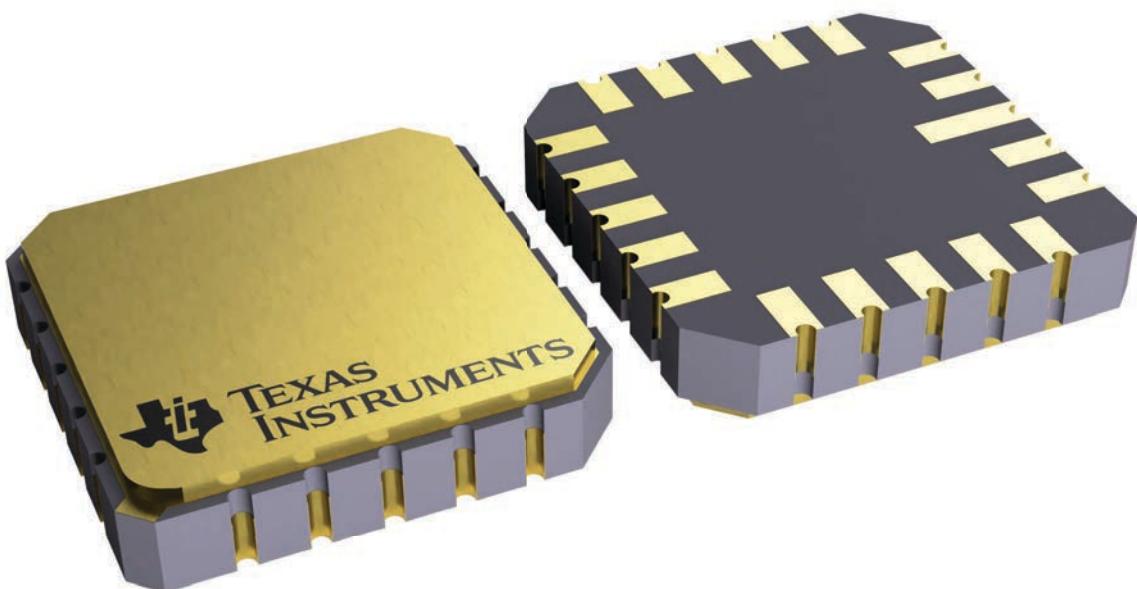
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



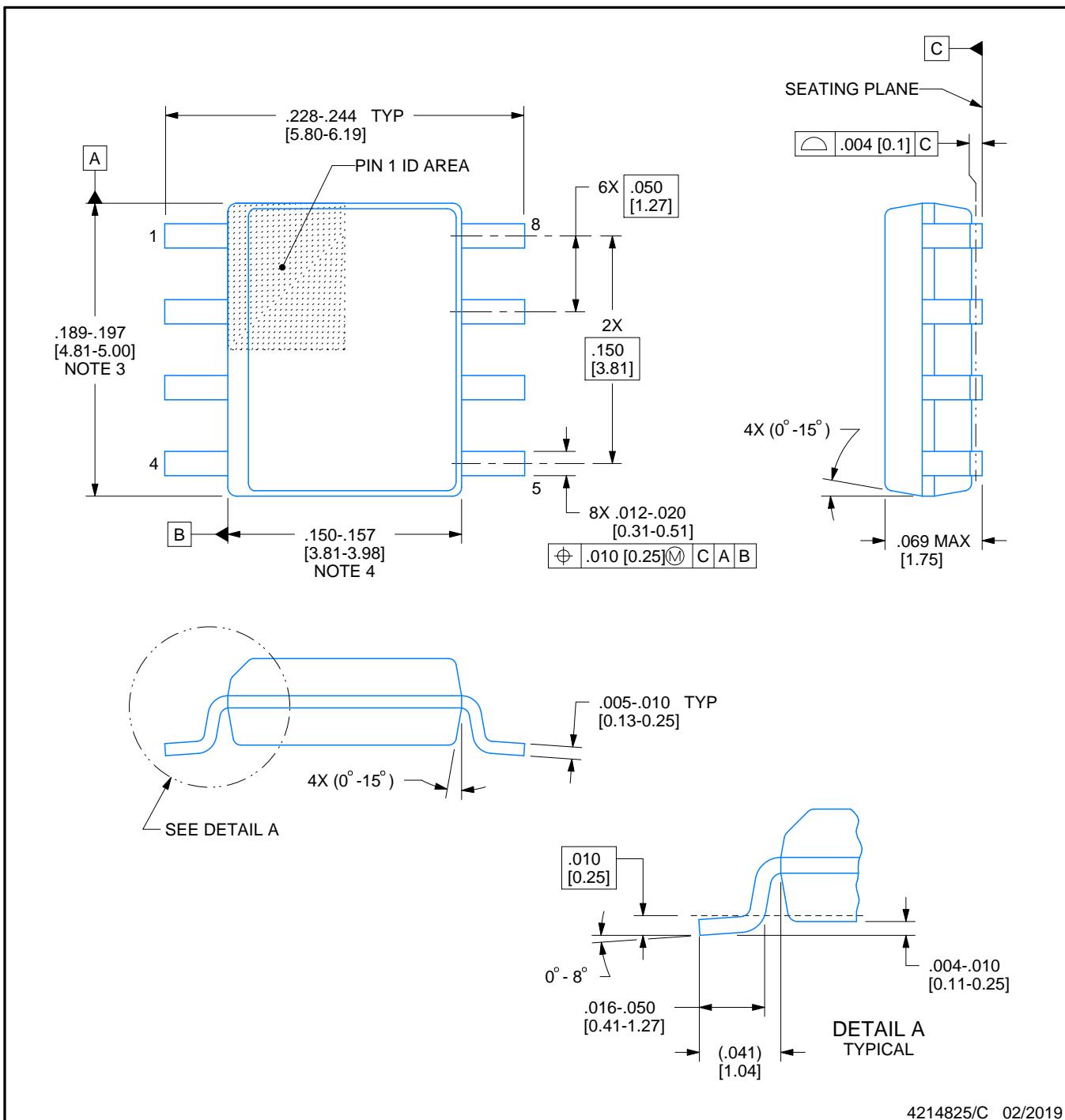
4229370VA\



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

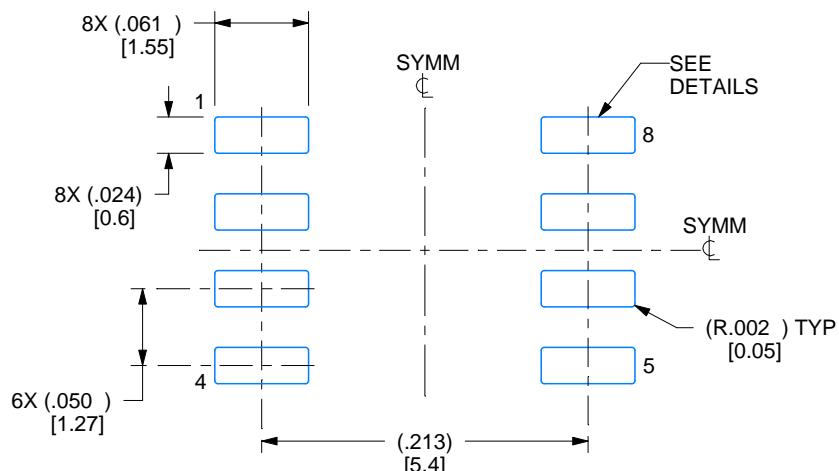
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

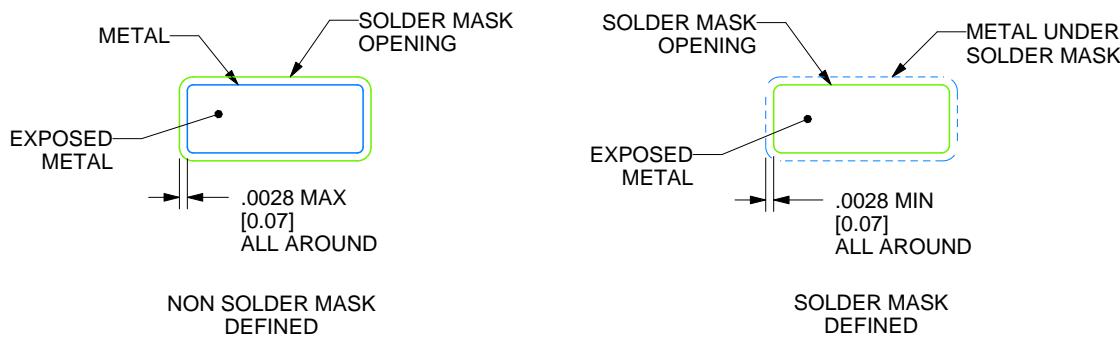
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

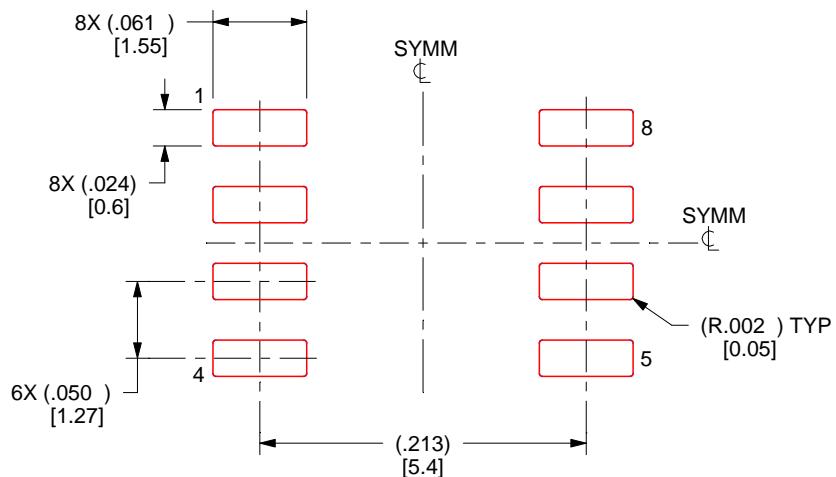
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

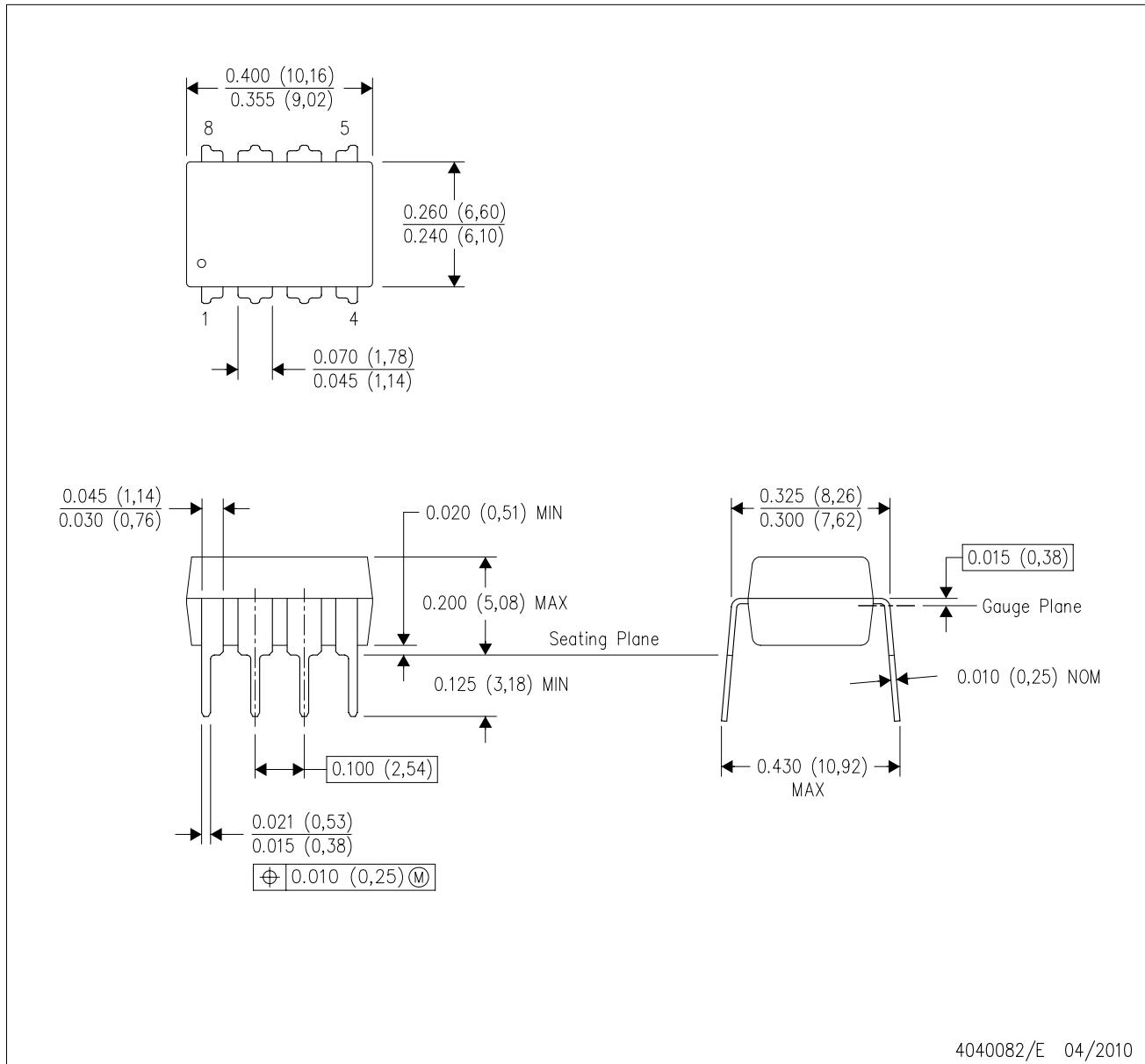
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001 variation BA.

4040082/E 04/2010

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