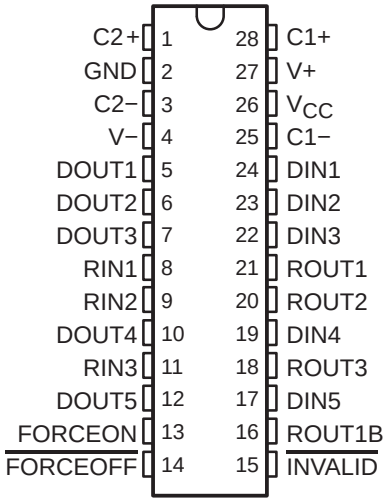
- **Auto-powerdown Plus**
- **Operate With 3-V to 5.5-V V_{CC} Supply**
- **Always-Active Noninverting Receiver Output (ROUT1B)**
- **Support Operation From 250 kbit/s to 1 Mbit/s**
- **Low Standby Current . . . 1 μA Typ**
- **External Capacitors . . . 4 × 0.1 μF**
- **Accept 5-V Logic Input With 3.3-V Supply**
- **Inter-Operable With SN65C3243, SN75C3243**
- **RS-232 Bus-Pin ESD Protection Exceeds ±15-kV Using Human-Body Model (HBM)**
- **Applications**
  - **Battery-Powered Systems, PDAs, Notebooks, Sub-Notebooks, Laptops, Palmtop PCs, Hand-Held Equipment, Modems, and Printers**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description/ordering information

The ’C3238 devices consist of five line drivers, three line receivers, and a dual charge-pump circuit with ±15-kV ESD protection pin to pin (serial-port connection pins, including GND). The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. In addition, these devices include an always-active noninverting output (ROUT1B), which allows applications using the ring indicator to transmit data while the device is powered down. These devices operate at data signaling rates up to 1 Mbit/s and at an increased slew-rate range of 24 V/μs to 150 V/μs.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−0°C to 70°C	SOIC (DW)	Tube of 20	SN75C3238DW	75C3238
		Reel of 1000	SN75C3238DWR	
	SSOP (DB)	Reel of 2000	SN75C3238DBR	75C3238
	TSSOP (PW)	Tube of 50	SN75C3238PW	CA3238
		Reel of 2000	SN75C3238PWR	
−40°C to 85°C	SOIC (DW)	Tube of 20	SN65C3238DW	65C3238
		Reel of 1000	SN65C3238DWR	
	SSOP (DB)	Reel of 2000	SN65C3238DBR	65C3238
	TSSOP (PW)	Tube of 50	SN65C3238PW	CB3238
		Reel of 2000	SN65C3238PWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

description/ordering information (continued)

Flexible control options for power management are featured when the serial-port and driver inputs are inactive. The auto-powerdown plus feature functions when FORCEON is low and $\overline{\text{FORCEOFF}}$ is high. During this mode of operation, if the device does not sense valid signal transitions on all receiver and driver inputs for 30 s, the built-in charge-pump and drivers are powered down, reducing the supply current to 1 μA. By disconnecting the serial port or placing the peripheral drivers off, auto-powerdown plus will occur if there is no activity in the logic levels for the driver inputs. Auto-powerdown plus can be disabled when FORCEON and $\overline{\text{FORCEOFF}}$ are high. With auto-powerdown plus enabled, the device automatically activates once a valid signal is applied to any receiver or driver input. $\overline{\text{INVALID}}$ is high (valid data) if any receiver input voltage is greater than 2.7 V or less than −2.7 V or has been between −0.3 V and 0.3 V for less than 30 μs. $\overline{\text{INVALID}}$ is low (invalid data) if all receiver input voltages are between −0.3 V and 0.3 V for more than 30 μs. Refer to Figure 5 for receiver input levels.

Function Tables

EACH DRIVER

INPUTS				OUTPUT	DRIVER STATUS
DIN	FORCEON	$\overline{\text{FORCEOFF}}$	TIME ELAPSED SINCE LAST RIN OR DIN TRANSITION	DOUT	
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown plus disabled
H	H	H	X	L	
L	L	H	<30 s	H	Normal operation with auto-powerdown plus enabled
H	L	H	<30 s	L	
L	L	H	>30 s	Z	Powered off by auto-powerdown plus feature
H	L	H	>30 s	Z	

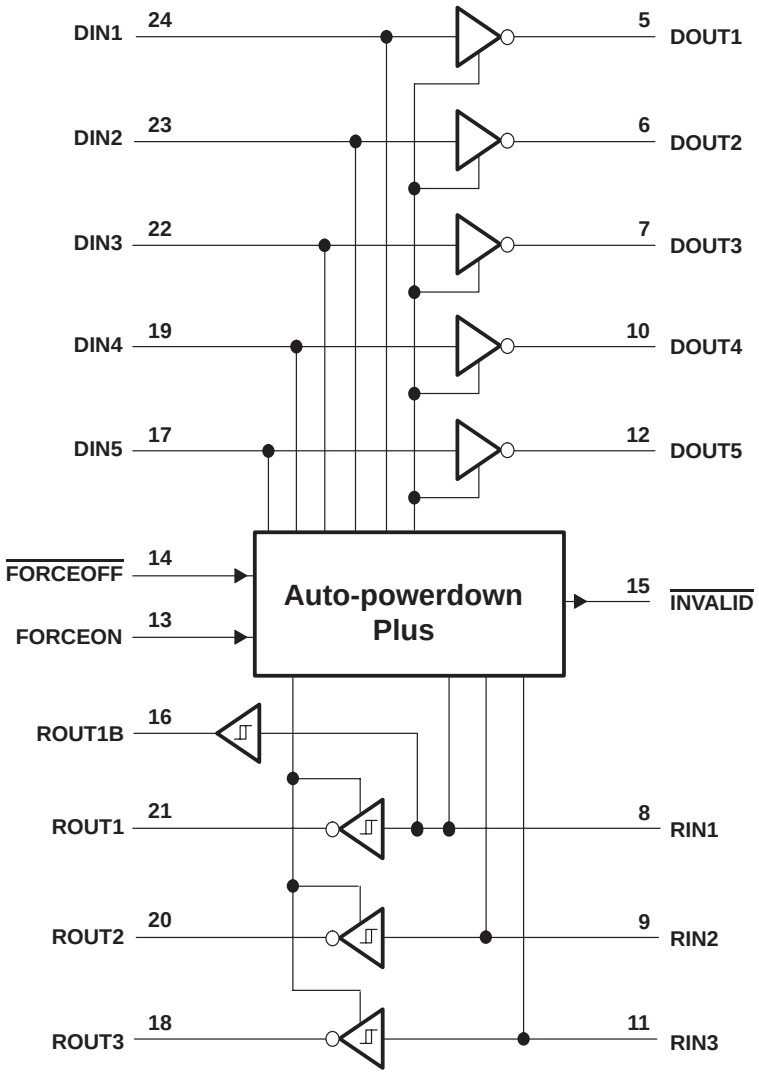
H = high level, L = low level, X = irrelevant, Z = high impedance

EACH RECEIVER

INPUTS				OUTPUTS		RECEIVER STATUS
RIN2	RIN1, RIN3−RIN5	$\overline{\text{FORCEOFF}}$	TIME ELAPSED SINCE LAST RIN OR DIN TRANSITION	ROUT1B	ROUT	
L	X	L	X	L	Z	Powered off while ROUT1B is active
H	X	L	X	H	Z	
L	L	H	<30 s	L	H	Normal operation with auto-powerdown plus disabled/enabled
L	H	H	<30 s	L	L	
H	L	H	<30 s	H	H	
H	H	H	<30 s	H	L	
Open	Open	H	>30 s	L	H	

H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.3 V to 6 V
Positive output supply voltage range, V+ (see Note 1) . . . . . −0.3 V to 7 V
Negative output supply voltage range, V− (see Note 1) . . . . . 0.3 V to −7 V
Supply voltage difference, V+ − V− (see Note 1) . . . . . 13 V
Input voltage range, V_I: Driver ($\overline{\text{FORCEOFF}}$, FORCEON) . . . . . −0.3 V to 6 V
Receiver . . . . . −25 V to 25 V
Output voltage range, V_O: Driver . . . . . − 13.2 V to 13.2 V
Receiver ($\overline{\text{INVALID}}$) . . . . . −0.3 V to V_{CC} + 0.3 V
Package thermal impedance, θ_{JA} (see Notes 2 and 3): DB package . . . . . 62°C/W
DW package . . . . . 46°C/W
PW package . . . . . 62°C/W
Operating virtual junction temperature, T_J . . . . . 150°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to network GND.
2. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4 and Figure 6)

				MIN	NOM	MAX	UNIT
	Supply voltage		V_{CC} = 3.3 V	3	3.3	3.6	V
			V_{CC} = 5 V	4.5	5	5.5	
V_{IH}	Driver and control high-level input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON	V_{CC} = 3.3 V	2			V
			V_{CC} = 5 V	2.4			
V_{IL}	Driver and control low-level input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON				0.8	V
V_I	Driver and control input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON		0		5.5	V
V_I	Receiver input voltage			−25		25	V
T_A	Operating free-air temperature		SN75C3238	0		70	°C
			SN65C3238	−40		85	

NOTE 4: Testing supply conditions are C1−C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.15 V; C1−C4 = 0.22 μF at V_{CC} = 3.3 V ± 0.3 V; and C1 = 0.047 μF and C2−C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

PARAMETER			TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
I_I	Input leakage current	$\overline{\text{FORCEOFF}}$, FORCEON			±0.01	±1	μA
I_{CC}	Supply current	Auto-powerdown plus disabled	No load, $\overline{\text{FORCEOFF}}$ and FORCEON at V_{CC}		0.5	2	mA
		Powered off	No load, $\overline{\text{FORCEOFF}}$ at GND		1	10	μA
		Auto-powerdown plus enabled	No load, $\overline{\text{FORCEOFF}}$ at V_{CC}, FORCEON at GND, All RIN are open or grounded		1	10	

‡ All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

NOTE 4: Testing supply conditions are C1−C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.15 V; C1−C4 = 0.22 μF at V_{CC} = 3.3 V ± 0.3 V; and C1 = 0.047 μF and C2−C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	All DOUT at R_L = 3 kΩ to GND			5	5.4		V
V_{OL}	Low-level output voltage	All DOUT at R_L = 3 kΩ to GND			−5	−5.4		V
I_{IH}	High-level input current	$V_I = V_{CC}$				±0.01	±1	µA
I_{IL}	Low-level input current	V_I at GND				±0.01	±1	µA
I_{OS}	Short-circuit output current‡	V_{CC} = 3.6 V,	V_O = 0 V			±35	±60	mA
		V_{CC} = 5.5 V,	V_O = 0 V			±40	±90	
r_o	Output resistance	V_{CC}, V+, and V− = 0 V,	V_O = ±2 V		300	10M		Ω
I_{off}	Output leakage current	$\overline{\text{FORCEOFF}}$ = GND	V_O = ±12 V,	V_{CC} = 3 V to 3.6 V			±25	µA
			V_O = ±10 V,	V_{CC} = 4.5 V to 5.5 V			±25	

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
‡ Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.
NOTE 4: Testing supply conditions are C1−C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.15 V; C1−C4 = 0.22 µF at V_{CC} = 3.3 V ± 0.3 V; and C1 = 0.047 µF and C2−C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
	Maximum data rate (see Figure 1)	R_L = 3 kΩ, One DOUT switching	C_L = 1000 pF		250			kbit/s
			C_L = 250 pF,	V_{CC} = 3 V to 4.5 V	1000			
			C_L = 1000 pF,	V_{CC} = 4.5 V to 5.5 V	1000			
$t_{sk(p)}$	Pulse skew§	C_L = 150 pF to 2500 pF,	R_L = 3 kΩ to 7 kΩ, See Figure 2			25		ns
SR(tr)	Slew rate, transition region (see Figure 1)	C_L = 150 pF to 1000 pF,	R_L = 3 kΩ to 7 kΩ,	V_{CC} = 3.3 V	18		150	V/µs

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
§ Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
NOTE 4: Testing supply conditions are C1−C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.15 V; C1−C4 = 0.22 µF at V_{CC} = 3.3 V ± 0.3 V; and C1 = 0.047 µF and C2−C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −1 mA	V_{CC} − 0.6 V	V_{CC} − 0.1 V		V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 3.3 V		1.5	2.4	V
		V_{CC} = 5 V		1.8	2.4	
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 3.3 V	0.6	1.2		V
		V_{CC} = 5 V	0.8	1.5		
V_{hys}	Input hysteresis ($V_{IT+} - V_{IT-}$)			0.3		V
I_{off}	Output leakage current (except ROUT1B)	$\overline{\text{FORCEOFF}}$ = 0 V		±0.05	±10	µA
r_i	Input resistance	V_I = ±3 V to ±25 V	3	5	7	kΩ

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

NOTE 4: Testing supply conditions are C1−C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.15 V; C1−C4 = 0.22 µF at V_{CC} = 3.3 V ± 0.3 V; and C1 = 0.047 µF and C2−C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 150 pF, See Figure 3		150		ns
t_{PHL}	Propagation delay time, high- to low-level output			150		ns
t_{en}	Output enable time	C_L = 150 pF, R_L = 3 kΩ, See Figure 4		200		ns
t_{dis}	Output disable time			200		ns
$t_{sk(p)}$	Pulse skew‡	See Figure 3		50		ns

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

‡ Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

NOTE 4: Testing supply conditions are C1−C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.15 V; C1−C4 = 0.22 µF at V_{CC} = 3.3 V ± 0.3 V; and C1 = 0.047 µF and C2−C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

AUTO-POWERDOWN PLUS SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{T+(valid)}$	Receiver input threshold for $\overline{\text{INVALID}}$ high-level output voltage	$\overline{\text{FORCEON}}$ = GND, $\overline{\text{FORCEOFF}}$ = V_{CC}			2.7	V
$V_{T-(valid)}$	Receiver input threshold for $\overline{\text{INVALID}}$ high-level output voltage	$\overline{\text{FORCEON}}$ = GND, $\overline{\text{FORCEOFF}}$ = V_{CC}	−2.7			V
$V_{T(invalid)}$	Receiver input threshold for $\overline{\text{INVALID}}$ low-level output voltage	$\overline{\text{FORCEON}}$ = GND, $\overline{\text{FORCEOFF}}$ = V_{CC}	−0.3		0.3	V
V_{OH}	$\overline{\text{INVALID}}$ high-level output voltage	I_{OH} = −1 mA, FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V_{CC}	V_{CC} − 0.6			V
V_{OL}	$\overline{\text{INVALID}}$ low-level output voltage	I_{OL} = 1.6 mA, FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V_{CC}			0.4	V

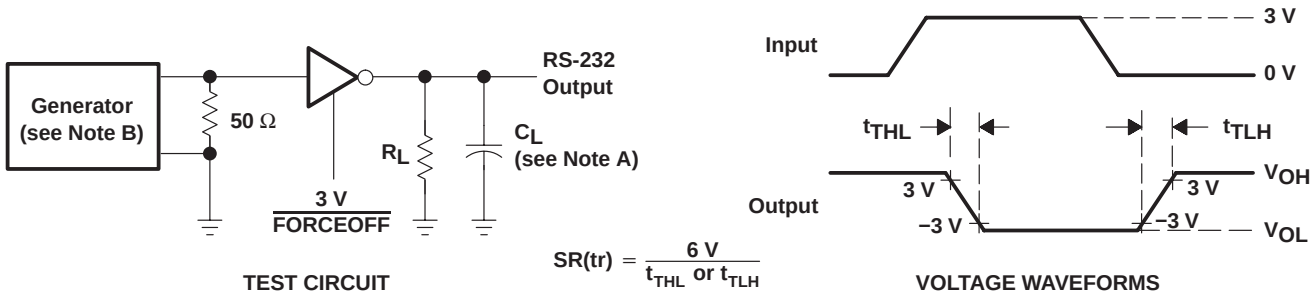
† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

PARAMETER		MIN	TYP†	MAX	UNIT
t_{valid}	Propagation delay time, low- to high-level output		0.1		µs
$t_{invalid}$	Propagation delay time, high- to low-level output		50		µs
t_{en}	Supply enable time		25		µs
t_{dis}	Receiver or driver edge to auto-powerdown plus	15	30	60	s

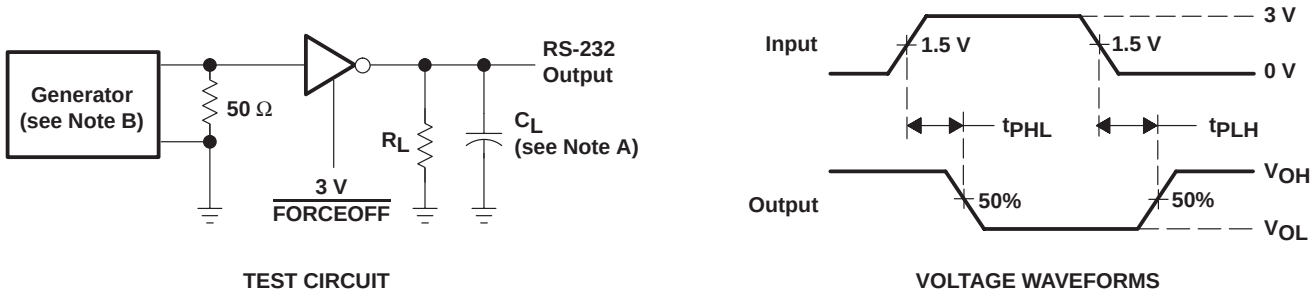
† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



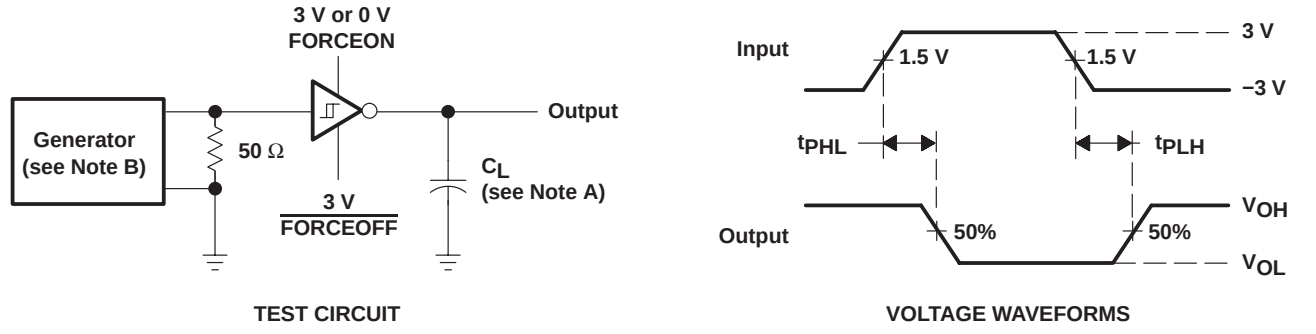
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 1 Mbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 1. Driver Slew Rate



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 1 Mbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

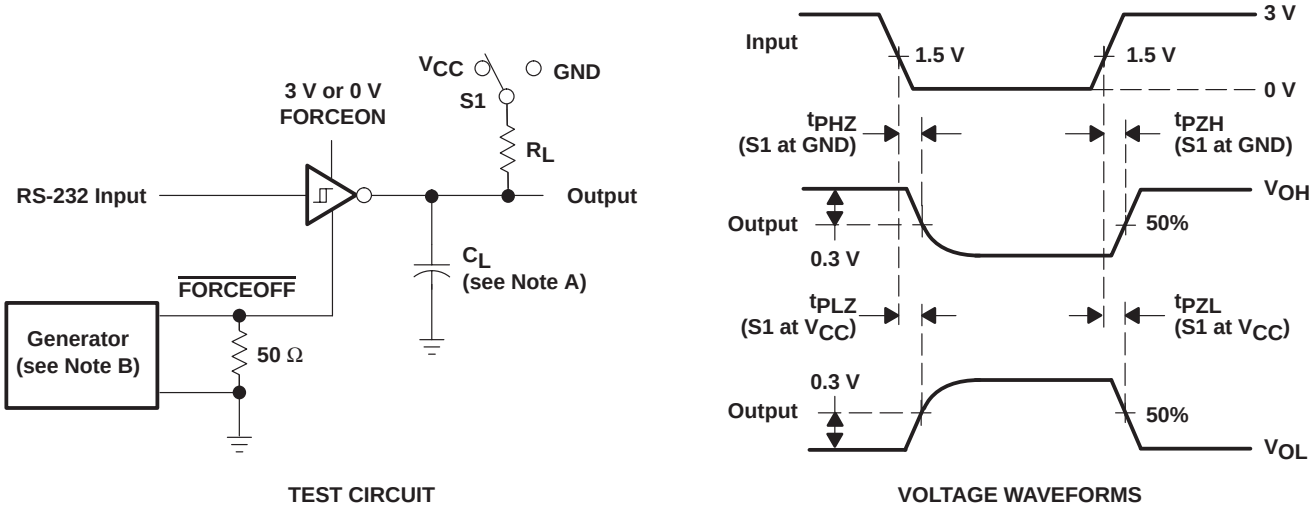
Figure 2. Driver Pulse Skew



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 3. Receiver Propagation Delay Times

PARAMETER MEASUREMENT INFORMATION

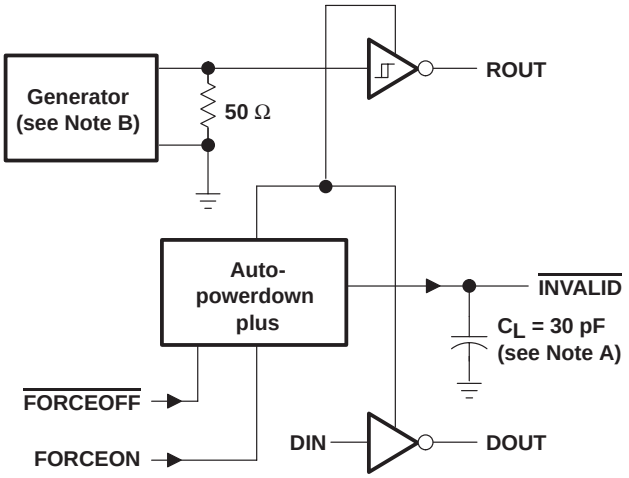


TEST CIRCUIT **VOLTAGE WAVEFORMS**

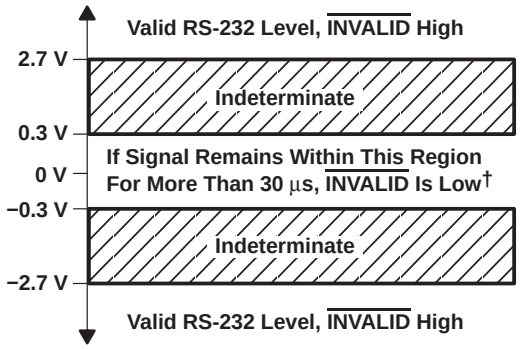
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.
C. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
D. t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 4. Receiver Enable and Disable Times

PARAMETER MEASUREMENT INFORMATION

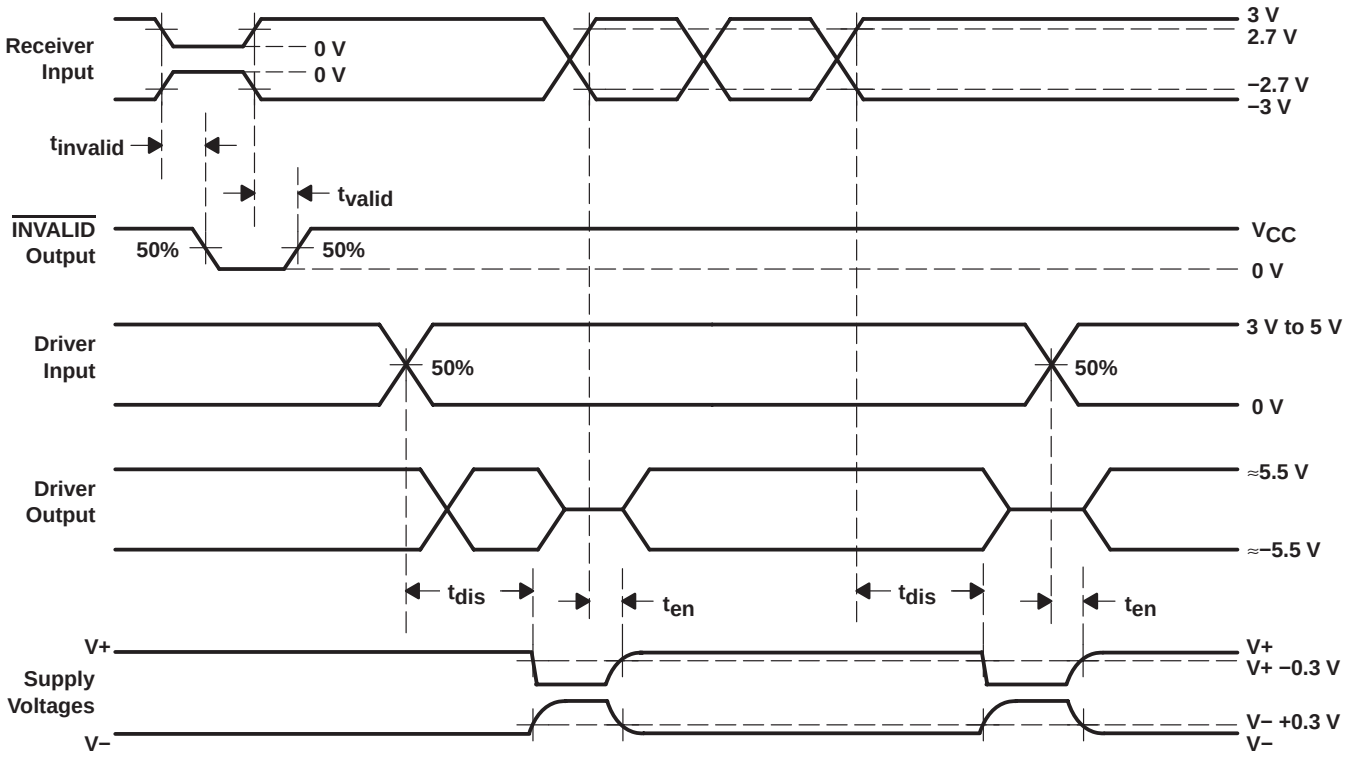


TEST CIRCUIT



† Auto-powerdown plus disables drivers and reduces supply current to 1 μA.

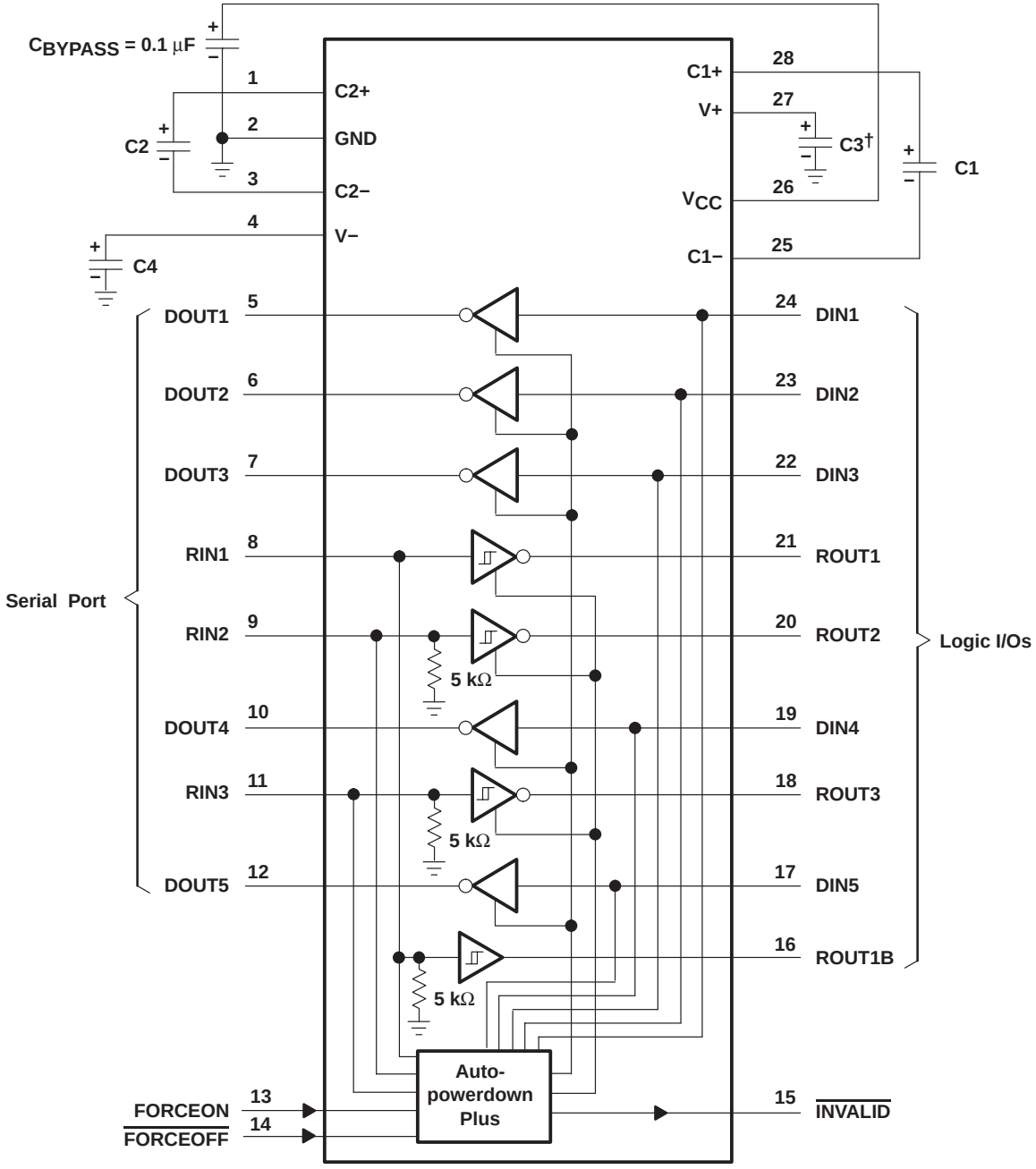
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 5 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.



Voltage Waveforms and Timing Diagrams

Figure 5. $\overline{\text{INVALID}}$ Propagation Delay Times and Supply Enabling Time

APPLICATION INFORMATION



† C3 can be connected to V_{CC} or GND.

NOTE A: Resistor values shown are nominal.

V_{CC} vs CAPACITOR VALUES

V_{CC}	C1	C2, C3, and C4
3.3 V ± 0.15 V	0.1 μF	0.1 μF
3.3 V ± 0.3 V	0.22 μF	0.22 μF
5 V ± 0.5 V	0.047 μ F	0.33 μF
3 V to 5.5 V	0.22 μF	1 μF

Figure 6. Typical Operating Circuit and Capacitor Values

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65C3238DBR	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3238
SN65C3238DBR.A	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3238
SN65C3238DBR.B	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3238
SN65C3238DWR	Active	Production	SOIC (DW) | 28	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3238
SN65C3238DWR.A	Active	Production	SOIC (DW) | 28	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3238
SN65C3238PW	Obsolete	Production	TSSOP (PW) | 28	-	-	Call TI	Call TI	-40 to 85	CB3238
SN65C3238PWR	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3238
SN65C3238PWR.A	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3238
SN65C3238PWR.B	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3238
SN75C3238DBR	Obsolete	Production	SSOP (DB) | 28	-	-	Call TI	Call TI	0 to 70	75C3238
SN75C3238DW	Active	Production	SOIC (DW) | 28	20 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3238
SN75C3238DW.A	Active	Production	SOIC (DW) | 28	20 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3238
SN75C3238DWR	Active	Production	SOIC (DW) | 28	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3238
SN75C3238DWR.A	Active	Production	SOIC (DW) | 28	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3238
SN75C3238PW	Obsolete	Production	TSSOP (PW) | 28	-	-	Call TI	Call TI	0 to 70	CA3238
SN75C3238PWR	Obsolete	Production	TSSOP (PW) | 28	-	-	Call TI	Call TI	0 to 70	CA3238

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

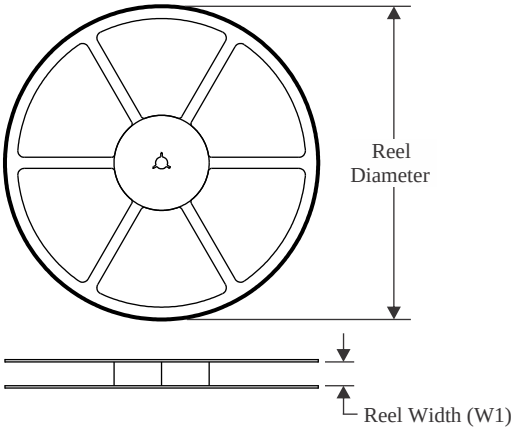
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

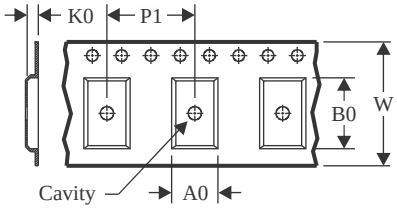
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

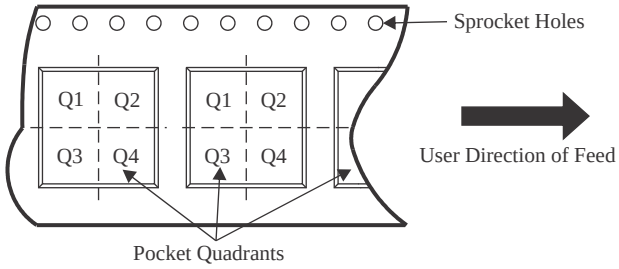


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

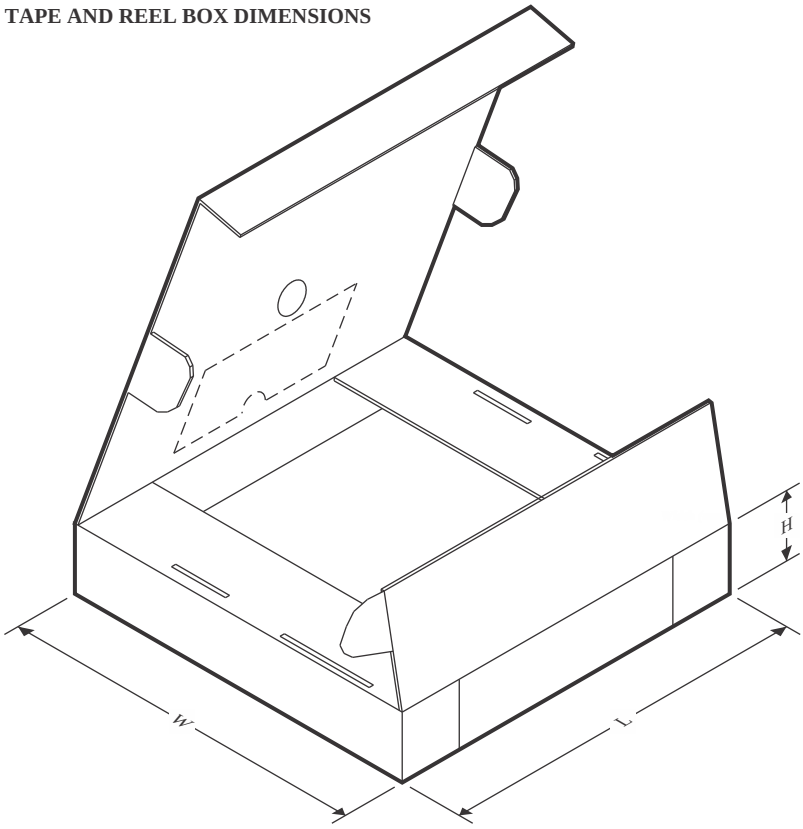
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65C3238DBR	SSOP	DB	28	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
SN65C3238DWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
SN65C3238PWR	TSSOP	PW	28	2000	330.0	16.4	6.75	10.1	1.8	12.0	16.0	Q1
SN75C3238DWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

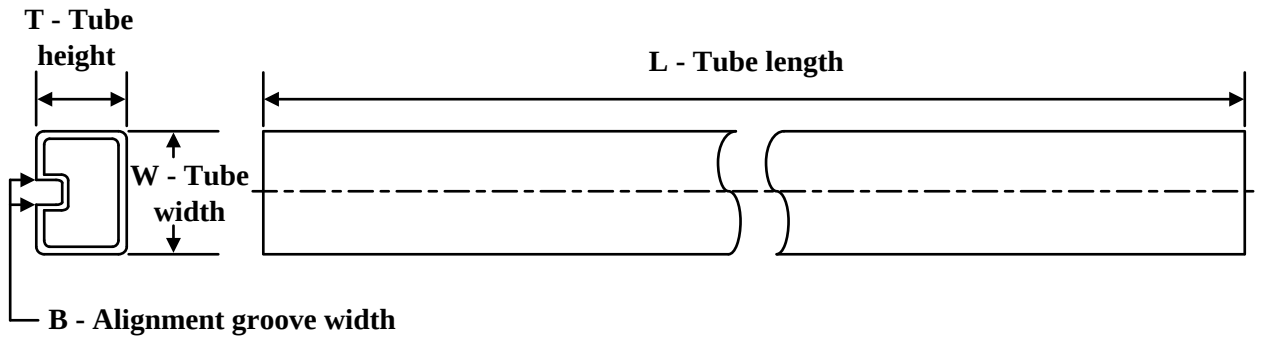
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65C3238DBR	SSOP	DB	28	2000	353.0	353.0	32.0
SN65C3238DWR	SOIC	DW	28	1000	350.0	350.0	66.0
SN65C3238PWR	TSSOP	PW	28	2000	353.0	353.0	32.0
SN75C3238DWR	SOIC	DW	28	1000	350.0	350.0	66.0

TUBE



*All dimensions are nominal

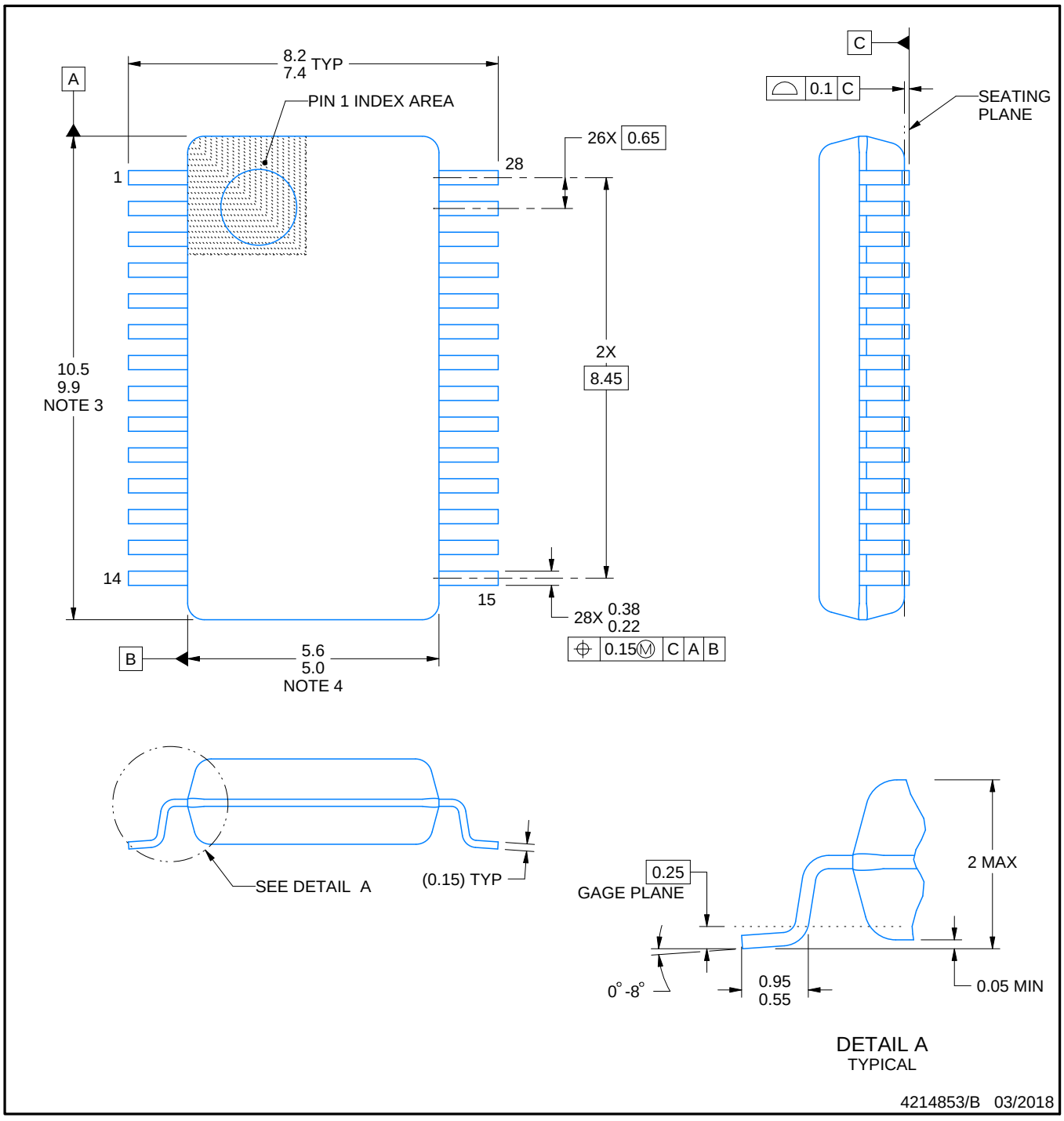
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75C3238DW	DW	SOIC	28	20	506.98	12.7	4826	6.6
SN75C3238DW.A	DW	SOIC	28	20	506.98	12.7	4826	6.6

PACKAGE OUTLINE

DB0028A

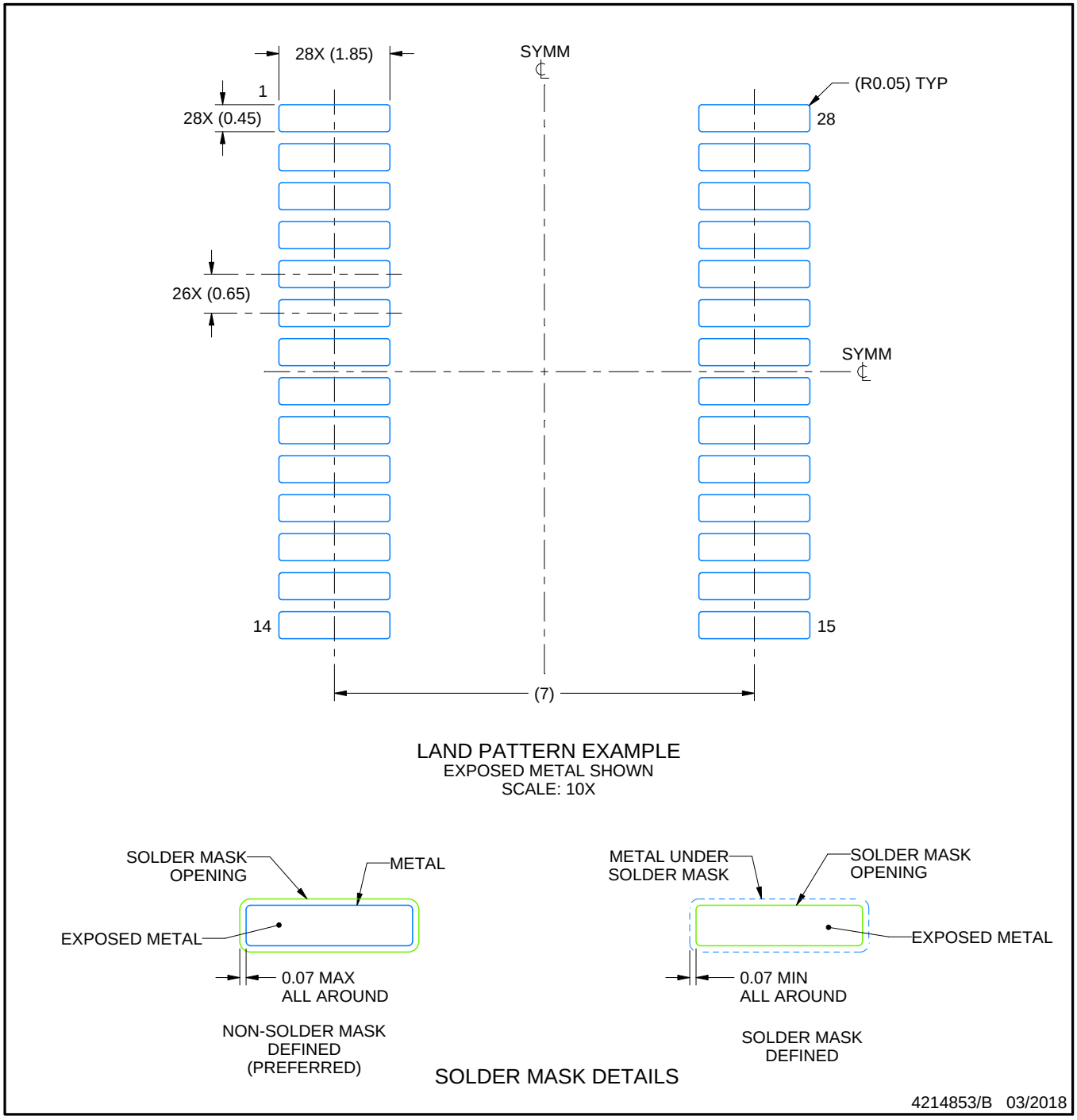
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



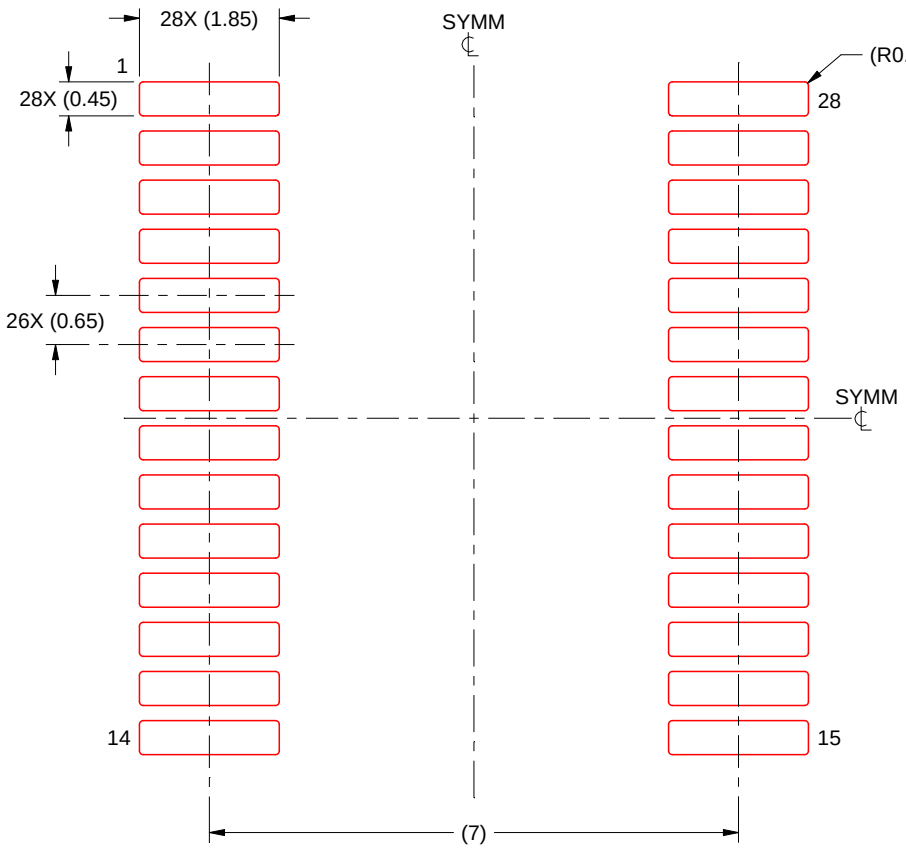
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



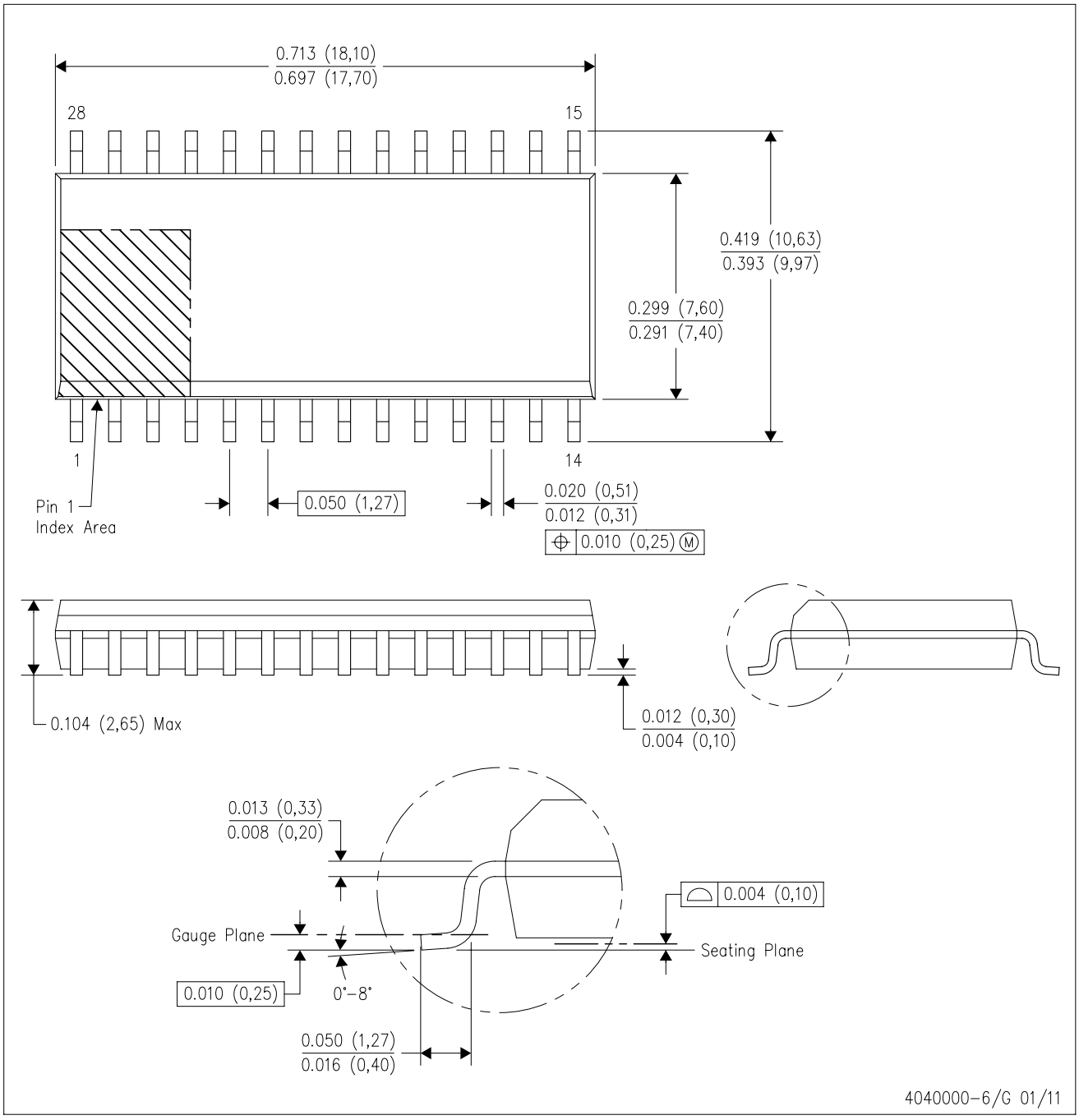
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214853/B 03/2018

NOTES: (continued)

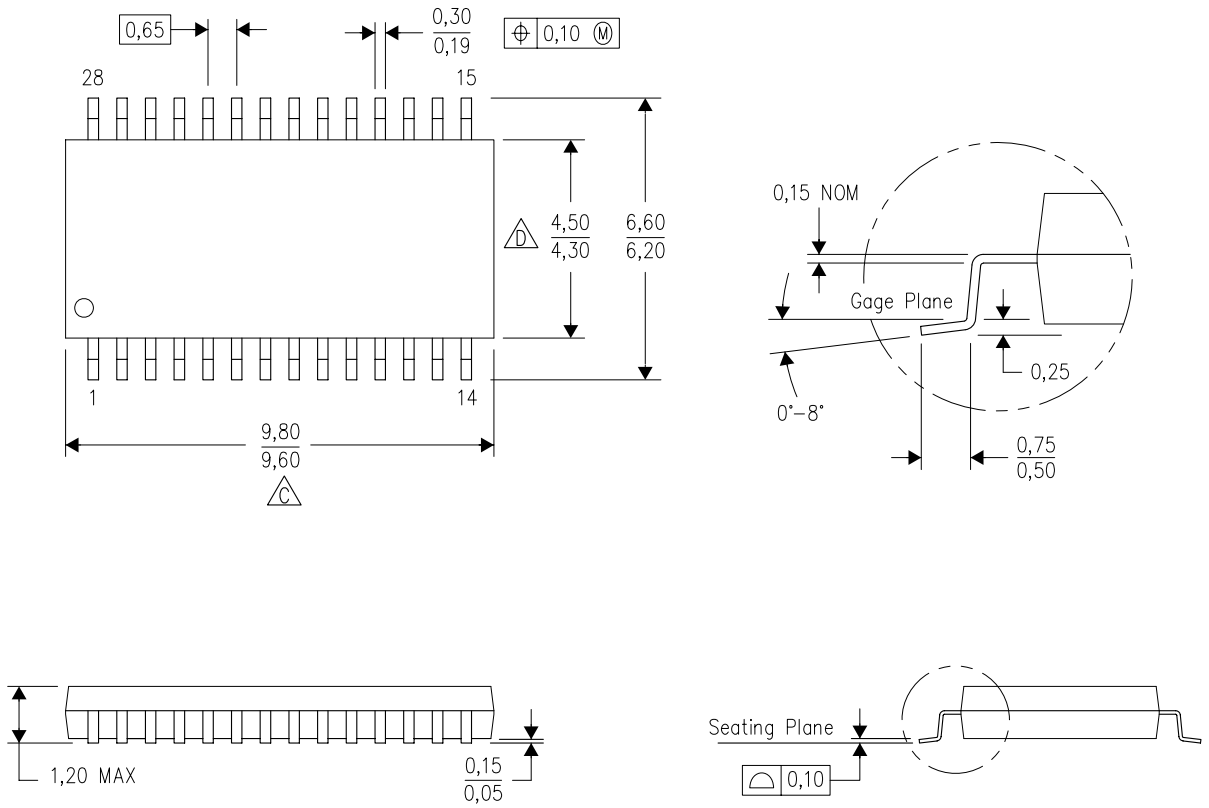
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AE.

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



4040064–7/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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