TCAL6408 8-Bit Translating I^{2}C-Bus, SMBus I/O Expander With Interrupt Output, Reset, and Agile I/O Configuration Registers

1 Features

- Operating power-supply voltage range of 1.08V to 3.6V
- Allows bidirectional voltage-level translation and GPIO expansion between 1.2V, 1.8V, 2.5V, and 3.3V I^{2}C bus and p-ports
- Low standby current consumption of 1µA typical at 1.8V
- 1MHz fast mode plus I^{2}C bus
- Hardware address pin allows two devices on the same I^{2}C, SMBus bus
- Active-low reset input ($\overline{\text{RESET}}$)
- Open-drain active-low interrupt output ($\overline{\text{INT}}$)
- Input or output configuration register
- Polarity inversion register
- Configurable I/O drive strength register
- Pull-up and pull-down resistor configuration register
- Internal power-on reset
- Noise filter on SCL or SDA inputs
- Latched outputs with high-current drive maximum capability for directly driving LEDs
- Latch-up performance exceeds 100mA per JESD 78, class II
- ESD protection exceeds JESD 22
  - 4000V Human-body model (A114-A)
  - 1000V Charged-device model (C101)

2 Applications

- Servers
- Routers (telecom switching equipment)
- Personal computers
- Personal electronics
- Industrial automation
- Gaming consoles
- Products with GPIO-limited processors

3 Description

The TCAL6408 device provides general purpose parallel input/output (I/O) expansion for the two-line bidirectional I^{2}C bus (or SMBus) protocol. The device can operate with a power supply voltage ranging from 1.08V to 3.6V on the I^{2}C bus side (V$_{CCI}$) and a power supply voltage ranging from 1.08V to 3.6V on the P-port side (V$_{CCP}$).

The device supports 100kHz (Standard-mode), 400kHz (Fast-mode), and 1MHz (fast-mode-plus) I^{2}C clock frequencies. I/O expanders such as the TCAL6408 provide a simple solution when additional I/Os are needed for switches, sensors, push-buttons, LEDs, fans, and so on.

The TCAL6408 has Agile I/O ports which include additional features designed to enhance the I/O performance in terms of speed, power consumption and EMI. The additional features are: programmable output drive strength, programmable pull-up and pull-down resistors, latchable inputs, maskable interrupt, interrupt status register, and programmable open-drain or push-pull outputs.

Package Information

PART NUMBER	PACKAGE[1]	PACKAGE SIZE[2]
TCAL6408	TSSOP (16)	6.4mm × 6.40mm
	UQFN (16)	2.6mm × 1.8mm
	X2QFN (16)	1.6mm x 1.6mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.


Simplified Schematic

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4 Pin Configuration and Functions

Figure 4-1. PW (TSSOP) Package, 16-Pin (Top View)
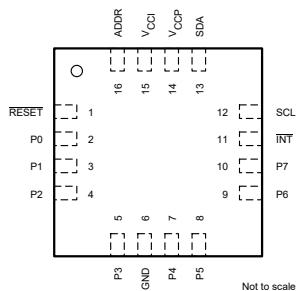
Figure 4-2. RSV (UQFN) Package, 16-Pin (Top View)
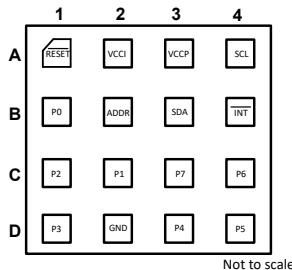
Figure 4-3. DTU (X2QFN) Package, 16-Pin (Top View)

Table 4-1. Pin Functions

NAME	PIN			TYPE[1]	DESCRIPTION
	PW (TSSOP)	RSV (UQFN)	DTU (X2QFN)		
ADDR	2	16	B2	I	Address input. Connect directly to V_{CCP} or ground
GND	8	6	D2	–	Ground
INT	13	11	B4	O	Interrupt output. Connect to V_{CCI} or V_{CCP} through a pull-up resistor
P0	4	2	B1	I/O	P-port input/output (push-pull design structure). At power on, P0 is configured as an input
P1	5	3	C2	I/O	P-port input/output (push-pull design structure). At power on, P1 is configured as an input
P2	6	4	C1	I/O	P-port input/output (push-pull design structure). At power on, P2 is configured as an input
P3	7	5	D1	I/O	P-port input/output (push-pull design structure). At power on, P3 is configured as an input
P4	9	7	D3	I/O	P-port input/output (push-pull design structure). At power on, P4 is configured as an input
P5	10	8	D4	I/O	P-port input/output (push-pull design structure). At power on, P5 is configured as an input
P6	11	9	C4	I/O	P-port input/output (push-pull design structure). At power on, P6 is configured as an input
P7	12	10	C3	I/O	P-port input/output (push-pull design structure). At power on, P7 is configured as an input
RESET	3	1	A1	I	Active-low reset input. Connect to V_{CCI} through a pull-up resistor, if no active connection is used
SCL	14	12	A4	I	Serial clock bus. Connect to V_{CCI} through a pull-up resistor
SDA	15	13	B3	I/O	Serial data bus. Connect to V_{CCI} through a pull-up resistor
V_{CCI}	1	15	A2	–	Supply voltage of I^{2}C bus. Connect directly to the supply voltage of the external I^{2}C controller
V_{CCP}	16	14	A3	–	Supply voltage of TCAL6408 for P-ports

(1)   I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

				MIN	MAX	UNIT
V_{CCI}, V_{CCP}	Supply voltage			−0.5	4	V
V_I	Input voltage[2]			−0.5	4	V
V_O	Output voltage[2]			−0.5	4	V
I_{IK}	Input clamp current		$V_I < 0$		−20	mA
I_{OK}	Output clamp current		$V_O < 0$		−20	mA
I_{IOK}	Input-output clamp current	P port	$V_O < 0$ or $V_O > V_{CCP}$		±20	mA
		SDA	$V_O < 0$ or $V_O > V_{CCI}$		±20	
I_{OL}	Continuous output low current[3]	P port	$V_O = 0$ to V_{CCP}		50	mA
		SDA	$V_O = 0$ to V_{CCI}		25	
I_{OH}	Continuous output high current[3]	P port	$V_O = 0$ to V_{CCP}		−50	mA
I_{CC}	Continuous current through GND				−200	mA
I_{CC}	Continuous current through V_{CCP}				160	mA
	Continuous current through V_{CCI}				10	
T_J	Junction temperature				130	°C
T_{stg}	Storage temperature			−65	150	°C

(1) *Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.*
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) Connecting an IO pin directly to GND is not allowed if this pin is set as output, because this will generate >150mA current which could damage the device. We recommend a >10kΩ pull down resistor connected to IO pin if user wants to connect the IO pin to GND.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±4000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC specification JS-002, all pins[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Product Folder Links: *TCAL6408*

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCI}, V_{CCP}	Supply voltage		1.08	3.6	V
V_{IH}	High-level input voltage	SCL, SDA, $\overline{RESET}$	$0.7 * V_{CCI}$	3.6	V
		P0-P7, ADDR	$0.7 * V_{CCP}$	3.6	
V_{IL}	Low-level input voltage	SCL, SDA, $\overline{RESET}$	-0.5	$0.3 * V_{CCI}$	V
		P0-P7, ADDR	-0.5	$0.3 * V_{CCP}$	V
I_{OH}	High-level output current	P0-P7		−10	mA
I_{OL}	Low-level output current ($V_{OL} \leq 0.3$ V)	P0-P7		25	mA
T_A	Ambient temperature		−40	125	°C
T_J	Junction temperature			125	°C

5.4 Thermal Information

THERMAL METRIC[1]		Package			UNIT
		PW (TSSOP)	RSV (UQFN)	DTU (X2QFN)	
		PINS	PINS	PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.7	123.1	143.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.1	65.0	55.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62.0	54.6	81.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	6.0	2.9	1.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	61.4	52.9	81.8	°C/W

(1)   For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCP}	MIN	TYP	MAX	UNIT
V_{IK}	Input diode clamp voltage		$I_I = -18$ mA	1.08 V to 3.6 V	−1.2			V
V_{PORR}	Power-on reset voltage, V_{CC} rising		$V_I = V_{CC}$ or GND, $I_O = 0$			0.85	1.0	V
V_{PORF}	Power-on reset voltage, V_{CC} falling		$V_I = V_{CC}$ or GND, $I_O = 0$			0.6	0.75	V
V_{IH}	High-level input voltage	SDA,SCL		1.08 to 3.6 V	$0.7 \times V_{CC}$			V
		P ports, ADDR, A1, A2, $\overline{RESET}$		1.08 to 3.6 V	$0.7 \times V_{CC}$			V
V_{IL}	Low-level input voltage	SDA,SCL		1.08 to 3.6 V			$0.4 \times V_{CC}$	V
		P ports, ADDR, A1, A2, $\overline{RESET}$		1.08 to 3.6 V			$0.3 \times V_{CC}$	V
V_{OH}	P-port high-level output voltage[1]		$I_{OH} = -8$ mA; CC-XX = 11b	1.08 V	0.8			V
				1.65 V	1.4			
				2.3 V	2.1			
				3 V	2.8			
			$I_{OH} = -2.5$ mA & CC-XX = 00b; $I_{OH} = -5$ mA & CC-XX = 01b; $I_{OH} = -7.5$ mA & CC-XX = 10b; $I_{OH} = -10$ mA & CC-XX = 11b;	1.08 V	0.75			
				1.65 V	1.4			
				2.3 V	2.1			
				3 V	2.8			
V_{OL}	Low-level output voltage	P ports	$I_{OL} = 8$ mA; CC-XX = 11b	1.08 V			0.2	V
				1.65 V			0.15	
				2.3 V			0.1	
				3.0 V			0.1	
		P ports	$I_{OL} = 2.5$ mA and CC-XX = 00b; $I_{OL} = 5$ mA and CC-XX = 01b; $I_{OL} = 7.5$ mA and CC-XX = 10b; $I_{OL} = 10$ mA and CC-XX = 11b;	1.08 V			0.25	V
				1.65 V			0.15	
				2.3 V			0.1	
				3.0 V			0.1	
I_{OL}	Low-level output current	SDA	$V_{OL} = 0.4$ V	1.08 V to 3.6 V	20			mA
		$\overline{INT}$	$V_{OL} = 0.4$ V		4			
I_I	Input leakage current	P ports	$V_I = V_{CC}$ or GND	1.08 V to 3.6 V			±1	µA
			$V_I = 3.6$ V	0 V			±1	
I_I	Input leakage current	SCL, SDA, $\overline{RESET}$	$V_I = V_{CC}$ or GND	1.08 V to 3.6 V			±1	
I_I	Input leakage current	ADDR	$V_I = V_{CC}$ or GND	1.08 V to 3.6 V			±1	µA

5.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CCP}	MIN	TYP	MAX	UNIT
I_{CC} (I_{CCI} + I_{CCP})	Quiescent current	Operating mode (400 kHz)	SDA, $\overline{RESET}$ = V_{CCI}, P port, ADDR = V_{CCP} or GND, I/O = inputs, f_{SCL} = 400 kHz, −40°C < T_A ≤ 85°C, IO resistors disabled	3.6 V		7	15	µA
				2.7 V		5	11	
				1.95 V		4	8	
				1.32 V		2	6	
			SDA, $\overline{RESET}$ = V_{CCI}, P port, ADDR = V_{CCP} or GND, I/O = inputs, f_{SCL} = 400 kHz, 85°C < T_A ≤ 125°C, IO resistors disabled	3.6 V		7	24	µA
				2.7 V		5	18	
				1.95 V		4	14	
				1.32 V		2	11	
		Operating mode (1 MHz)	SDA, $\overline{RESET}$ = V_{CCI}, P port, ADDR = V_{CCP} or GND, I/O = inputs, f_{SCL} = 1 MHz, −40°C < T_A ≤ 85°C, IO resistors disabled	3.6 V			34	µA
				2.7 V			24	
				1.95 V			18	
				1.32 V			12	
			SDA, $\overline{RESET}$ = V_{CCI}, P port, ADDR = V_{CCP} or GND, I/O = inputs, f_{SCL} = 1 MHz, 85°C < T_A ≤ 125°C, IO resistors disabled	3.6 V			42	µA
				2.7 V			30	
				1.95 V			22	
				1.32 V			16	
		Standby mode	SCL, SDA, $\overline{RESET}$ = V_{CCI}, P port, ADDR = V_{CCP} or GND, I/O = inputs, I_O = 0, f_{SCL} = 0 kHz, −40°C < T_A ≤ 85°C , IO resistors disabled	3.6 V		1.5	3	µA
				2.7 V		1.2	2.0	
				1.95 V		0.6	1.6	
				1.32 V		0.6	1.4	
			SCL, SDA, $\overline{RESET}$ = V_{CCI}, P port, ADDR = V_{CCP} or GND, I/O = inputs, I_O = 0, f_{SCL} = 0 kHz, 85°C < T_A ≤ 125°C , IO resistors disabled	3.6 V			14	µA
				2.7 V			10	
				1.95 V			8	
				1.32 V			6	
$R_{pu(int)}$	internal pull-up resistance	P port			70	100	140	kΩ
$R_{pd(int)}$	internal pull-down resistance							
C_I	Input pin capacitance	SCL	V_I = V_{CC} or GND	1.08 V to 3.6 V		2.5	5	pF
C_{IO}	Input-output pin capacitance	SDA	V_{IO} = V_{CC} or GND	1.08 V to 3.6 V		6	8	pF
		P port	V_{IO} = V_{CC} or GND	1.08 V to 3.6 V		6	8.5	

(1) Each I/O must be externally limited to a maximum of 25 mA, CC-XX refers to output drive strength register setting.

5.6 Timing Requirements

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
RESET				
t_w	Reset pulse duration	80		ns
t_{REC}	Reset recovery time	0		ns
t_{RESET}	Time to reset	400		ns
P-Ports				
t_{PH}	Minimum pulse width on P-Port that causes an interrupt	30		ns

Product Folder Links: *TCAL6408*

5.7 I²C Bus Timing Requirements

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
I²C Bus - Standard Mode					
t_{scl}	I²C clock frequency		0	100	kHz
t_{sch}	I²C clock high time		4		µs
t_{scl}	I²C clock low time		4.7		µs
t_{sp}	I²C spike time			50	ns
t_{sds}	I²C serial-data setup time		250		ns
t_{sdh}	I²C serial-data hold time		0		ns
t_{icr}	I²C input rise time			1000	ns
t_{icf}	I²C input fall time			300	ns
t_{ocf}	I²C output fall time	10-pF to 400-pF bus		300	ns
t_{buf}	I²C bus free time between stop and start		4.7		µs
t_{sts}	I²C start or repeated start condition setup		4.7		µs
t_{sth}	I²C start or repeated start condition hold		4		µs
t_{sps}	I²C stop condition setup		4		µs
$t_{vd(data)}$	Valid data time	SCL low to SDA output valid		3.45	µs
$t_{vd(ack)}$	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low		3.45	µs
C_b	I²C bus capacitive load			400	pF
I²C Bus - Fast Mode					
t_{scl}	I²C clock frequency		0	400	kHz
t_{sch}	I²C clock high time		0.6		µs
t_{scl}	I²C clock low time		1.3		µs
t_{sp}	I²C spike time			50	ns
t_{sds}	I²C serial-data setup time		100		ns
t_{sdh}	I²C serial-data hold time		0		ns
t_{icr}	I²C input rise time		20	300	ns
t_{icf}	I²C input fall time		20 × (V_{CC} / 5.5 V)	300	ns
t_{ocf}	I²C output fall time	10-pF to 400-pF bus	20 × (V_{CC} / 5.5 V)	300	ns
t_{buf}	I²C bus free time between stop and start		1.3		µs
t_{sts}	I²C start or repeated start condition setup		0.6		µs
t_{sth}	I²C start or repeated start condition hold		0.6		µs
t_{sps}	I²C stop condition setup		0.6		µs
$t_{vd(data)}$	Valid data time	SCL low to SDA output valid		0.9	µs
$t_{vd(ack)}$	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low		0.9	µs
C_b	I²C bus capacitive load			400	pF
I²C Bus - Fast Mode Plus					
t_{scl}	I²C clock frequency		0	1000	kHz
t_{sch}	I²C clock high time		0.26		µs
t_{scl}	I²C clock low time		0.5		µs
t_{sp}	I²C spike time			50	ns
t_{sds}	I²C serial-data setup time		50		ns
t_{sdh}	I²C serial-data hold time		0		ns

5.7 I²C Bus Timing Requirements (continued)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
t_{icr}	I²C input rise time			120	ns
t_{icf}	I²C input fall time		20 × (V_{CC} / 5.5 V)	120	ns
t_{ocf}	I²C output fall time	10-pF to 550-pF bus	20 × (V_{CC} / 5.5 V)	120	ns
t_{buf}	I²C bus free time between stop and start		0.5		µs
t_{sts}	I²C start or repeated start condition setup		0.26		µs
t_{sth}	I²C start or repeated start condition hold		0.26		µs
t_{sps}	I²C stop condition setup		0.26		µs
$t_{vd(data)}$	Valid data time	SCL low to SDA output valid		0.45	µs
$t_{vd(ack)}$	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low		0.45	µs
C_b	I²C bus capacitive load			550	pF

5.8 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
t_{iv}	Interrupt valid time (R_{PU} = 4.7kΩ, C_L = 100 pF)	P port	$\overline{INT}$			1	µs
t_{ir}	Interrupt reset delay time (R_{PU} = 4.7kΩ, C_L = 100 pF)	SCL	$\overline{INT}$			1	µs
t_{pv}	Output data valid time	SCL	P port			400	ns
t_{ps}	Input data setup time	P port	SCL	0			ns
t_{ph}	Input data hold time	P port	SCL	300			ns
t_{skew_fall}	Skew time from SCL to SDA (Sim only) - Falling Edge	SCL	SDA	5		80	ns
t_{skew_rise}	Skew time from SCL to SDA (Sim only) - Rising Edge	SCL	SDA	-20		80	ns

5.9 Typical Characteristics

T_A = 25°C (unless otherwise noted)
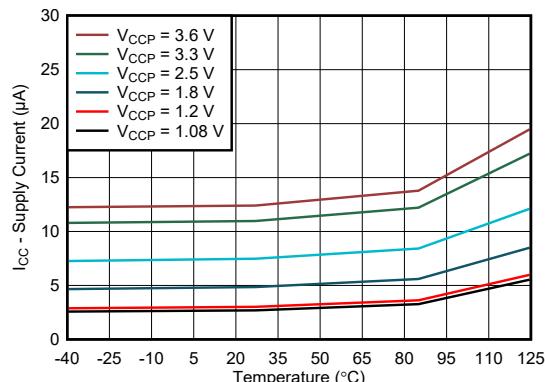
**Figure 5-1. Supply Current vs Temperature - FM mode**
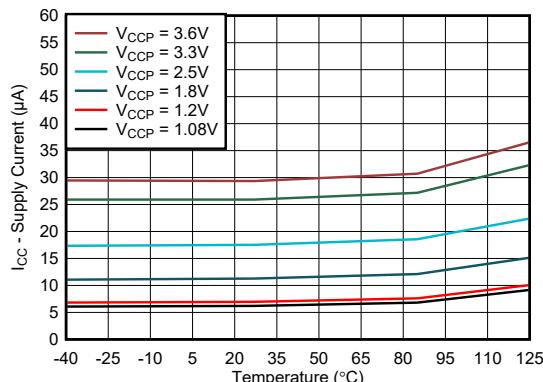
**Figure 5-2. Supply Current vs Temperature - FM+ mode**
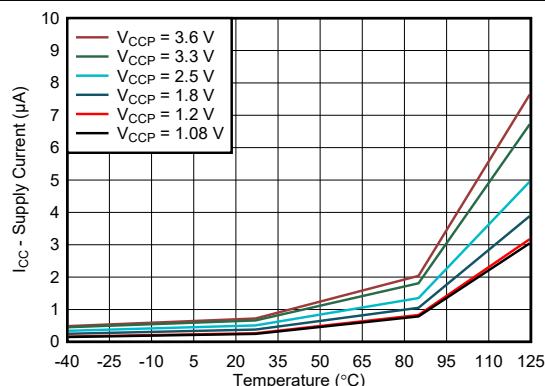

Figure 5-3. Standby Supply Current vs Temperature
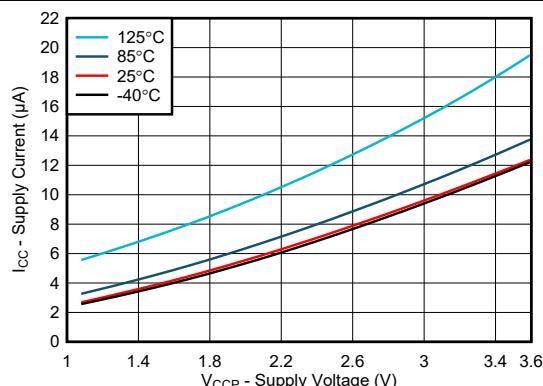
**Figure 5-4. Supply Current vs Supply Voltage - FM mode**
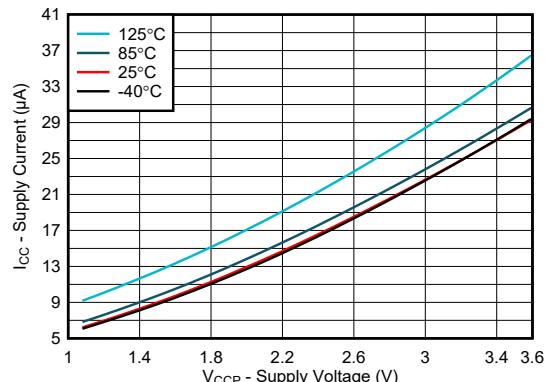
**Figure 5-5. Supply Current vs Supply Voltage - FM+ mode**
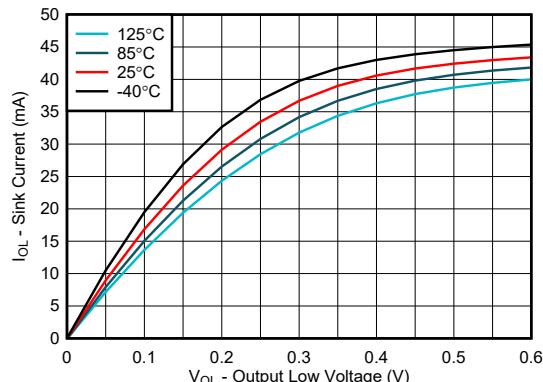
Figure 5-6. I/O Sink Current vs Output Low Voltage, V_{CCP} = 1.08 V

5.9 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)
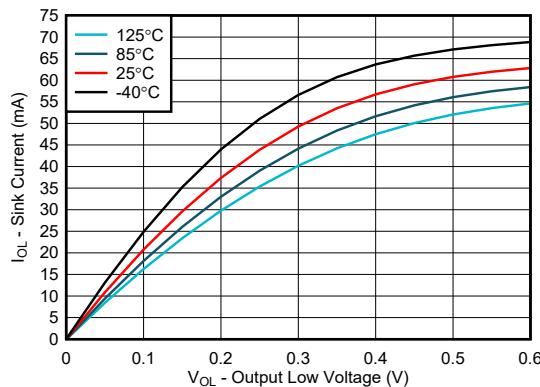
Figure 5-7. I/O Sink Current vs Output Low Voltage, V_{CCP} = 1.2 V
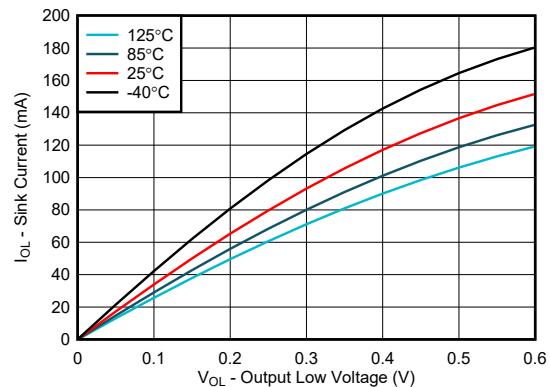
Figure 5-8. I/O Sink Current vs Output Low Voltage, V_{CCP} = 1.8 V
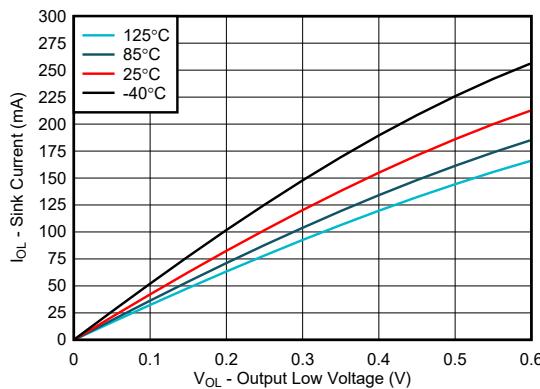
Figure 5-9. I/O Sink Current vs Output Low Voltage, V_{CCP} = 2.5 V
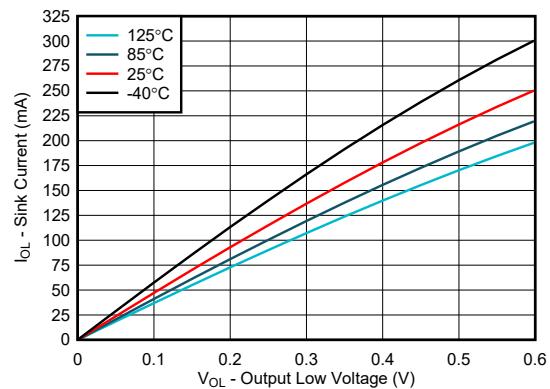
Figure 5-10. I/O Sink Current vs Output Low Voltage, V_{CCP} = 3.3 V
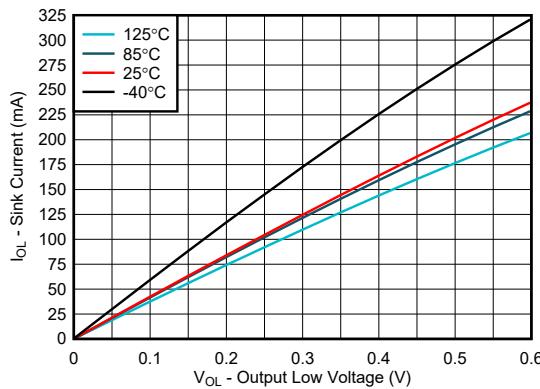
Figure 5-11. I/O Sink Current vs Output Low Voltage, V_{CCP} = 3.6 V
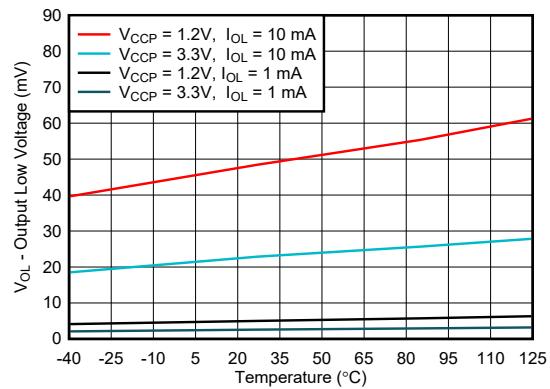
Figure 5-12. I/O Low Voltage vs Temperature

Product Folder Links: *TCAL6408*

5.9 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)
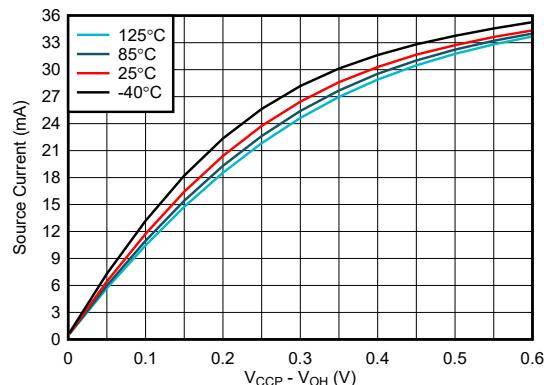
Figure 5-13. I/O Source Current vs Output High Voltage , V_{CCP} = 1.08 V
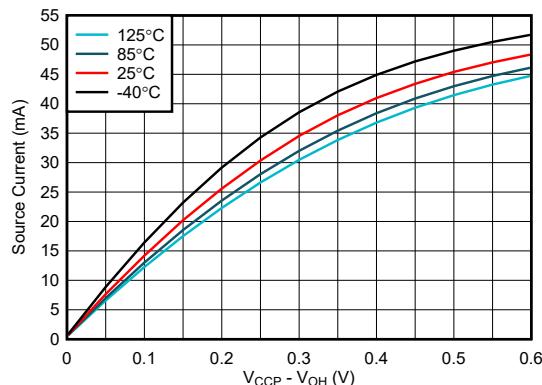
Figure 5-14. I/O Source Current vs Output High Voltage, V_{CCP} = 1.2 V
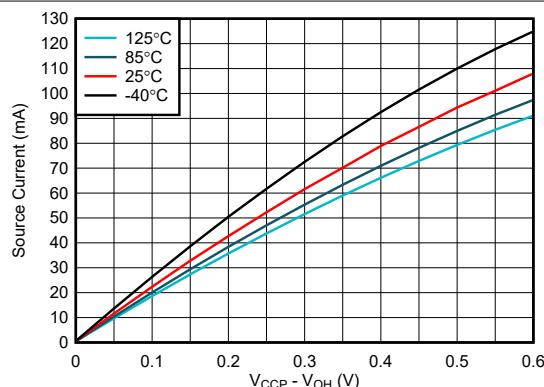
Figure 5-15. I/O Source Current vs Output High Voltage, V_{CCP} = 1.8 V
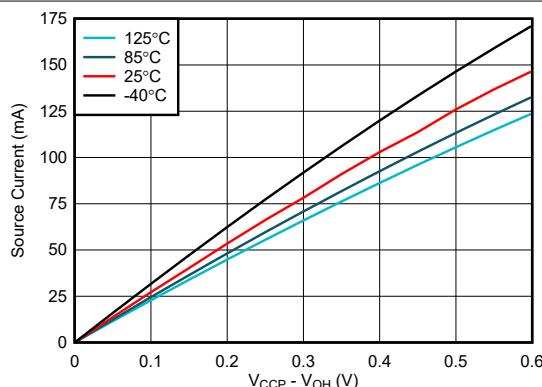
Figure 5-16. I/O Source Current vs Output High Voltage, V_{CCP} = 2.5 V
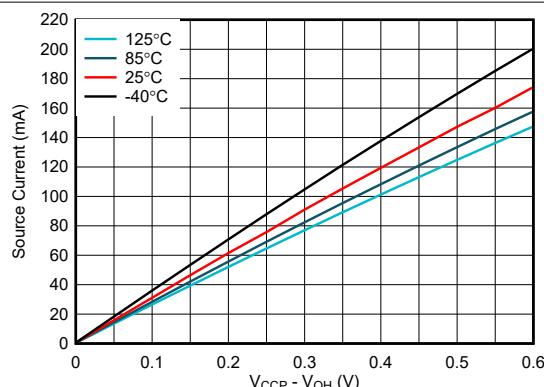
Figure 5-17. I/O Source Current vs Output High Voltage, V_{CCP} = 3.3 V
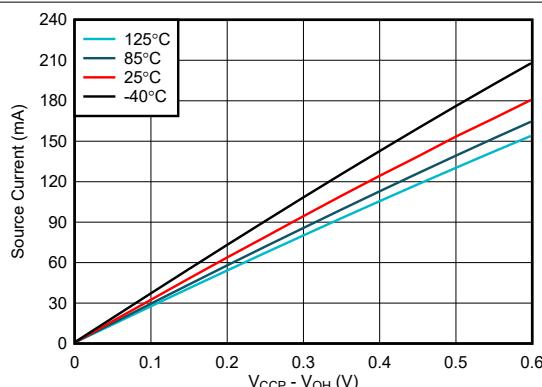
Figure 5-18. I/O Source Current vs Output High Voltage, V_{CCP} = 3.6 V

5.9 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)
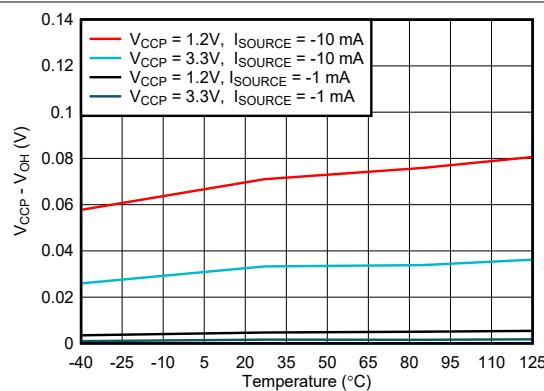
Figure 5-19. I/O High Voltage vs Temperature

6 Parameter Measurement Information

SDA LOAD CONFIGURATION

VOLTAGE WAVEFORMS
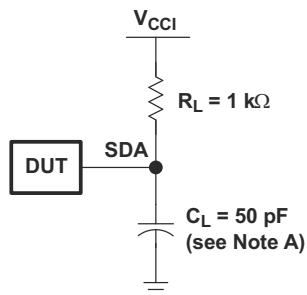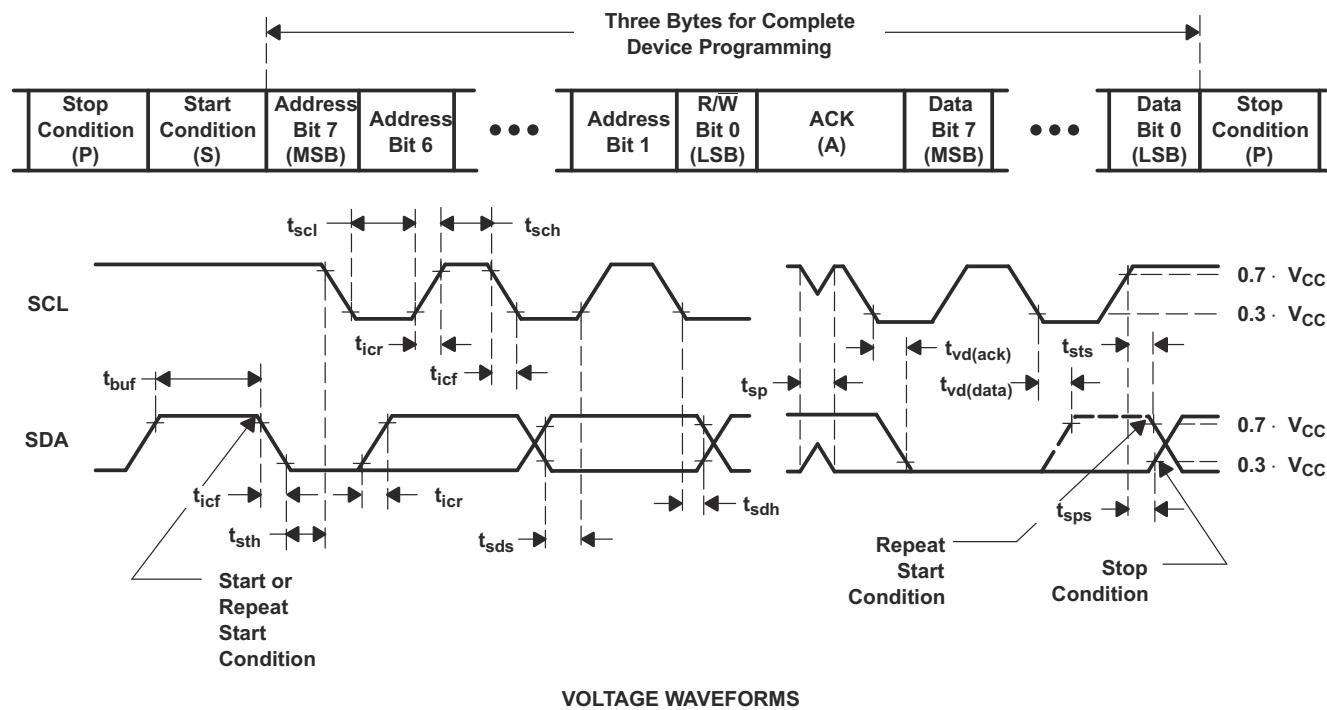
BYTE	DESCRIPTION
1	I^{2}C address
2, 3	P-port data

A. C_L includes probe and jig capacitance. tocf is measured with C_L of 10pF or 400pF.

B.   All inputs are supplied by generators having the following characteristics: PRR ≤ 10MHz, Z_O = 50Ω, t_r/t_f ≤ 30ns.

C.   All parameters and waveforms are not applicable to all devices.

Figure 6-1. I^{2}C Interface Load Circuit and Voltage Waveforms
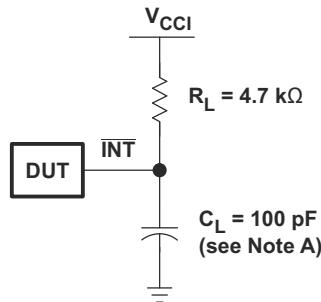
INTERRUPT LOAD CONFIGURATION
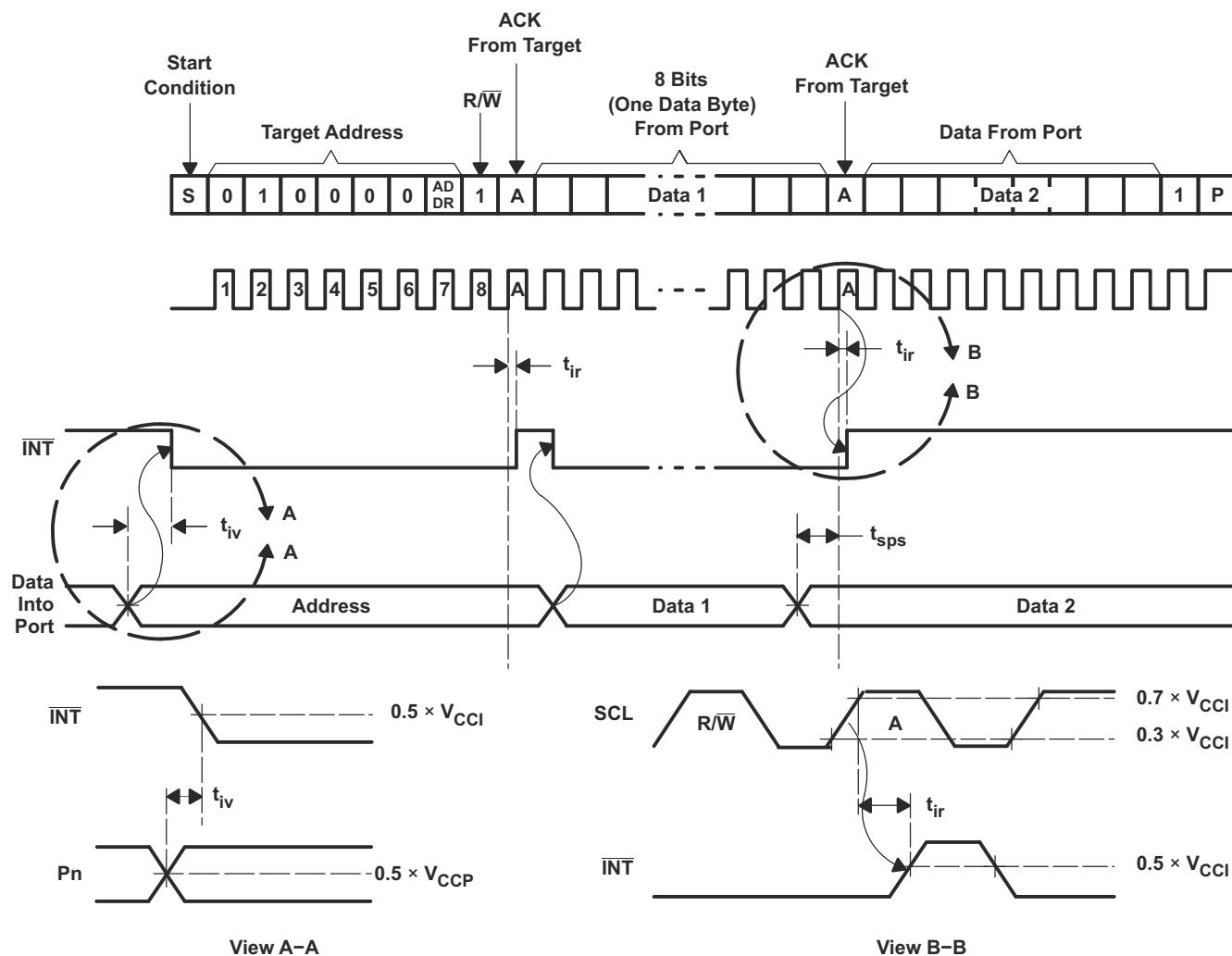
A. C_L includes probe and jig capacitance.
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10MHz, Z_O = 50Ω, t_r/t_f ≤ 30ns.
C. All parameters and waveforms are not applicable to all devices.

Figure 6-2. Interrupt Load Circuit and Voltage Waveforms
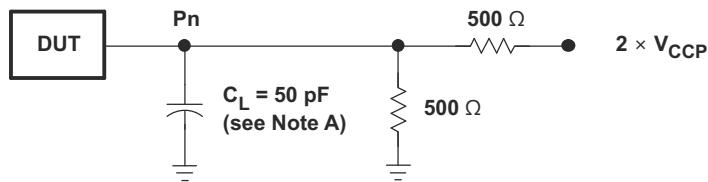
Figure 6-3. P-Port Load Circuit and Timing Waveforms
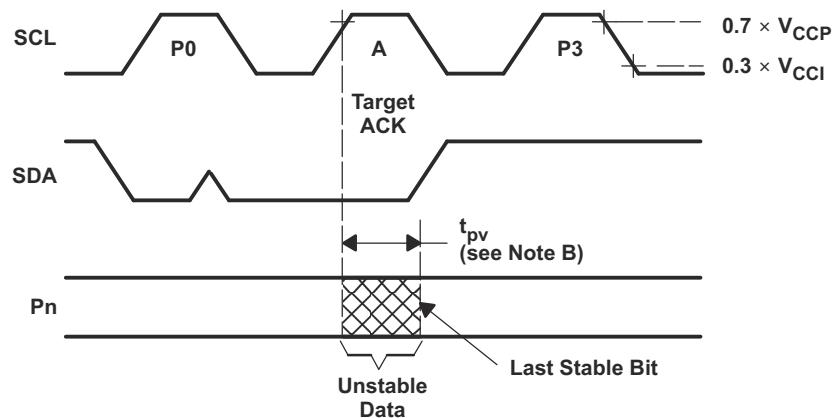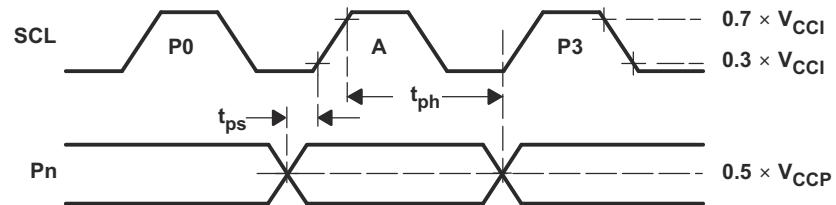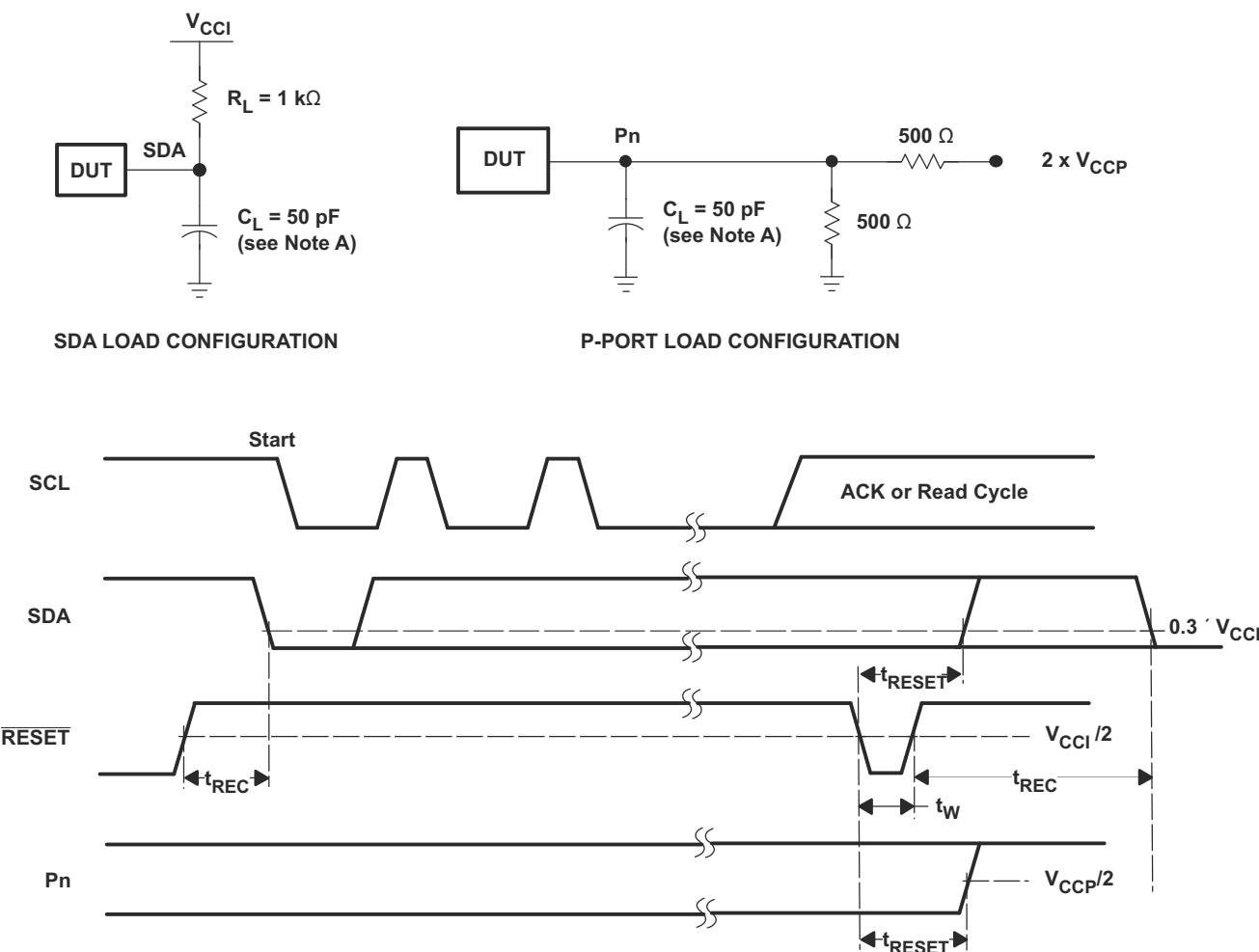
A. C_L includes probe and jig capacitance.
B. t_{pv} is measured from $0.7 \times V_{CC}$ on SCL to 50% I/O (Pn) output.
C. All inputs are supplied by generators having the following characteristics: PRR ≤ 10MHz, $Z_O = 50\Omega$, $t_r/t_f \leq 30$ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Product Folder Links: *TCAL6408*

SDA LOAD CONFIGURATION   P-PORT LOAD CONFIGURATION

A. C_L includes probe and jig capacitance.
B.   All inputs are supplied by generators having the following characteristics: PRR ≤ 10MHz, Z_O = 50Ω, t_r/t_f ≤ 30ns.
C.   The outputs are measured one at a time, with one transition per measurement.
D.   I/Os are configured as inputs.
E.   All parameters and waveforms are not applicable to all devices.

Figure 6-4. Reset Load Circuits and Voltage Waveforms

7 Detailed Description

7.1 Overview

The TCAL6408 supports voltage translation over a wide supply voltage range. This allows the device to interface with modern processors on the I^{2}C side, where supply levels are lower to conserve power. In contrast to the dropping power supplies of processors, some PCB components (such as LEDs) still require a higher voltage power supply.

The V$_{CCI}$ pin is the power supply for the I^{2}C bus, and therefore the pull-up resistors connected to the SCL, SDA, and RESET pins should be terminated at V$_{CCI}$. The INT output has an open-drain structure and requires an external pull-up resistor to V$_{CCP}$ or V$_{CCI}$ depending on the application. The V$_{CCP}$ pin is the power supply for the P-ports. If the external pull-up resistors are used on any P-port, or if the LEDs are driven by any P-port, then the one or more of the resistors or LEDs connected to P0-P7 should be terminated at V$_{CCP}$. The device P-ports configured as outputs have the ability to sink up to 25mA for directly driving LEDs, but the current must be limited externally with an additional resistance.

The TCAL6408 digital core consists of 8-bit data registers, which allow the user to configure the I/O port characteristics. At power-up or after a software reset call, the I/Os are configured as inputs. However, the system controller can configure the I/Os as either inputs or outputs by writing to the Configuration registers. The data for each input or output is kept in the corresponding Input Port or Output Port register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. The system controller can read all registers. Additionally, the TCAL6408 has Agile I/O functionality, which is specifically targeted to enhance the I/O ports. The Agile I/O features and registers include programmable output drive strength, programmable pull-up and pull-down resistors, latchable inputs, maskable interrupts, interrupt status register, and programmable open-drain or push-pull outputs. These configuration registers improve the I/O by increasing flexibility and allowing the user to optimize their design for power consumption, speed, and EMI.

Other features of the device include an interrupt that is generated on the $\overline{\text{INT}}$ pin whenever an input port changes state. The device can be reset to its default state by issuing a software reset command or by cycling power to the device and causing a power-on reset. The ADDR hardware selectable address pin allows two TCAL6408 devices to be connected to the same I^{2}C bus.

The TCAL6408 open-drain interrupt ($\overline{\text{INT}}$) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system controller that an input state has changed. The $\overline{\text{INT}}$ pin can be connected to the interrupt input of a processor. By sending an interrupt signal on this line, the device can inform the processor if there is incoming data on the remote I/O ports without having to communicate through the I^{2}C bus. Thus, the device can remain a simple target device.

The system controller can re-initialize I^{2}C/SMBus state machine in the event of a timeout or other improper operation by asserting a low on the $\overline{\text{RESET}}$ input pin without resetting the sticky registers to default values.

One hardware pin (ADDR) can be used to program and vary the fixed I^{2}C address, and allow two devices to share the same I^{2}C bus or SMBus.

7.2 Functional Block Diagrams
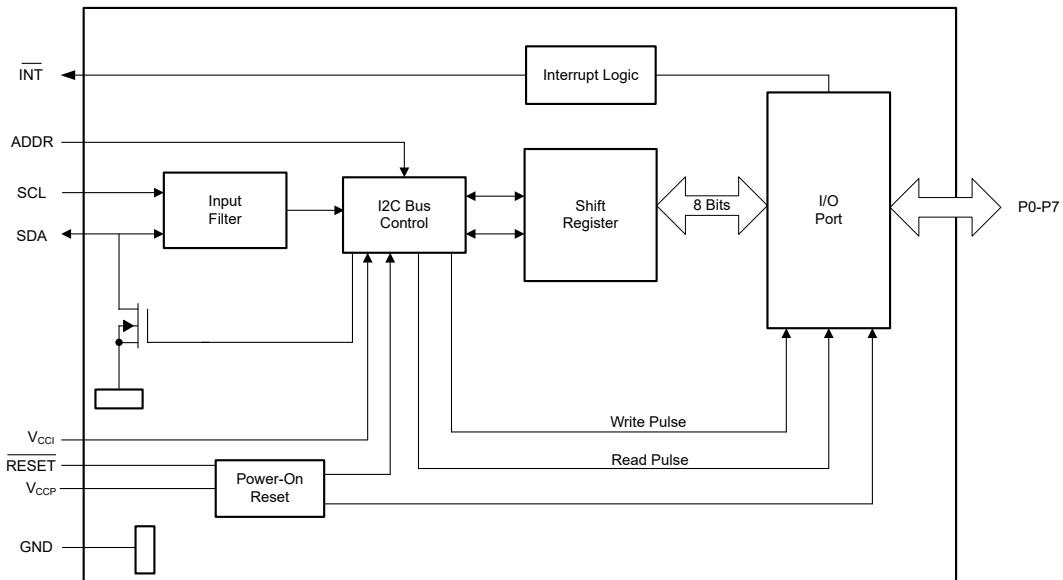
Figure 7-1. Logic Diagram (Positive Logic)
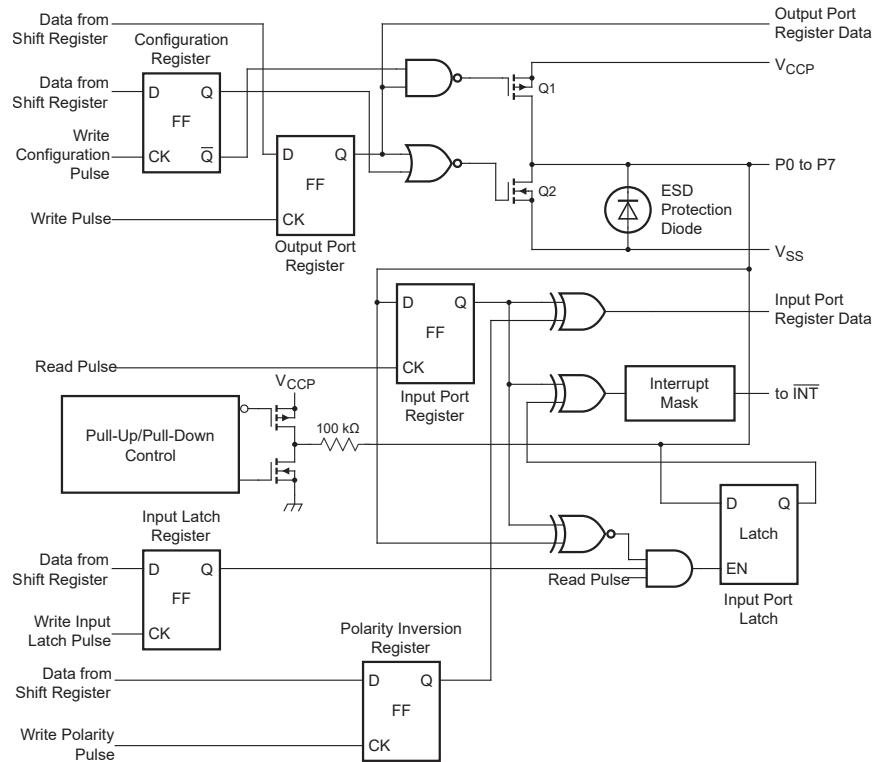
A.   On power up or reset, all registers return to default values.

Figure 7-2. Simplified Schematic of P0 to P7

7.3 Feature Description

7.3.1 Voltage Translation

Table 7-1 lists all of the optional voltage supply level combinations for the I^{2}C bus (V$_{CCI}$) and the P-ports (V$_{CCP}$) supported by the TCAL6408.

Table 7-1. Voltage Translation

V$_{CCI}$ (SDA AND SCL OF I^{2}C Controller) (V)	V$_{CCP}$ (P-PORTS) (V)
1.2	1.2
1.2	1.8
1.2	2.5
1.2	3.3
1.8	1.2
1.8	1.8
1.8	2.5
1.8	3.3
2.5	1.2
2.5	1.8
2.5	2.5
2.5	3.3
3.3	1.2
3.3	1.8
3.3	2.5
3.3	3.3

7.3.2 I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 are off (see Section 7.2), which creates a high-impedance input. The input voltage may be raised above the supply voltage to a maximum of 3.6V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the output port register. In this case, there are low-impedance paths between the I/O pin and either supply or GND. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.

7.3.3 Adjustable Output Drive Strength

The output drive strength registers allow the user to control the drive level of the GPIO. Each GPIO can be configured independently to one of the four possible current levels. By programming these bits the user is changing the number of transistor pairs or 'fingers' that drive the I/O pad. Figure 7-3 shows a simplified output stage. The behavior of the pad is affected by the Configuration register, the output port data, and the output drive strength register. When the output drive strength register bits are programmed to 01b, then only two of the fingers are active, reducing the current drive capability by 50%.
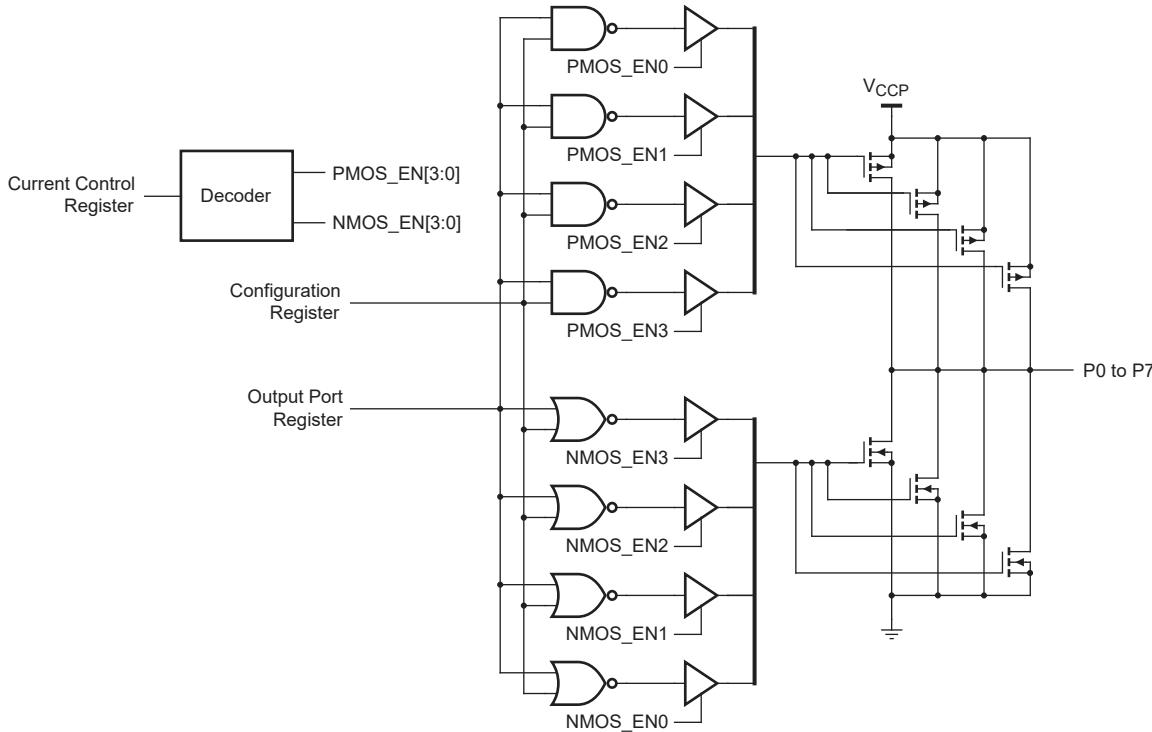
Figure 7-3. Simplified Output Stage

A function of the output drive selection causes a peak current to occur when the output switches. Reducing the current drive capability may reduce the system noise that occurs. This peak current runs through the supply and GND package inductance and creates a noise (some radiated, but more critically Simultaneous Switching Noise (SSN)). In other words, switching many outputs at the same time will create ground and supply noise. The output drive strength control through the Output Drive Strength registers allows the user to mitigate SSN issues without the need of additional external components.

7.3.4 Interrupt Output ($\overline{INT}$)

Any rising or falling edge of the port inputs in the input mode generates an interrupt, provided the interrupt feature is unmasked. After time t_{iv}, the $\overline{INT}$ signal is valid. Resetting the interrupt circuit is achieved when data on the port is changed back to the original setting or when data is read from the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) bit after the rising edge of the SCL signal. Interrupts that occur during the ACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{INT}$.

Reading from or writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the input port register.

The $\overline{INT}$ output has an open-drain structure and requires an external pull-up resistor to V_{CCP} or V_{CCI} depending on the application. The pull-up resistor for $\overline{INT}$ should be connected to the voltage source of the device that requires the interrupt information.

7.3.5 Reset Input ($\overline{RESET}$)

The $\overline{RESET}$ input can be asserted to initialize the system while keeping the V_{CCP} supply at its operating level. A reset can be accomplished by holding the $\overline{RESET}$ pin low for a minimum of t_W. The TCAL6408 registers and I2C/SMBus state machine are changed to their default state once $\overline{RESET}$ is low (0). When $\overline{RESET}$ is high (1), the I/O levels at the P port can be changed externally or through the controller. This input requires a pull-up resistor to V_{CCI}, if no active connection is used. When $\overline{RESET}$ is toggled the input port register is updated to reflect the state of the GPIO pins.

7.3.6 Software Reset Call

The software reset call is a command sent from the controller on the I^{2}C bus that instructs all devices that support the command to be reset to the power-up default state. To function as expected, the I^{2}C bus must be functional, and no devices can be hanging the bus.

The software reset call is defined as the following steps:

1. The I^{2}C bus controller sends a start condition.
2. The address used is the reserved general call I^{2}C bus address '0000 0000' with the R/W bit set to 0. The byte sent is 0x00.
3. Any devices supporting the general call functionality will ACK. If the R/W bit is set to 1 (read), then the device will NACK.
4. When the general call address is acknowledged, the controller sends only 1 byte of data equal to 0x06. If the data byte is any other value, then the device does not acknowledge or reset. If more than 1 byte is sent, then no more bytes is acknowledged, and the device ignores the I^{2}C message considering as invalid.
5. After the 1 byte of data (0x06) is sent, the controller sends a STOP condition to end the Software Reset sequence. The device ignores a repeated START condition and no reset is performed.

When the previous steps are completed successfully, the device performs a reset. This clears all register values back to power-on defaults.

7.4 Device Functional Modes

7.4.1 Power-On Reset

When power (from 0V) is applied to V$_{CCP}$, an internal power-on reset holds the TCAL6408 in a reset condition until the supply has reached V$_{POR}$. At that time, the reset condition is released, and the TCAL6408 registers and I^{2}C/SMBus state machine initializes to their default states. After that, V$_{CCP}$ must be lowered to below V$_{PORF}$ and back up to the operating voltage for a power-reset cycle.

7.5 Programming

7.5.1 I^{2}C Interface

The bidirectional I^{2}C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pull-up resistor when connected to the output stages of a device. Data transfer can only be initiated when the bus is not busy.

A controller initiates I^{2}C communication with this device by sending a Start condition, a high-to-low transition on the SDA input/output, while the SCL input is high (see Figure 7-4). After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/$\overline{W}$).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. The address input of the target device must not be changed between the Start and the Stop conditions.

On the I^{2}C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop) (see Figure 7-5).

The controller sends a Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high (see Figure 7-4).

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 7-6). When a target receiver is addressed, it must generate an ACK after each byte is received. Similarly, the controller must generate an ACK after each byte that it receives from the target transmitter. Setup and hold times must be met for proper operation.

A controller receiver signals an end of data to the target transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the target. The controller receiver does this by holding the SDA line high. In this event, the transmitter must release the data line to enable the controller to generate a Stop condition.
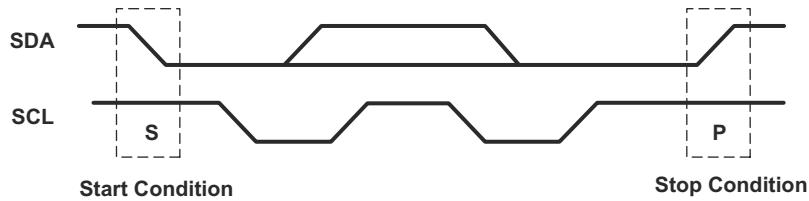
Figure 7-4. Definition of Start and Stop Conditions
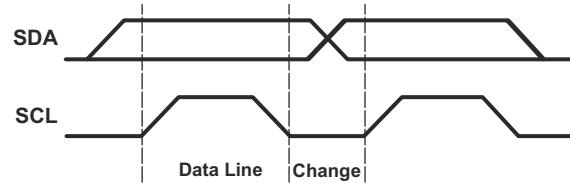
Figure 7-5. Bit Transfer
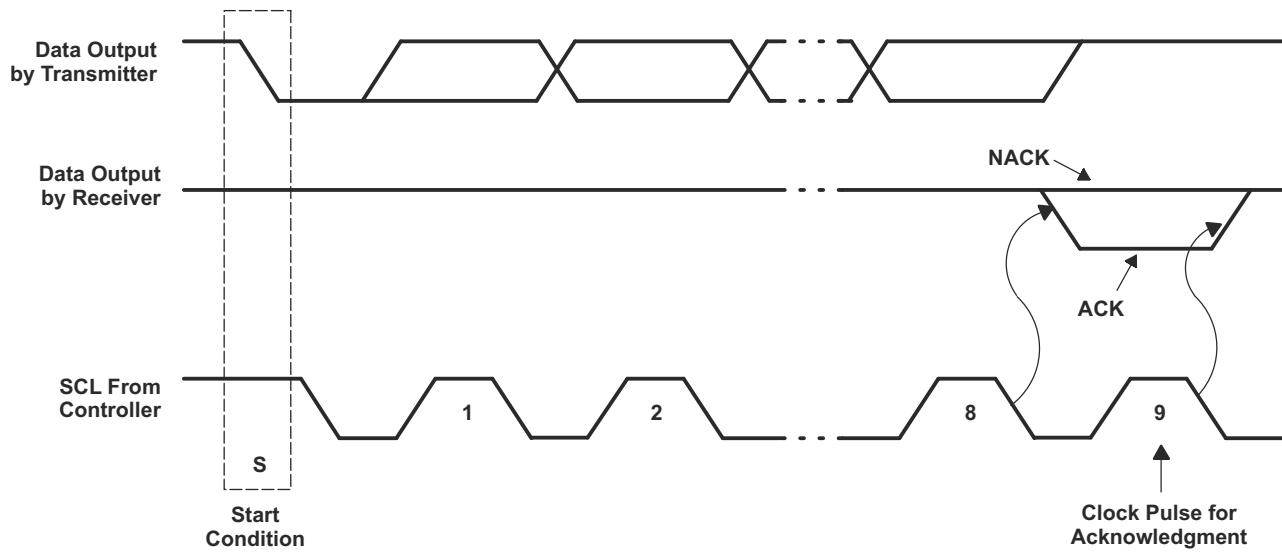
Figure 7-6. Acknowledgment on the I²C Bus

Table 7-2. Interface Definition

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Device I²C address	L	H	L	L	L	L	ADDR	R/$\overline{W}$
I/O data bus	P7	P6	P5	P4	P3	P2	P1	P0

Product Folder Links: *TCAL6408*

7.6 Register Maps

7.6.1 Device Address

Figure 7-7 shows the address of the TCAL6408.

Device Address

| 0 | 1 | 0 | 0 | 0 | 0 | AD DR | R/W̄ |

Fixed   **Programmable**
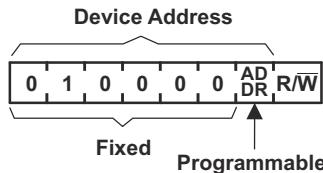
Figure 7-7. TCAL6408 Address

Table 7-3. Address Reference

ADDR	I²C BUS TARGET ADDRESS
L	32 (decimal), 20 (hexadecimal)
H	33 (decimal), 21 (hexadecimal)

The last bit of the target address defines the operation (read or write) to be performed. A high (1) selects a read operation, while a low (0) selects a write operation.

7.6.2 Control Register and Command Byte

Following the successful acknowledgment of the address byte, the bus controller sends a command byte, which is stored in the control register in the TCAL6408. The lower two bits of this data byte reflect the internal registers (input, output, polarity inversion, or configuration) that are affected. Bit 6 in conjunction with the lower four bits of the Command byte are used to point to the extended features of the device (Agile IO). The command byte is sent only during a write transmission.

Once a new command has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent. Upon power-up, hardware reset, or software reset, the control register defaults to 00h.
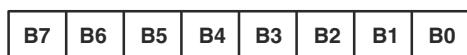
| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |

Figure 7-8. Control Register Bits

Table 7-4. Command Byte

B7	B6	B5	B4	B3	B2	B1	B0	COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
0	0	0	0	0	0	0	0	00	Input Port	Read byte	xxxx xxxx
0	0	0	0	0	0	0	1	01	Output Port	Read/write byte	1111 1111
0	0	0	0	0	0	1	0	02	Polarity Inversion	Read/write byte	0000 0000
0	0	0	0	0	0	1	1	03	Configuration	Read/write byte	1111 1111
0	1	0	0	0	0	0	0	40	Output Drive Strength 0	Read/write byte	1111 1111
0	1	0	0	0	0	0	1	41	Output Drive Strength 1	Read/write byte	1111 1111
0	1	0	0	0	0	1	0	42	Input latch register	Read/write byte	0000 0000
0	1	0	0	0	0	1	1	43	Pull-up/pull-down enable register	Read/write byte	0000 0000
0	1	0	0	0	1	0	0	44	pull-up/pull-down selection register	Read/write byte	1111 1111
0	1	0	0	0	1	0	1	45	Interrupt mask register	Read/write byte	1111 1111
0	1	0	0	0	1	1	0	46	Interrupt status register	Read byte	0000 0000

Table 7-4. Command Byte (continued)

CONTROL REGISTER BITS								COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B7	B6	B5	B4	B3	B2	B1	B0				
0	1	0	0	1	1	1	1	4F	Output port configuration register	Read/write byte	0000 0000

7.6.3 Register Descriptions

The Input Port register (register 0) reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. The input port register is read only. Writes to this register have no effect. The default value (X) is determined by the externally applied logic level. Before a read operation, a write transmission is sent with the command byte to indicate to the I^{2}C device that the Input Port register will be accessed next.

Table 7-5. Register 0 (Input Port Register)

BIT	I-7	I-6	I-5	I-4	I-3	I-2	I-1	I-0
DEFAULT	X	X	X	X	X	X	X	X

The Output Port register (register 1) shows the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

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Table 7-6. Register 1 (Output Port Register)

BIT	O-7	O-6	O-5	O-4	O-3	O-2	O-1	O-0
DEFAULT	1	1	1	1	1	1	1	1

The Polarity Inversion register (register 2) allows polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written to '1'), the corresponding port pin polarity is inverted. If a bit in this register is cleared (written to a '0'), the corresponding port pin's original polarity is retained.

Table 7-7. Register 2 (Polarity Inversion Register)

BIT	P-7	P-6	P-5	P-4	P-3	P-2	P-1	P-0
DEFAULT	0	0	0	0	0	0	0	0

The Configuration register (register 3) configures the direction of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

Table 7-8. Register 3 (Configuration Register)

BIT	C-7	C-6	C-5	C-4	C-3	C-2	C-1	C-0
DEFAULT	1	1	1	1	1	1	1	1

The output drive strength registers control the output drive level of the P port GPIO buffers. Each GPIO can be configured independently to the desired output current level by two register control bits. For example, Port P7 is controlled by register 41 (bits 7 and 6), port P6 is controlled by register 41 (bits 5 and 4), and so on. The output drive level of the GPIO is programmed 00b = 0.25x drive strength, 01b = 0.5x drive strength, 10b = 0.75x drive strength, or 11b = 1x for full drive strength capability.

Table 7-9. Registers 40, and 41 (Output Drive Strength Registers)

BIT	CC-3	CC-3	CC-2	CC-2	CC-1	CC-1	CC-0	CC-0
DEFAULT	1	1	1	1	1	1	1	1
BIT	CC-7	CC-7	CC-6	CC-6	CC-5	CC-5	CC-4	CC-4
DEFAULT	1	1	1	1	1	1	1	1

The Input latch register enables and disables the input latch feature of the P port GPIO pins. This register is effective only when the pin is configured as an input port. When an input latch register bit is 0, the corresponding input pin state is not latched. A state change in the corresponding input pin generates an interrupt. A read of the input register clears the interrupt. If the input goes back to its initial logic state before the input port register is read, then the interrupt is cleared.

When an input latch register bit is set to 1, the corresponding input pin state is latched. A change of state of the input generates an interrupt and the input logic value is loaded into the corresponding bit of the input port register (registers 0 and 1). A read of the input port register clears the interrupt. However, if the input pin returns to its initial logic state before the input port register is read, then the interrupt is not cleared and the corresponding bit of the input port register keeps the logic value that initiated the interrupt.

For example, if the P4 input was at a logic 0 state and then transitions to a logic 1 state followed by going back to the logic 0 state, the input port register will capture this change and an interrupt will be generated (if unmasked). When the read is performed on the input port 0 register, the interrupt is cleared, assuming there were no additional inputs that have changed, and bit 4 of the input port register will read '1'. The next read of the input port register bit 4 should now read '0'.

An interrupt remains active when a non-latched input simultaneously switches state with a latched input and then returns to its original state. A read of the input register reflects only the change of state of the latched input and also clears the interrupt. If the input latch register changes from a latched to a non-latched configuration, the interrupt will be cleared if the input logic value returns to its original state.

Product Folder Links: *TCAL6408*

If the input pin is changed from a latched to a non-latched input, a read from the input port register reflects the current port logic level. If the input pin is changed from a non-latched to a latched input, the read from the input register reflects the latched logic level.

Table 7-10. Register 42 (Input Latch Register)

BIT	L-7	L-6	L-5	L-4	L-3	L-2	L-1	L-0
DEFAULT	0	0	0	0	0	0	0	0

The pull-up/pull-down enable register allows the user to enable or disable pull-up/pull-down resistors on the GPIO pins. Setting the bit to logic 1 enables the selection of pull-up/pull-down resistors. Setting the bit to logic 0 disconnects the pull-up/pull-down resistors from the GPIO pins. The resistors are disabled when the GPIOs are configured as outputs Use the pull-up/pull-down selection register to select either a pull-up or pull-down resistor.

Table 7-11. Register 43 (Pull-Up/Pull-Down Enable Register)

BIT	PE-7	PE-6	PE-5	PE-4	PE-3	PE-2	PE-1	PE-0
DEFAULT	0	0	0	0	0	0	0	0

The pull-up/pull-down selection register allows the user to configure each GPIO to have a pull-up or pull-down resistor by programming the respective register bit. Setting a bit to a logic 1 selects a 100kΩ pull-up resistor for that GPIO pin. Setting a bit to logic 0 selects a 100kΩ pull-down resistor for that GPIO pin. If the pull-up/pull-down feature is disabled through register 43, writing to this register has no effect on the GPIO pin.

Table 7-12. Register 44 (Pull-Up/Pull-Down Selection Register)

BIT	PUD-7	PUD-6	PUD-5	PUD-4	PUD-3	PUD-2	PUD-1	PUD-0
DEFAULT	1	1	1	1	1	1	1	1

The Interrupt mask register is defaulted to logic 1 upon power-on, disabling interrupts during system start-up. Interrupts may be enabled by setting corresponding mask bits to logic 0.

If an input changes state and the corresponding bit in the interrupt mask register is to 1, the interrupt is masked and the interrupt pin is not asserted. If the corresponding bit in the interrupt mask register is set to 0, the interrupt pin is asserted.

When an input changes state and the resulting interrupt is masked, setting the interrupt mask register bit to 0 will cause the interrupt pin to be asserted. If the interrupt mask bit of an input that is already currently the source of an interrupt is set to 1, the interrupt pin is de-asserted.

Table 7-13. Register 45 (Interrupt Mask Register)

BIT	M-7	M-6	M-5	M-4	M-3	M-2	M-1	M-0
DEFAULT	1	1	1	1	1	1	1	1

The Interrupt status register is a read only register used to identify the source of an interrupt. When read, a logic 1 indicates that the corresponding input pin was the source of the interrupt. A logic 0 indicates that the input pin is not the source of an interrupt. When a corresponding bit in the interrupt mask register is set to 1 (masked), the interrupt status bit will return to logic 0.

Table 7-14. Register 46 (Interrupt Status Register)

BIT	S-7	S-6	S-5	S-4	S-3	S-2	S-1	S-0
DEFAULT	0	0	0	0	0	0	0	0

The output port configuration register selects port-wise push-pull or open-drain I/O stage. A logic 0 configures the I/O as push-pull (Q1 and Q2 are active, see Figure 7-2). A logic 1 configures the I/O as open-drain (Q1 is disabled, Q2 is active) and the recommended command sequence is to program this register (4F) before the Configuration register (03) sets the port pins as outputs.

**Table 7-15. Register 4F (Output Port Configuration Register)**

| BIT	Reserved							ODEN-0
DEFAULT	0	0	0	0	0	0	0	0

7.6.4 Bus Transactions

Data is exchanged between the controller and TCAL6408 through write and read commands.

7.6.4.1 Writes

Data is transmitted to the TCAL6408 by sending the device address and setting the least-significant bit (LSB) to a logic 0 (see Figure 7-7 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte. There is no limitation on the number of data bytes sent in one write transmission.
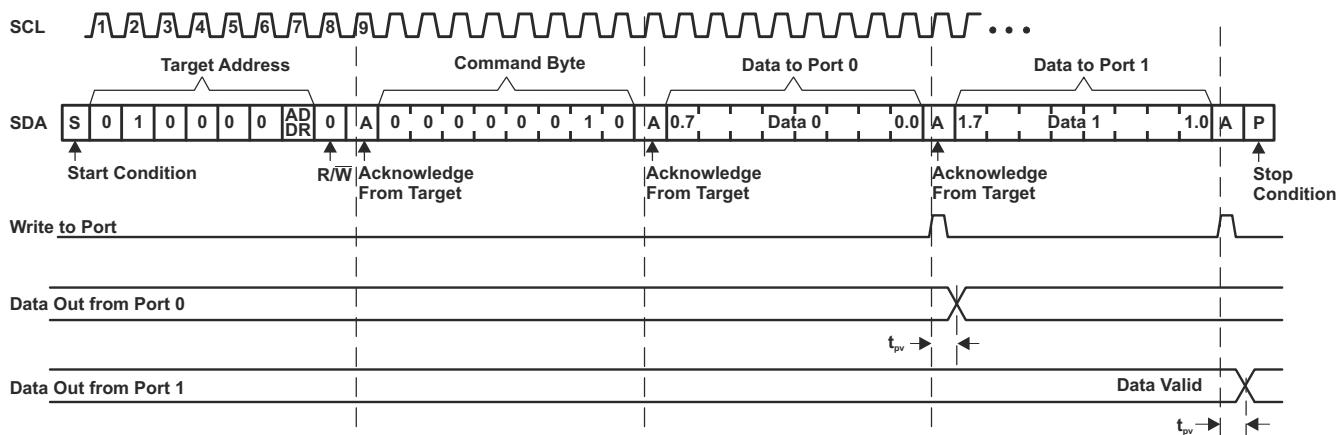
Figure 7-9. Write to Output Port Registers
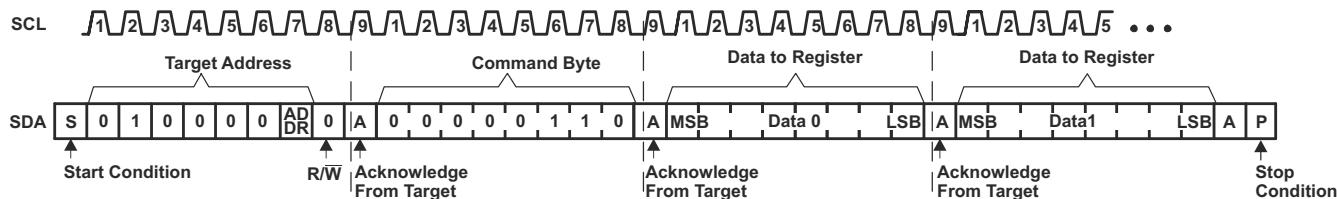
Figure 7-10. Write to Configuration Registers

7.6.4.2 Reads

The bus controller must first send the TCAL6408 address with the LSB set to a logic 0 (see Figure 7-7 for device address). The command byte is sent after the address and determines which register is accessed.

Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus controller must not acknowledge the data.
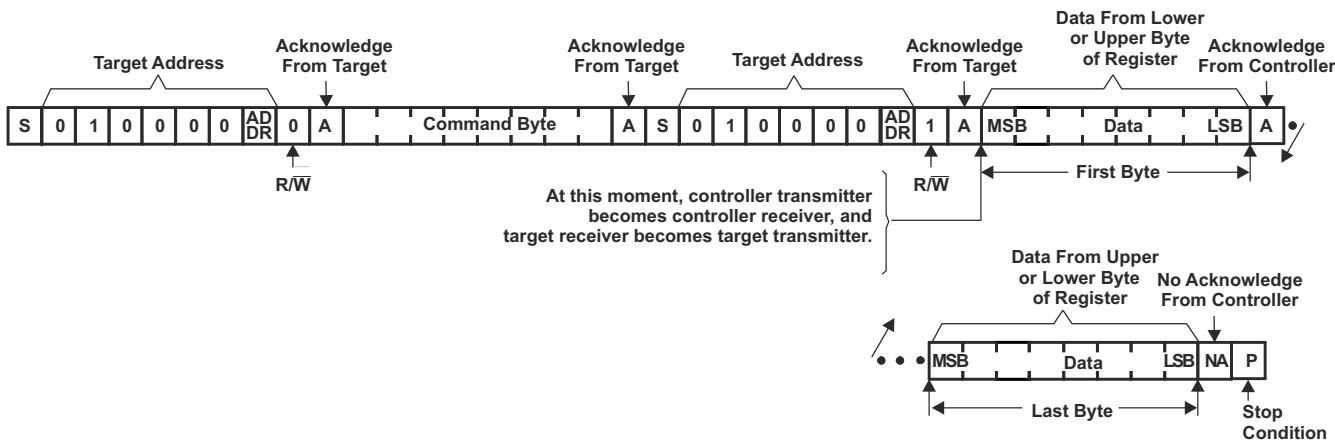
Figure 7-11. Read From Register
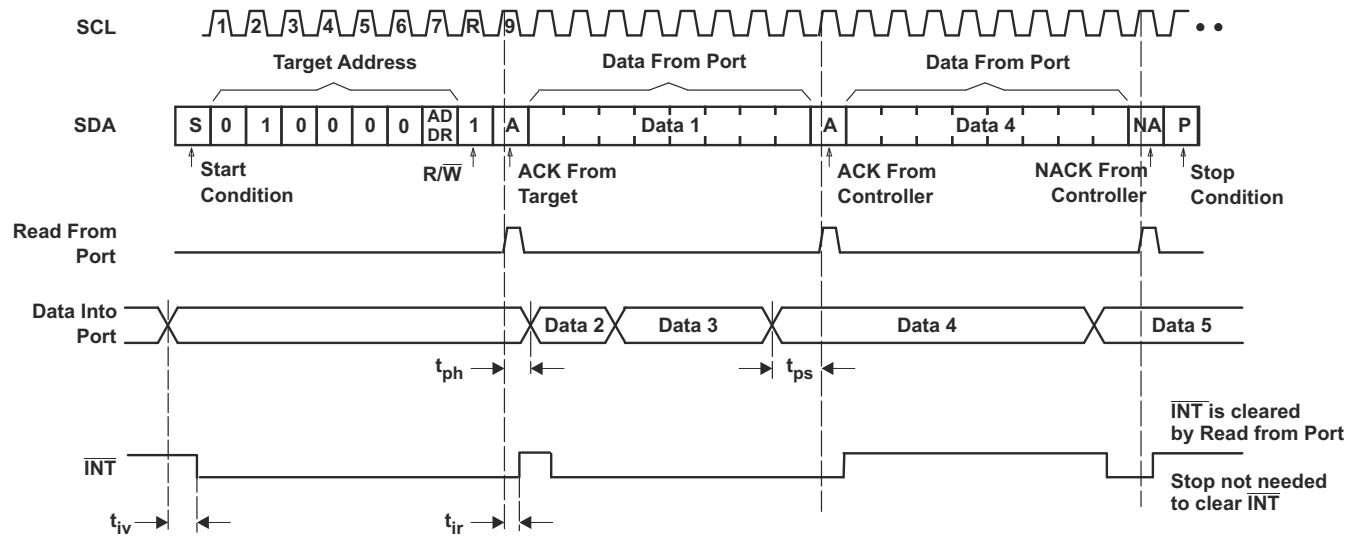
A. Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (read Input Port register).

B. This figure eliminates the command byte transfer, a restart, and target address call between the initial target address call and actual data transfer from P port (see Figure 7-11).

Figure 7-12. Read Input Port Register

Product Folder Links: *TCAL6408*

8 Application and Implementation

> **Note**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

TCAL6408 is used in applications where this device is connected as a target to an I^2C controller (processor); the I^2C bus may contain any number of other target devices. The TCAL6408 is in a remote location from the controller, placed close to the GPIOs to which the controller needs to monitor or control.

A typical application of the TCAL6408 operates with a lower voltage on the controller side (V_{CCI}), and a higher voltage on the P-port side (V_{CCP}). The P-ports can be configured as outputs connected to inputs of devices such as enable, reset, power select, the gate of a switch, and LEDs. The P-ports can also be configured as inputs to receive data from interrupts, alarms, status outputs, or push buttons.

8.2 Typical Application

shows an application in which the TCAL6408 can be used.
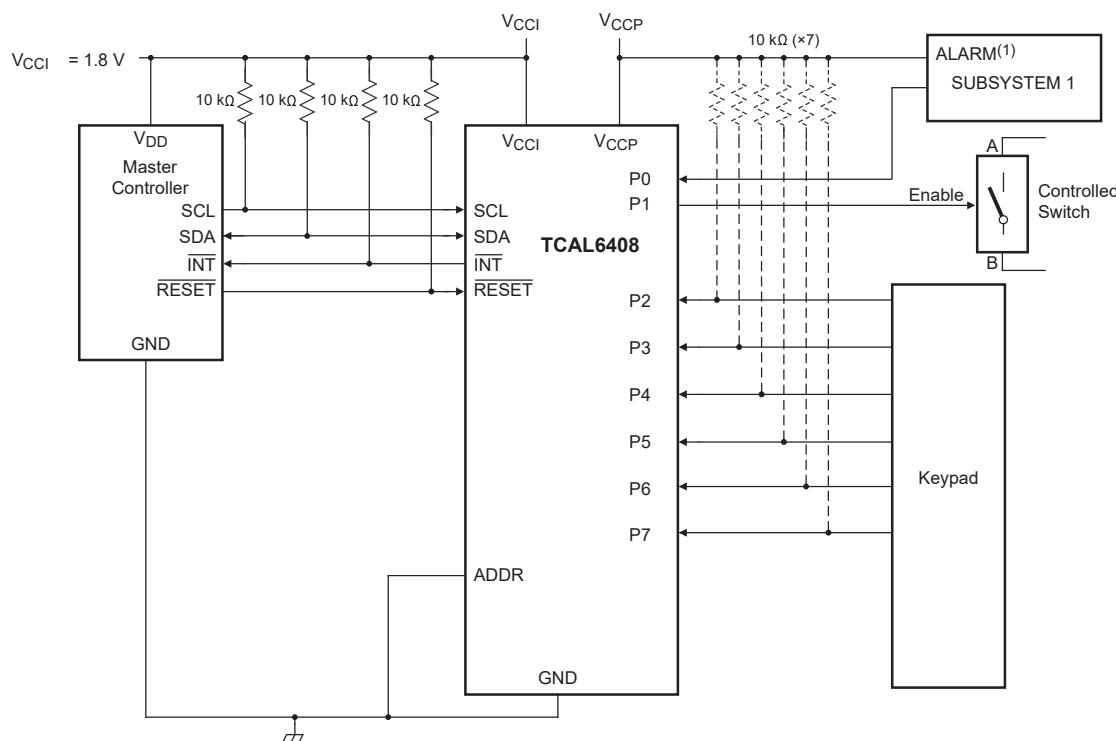
A. Device address configured as 0100000 for this example.
B. P0 and P2–P7 are configured as inputs.
C. P1 is configured as an output.
D. Resistors are required for inputs (on P port) that may float. If a driver to an input will never let the input float, a resistor is not needed. Outputs (in the P port) do not need pullup resistors.

Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
I^{2}C input voltage (V$_{CCI}$)	1.8V
P-port input/output voltage (V$_{CCP}$)	3.6V
Output current rating, P-port sinking (I$_{OL}$)	25mA
Output current rating, P-port sourcing (I$_{OH}$)	10mA
I^{2}C bus clock (SCL) speed	1MHz

8.2.2 Detailed Design Procedure

The pull-up resistors, R$_P$, for the SCL and SDA lines need to be selected appropriately and take into consideration the total capacitance of all targets on the I^{2}C bus. The minimum pull-up resistance is a function of V$_{CCI}$, V$_{OL,(max)}$, and I$_{OL}$:

$$R_{p(min)} = \frac{V_{CCI} - V_{OL(max)}}{I_{OL}}$$
(1)

The maximum pull-up resistance is a function of the maximum rise time, t$_r$ (120ns for fast-mode-plus operation, f$_{SCL}$ = 1MHz) and bus capacitance, C$_b$:

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b}$$
(2)

The maximum bus capacitance for an I^{2}C bus must not exceed 400pF for standard-mode or fast-mode operation, or 550pF for fast-mode-plus. The bus capacitance can be approximated by adding the capacitance of the TCAL6408, C$_i$ for SCL, or C$_{io}$ for SDA. Plus the capacitance of wires, connections, traces, and the capacitance of additional targets on the bus.

8.2.2.1 Minimizing I$_{CC}$ When I/Os Control LEDs

As shown in Figure 8-2, normally I/Os are connected to V$_{CCP\,CC}$ through a resistor when the I/Os are used to control LEDs. For a P-port configured as an input, current consumption increases as V$_I$ becomes lower than V$_{CCP\,CC}$. The LEDs are diodes with threshold voltage V$_T$, and are off when a P-port is configured as an input, but the voltages at the P-port will be equal to V$_{CCPCC\,CC}$ minus V$_T$.

For battery-powered applications, it is essential that the voltage of P-ports controlling the LEDs is greater than or equal to V$_{CCP\,CC}$ when the P-ports are configured as input to minimize current consumption. Figure 8-2 shows a high-value resistor in parallel with the LED. Figure 8-3 shows V$_{CCP\,CC}$ less than the LED supply voltage by at least V$_T$. Both of these methods maintain the I/O V$_I$ at or above V$_{CCP\,CC}$ and prevent additional supply current consumption when the P-port is configured as an input and the LED is off.
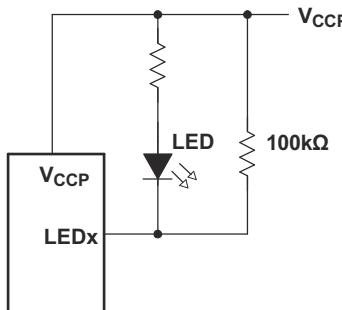

Figure 8-2. High-Value Resistor in Parallel with LED

Product Folder Links: *TCAL6408*
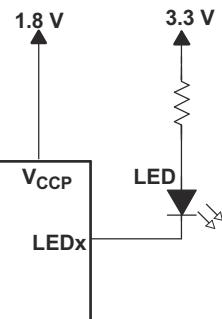
Figure 8-3. Device Supplied by a Lower Voltage

8.2.3 Application Curves

Standard-mode: f_{SCL} = 100kHz, t_r = 1 μs
Fast-mode: f_{SCL} = 400kHz, t_r = 300ns
Fast-mode plus: f_{SCL} = 1MHz, t_r = 120ns

Figure 8-4. Maximum Pullup Resistance ($R_{p(max)}$) vs Bus Capacitance (C_b)

V_{OL} = 0.2 × V_{CC}, I_{OL} = 2mA when V_{CC} ≤ 2V
V_{OL} = 0.4V, I_{OL} = 3mA when V_{CC} > 2V

Figure 8-5. Minimum Pullup Resistance ($R_{p(min)}$) vs Pullup Reference Voltage (V_{CC})
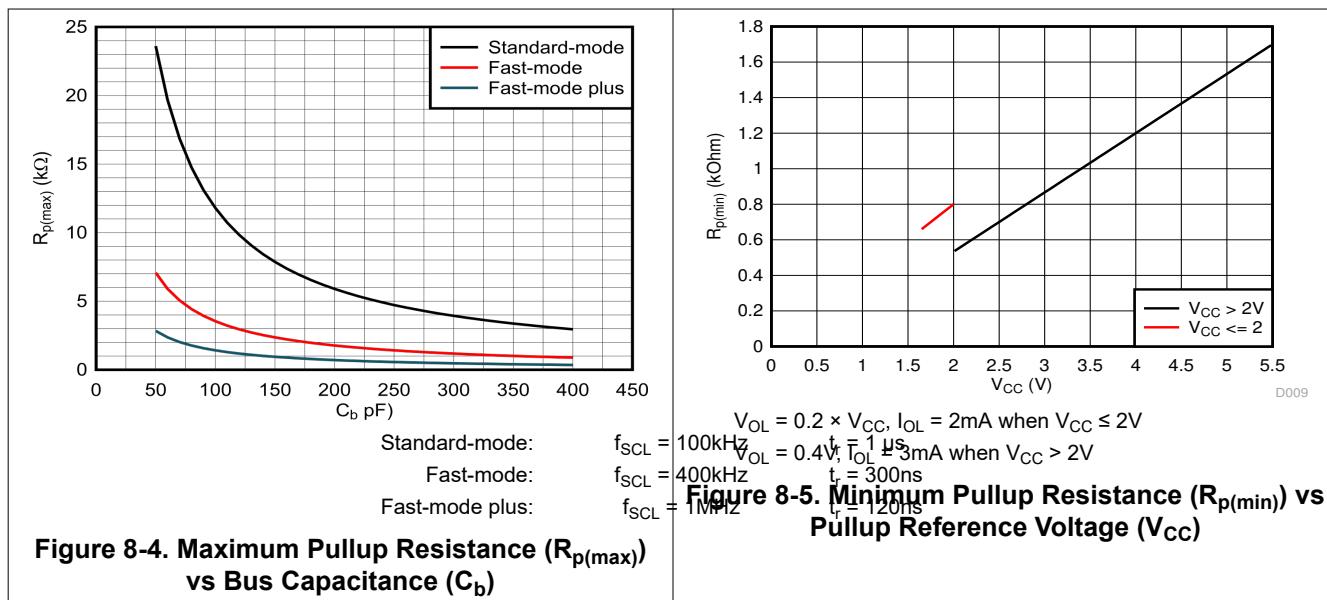
8.3 Power Supply Recommendations

8.3.1 Power-On Reset Requirements

In the event of a glitch or data corruption, TCAL6408 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

Figure 8-6 and Figure 8-7 shows the two types of power-on reset.
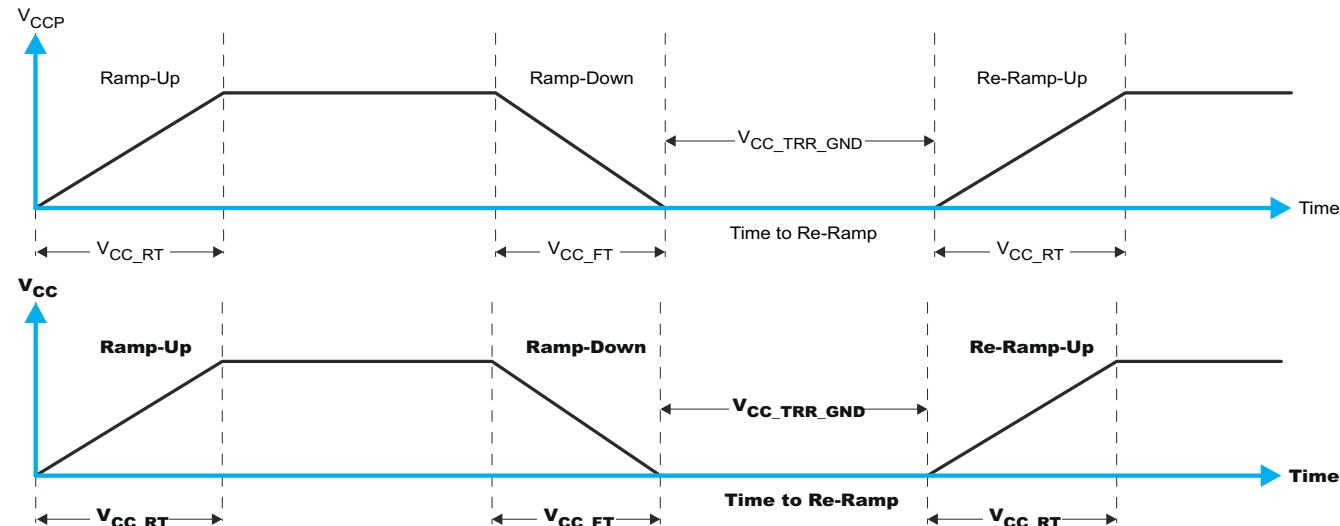
Figure 8-6. V_{CCP} is Lowered Below 0.2V or 0V and Then Ramped Up
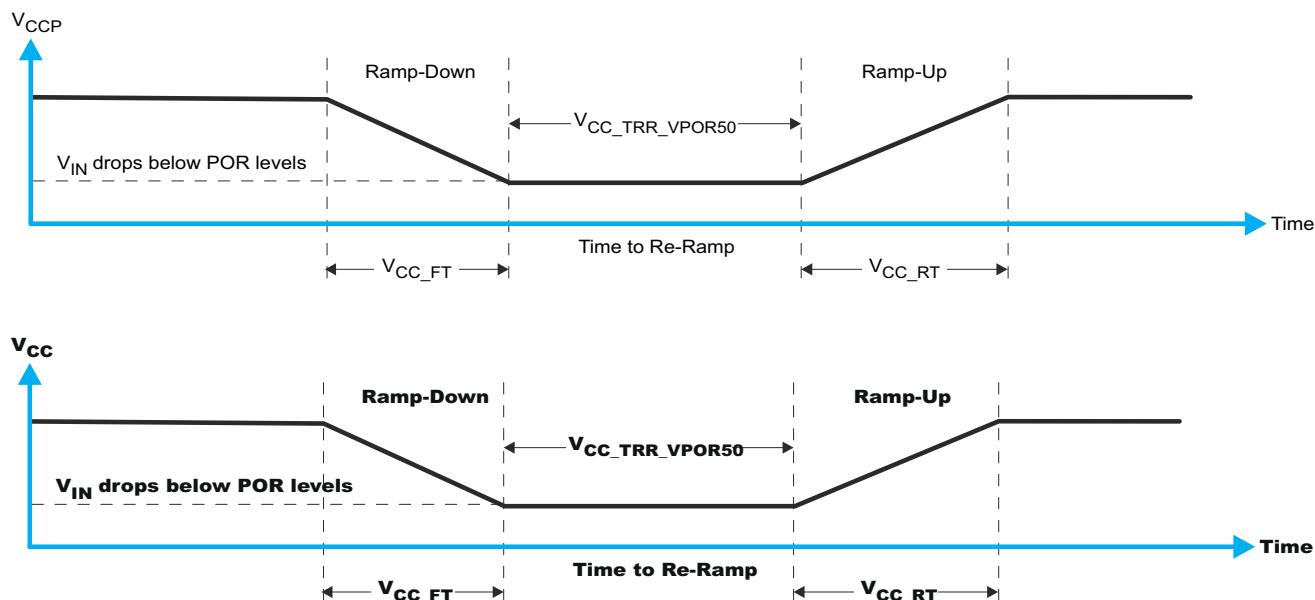
Figure 8-7. V_{CCP} is Lowered Below the POR Threshold, then Ramped Back Up

Table 8-2 lists the performance of the power-on reset feature for both types of power-on reset.

Table 8-2. Recommended Supply Sequencing and Ramp Rates

PARAMETER[1] [2]		MIN	TYP	MAX	UNIT
t_{FT} Fall rate	See Figure 8-6	0.1		2000	ms

Table 8-2. Recommended Supply Sequencing and Ramp Rates (continued)

| PARAMETER[1] [2]			MIN	TYP	MAX	UNIT
t_{RT}	Rise rate	See Figure 8-6	0.1		2000	ms
t_{TRR_GND}	Time to re-ramp (when V_{CC} drops to GND)	See Figure 8-6	1			µs
t_{TRR_POR50}	Time to re-ramp (when V_{CC} drops to $V_{POR\_MIN} - 50mV$)	See Figure 8-7	1			µs
V_{CC_GH}	Level that V_{CCP} can glitch down to, but not cause a functional disruption when $V_{CCP\_GW} = 1µs$	See Figure 8-8			1.0	V
t_{GW}	Glitch width that will not cause a functional disruption when $V_{CCP\_GH} = 0.5 \times V_{CCx}$	See Figure 8-8			10	µs
V_{PORF}	Voltage trip point of POR on falling V_{CC}			0.6		V
V_{PORR}	Voltage trip point of POR on rising V_{CC}				1.0	V

(1) T_A = 25°C (unless otherwise noted).
(2)   Not tested. Specified by design.

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. For more information on how to measure these specifications, see Figure 8-8 and Table 8-2.

Figure 8-8. Glitch Width and Glitch Height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I2C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CCP} being lowered to or from 0. For more details on this specification, see Figure 8-9 and Table 8-2.

Product Folder Links: *TCAL6408*

Figure 8-9. V$_{POR}$

Product Folder Links: *TCAL6408*
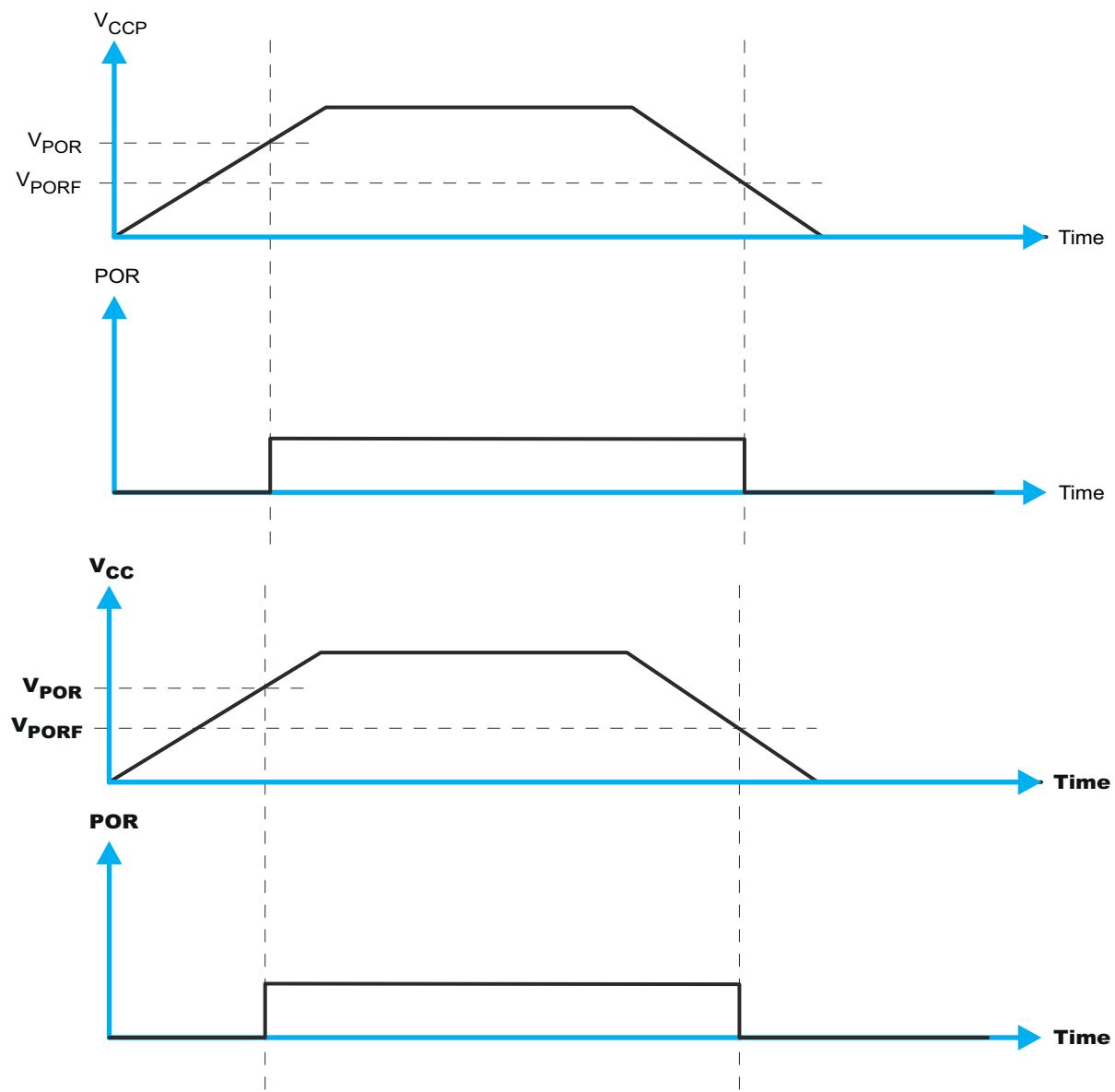
8.4 Layout

8.4.1 Layout Guidelines

For device reliability, follow common printed circuit board (PCB) layout practices. Additional concerns related to high-speed data transfer, such as matched impedance and differential pairs, are not a concern for I^{2}C signal speeds.

It is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces in all PCB layouts. Bypass and decoupling capacitors are commonly used to control the voltage on the supply pins. Using a larger capacitor provides additional power in the event of a short power supply glitch, and using a smaller capacitor filters out high-frequency ripple. These capacitors should be placed as close to the TCAL6408 as possible. Figure 8-10 shows these best practices.

For the layout example provided in Figure 8-10 , it is possible to fabricate a PCB with only 2 layers by using the top layer for signal routing and the bottom layer as a split plane for power and ground (GND). However, a 4 layer board is preferable for boards with higher density signal routing. On a 4 layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface mount component pad which needs to attach to power or GND and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace needs to be routed to the opposite side of the board, but this technique is not demonstrated in Figure 8-10 .

8.4.2 Layout Example
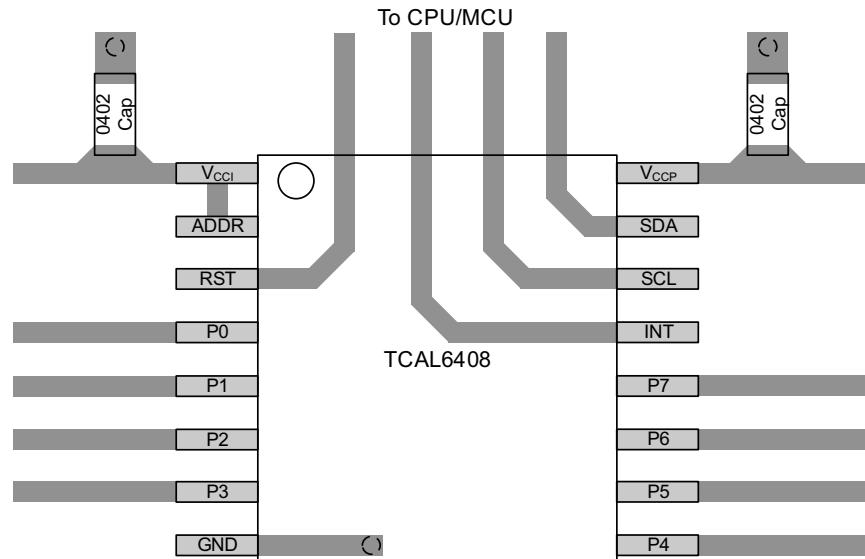
Figure 8-10. TCAL6408 Layout

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (November 2023) to Revision C (January 2025)	Page
• Added a footnote in *Absolute Maximum Ratings* for IO connection to GND.	4

Changes from Revision A (December 2022) to Revision B (November 2023)	Page
• Changed the *Device Information* table to the *Package Information* table. Deleted the *Product Preview* note...	1

Changes from Revision * (November 2022) to Revision A (December 2022)	Page
• Changed the document status from: *Advanced Information* to: *Production* data...	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TCAL6408DTUR	Active	Production	X2QFN (DTU) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	NG
TCAL6408DTUR.A	Active	Production	X2QFN (DTU) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	NG
TCAL6408PWR	Active	Production	TSSOP (PW) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL6408
TCAL6408PWR.A	Active	Production	TSSOP (PW) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL6408
TCAL6408RSVR	Active	Production	UQFN (RSV) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	6408
TCAL6408RSVR.A	Active	Production	UQFN (RSV) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	6408

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS
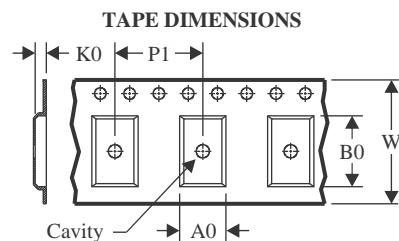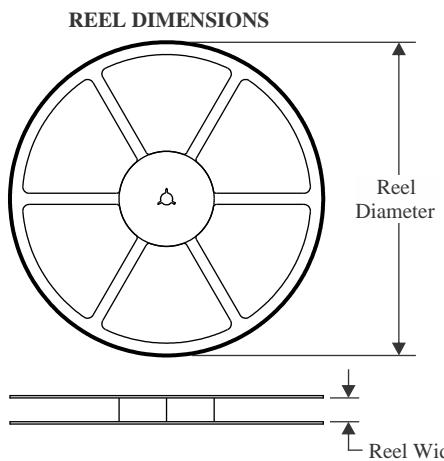
TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE
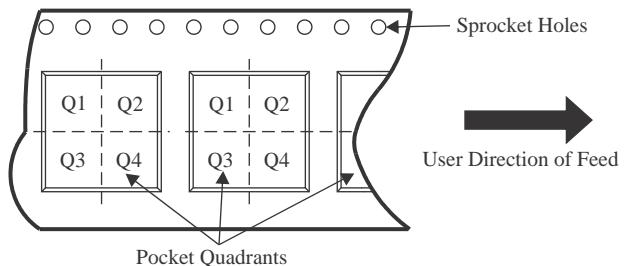
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCAL6408DTUR	X2QFN	DTU	16	3000	180.0	9.5	1.75	1.75	0.5	4.0	8.0	Q1
TCAL6408PWR	TSSOP	PW	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TCAL6408RSVR	UQFN	RSV	16	3000	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS
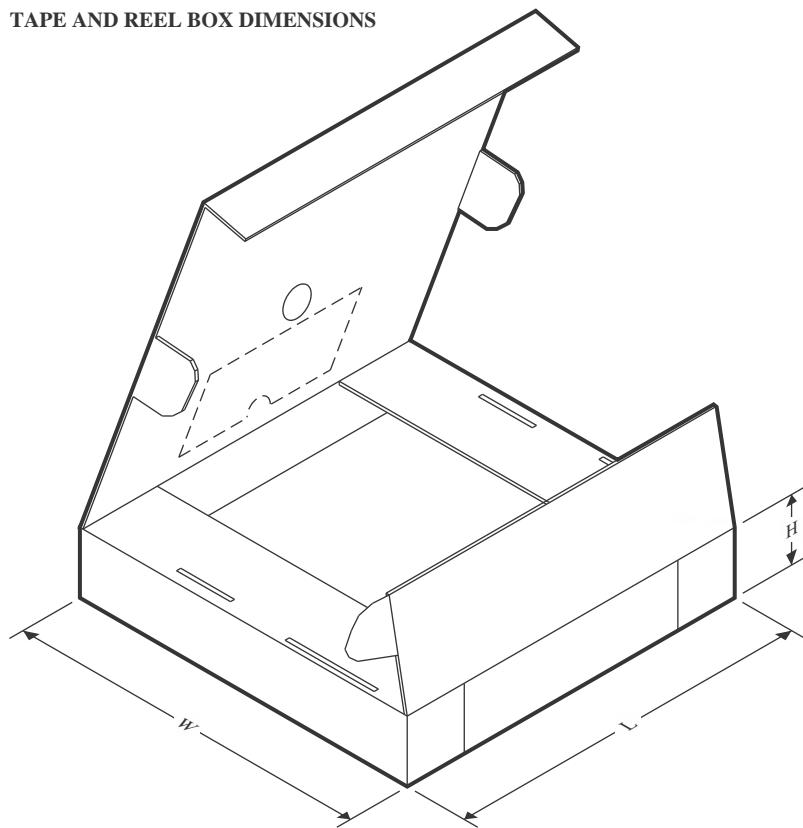
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCAL6408DTUR	X2QFN	DTU	16	3000	189.0	185.0	36.0
TCAL6408PWR	TSSOP	PW	16	3000	353.0	353.0	32.0
TCAL6408RSVR	UQFN	RSV	16	3000	189.0	185.0	36.0

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.
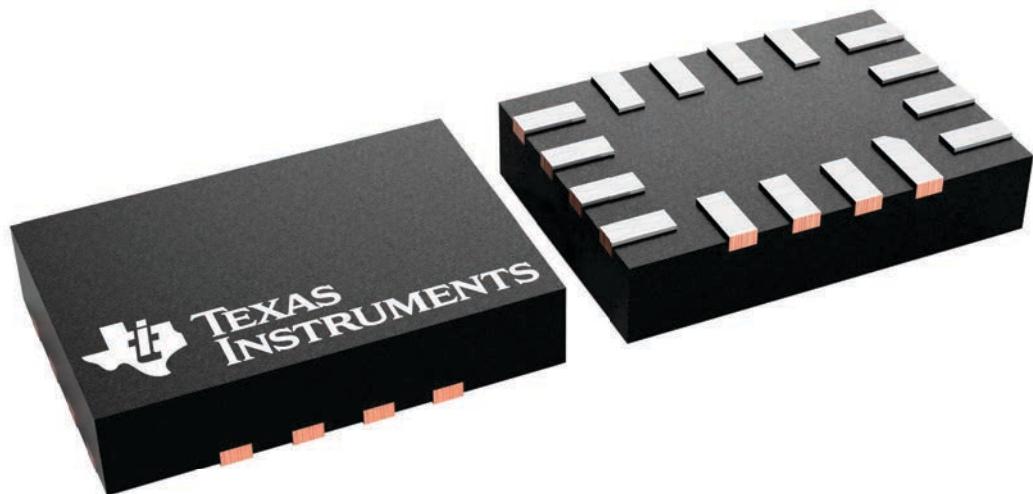
4231225/A

B   1.85 / 1.75   A

PIN 1 INDEX AREA

2.65 / 2.55

0.55 / 0.45

0.05 / 0.00

C

SEATING PLANE

0.05 C

2X 1.2

SYMM

5   8

15X 0.45 / 0.35

4   9

SYMM

2X 1.2

12X 0.4

1   12

16   13

0.55 / 0.45

PIN 1 ID
(45° X 0.1)

16X 0.25 / 0.15

⊕ 0.07 Ⓜ C A B
  0.05 Ⓜ

(0.13) TYP
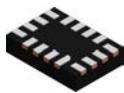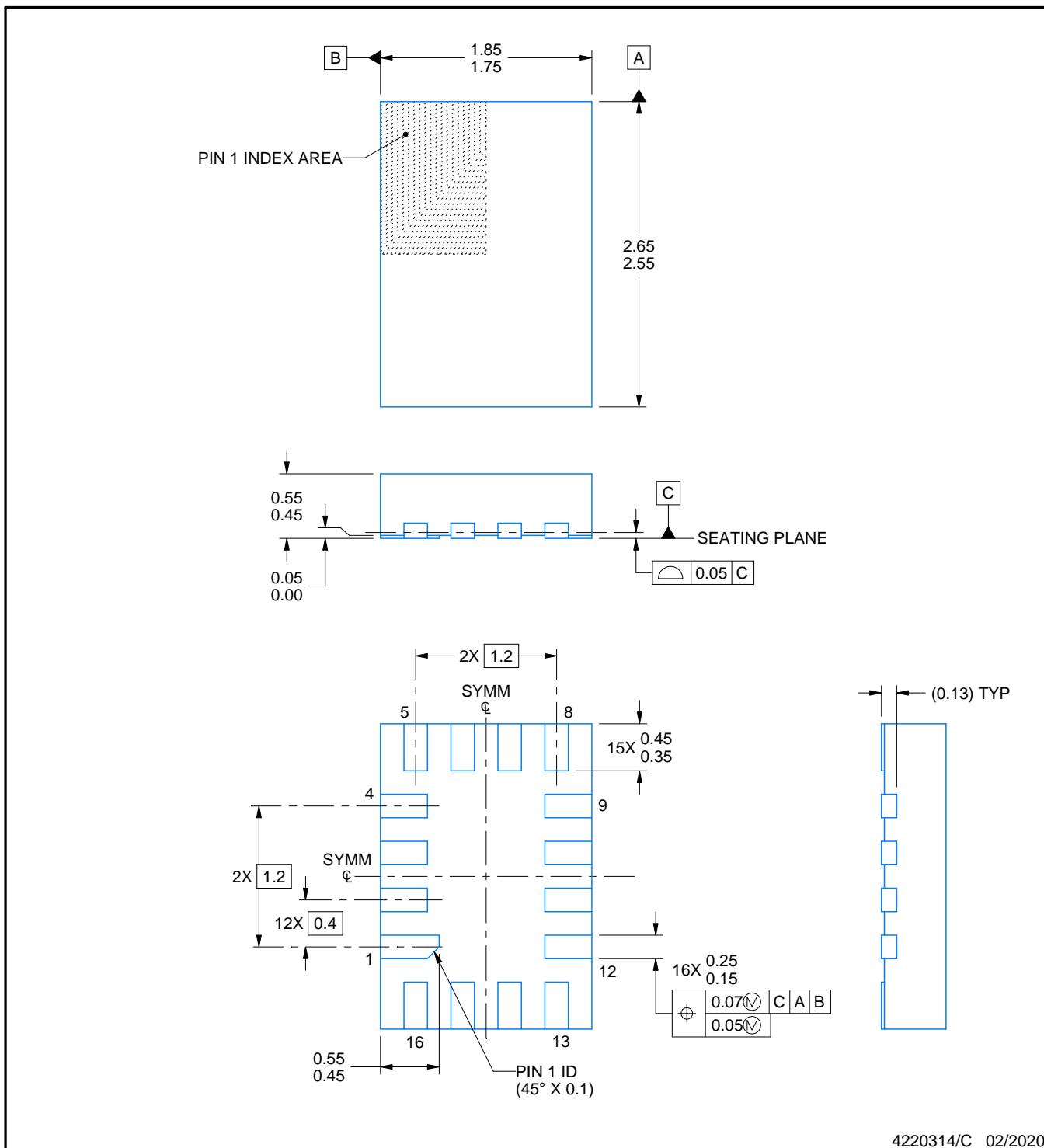
4220314/C   02/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

RSV0016A

(0.7)

SYMM
℄

16

13

SEE SOLDER MASK
DETAIL

16X (0.2)

1

12

12X (0.4)

SYMM
℄

(2.4)

(R0.05) TYP

4

9

15X (0.6)

5

8

(1.6)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

0.05 MAX
ALL AROUND

METAL EDGE

EXPOSED METAL

SOLDER MASK
OPENING

NON SOLDER MASK
DEFINED
(PREFERRED)

0.05 MIN
ALL AROUND

METAL UNDER
SOLDER MASK
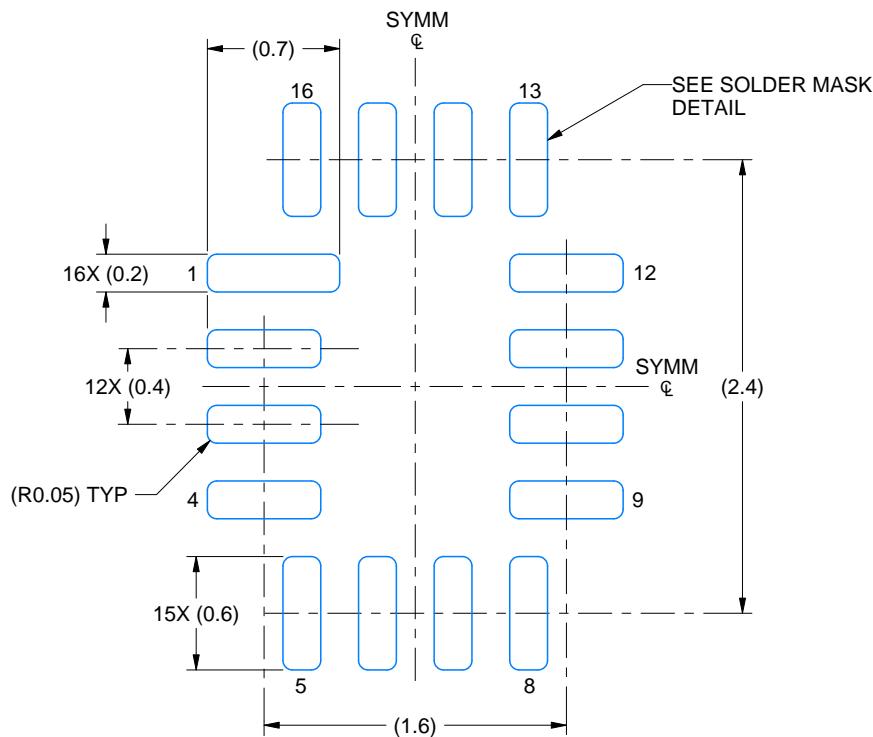
EXPOSED
METAL

SOLDER MASK
OPENING

SOLDER MASK DEFINED
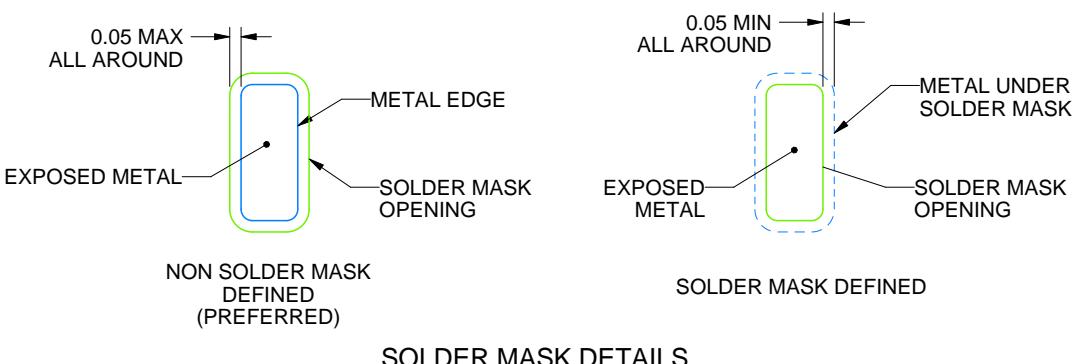
SOLDER MASK DETAILS

4220314/C   02/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

(0.7)

16   13

16X (0.2)   1   12

12X (0.4)

(R0.05) TYP

4   9

15X (0.6)

5   8

SYMM
℄

SYMM
℄

(2.4)

(1.6)
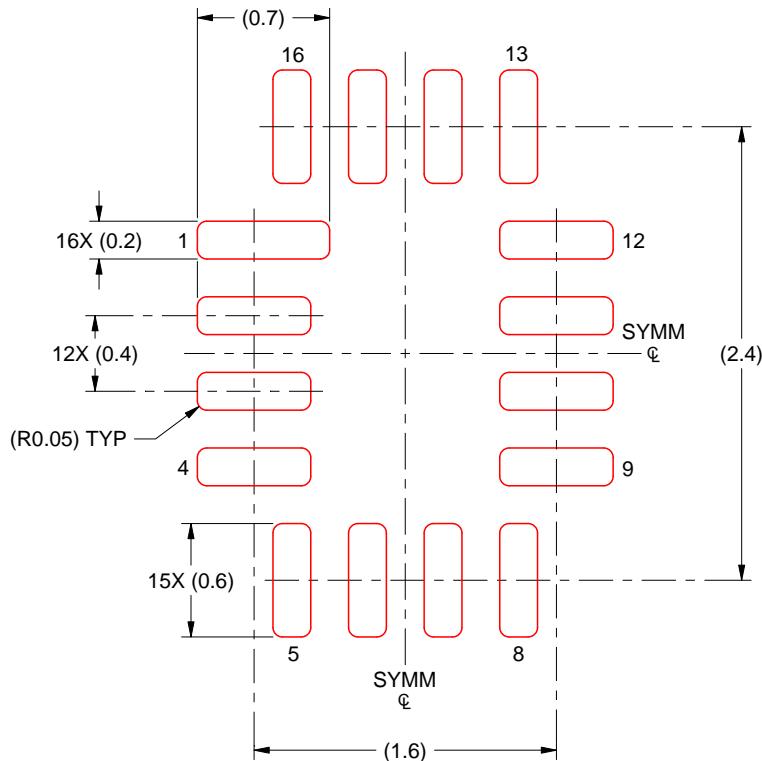
SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 25X

4220314/C   02/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.

6.6
6.2 TYP

A

PIN 1 INDEX AREA

14X 0.65

16

1

2X

4.55

5.1
4.9
NOTE 3

8

9

B

4.5
4.3
NOTE 4

16X 0.30
0.17

⊕ 0.1 Ⓜ C A B

SEATING
PLANE

C

⌒ 0.1 C

4X (0°-12°)

1.2 MAX

SEE DETAIL A

(0.15) TYP

0.25
GAGE PLANE

0.15
0.05

0°-8°

0.75
0.50

DETAIL A
TYPICAL

4220204/B   12/2023
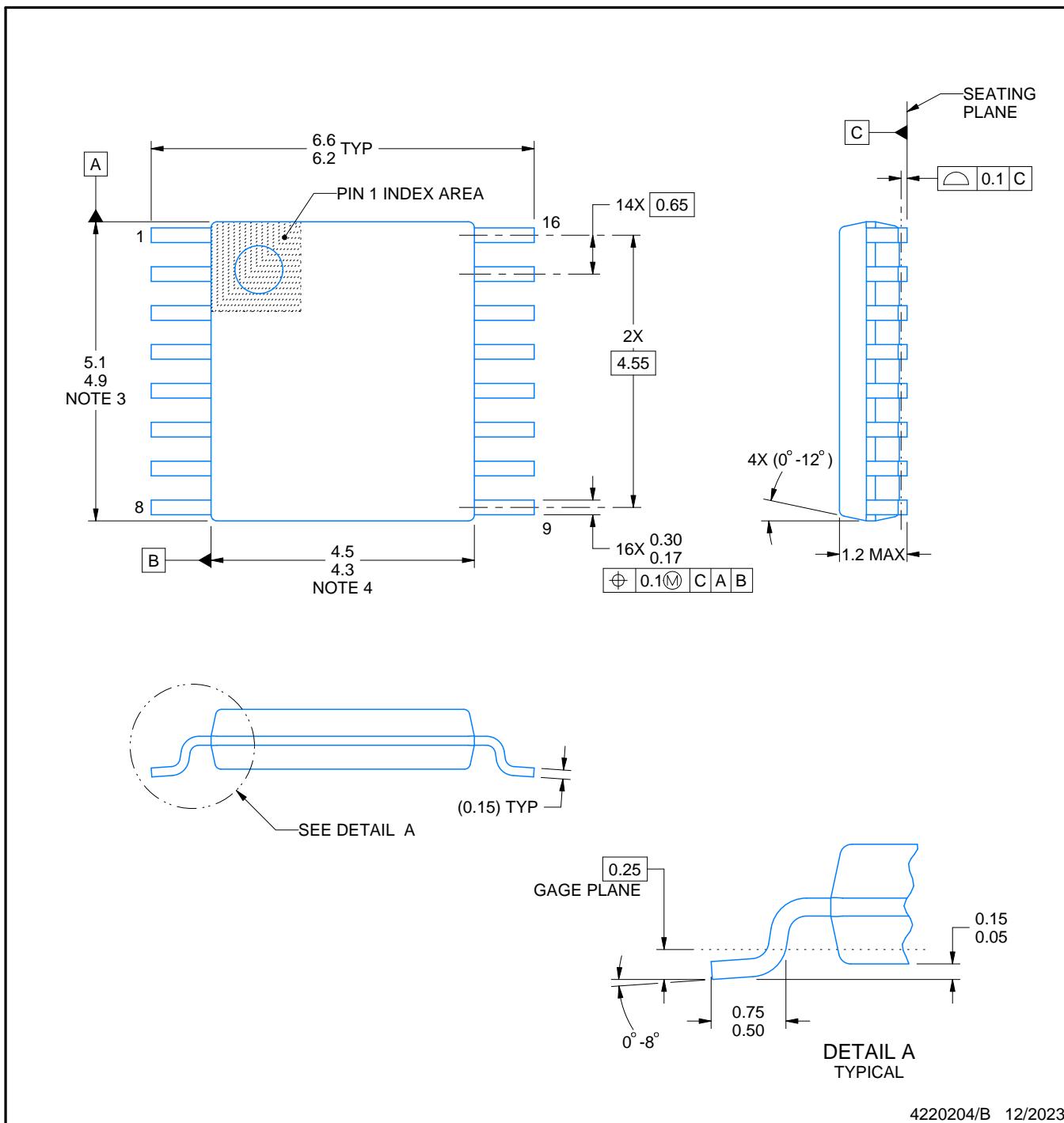
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

16X (1.5)

SYMM

1

16X (0.45)

(R0.05) TYP

16

SYMM

14X (0.65)

8

9

(5.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
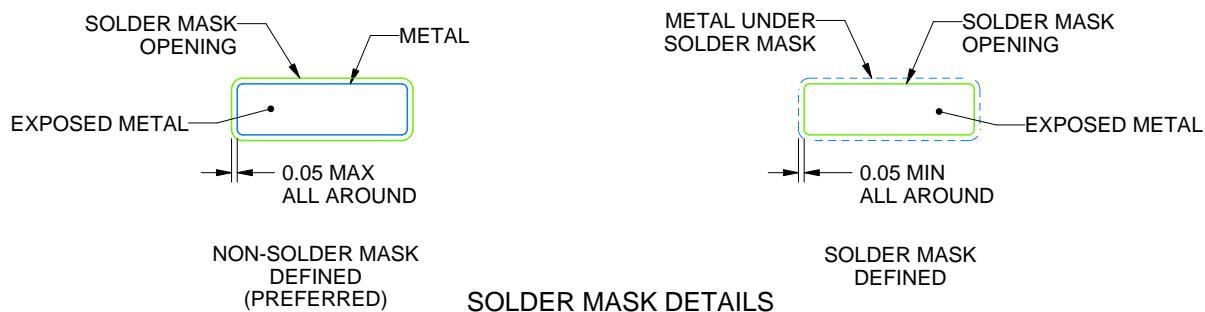
4220204/B   12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

16X (1.5)

SYMM

1

16X (0.45)

(R0.05) TYP

16

SYMM

14X (0.65)

8

9

(5.8)
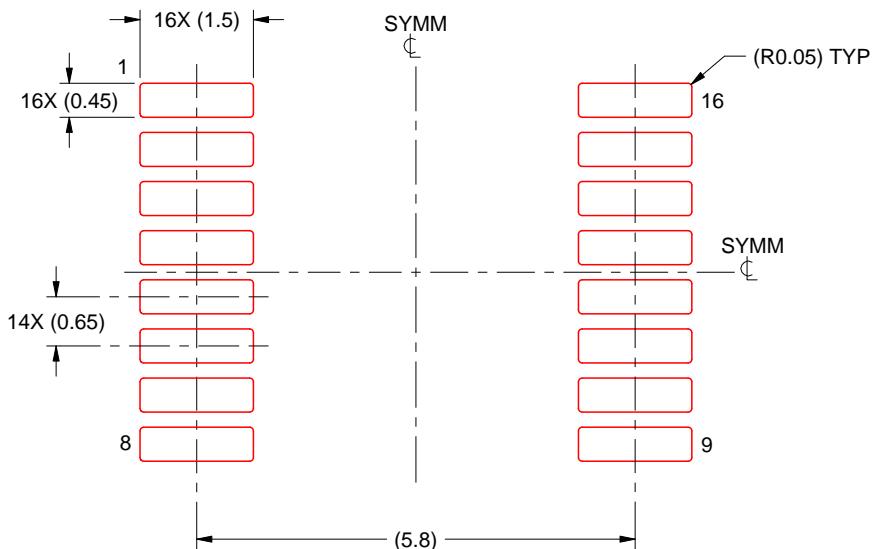
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B   12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

B 1.65 / 1.55

A

PIN A1
INDEX AREA

1.65 / 1.55

C

SEATING PLANE

0.05 C

0.4 / 0.3

// 0.05 C

(0.115) TYP

(0.115) TYP

□16X 0.22 / 0.12

SYMM

(0.25)

(0.1)

SYMM

D   C   B   A

1   2   3   4

PIN 1 ID

1.2

1.2

0.4 TYP

0.4 TYP

4228238/B   03/2022

PicoStar is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is for Embedded Application only.

DTU0016A

X2QFN **- 0.4 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD

(1.2) TYP

(0.4) TYP

(R0.05) TYP

(0.4) TYP

(1.2) TYP

SYMM
₵

SYMM
₵

16X (⬜0.17)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:50X

0.0325 MAX

0.0325 MIN

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED
METAL

EXPOSED
METAL

NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4228238/B   03/2022

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

(1.2) TYP

(0.4) TYP

16X (□0.17)

(0.4) TYP

(1.2) TYP

SYMM
℄

(R0.05) TYP

SYMM
℄

SOLDER PASTE EXAMPLE
BASED ON 0.0625 mm THICK STENCIL
SCALE:50X

4228238/B 03/2022

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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