TCAN285x-Q1 Automotive CAN FD SIC and LIN System Basis Chip (SBC) with Wake Inputs and High-side Switches

1 Features

- AEC-Q100 qualified for automotive applications
- Meets the requirements for CAN flexible data (FD) including the signal improvement capability (SIC) per ISO 11898-2:2024
- Local interconnect network (LIN) physical layer specification ISO/DIS 17987–4:2024 compliant and conforms to SAEJ2602 recommended practice for LIN
- Functional Safety Quality-Managed
- Simplifies system power management with up to three regulators
  - Low drop out (LDO) regulator supporting up to 250mA for 3.3V or 5V MCUs (VCC1)
  - Short-to-battery protected 5V LDO regulator supporting up to 200mA externally (VCC2)
  - Control of an external PNP transistor supporting up to 350mA at 1.8V, 2.5V, 3.3V, or 5V (VEXCC)
- Multiple methods to wake from sleep mode
  - CAN and LIN bus wake up pattern (WUP)
  - Optional, CAN selective wake up frame (WUF) capability (partial networking)
  - Local wake up (LWU) using WAKE pins
    - Cyclic sensing wake up support with HSS4
  - Digital wake up using the SW pin
- Four high-side switches for loads up to 150mA
- Protection and diagnostic features
  - Timeout, window, and Q&A watchdog support
  - Undervoltage (UV), overvoltage (OV), and short-circuit supervision on regulator outputs
  - Fail-safe output (LIMP)
  - UV supervision of VSUP and VHSS; OV supervision of VHSS
  - Advanced CAN bus fault diagnostics
  - ±58V CAN bus fault tolerance
  - Integrated system level ESD protection
- Customer-accessible EEPROM to save device configuration
- QFN (32) package with improved automated optical inspection (AOI) capability

2 Applications

- Body electronics and lighting
- Body Control Modules
- Infotainment and cluster
- Hybrid, electric and power train systems
- Industrial transportation

3 Description

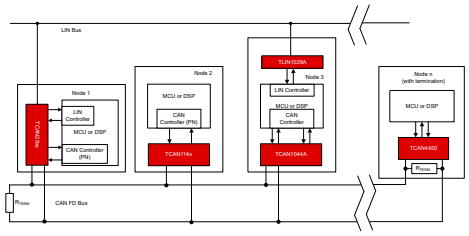
The TCAN285x-Q1 is a family of system basis chips (SBC) that provide a control area network flexible data rate capable (CAN FD) transceiver that supports selective wake. The TCAN2857-Q1 includes a local interconnect network (LIN) transceiver. The CAN FD transceiver supports data rates up to 8Mbps while the LIN transceiver supports fast mode data rates up to 200kbps. The VCC1 LDO provides 3.3V or 5V ±2% with up to 250mA of current and determines the digital IO logic levels. If more current is needed, an external PNP transistor can be used to support up to 350mA and voltages of 1.8V, 2.5V, 3.3V, or 5V. VCC2 LDO provides 5V up to 200mA.

The TCAN285x-Q1 includes features such as LIMP, three local wake inputs and four high side switches. The high side switch can be on/off, 10-bit PWM or timer controlled. Controlling an external CAN FD, LIN transceiver, CAN SBC or LIN SBC is possible using the GFO pin. The WAKE pins can be configured for static sensing, cyclic sensing (with HSS4 pin) and pulse based for waking up. These devices provide EEPROM to store specific device configuration information; thus, avoiding extensive reprogramming after power fluctuations. WAKE1 and WAKE2 can enable an internal switch between pins to enable external V_{BAT} monitoring. WAKE3 can be configured as a direct drive control pin for any combinations of high-side switches when cyclic sensing wake is enabled.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TCAN2855-Q1 TCAN2857-Q1	QFN (RHB, 32)	5mm × 5mm

(1) For more information, see Mechanical, Packaging and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

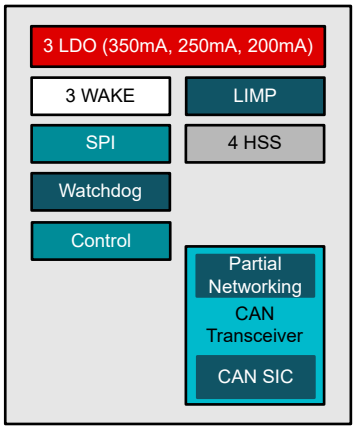


Figure 3-1. TCAN2855-Q1 Diagram

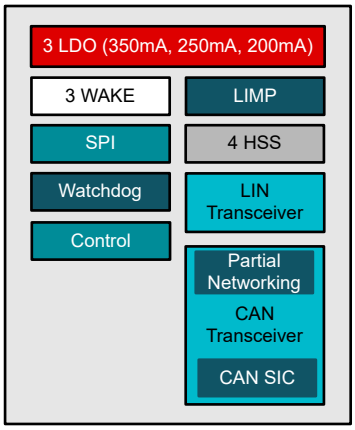


Figure 3-2. TCAN2857-Q1 Diagram

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4 Device Comparison Table

Device Number	CAN FD SIC Transceiver	LIN Transceiver	Selective Wake	3.3V LDO	5V LDO
TCAN28553RHBQ1	X		X	X	
TCAN28555RHBQ1	X		X		X
TCAN28573RHBQ1	X	X	X	X	
TCAN28575RHBQ1	X	X	X		X

5 Pin Configuration and Functions

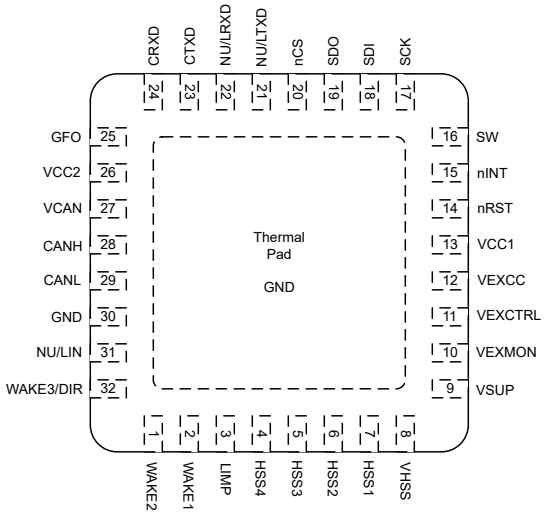


Figure 5-1. RHB Package, 32 Pin (QFN)
Top View

Table 5-1. Pin Functions RHB Package

PIN			TYPE	DESCRIPTION
NO.	TCAN2855-Q1	TCAN2857-Q1		
1	WAKE2	WAKE2	high voltage	Local wake input terminal, high voltage capable
2	WAKE1	WAKE1	high voltage	Local wake input terminal, high voltage capable
3	LIMP	LIMP	high voltage	Limp home output (Active low; open-drain output)
4	HSS4	HSS4	high voltage	High side switch
5	HSS3	HSS3	high voltage	High side switch
6	HSS2	HSS2	high voltage	High side switch
7	HSS1	HSS1	high voltage	High side switch
8	VHSS	VHSS	power	High side switch power
9	VSUP	VSUP	high voltage power	High voltage supply from the battery
10	VEXMON	VEXMON	power	External PNP emitter connection, shunt connection. Connect to VSUP if external PNP LDO is not used. DO not leave floating.
11	VEXCTRL	VEXCTRL	power	External PNP base control
12	VEXCC	VEXCC	power	External PNP collector connection feedback
13	VCC1	VCC1	power	LDO supply output: 3.3V or 5V
14	nRST	nRST	digital	VCC output monitor pin (active low) and device reset input
15	nINT	nINT	digital	Interrupt output (active low)
16	SW	SW	digital	Programming mode input pin (SPI configurable active high or active low)
17	SCK	SCK	digital	SPI clock input
18	SDI	SDI	digital	SPI data input
19	SDO	SDO	digital	SPI data output
20	nCS	nCS	digital	Chip select input (active low)
21	NU	LTXD	digital	LIN transmit data input (low for dominant and high for recessive bus states). NU is not used and must not be connected to anything.

Table 5-1. Pin Functions RHB Package (continued)

PIN			TYPE	DESCRIPTION
NO.	TCAN2855-Q1	TCAN2857-Q1		
22	NU	LRXD	digital	LIN receive data output (low for dominant and high for recessive bus states), tri-state. NU is not used and must not be connected to anything.
23	CTXD	CTXD	digital	CAN transmit data input (low for dominant and high for recessive bus states).
24	CRXD	CRXD	digital	CAN receive data output (low for dominant and high for recessive bus states), tri-state.
25	GFO	GFO	digital	Function output pin (SPI configurable)
26	VCC2	VCC2	power	5V LDO output
27	VCAN	VCAN	power	CAN FD transceiver 5V power supply input
28	CANH	CANH	bus I/O	High level CAN bus I/O line
29	CANL	CANL	bus I/O	Low level CAN bus I/O line
30	GND	GND	power	Ground connection: Must be soldered to ground
31	NU	LIN	high voltage I/O	LIN bus input/output pin: NU is not used and must not be connected to anything.
32	WAKE3/DIR	WAKE3/DIR	high voltage	Local wake input terminal, high voltage capable. Direct drive to control any HSSx when configured
PAD(1)	GND	GND	power	Ground connection: Must be soldered to ground

(1) The thermal pad, PAD, is a device ground pin must be soldered to GND

6 Specifications

6.1 Absolute Maximum Ratings

Over recommended operating range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VSUP	Supply voltage (2)	–0.3	40	V
VHSS	High-side switches supply voltage (2)	–0.3	40	V
VEXMON	External PNP emitter monitor voltage	V_{SUP}–0.7	40 and $V_O \le V_{SUP}$+0.3	V
VEXCC	External PNP collector feedback voltage(2)	–0.3	40 and $V_O \le V_{SUP}$+0.3	V
VEXCTRL	External PNP base control voltage	–0.3	40 and $V_O \le V_{SUP}$+0.3	V
VCC1	Regulated 3.3V and 5V output supply	–0.3	6	V
V_{nRST}	Reset output voltage	-0.3	V_{CC} + 0.3	V
VCAN	CAN transceiver supply voltage	–0.3	6	V
VCC2	5V output supply(2)	–1	28	V
V_{BUSCAN}	CAN bus I/O voltage (CANH, CANL)	–58	58	V
V_{BUSLIN}	LIN bus I/O voltage	–58	58	V
V_{WAKE}	WAKE input voltage	–0.3	40	V
V_{HSSx}	High-side switch pin output voltage range	–0.3	40 and $V_O \le$ VHSS+0.3	V
V_{LIMP}	LIMP pin output voltage range	–0.3	40 and $V_O \le V_{SUP}$+0.3	V
V_{LOGIC_IN}	Logic pin input voltage range (SW, SDI, SCK, nCS, nRST, LTXD, CTXD)	–0.3	6	V
V_{LOGIC_OUT}	Logic pin output voltage range (SDO, nRST, LRXD, CRXD, GFO)	–0.5	6	V
$I_{O(LOGIC)}$	Logic pin output current (SDO, LRXD, CRXD, GFO)		8	mA
$I_{(WAKE)}$	WAKE pin input current		3	mA
$I_{(LIMP)}$	LIMP pin input current		20	mA
$I_{O(nRST)}$	Reset output current	–5	5	mA
T_J	Junction temperature	–55	165	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Able to support load dumps of up to 40 V for 300ms

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM) Classification Level H2, V_{SUP}, CANL/H, LIN, VSUP, VHSS and WAKE, per AEC Q100-002(1)		±8000	V
		Human body model (HBM) Classification Level 3A, all other pins, per AEC Q100-002(1)		±4000	
		Charged device model (CDM) Classification Level C5, per AEC Q100-011	Corner pins	±750	
			Other pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 IEC ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge according to IEC 62228-2 for LIN and IEC 62228-3 for CAN(1)	contact discharge, LIN, CANH, CANL, VSUP(5), VHSS(5), WAKE, VEXCC, VCC2	±8000	V
$V_{(ESD)}$	Electrostatic discharge according to IEC 62228-2 for LIN	Indirect ESD, LIN	±15000	V
$V_{(ESD)}$	Electrostatic discharge according to SAE J2962-1 for LIN and J2962-2 for CAN(2)	contact discharge (LIN, CANH, CANL)	±8000	V
		air-gap discharge (CANH, CANL)	±15000	
		air-gap discharge (LIN)	±25000	
ISO7637-2 and IEC 62215-3 Transients, LIN, CANH/L, VSUP, VHSS and WAKE(3)		Pulse 1	-100	V
		Pulse 2	75	
		Pulse 3a	-150	
		Pulse 3b	100	
IS07637-3 Slow Transient Pulse CAN and LIN bus terminals to GND(4)		Direct coupling capacitor "slow transient pulse" with 100 nF coupling capacitor - powered	±30	V

(1) IEC 62228-2 and IEC 62228-3 ESD performed by a third party. Different system-level configurations may lead to different results. See compliance report for circuit configuration.
(2) SAE J2962-1 and SAE J2962-2 testing performed at 3rd party US3 approved EMC test facility.
(3) ISO 7637-2 according to IEC 62228-2 and IEC 62228-3 are system-level transient tests. Different system-level configurations can lead to different results. See compliance report for circuit configuration.
(4) ISO 7637-3 is a system-level transient test. Different system-level configurations may lead to different results.
(5) VSUP and VHSS are connected together on board and not tested separately

6.4 Recommended Operating Conditions

Over recommended operating range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VSUP	Supply voltage range (1) (2)	5.5		28	V
VSUP	Reduced operation supply voltage range (1) (2)	4.5		28	V
VHSS	High-side switches supply voltage	5		28	V
VCAN	CAN Transceiver supply voltage	4.75	5	5.25	V
V_{LIN}	LIN bus input voltage	0		28	V
$I_{OH(DO)}$	Digital output high level current	–2			mA
$I_{OL(DO)}$	Digital output low level current			2	mA
$I_{O(LIMP)}$	LIMP pin current when configured as LIMP			6	mA
$C_{(VSUP)}$	V_{SUP} supply capacitance	100			nF
$C_{(VEXCC)}$	VEXCC supply capacitance;	1			µF
ESR_C	VEXCC ESR capacitance requirements	1		150	mΩ
$C_{(VCC1/2)}$	VCC1 and VCC2 effective supply capacitance required for LDO stability; no load to full load	1			µF
ESR_{CO}	VCC1 and VCC2 output ESR capacitance requirements	0.001		1	Ω
TSDWR	Thermal shut down warning	145		165	°C
TSDWF	Thermal shut down warning release	135		155	°C
TSDWHYS	Thermal shut down warning hysteresis		10.0		°C
TSDR	Thermal shut down	165		200	°C
TSDF	Thermal shut down release	155		190	°C
TSDHYS	Thermal shut down hysteresis		10.0		°C
T_J	Operating junction temperature range	–40		150	°C

(1) When VCC1 is 3.3V, VCC1 works with a VSUP of 4.5V but other LDOs are in pass through mode and output voltage is not at regulated value. For all LDOs to be in regulation and CAN transceiver to be operational, VSUP needs to be at or above 5.5V.

(2) When VSUP is above 4.5V, the LIN transceiver functions but does not always meet the electrical or timing parameters.

6.5 Thermal Information

THERMAL METRIC[1]		TCAN285x-Q1 RHB (QFN) 32-PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	21.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	11.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.6 Supply Characteristics

Over recommended operating range (unless otherwise noted). Typical values are specified at VSUP = 14V and T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Battery Supply Input (VSUP)						
$ISUP_{normdom}$	Battery supply current device in normal mode with CAN FD and LIN bus dominant	Normal mode; CAN and LIN transceivers on and dominant; no external pull-up on LIN node, VEXCC, VCC1 = On with no load, VCC2 ON and connected to VCAN; VSUP = 14V		40	60	mA
$ISUP_{normrex}$	Battery supply current device in normal mode with CAN FD and LIN bus recessive	Normal mode; CAN and LIN transceivers on and recessive; no external pull-up on LIN node; VEXCC, VCC1 On with no load, VCC2 ON and connected to VCAN ; VSUP = 14V		5	7.5	mA
$ISUP_{stbyswo}$	Battery supply current, standby mode with selective wake off	Standby mode; selective wake off; VEXCC, VCC1 and VCC2 = On with no load; 6.5V ≤ VSUP ≤ 19V; CAN and LIN transceivers are wake capable and buses - recessive; all HSS and WAKE pins are off, WD off; Long Window has expired		80	150	µA
$ISUP_{stbyswolp}$	Battery supply current, low power standby mode with selective wake off	Standby mode; selective wake off; VEXCC, VCC2 = off and VCC1 = On with no load; VSUP=14V; CAN and LIN transceivers are wake capable and buses - recessive; All HSS and WAKE pins are off, Watchdog is off; T_j ≤ 85°C, Long Window has expired		50	70	µA
$ISUP_{slpswo}$	Battery supply current, sleep mode with selective wake off	Sleep mode; selective wake off; VEXCC, VCC1 and VCC2 = off; 6.5V ≤ VSUP ≤ 19V; transceivers are wake capable; All HSSx and WAKEx are off; T_j ≤ 85°C		35	60	µA
$ISUP_{slpswodr}$	Battery supply current, sleep mode with selective wake off and HSS4 direct drive	Sleep mode; selective wake off; VEXCC and VCC2 = off; VCC1 = On with no load; 6.5V ≤ VSUP ≤ 18V; CAN and LIN transceivers are wake capable; One HSSx turned on for 120µs every 50ms by WAKE3/DIR pin; All other HSSx and WAKEx are off; T_J ≤ 25°C[2]		50	60	µA

6.6 Supply Characteristics (continued)

Over recommended operating range (unless otherwise noted). Typical values are specified at VSUP = 14V and T_J = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$ISUP_{slpswodr}$	Battery supply current, sleep mode with selective wake off and HSS4 direct drive	Sleep mode; selective wake off; VEXCC and VCC2 = off; VCC1 = On with no load; 6.5V ≤ VSUP ≤ 18V; CAN and LIN transceivers are wake capable; One HSSx turned on for 120µs every 50ms by WAKE3/DIR pin; All other HSSx and WAKEx are off; T_J ≤ 85°C(3)			60	75	µA
$ISUP_{slpswotrx}$	Battery supply current, sleep mode with selective wake off; LDO's and transceivers off	Sleep mode; selective wake off; VEXCC, VCC1 and VCC2 = off; 6.5V ≤ VSUP ≤ 19V; transceivers are off; All HSSx are off; one WAKE pin enabled and grounded or floating; T_J ≤ 85°C			18	42	µA
$VSUP_{(PU)R}$	Supply on detection (4)	VSUP rising; see Figure 7-18		3.1	3.4	3.7	V
$VSUP_{(PU)F}$	Supply off detection (4)	VSUP falling; see Figure 9-8 and Figure 9-9		2.7	3	3.3	V
$VSUP_{(PU)HYS}$	Supply off detection hysteresis (4)			50		550	mV
$UVSUP_{5R}$	Supply undervoltage recovery	VSUP rising; see Figure 7-18, Figure 9-8 and Figure 9-9		4.9		5.5	V
$UVSUP_{5F}$	Supply undervoltage detection	VSUP falling; see Figure 9-8 and Figure 9-9		4.5		5.1	V
$UVSUP_{5HYS}$	Supply undervoltage detection hysteresis			200		600	mV
$UVSUP_{33R}$	Supply undervoltage recovery	VSUP rising; see Figure 7-18, Figure 9-8 and Figure 9-9		3.7		4.4	V
$UVSUP_{33F}$	Supply undervoltage detection	VSUP falling; see Figure 9-8 and Figure 9-9		3.55		4.25	V
$UVSUP_{33HYS}$	Supply undervoltage detection hysteresis			50		300	mV
Incremental Current Consumption for Features							
$ISUP_{slpswoact}$	Battery supply current, sleep mode with selective wake on and WUP has taken place on CAN bus - bus active (4)	Additional current when selective wake is enabled and bus active; VEXCC, VCC1 and VCC2 = off; LIN in wake capable or off			480	550	µA
$ISUP_{HSSNOLOAD}$	Incremental battery supply current for each HSS. (3)	One HSS = On but no load, other HSS off, T_J ≤ 85°C			35	60	µA
$ISUP_{CANBIAS}$	Additional current consumption when CAN outputs are in automatic bias (before tSILENCE expires)	Sleep or Standby mode before $t_{SILENCE}$ expires	VSUP =14V; T_J ≤ 85°C		65	75	µA
$ISUP_{WD}$	Incremental battery supply current when watchdog is enabled for Window or Q&A	Standby mode; selective wake off; VEXCC, VCC2 = off and VCC1 = On with no load; VSUP 14V; CAN and LIN transceivers are wake capable and buses - recessive; All HSS and WAKE pins are off, Watchdog is enabled (Window, Q&A), T_J ≤ 85°C			45	55	µA
$ISUP_{WDTO}$	Incremental battery supply current when Timeout watchdog is enabled.	Standby mode; selective wake off; VEXCC, VCC2 = off and VCC1 = On with no load; VSUP 14V; CAN and LIN transceivers are wake capable and buses - recessive; All HSS and WAKE pins are off, Watchdog is enabled (Timeout), T_J ≤ 85°C			2	2.5	µA
$ISUP_{wake}$	Incremental battery supply current for each WAKEx pin when enabled	WAKEx pin enabled, VSUP=14V, T_J ≤ 85°C			1	2	µA

6.6 Supply Characteristics (continued)

Over recommended operating range (unless otherwise noted). Typical values are specified at VSUP = 14V and T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$ISUP_{CS-WK}$	Incremental battery current when cyclic sensing wake is enabled in Sleep mode	Sleep mode; cyclic sensing wake enabled, VSUP=14V, T_J ≤ 85°C, TIMERx with ON width = 1ms, period = 100ms		5	8	µA
$IEXCC_{slp}$	Incremental battery supply current draw when VEXCC is enabled	Sleep mode; VEXCC enabled in stand-alone configuration and no load; includes current into VSUP, VEXMON, VEXCTRL and VEXCC pins. T_J ≤ 85°C		40	60	µA
VHSS						
$IHSS_{NOLOAD}$	Additional current draw for each HSS turned ON (3)	For each HSS turned ON, No load on HSS output		100	140	µA
$UVHSS_R$	High-side switches supply undervoltage recovery	VHSS rising	4.6		4.9	V
$UVHSS_F$	High-side switches supply undervoltage detection; High-side switches turn-off if HSS_UV_SD_DIS = 0b	VHSS falling	4.4		4.7	V
$UVHSS_{HYS}$	High-side switches supply undervoltage detection hysteresis		100			mV
$OVHSS_R$	VHSS over-voltage rising threshold; High-side switches turn-off if HSS_OV_SD_DIS = 0b	VHSS rising	20		22	V
$OVHSS_F$	VHSS over-voltage falling threshold; VHSS must be below this threshold to enable the high-side switches again	VHSS falling	18.8		21.2	V
$OVHSS_{HYS}$	VHSS over-voltage threshold hysteresis		800		1200	mV
VCC1 Regulator						
$VCC1_5$	Regulated output	VSUP = 5.5V to 28V, ICC1 = 1 to 250mA	4.9	5	5.1	V
$VCC1_{33}$	Regulated output	VSUP = 5.5V to 28V, ICC1 = 1 to 250mA	3.234	3.3	3.366	V
$ICC1_{SINK}$	VCC1 current sink capability	VSUP = 14V and register 8'h0D[3] = 0b	–17	–11	–7	µA
		VSUP = 14V and register 8'h0D[3] = 1b	–155	–112	–75	µA
$ICC1_{LIM}$	VCC1 output current limit	VCC1 short to ground	300		750	mA
$UVCC1_{5RPR}$	VCC1 undervoltage recovery threshold pre-warning	VCC1 rising	4.65		4.9	V
$UVCC1_{5FPR}$	VCC1 undervoltage detection threshold pre-warning	VCC1 falling	4.55		4.8	V
$UVCC1_{5PRHYS}$	Undervoltage pre-warning 5V LDO hysteresis		70		130	mV
$UVCC1_{5R1}$	VCC1 undervoltage recovery threshold 1	VCC1 rising, Register 8'h0E[4:3] = 00b	4.60		4.85	V
$UVCC1_{5F1}$	VCC1 undervoltage detection threshold 1	VCC1 falling, Register 8'h0E[4:3] = 00b	4.50		4.75	V
$UVCC1_{5R2}$	VCC1 undervoltage recovery threshold 2	VCC1 rising, Register 8'h0E[4:3] = 01b	3.85		4.15	V
$UVCC1_{5F2}$	VCC1 undervoltage detection threshold 2	VCC1 falling, Register 8'h0E[4:3] = 01b	3.75		4.05	V
$UVCC1_{5R3}$	VCC1 undervoltage recovery threshold 3	VCC1 rising, Register 8'h0E[4:3] = 10b	3.25		3.55	V
$UVCC1_{5F3}$	VCC1 undervoltage detection threshold 3	VCC1 falling, Register 8'h0E[4:3] = 10b	3.15		3.45	V

6.6 Supply Characteristics (continued)

Over recommended operating range (unless otherwise noted). Typical values are specified at VSUP = 14V and T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$UVCC1_{5R4}$	VCC1 undervoltage recovery, threshold 4	VCC1 rising, Register 8'h0E[4:3] = 11b	4.6		4.85	V
$UVCC1_{5F4}$	VCC1 undervoltage detection, threshold 4	VCC1 falling, Register 8'h0E[4:3] = 11b	3.375		3.675	V
$UVCC1_{5HYS4}$	Undervoltage detection 5V LDO hysteresis, threshold 1-3	Register 8'h0E[4:3] = 11b		1200		mV
$UVCC1_{5HYS}$	Undervoltage detection 5V LDO hysteresis, threshold 1-3	Register 8'h0E[4:3] = 00b, 01b or 10b	50		150	mV
$UVCC1_{33RPR}$	VCC1 undervoltage recovery threshold pre-warning	VCC1 rising	3.1		3.28	V
$UVCC1_{33FPR}$	VCC1 undervoltage detection threshold pre-warning	VCC1 falling	3		3.2	V
$UVCC1_{33PRHYS}$	Undervoltage pre-warning 3.3V LDO hysteresis		60		120	mV
$UVCC1_{33R1}$	VCC1 undervoltage recovery threshold 1	VCC1 rising, Register 8'h0E[4:3] = 00b	3		3.2	V
$UVCC1_{33F1}$	VCC1 undervoltage detection threshold 1	VCC1 falling, Register 8'h0E[4:3] = 00b	2.95		3.15	V
$UVCC1_{33R2}$	VCC1 undervoltage recovery threshold 2	VCC1 rising, Register 8'h0E[4:3] = 01b	2.55		2.75	V
$UVCC1_{33F2}$	VCC1 undervoltage detection threshold 2	VCC1 falling, Register 8'h0E[4:3] = 01b	2.5		2.7	V
$UVCC1_{33R3}$	VCC1 undervoltage recovery threshold 3	VCC1 rising, Register 8'h0E[4:3] = 10b	2.25		2.45	V
$UVCC1_{33F3}$	VCC1 undervoltage detection threshold 3	VCC1 falling, Register 8'h0E[4:3] = 10b	2.2		2.4	V
$UVCC1_{33R4}$	VCC1 undervoltage recovery, threshold 4	VCC1 rising, Register 8'h0E[4:3] = 11b	3		3.2	V
$UVCC1_{33F4}$	VCC1 undervoltage detection, threshold 4	VCC1 falling, Register 8'h0E[4:3] = 11b	2.2		2.4	V
$UVCC1_{33HYS4}$	Undervoltage detection 3.3V LDO hysteresis, threshold 4	Register 8'h0E[4:3] = 11b		800		mV
$UVCC1_{33HYS}$	Undervoltage detection 3.3V LDO hysteresis, threshold 1-3	Register 8'h0E[4:3] = 00b, 01b or 10b	30		80	mV
$OVCC1_{5R1}$	Over voltage 5V VCC threshold to enter sleep mode or fail-safe mode	Ramp Up, Register 8'h0C[7] = 0b	5.25		5.5	V
$OVCC1_{5F1}$	Over voltage 5V VCC1 threshold	Ramp Down, Register 8'h0C[7] = 0b	5.15		5.4	V
$OVCC1_{5R2}$	Over voltage 5V VCC1 threshold to enter sleep mode or fail-safe mode	Ramp Up, Register 8'h0C[7] = 1b	5.47		5.73	V
$OVCC1_{5F2}$	Over voltage 5V VCC1 threshold	Ramp Down, Register 8'h0C[7] = 1b	5.37		5.63	V
$OVCC1_{5HYS}$	Over voltage 5V VCC threshold hysteresis		50		150	mV
$OVCC1_{33R1}$	Over voltage 3.3V VCC1 threshold to enter sleep mode or fail-safe mode	Ramp up, Register 8'h0C[7] = 0b	3.45		3.6	V
$OVCC1_{33F1}$	Over voltage 3.3V VCC1 threshold	Ramp down, Register 8'h0C[7] = 0b	3.4		3.55	V
$OVCC1_{33R2}$	Over voltage 3.3V VCC1 threshold	Ramp Up, Register 8'h0C[7] = 1b	3.6		3.8	V
$OVCC1_{33F2}$	Over voltage 3.3V VCC1 threshold to enter sleep mode or fail-safe mode	Ramp Down, Register 8'h0C[7] = 1b	3.5		3.7	V
$OVCC1_{33HYS1}$	Over voltage 3.3V VCC threshold hysteresis	OVCC1_SEL Register 8'h0C[7] = 0b	30	50	80	mV

6.6 Supply Characteristics (continued)

Over recommended operating range (unless otherwise noted). Typical values are specified at VSUP = 14V and T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$OVCC1_{33HYS2}$	Over voltage 3.3V VCC threshold hysteresis	OVCC1_SEL Register 8'h0C[7] = 1b	70	105	140	mV
$VCC1_{5SC}$	VCC1 short circuit threshold to enter sleep mode or fail-safe mode for 5V LDO	VSUP ≥ $VSUP_{(PU)}$	1.7		2.3	V
$VCC1_{33SC}$	VCC1 short circuit threshold to enter sleep mode or fail-safe mode for 3.3V LDO	VSUP ≥ $VSUP_{(PU)}$		1.22	1.26	V
$V_{5DROP1VCC1}$	Dropout voltage (VCC1=5V Configuration)	VSUP = 3.5V, ICC1 = 50mA			500	mV
$V_{5DROP2VCC1}$	Dropout voltage (VCC1=5V Configuration)	VSUP = 5V, ICC1 = 150mA			500	mV
$V_{33DROP1VCC1}$	Dropout voltage (VCC1=3.3V Configuration)	VSUP = 3.5V, ICC1 = 50mA			500	mV
VCC2 Regulator						
VCC2nom	Normal operation regulated output	VSUP = 14V, ICC2 = 5 to 200mA	4.9	5	5.1	V
VCC2red	Reduced operation regulated output	VSUP = 8V - 18V; ICC2 = 10µA - 5mA; Tj = 25°C - 125°C	4.95	5	5.05	V
$ICC2_{LIM}$	VCC2 output current limit	VCC2 = 2.5V	250		650	mA
$UVCC2_R$	Undervoltage recovery VCC2	VCC2 rising	4.6		4.9	V
$UVCC2_F$	Undervoltage detection VCC2	VCC2 falling	4.5		4.75	V
$UVCC2_{HYS}$	Undervoltage detection VCC2 hysteresis		70		175	mV
$OVCC2_R$	Over voltage VCC2 LDO threshold	Ramp Up	5.37		5.63	V
$OVCC2_F$	Over voltage VCC2 LDO threshold	Ramp Down	5.2		5.5	V
$OVCC2_{HYS}$	Over voltage VCC2 LDO threshold hysteresis		70		175	mV
$VCC2_{SC}$	VCC2 LDO short circuit threshold	VSUP ≥ $VSUP_{(PU)}$	1.7		2.3	V
$V_{5DROP1VCC2}$	Dropout voltage (5V LDO output, VCC2)	VSUP = 3.5V, ICC2 = 50mA			500	mV
$V_{5DROP2VCC2}$	Dropout voltage (5V LDO output VCC2)	VSUP = 5V, ICC2 = 30mA			500	mV
VEXCC Regulator						
$VEXCC_{18}$	1.8V PNP output voltage supported	5.5V ≤ VSUP ≤ 28V 10mA ≤ I_{VCCEXT} ≤ 350mA	1.764	1.8	1.836	V
$VEXCC_{25}$	2.5V PNP output voltage supported	5.5V ≤ VSUP ≤ 28V 10mA ≤ I_{VCCEXT} ≤ 350mA	2.45	2.5	2.55	V
$VEXCC_{33}$	3.3V PNP output voltage supported	5.5V ≤ VSUP ≤ 28V 10mA ≤ I_{VCCEXT} ≤ 350mA	3.234	3.3	3.366	V
$VEXCC_5$	5V PNP output voltages supported	5.5V ≤ VSUP ≤ 28V 10mA ≤ I_{VCCEXT} ≤ 350mA	4.9	5	5.1	V
$VEXCC_{ACC}$	PNP output voltages accuracy	5.5V ≤ VSUP ≤ 28V 10mA ≤ I_{VCCEXT} ≤ 350mA	–2		2	%
$UVEXCC_R$	VEXCC exiting undervoltage event	5.5 V ≤ VSUP ≤ 28V	0.87	0.9	0.93	V_{EXCC}
$UVEXCC_F$	VEXCC entering undervoltage event	5.5V ≤ VSUP ≤ 28V	0.81	0.85	0.89	V_{EXCC}
$UVEXCC_{HSY}$	VEXCC entering undervoltage hysteresis	5.5V ≤ VSUP ≤ 28V	30		350	mV
$OVEXCC_R$	VEXCC entering overvoltage event	5.5V ≤ VSUP ≤ 28V	1.12	1.15	1.18	V_{EXCC}
$OVEXCC_F$	VEXCC exiting overvoltage event	5.5V ≤ VSUP ≤ 28V	1.07	1.1	1.13	V_{EXCC}
$OVEXCC_{HYS}$	VEXCC exiting overvoltage hysteresis	5.5V ≤ VSUP ≤ 28V	45		300	mV

6.6 Supply Characteristics (continued)

Over recommended operating range (unless otherwise noted). Typical values are specified at VSUP = 14V and T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$VEXCC_{SC18}$	VEXCC short circuit detect for 1.8V and 2.5V	5.5V ≤ VSUP ≤ 28V		1.1	1.26	V
$VEXCC_{SC}$	VEXCC short circuit detect for 3.3V and 5V	5.5V ≤ VSUP ≤ 28V	1.7		2.3	V
IVEXCC	Input current on VEXCC	VEXCC = 5V, 3.3V, 2.5V and 1.8V		3	10	µA
VVEXCTRL	Voltage output on base pin of external PNP	5.5V ≤ VSUP ≤ 28V			28	V
IVEXCTRL	Drive current at the base pin of external PNP	VVEXCTRL = 13.5V	20	40	60	mA
$IVEXCTRL_{LKG}$	Current on base pin VEXCTRL leakage	VVEXCTRL = 13.5V; T_j = 25°C			5	µA
IVEXMON	VEXMON pin input current	VEXMON = VSUP	0	3	10	µA
$IVEXMON_{LKG}$	VEXMON pin input leakage current ext PNP disabled	VEXMON = VSUP; T_j = 25°C			5	µA
VSHUNTTH	Output current shunt voltage threshold (1)		0.15		0.44	V
$t_{RLINC-3P3V}$	Current increase regulation reaction time	VEXCC = 3.3V to 0V, Max IVEXCTRL = 20mA, See Figure 8-8			20	µs
$t_{RLDEC-3P3V}$	Current decrease regulation reaction time	VEXCC = 0V to 3.3V, Max IVEXCTRL = 20mA, See Figure 8-8			5	µs
$t_{RLINC-5V}$	Current increase regulation reaction time	VEXCC = 5V to 0V; Max IVEXCTRL = 20mA, See Figure 8-8			20	µs
$t_{RLDEC-5V}$	Current decrease regulation reaction time	VEXCC = 0V to 5V; Max IVEXCTRL = 20mA, See Figure 8-8			5	µs
$Ratio_{ICC3/ICC1}$	Load sharing ratio ICC3:ICC1	6.0V ≤ V_{SUP} ≤ 28V; SBC Normal Mode; LS ratio for a 900mΩ shunt resistor and total load current of 300mA	1.4	2	2.6	
$Ratio_{ICC3/ICC1}$	Load sharing ratio ICC3:ICC1	6.0V ≤ V_{SUP} ≤ 28V; SBC Normal Mode; LS ratio for a 4.3Ω shunt resistor and total load current of 300mA	0.7	1	1.3	
VCAN Supply Input						
IVCAN	Supply current	Normal mode: Recessive, V_{TXD} = VCC1 , VEXCC, VCC1 and VCC2 = On with no load		3	5	mA
		Normal mode: Dominant, V_{TXD} = 0V, R_L = 60Ω and C_L = open, typical bus load, VEXCC, VCC1 and VCC2 = On with no load			60	mA
		Normal mode: Dominant, V_{TXD} = 0V, R_L = 50Ω and C_L = open, high bus load, VEXCC, VCC1 and VCC2 = On with no load			65	mA
		Normal mode: Dominant with bus fault, V_{TXD} = 0V, CANH = - 25V, R_L and C_L = open, VEXCC, VCC1 and VCC2 = On with no load			100	mA
$UVCAN_R$	Supply undervoltage recovery	VCAN rising	4.6		4.85	V
$UVCAN_F$	Supply undervoltage detection	VCAN falling	4.5		4.75	V
$UVCAN_{HYS}$	VCAN Supply undervoltage detections hysteresis		50	100	150	mV

(1) Threshold at which the current limit starts to operate and is only active when VEXCC is configured for stand-alone configuration

(2) Additional current is consumed for each additional HSS turned on using direct drive
(3) Add $I_{HSSNOLOAD}$ and $ISUP_{HSS}$ to determine the total battery current draw.
(4) Specified by design

6.7 Electrical Characteristics

Over recommended operating range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CAN Driver						
$V_{CANH(D)}$	Bus output voltage (dominant) CANH	See Figure 7-4, V_{CTXD} = 0V, R_L =45Ω to 65Ω, C_L = open, R_{CM} = open	3.0		4.26	V
$V_{CANL(D)}$	Bus output voltage (dominant) CANL		0.75		2.01	V
$V_{CANH(R)}$ $V_{CANL(R)}$	Bus output voltage (recessive)	See Figure 7-1 and Figure 7-4 V_{CTXD} = VCC1, R_L = open (no load), R_{CM} = open	2	2.5	3	V
$V_{CANH(R)}$ $V_{CANL(R)}$	Terminated bus output voltage (recessive)	V_{CTXD} = VCC1, 45Ω ≤ R_L ≤ 65Ω, Split termination capacitance 4.7nF	2.256		2.756	V
$V_{(DIFF)}$	Maximum differential voltage rating	$V_{(DIFF)}$ = V_{CANH} – V_{CANL}	–42		42	V
$V_{DIFF(D)}$	Differential output voltage(dominant) on normal bus load	See Figure 7-1 and Figure 7-4 , V_{CTXD} = 0V, 45Ω ≤ R_L ≤ 65Ω, C_L = open, R_{CM} = open	1.5		3	V
$V_{DIFF(D)}$	Differential output voltage(dominant) over extended differential load range	See Figure 7-1 and Figure 7-4 V_{CTXD} = 0V, 45Ω ≤ R_L ≤ 70Ω, C_L = open, R_{CM} = open	1.5		3.3	V
$V_{DIFF(D)}$	Differential output voltage(dominant) on effective resistance during arbitration	See Figure 7-1 and Figure 7-4 V_{CTXD} = 0V, R_L = 2.24kΩ, C_L = open, R_{CM} = open	1.5		5	V
$V_{DIFF(R)}$	Differential output voltage(recessive)	See Figure 7-1 and Figure 7-4 , V_{CTXD} = VCC1, R_L = 45Ω ≤ R_L ≤ 65Ω, C_L = open, R_{CM} = open	–50		50	mV
		See Figure 7-1 and Figure 7-4 V_{CTXD} = VCC1, R_L = open (no load), C_L = open, R_{CM} = open	–50		50	mV
$V_{CANH(INACT)}$	Bus output voltage on CANH with bus biasing inactive	See Figure 7-1 and Figure 7-4 , V_{CTXD} = VCC1, R_L = open, C_L = open, R_{CM} = open	–0.1		0.1	V
$V_{CANL(INACT)}$	Bus output voltage on CANL with bus biasing inactive		–0.1		0.1	V
$V_{DIFF(INACT)}$	Bus output voltage on CANH - CANL (recessive) with bus biasing inactive		–0.2		0.2	V
V_{SYM}	Output symmetry (dominant or recessive) ($V_{O(CANH)}$ + $V_{O(CANL)}$)/V_{REC} , where V_{REC} is the sum of $V_{CANH(R)}$ and $V_{CANL(R)}$, the recessive voltage levels of CANH and CANL (9)	See Figure 7-1 and Figure 7-4 , 45 Ω ≤ R_L ≤ 65Ω, C_L = open, R_{CM} = open, C_1 = 4.7nF, CTXD = 250kHz, 1MHz, 2.5MHz	0.95		1.05	V/V
V_{SYM_DC}	Output symmetry (dominant or recessive) (V_{CC} – $V_{O(CANH)}$) – $V_{O(CANL)}$)	See Figure 7-1 and Figure 7-4 , R_L = 60Ω, C_L = open, R_{CM} = open, C_1 = 4.7nF	–400		400	mV
$I_{CANH(OS)}$	Short-circuit steady-state output current, dominant See Figure 7-1 and Figure 7-8	–3.0V ≤ V_{CANH} ≤ +18.0V, CANL = open, V_{CTXD} = 0V	–100			mA
$I_{CANL(OS)}$		–3.0V ≤ V_{CANL} ≤ +18.0V, CANH = open, V_{CTXD} = 0V			100	mA
I_{OS_REC}	Short-circuit steady-state output current, recessive See Figure 7-1 and Figure 7-8	–42V ≤ V_{BUS} ≤ +42V, V_{BUS} = CANH = CANL	–5		5	mA
$R_{SE\_SIC\_ACT\_REC}$	Single ended SIC impedance	2V ≤ $V_{CANH/L}$ ≤ VCAN - 2V See Figure 7-22	37.5		66.5	Ω
$R_{DIFF\_SIC\_ACT\_REC}$	Differential SIC impedance (CANH to CANL)	2V ≤ $V_{CANH/L}$ ≤ VCAN - 2V See Figure 7-22	75		133	Ω
CAN Receiver						
$V_{DIFF\_RX(D)}$	Receiver dominant state differential input voltage range, bus biasing active	–12.0V ≤ V_{CANL} ≤ +12.0V –12.0V ≤ V_{CANH} ≤ +12.0V See Figure 7-5 and Table 8-3	0.9		8	V
$V_{DIFF\_RX(R)}$	Receiver recessive state differential input voltage range, bus biasing active		–3		0.5	V

6.7 Electrical Characteristics (continued)

Over recommended operating range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{HYS}	Hysteresis voltage for input-threshold, normal and selective wake modes			135		mV
$V_{DIFF\_RX(D\_INACT)}$	Receiver dominant state differential input voltage range, bus biasing inactive	–12.0V ≤ V_{CANL} ≤ +12.0V –12.0V ≤ V_{CANH} ≤ +12.0V See Figure 7-5 and Table 8-3	1.15		8	V
$V_{DIFF\_RX(R\_INACT)}$	Receiver recessive state differential input voltage range, bus biasing inactive		–3		0.4	V
V_{CM_NORM}	Common mode range: normal		–12		12	V
V_{CM_STBY}	Common mode range: standby mode		–12		12	V
$I_{LKG(OFF)}$	Power-off (unpowered) bus input leakage current	CANH = CANL = 5V, VCAN = VSUP pulled to GND using 0Ω and 47kΩ resistor			5	µA
C_I	Input capacitance to ground (CANH or CANL)	(9)			20	pF
C_{ID}	Differential input capacitance	(9)			10	pF
$R_{DIFF\_PAS\_REC}$	Differential input resistance during passive recessive state	V_{CTXD} = VCC1, normal mode: –2.0V ≤ V_{CANH} ≤ +7.0V; –2.0V ≤ V_{CANL} ≤ +7.0V	12		100	kΩ
R_{SE_CANH} R_{SE_CANL}	Single ended Input resistance during passive recessive state	–2.0V ≤ V_{CANH} ≤ +7.0V –2.0V ≤ V_{CANL} ≤ +7.0V	6		50	kΩ
m_R	Input resistance matching: [1 – ($R_{IN(CANH)}$ / $R_{IN(CANL)}$)] × 100%	V_{CANH} = V_{CANL} = 5.0V	–1		1	%
LIN						
V_{OH}	HIGH level output voltage(1)	LIN recessive, LTXD = high, I_O = 0mA, VSUP = 5.5V to 28V	0.85			VSUP
V_{OL}	LOW level output voltage(1)	LIN dominant, LTXD = low, VSUP = 5.5V to 28V			0.2	VSUP
V_{IH}	HIGH level input voltage(1)	LIN recessive, LTXD = high, I_O = 0mA, VSUP = 5.5V to 28V	0.47		0.6	VSUP
V_{IL}	LOW level input voltage(1)	LIN dominant, LTXD = low, VSUP = 5.5V to 28V	0.4		0.53	VSUP
$V_{SUP\_NON\_OP}$	V_{SUP} where impact of recessive LIN bus < 5% (ISO/DIS 17987 Param 11)	LTXD & LRXD open, V_{LIN} = 5.5V to 45 V, VCC = no load	–0.3		40	V
I_{BUS_LIM}	Limiting current (ISO/DIS 17987-4 Param 12)	LTXD = 0V, V_{LIN} = 18V, VSUP = 18V	40	90	200	mA
$I_{BUS\_PAS\_dom}$	Receiver leakage current, dominant (ISO/DIS 17987 Param 13)	V_{LIN} = 0V, VSUP = 12V Driver off/ recessive;	–1			mA
$I_{BUS\_PAS\_rec1}$	Receiver leakage current, recessive (ISO/DIS 17987 Param 14)	V_{LIN} ≥ VSUP, 5.5V ≤ VSUP ≤ 28V Driver off;			20	µA
$I_{BUS\_PAS\_rec2}$	Receiver leakage current, recessive (ISO/DIS 17987 Param 14)	V_{LIN} = VSUP, Driver off;	–5		5	µA
$I_{BUS\_NO\_GND}$	Leakage current, loss of ground (ISO/DIS 17987 Param 15)	GND = VSUP, VSUP = 12V, 0V ≤ V_{LIN} ≤ 28V;	–1		1	mA
$I_{BUSrec\_NO\_GND}$	Leakage current, loss of ground LIN bus is in recessive state	GND = VSUP, VSUP = 12V = V_{LIN} V;	–100		100	µA
$I_{BUS\_NO\_BAT}$	Leakage current, loss of supply (ISO/DIS 17987 Param 16)	0V ≤ V_{LIN} ≤ 28V, VSUP = GND;			10	µA
V_{BUSdom}	Low level input voltage (ISO/DIS 17987 Param 17)	LIN dominant (including LIN dominant for wake up);			0.4	VSUP
V_{BUSrec}	High level input voltage (ISO/DIS 17987 Param 18)	LIN recessive;	0.6			VSUP

6.7 Electrical Characteristics (continued)

Over recommended operating range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BUS_CNT}	Receiver center threshold (ISO/DIS 17987 Param 19)	$V_{BUS\_CNT} = (V_{IL} + V_{IH})/2$;	0.475	0.5	0.525	VSUP
V_{HYS}	Hysteresis voltage (ISO/DIS 17987 Param 20) (2)	$V_{HYS} = (V_{IH} - V_{IL})$; $V_{HYS} = (V_{th\_rec} - V_{th\_dom})$(3)	0.07		0.175	VSUP
V_{SERIAL_DIODE}	Serial diode LIN terminal pullup path (ISO/DIS 17987 Param 21)	By design and characterization	0.4	0.7	1.0	V
R_{LIN}	Internal pullup resistor to V_{SUP} on LIN (ISO/DIS 17987 Param 26)	Normal and Standby modes	27.66	35	48	kΩ
I_{RSLEEP}	Pull-up current source to V_{SUP}	Sleep mode, VSUP = 14V, LIN = GND	–13	–10	–7	µA
$C_{LIN,PIN}$	Capacitance of the LIN pin	By design and characterization			25	pF
LIMP Output (Open-drain)						
V_{OL}	Open-drain output voltage (active low)	External Pull-up; 4.5V < V < 28V, I_{LIMP} = – 6mA		0.5	1	V
$I_{LKG(LIMP)}$	Output current (inactive)	V_{LIMP} = 0V to 28V	–2		2	µA
HSS1, HSS2, HSS3, HSS4 (High voltage output)						
R_{dson}	HSS output drain-to-source on resistance	I_O = – 60mA		7	12	Ω
R_{dson}	HSS output drain-to-source on resistance	I_O = – 60mA, VHSS = 14V, TA = 25°C			7	Ω
$I_{OC(HSS)}$	HSS overcurrent detection limit	VHSS = 14V	150	200	300	mA
$I_{OL(HSS)}$	HSS open load current detection threshold when on and current is falling	VHSS = 14V	0.4		3.0	mA
$I_{OLHYS(HSS)}$	HSS open load current hysteresis	VHSS = 14V	0.05	0.45	1	mA
I_{lkg}	Leakage current	HSS = 0V, Sleep Mode	–1		1	µA
t_R	Output rise time (HSS)	6V ≤ VHSS ≤ 18V, R_L = 220 Ω, 20%/80%	0.45		2.5	V/µs
t_F	Output fall time (HSS)	6V ≤ VHSS ≤ 18V, R_L = 220 Ω, 80%/20%	0.45		2.5	V/µs
t_{HSS_on}	Switching on delay (HSS) from SPI command to on	VHSS = 14V, I_{LOAD} = 60mA, V_{OUT} = 80% of VHSS	30		90	µs
t_{HSS_off}	Switching off delay (HSS) from SPI command to off	VHSS = 14V, I_{LOAD} = 60mA, V_{OUT} = 20% of VHSS	30		90	µs
$t_{R\_DD\_SR0}$	Output rise time for HSS in direct drive mode with slow slew rate option	HSS_CNTLx=1000b, VHSS = 13.5V, R_L = 2.2kΩ, HSSx going from 20% to 80% of VHSS	1.05	1.3	1.6	V/µs
$t_{F\_DD\_SR0}$	Output fall time for HSS in direct drive mode with slow slew rate option	HSS_CNTLx=1000b, VHSS = 13.5V, R_L = 2.2kΩ, HSSx going from 80% to 20% of VHSS	0.95	1.15	1.4	V/µs
$t_{R\_DD\_SR1}$	Output rise time (HSS) for HSS in direct drive mode with fast slew rate option	HSS_CNTLx=1001b, VHSS = 13.5V, R_L = 2.2kΩ, HSSx going from 20% to 80% of VHSS	2.0	2.4	2.85	V/µs
$t_{F\_DD\_SR1}$	Output fall time for HSS in direct drive mode with fast slew rate option	HSS_CNTLx=1001b, VHSS = 13.5V, R_L = 2.2kΩ, HSSx going from 80% to 20% of VHSS	2.0	2.4	2.85	V/µs
$t_{HSSDD\_EN\_SR0}$	Enable time from edge change on WAKE3/DIR when configured for direct drive slow slew rate option	HSS_CNTLx=1000b, VHSS = 13.5V, R_L = 2.2kΩ, HSSx = 80% of VHSS	25	35	42	µs
$t_{HSSDD\_DIS\_SR0}$	Disable time from edge change on WAKE3/DIR when configured for direct drive with slow slew rate option	HSS_CNTLx=1000b, VHSS = 13.5V, R_L = 2.2kΩ, HSSx = 20% of VHSS	35	55	65	µs

6.7 Electrical Characteristics (continued)

Over recommended operating range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{HSSDD\_EN\_SR1}$	Enable time from edge change on WAKE3/DIR when configured for direct drive with fast slew rate option	HSS_CNTLx=1001b, VHSS = 13.5V, R_L = 2.2kΩ, HSSx = 80% of VHSS	20	30	35	µs
$t_{HSSDD\_DIS\_SR1}$	Disable time from edge change on WAKE3/DIR when configured for direct drive with fast slew rate option	HSS_CNTLx=1001b, VHSS = 13.5V, R_L = 2.2kΩ, HSSx = 20% of VHSS	20	33	38	µs
t_{OCFLTR}	HSS overcurrent filter time for overcurrent fault indication	VHSS = 14V		16		µs
t_{OLFLTR}	HSS open load filter time for open load fault indication	VHSS = 14V		64		µs
t_{OCOFF}	HSS overcurrent shut off time. HSS will be turned off if overcurrent persists for this duration	$I_{O(HSS)} > I_{OC(HSS)}$	250		350	µs
WAKE1, WAKE2, WAKE3 Input Terminal (High voltage input)						
V_{IH}	High-level input voltage: Sleep, selective wake-up or standby mode, WAKE pin enabled (7)	Register setting 00b VCC1 based	0.7			VCC1
		Register setting 01b	2.5		3.5	V
		Register setting 10b	3.8		5	V
		Register setting 11b	5.6		7	V
V_{IL}	Low-level input voltage: Sleep, selective wake-up or standby mode, WAKE pin enabled (7)	Register setting 00b VCC1 based			0.3	VCC1
		Register setting 01b	1.5		2.8	V
		Register setting 10b	3.0		4.2	V
		Register setting 11b	5		6.3	V
I_{IL}	Low-level input current(8)	WAKE = 1V		1.2	2.2	µA
I_{LKG}	Leakage current when Vbat monitoring enabled	V_{WAKE1} = 4V - 28V		2	4	µA
R_{DSON}	On resistance of Vbat switch when Vbat monitoring enabled	V_{WAKE1} = 4V - 28V, switch current = 500µA		155	400	Ω
t_{WAKE}	Wake up hold time from a wake edge on WAKE in standby or sleep mode for static sensing.	See Figure 8-32 and Figure 8-33			140	µs
$t_{WAKE\_INVALID}$	WAKE pin pulses shorter than this will be filtered out in standby or sleep mode for static sensing.	See Figure 8-32 and Figure 8-33	10			µs
SW Input Terminal						
V_{IH}	High-level input voltage: SW	VCC1 Present	0.7			VCC1
V_{IL}	Low-level input voltage: SW	VCC1 Present			0.3	VCC1
$V_{IHSWINT}$	SW pin high-level input voltage when VCC1 is missing for sleep or fail-safe mode	Register 8'h0E[1] = 1 and/or 8'h0E[2] = 1 and VCC1missing in sleep or fail-safe mode	1.2			V
$V_{ILSWINT}$	SW low-level input voltage when VCC1 is missing for sleep or fail-safe mode	Register 8'h0E[1] = 1 and/or 8'h0E[2] = 1 and VCC1missing in sleep or fail-safe mode			0.4	V
$I_{IHSWINT-PD}$	High-level input leakage current for SW pin (active-high) when VCC1 is off	VCC1 off, internal pulldown enabled, Vin = 1.5V	18		32	µA
$I_{ILSWINT-PD}$	Low-level input leakage current for SW pin (active-high) when VCC1 is off	VCC1 off, internal pulldown enabled, Vin = 0V	–1		1	µA
$I_{IHSWINT-PU}$	High-level input leakage current for SW pin (active-low) when VCC1 is off	VCC1 off, internal pullup enabled, Vin = 1.5V	–60		–20	µA
$I_{ILSWINT-PU}$	Low-level input leakage current for SW pin (active-low) when VCC1 is off	VCC1 off, internal pullup enabled Vin = 0V	–85		–35	µA

6.7 Electrical Characteristics (continued)

Over recommended operating range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level input leakage current (SW pullup)	Inputs = VCC1 ± 2%	–1		1	µA
I_{IL}	Low-level input leakage current (SW Pull-up)	Inputs = 0V, VCC1 ± 2%	–140		–2	µA
I_{IH}	High-level input leakage current (SW pulldown)	Inputs = VCC1 ± 2%	15		140	µA
I_{IL}	Low-level input leakage current (SW Pull-down)	Inputs = 0V, VCC1 ± 2%	–1		1	µA
Rpu	Pull-up resistor (SW pin)	The SW pin has pullup resistor configured (SW pin is configured active low)	40	60	80	kΩ
Rpd	Pull-down resistor (SW pin)	The SW pin has pulldown resistor configured (SW pin is configured active high)	40	60	80	kΩ
$I_{LKG(OFF)}$	Unpowered leakage current	Inputs = 5.5V, VCC1 = VSUP = 0V; T_J = -40 to 85 °C	–1	0	1	µA
SDI, SCK, nCS, CTXD, LTXD Input Terminals						
V_{IH}	High-level input voltage		0.7			VCC1
V_{IL}	Low-level input voltage				0.3	VCC1
I_{IH}	High-level input leakage current (Internal pullup)	Inputs = VCC1 ± 2%	–1		1	µA
I_{IH}	High-level input leakage current (Internal pulldown)	Inputs = VCC1 ± 2%	15		140	µA
I_{IL}	Low-level input leakage current (Internal Pull-up)	Inputs = 0V, VCC1 ± 2%	–140		–2	µA
I_{IL}	Low-level input leakage current (Internal Pull-down)	Inputs = 0V, VCC1 ± 2%	–1		1	µA
C_{IN}	Input Capacitance	at 20MHz	2		10	pF
$I_{LKG(OFF)}$	Unpowered leakage current	Inputs = 5.5V, VCC1 = VSUP = 0V; T_J -40 to 85°C	–1	0	1	µA
Rpd	Pull-down resistor (SDI, SCK, and SW pins)	These pins have a pulldown resistor if configured accordingly.	40	60	80	kΩ
Rpu	Pull-up resistor (SDI, SCK, nCS, SW, CTXD and LTXD pins)	The SDI, SCK, and SW pins have a pullup resistor if configured accordingly. nCS, CTXD, and LTXD always have a pullup.	40	60	80	kΩ
CRXD, LRXD, SDO, GFO, nINT Output Terminals						
V_{OH}	HIGH level output voltage	I_{OH} = -2mA	0.8			VCC1
V_{OL}	LOW level output voltage	I_{OL} = 2mA			0.2	VCC1
$I_{LKG(OFF)}$	Unpowered leakage current	VSUP = 0V; VCC1 = 0V; V_O = 0V to VCC1 output level of either 3.3V or 5V	–5		5	µA
nRST Terminal (input/output)						
V_{IH}	High level input switching threshold voltage	Based off of internal voltage	2.1			V
V_{IL}	Low level input switching threshold voltage	Based off of internal voltage			0.8	V
I_{OL}	Low-level output current, open drain	nRST = 0.4V	1.5			mA
I_{LKG}	Leakage current, high-level	nRST = VCC1	–5		5	µA
R_{PU}	Pull-up resistance (Output pulled up to VCC1)		10	30	50	kΩ
LIN Duty Cycle						

6.7 Electrical Characteristics (continued)

Over recommended operating range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
D1	Duty Cycle 1 (ISO/DIS 17987 Param 27 and J2602 Normal battery)(4) (5)	$TH_{REC(MAX)}$ = 0.744 × VSUP, $TH_{DOM(MAX)}$ = 0.581 × VSUP, VSUP = 7V to 18V, t_{BIT} = 50/52µs, D1 = $t_{BUS\_rec(min)}$/(2 × t_{BIT}), (See Figure 7-13, Figure 7-14)	0.396			
D2	Duty Cycle 2 (ISO/DIS 17987 Param 28 and J2602 Normal battery)(4) (5)	$TH_{REC(MIN)}$ = 0.422 × VSUP, $TH_{DOM(MIN)}$ = 0.284 × VSUP, VSUP = 7.6V to 18V, t_{BIT} = 50/52µs, D2 = $t_{BUS\_rec(MAX)}$/(2 × t_{BIT}) (See Figure 7-13, Figure 7-14)			0.581	
D3	Duty Cycle 3 (ISO/DIS 17987 Param 29 and J2602 Normal battery)(4) (5)	$TH_{REC(MAX)}$ = 0.778 × VSUP, $TH_{DOM(MAX)}$ = 0.616 × VSUP, VSUP = 7V to 18V, t_{BIT} = 96µs (10.4 kbps), D3 = $t_{BUS\_rec(min)}$/(2 × t_{BIT}), (See Figure 7-13, Figure 7-14)	0.417			
D4	Duty Cycle 4 (ISO/DIS 17987 Param 30 and J2602 Normal battery)(4) (5)	$TH_{REC(MIN)}$ = 0.389 × VSUP, $TH_{DOM(MIN)}$ = 0.251 × VSUP, VSUP = 7.6V to 18V, t_{BIT} = 96µs (10.4 kbps), D4 = $t_{BUS\_rec(MAX)}$/(2 × t_{BIT}) (See Figure 7-13, Figure 7-14)			0.59	
$D1_{LB}$	Duty Cycle 1 J2602 Low battery (5) (6)	$TH_{REC(MAX)}$ = 0.665 × VSUP, $TH_{DOM(MAX)}$ = 0.499 × VSUP, VSUP = 5.5V to 7V, t_{BIT} = 50/52µs, $D1_{LB}$ = $t_{BUS\_rec(min)/(2 \times tBIT)}$ (See Figure 7-13, Figure 7-14)	0.396			
$D2_{LB}$	Duty Cycle 2 J2602 Low battery(5) (6)	$TH_{REC(MIN)}$ = 0.496 × VSUP, $TH_{DOM(MIN)}$ = 0.361 × VSUP, VSUP = 6.1V to 7.6V, t_{BIT} = 50/52µs, $D2_{LB}$ = $t_{BUS\_rec(MAX)}$/(2 × t_{BIT}) (See Figure 7-13, Figure 7-14)			0.581	
$D3_{LB}$	Duty Cycle 3 J2602 Low battery (5) (6)	$TH_{REC(MAX)}$ = 0.665 × VSUP, $TH_{DOM(MAX)}$ = 0.499 × VSUP, VSUP = 5.5V to 7V, t_{BIT} = 96µs, $D3_{LB}$ = $t_{BUS\_rec(min)/(2 \times tBIT)}$ (See Figure 7-13, Figure 7-14)	0.417			
$D4_{LB}$	Duty Cycle 4 J2602 Low battery (5) (6)	$TH_{REC(MIN)}$ = 0.496 × VSUP, $TH_{DOM(MIN)}$ = 0.361 × VSUP, VSUP = 6.1V to 7.6V, t_{BIT} = 96µs, $D4_{LB}$ = $t_{BUS\_rec(MAX)}$/(2 × t_{BIT}) (See Figure 7-13, Figure 7-14)			0.59	
$T_{r\text{-}d\ max}$	$t_{REC(MAX)}$ - $t_{DOM(MIN)}$ (5)	$TH_{REC(MAX)}$ = 0.744 × VSUP, $TH_{DOM(MAX)}$ = 0.581 × VSUP, VSUP = 7V to 18V, t_{BIT} = 52µs (19.231 kbps), (See Figure 7-13, Figure 7-14)			10.8	µs
$T_{d\text{-}r\ max}$	$t_{DOM(MAX)}$ - $t_{REC(MIN)}$ (5)	$TH_{REC(MIN)}$ = 0.422 × VSUP, $TH_{DOM(MIN)}$ = 0.284 × VSUP, VSUP = 7.6V to 18V, t_{BIT} = 52µs (19.231 kbps), (See Figure 7-13, Figure 7-14)			8.4	µs
$T_{r\text{-}d\ max}$	$t_{REC(MAX)}$ - $t_{DOM(MIN)}$ (5)	$TH_{REC(MAX)}$ = 0.778 × VSUP, $TH_{DOM(MAX)}$ = 0.616 × VSUP, VSUP = 7V to 18V, t_{BIT} = 96µs (10.4 kbps), (See Figure 7-13, Figure 7-14)			15.9	µs
$T_{d\text{-}r\ max}$	$t_{DOM(MAX)}$ - $t_{REC(MIN)}$ (5)	$TH_{REC(MIN)}$ = 0.389 × VSUP, $TH_{DOM(MIN)}$ = 0.251 × VSUP, VSUP = 7.6V to 18V, t_{BIT} = 96µs (10.4 kbps), (See Figure 7-13, Figure 7-14)			17.28	µs

(1) SAE J2602 loads include: commander: 5.5nF; 4kΩ and for a responder: 5.5nF; 875Ω
(2) V_{HYS} is defined for both ISO 17987 and SAE J2602-1.

(3) V_{HYS} = (V_{th_rec} - V_{th_dom}) where V_{th_rec} and V_{th_dom} are the actual voltage values from V_{BUSrec} and V_{BUSdom}
(4) ISO 17987 loads include 1nF; 1kΩ/ 6.8nF; 660Ω/ 10nF; 500Ω; with t_{BIT} values of 50µs and 96µs
(5) SAE J2602 loads include: commander: 5.5nF; 4kΩ/ 889pF; 20kΩ and for a responder: 5.5nF; 875Ω/ 889pF; 900Ω; with t_{BIT} values of 52µs and 96µs
(6) ISO 17987 does not have a low battery specification. Using the ISO 17987 loads, these low battery duty cycle parameters are covered for t_{BIT} values of 50µs and 96µs
(7) Selected using Register 8'h12[1:0] for WAKE1; Register 8'h2B[5:4] for WAKE2; Register 8'h2B[1:0] for WAKE3
(8) Current based off of setting 11b for the WAKEx pin
(9) Specified by design and characterization

6.8 Timing Requirements

Over recommended operating range (unless otherwise noted)

Parameter		Test Condition	MIN	NOM	MAX	UNIT
Supply						
t_{PWRUP}	Time after VSUP exceeds UVSUP and VCC1> UVCC1 (5)	Device powers up enters restart			3.5	ms
t_{VCCSS}	Softstart time for VCC1, VCC2 and VEXCC (5)	Time required for VCC1, VCC2 and VEXCC to ramp from 0V to 90% of regulated value		0.75	1.25	ms
t_{UVFLTR}	Under-voltage detection filter time for VCC1, VCC2 and VEXCC (5)		25		50	µs
$t_{UVCC1PR}$	Under-voltage filter time for VCC1 pre-warning (5)		2		12	µs
$t_{UVCANFLTR}$	Under-voltage filter time for VCAN (5)		2		10	µs
t_{OVFLTR}	Over-voltage detect filter time on VCC1, VCC2 and VEXCC (5)		20		45	µs
$t_{OVFLTRVHSS}$	Over-voltage detect filter time on VHSS (5)		4		12	µs
t_{VSC}	Short to ground on VCC1, VCC2 and VEXCC detection filter time (5)		75	100	125	µs
t_{VSCLS}	Short to ground for VCC1 and VEXCC detection filter time when load sharing (5)		75	100	125	µs
t_{LDOON}	Time LDO is on to determine if a fault event is present after a previous uncleared detection (5)	See Figure 7-19			3.8	ms
t_{LDOOFF}	Time VCC1 LDO is off in fail-safe mode before accepting wake events and checking for fault conditions (5)		250	300	350	ms
Mode Change						
$t_{MODE\_STBY\_NOM\_CTRX}$	CAN transceiver state change time based upon SPI write from off or wake capable to on or listen state where CRXD mirror CAN bus (5)				70	µs
$t_{MODE\_STBY\_NOM\_LTRX}$	LIN transceiver state change time based upon SPI write from off or wake capable to on or fast state where LRXD mirror LIN bus (5)				70	µs
$t_{MODE\_NOM\_SLP}$	Time from SPI sleep command where CAN and/or LIN transceiver is off and RXD does not reflect the bus (5)	See Figure 7-20			200	µs
$t_{MODE\_NOM\_STBY}$	SPI write to go to standby from normal mode (5)	See Figure 7-21			70	µs
Device Timing						
t_{RSTN_act}	Reset delay after recovering from undervoltage (VCC1 ≥ UVCC1R to nRST release) (5)	See Figure 7-18, Figure 7-19, Figure 8-29 and Figure 9-8 as examples	1.5	2	2.5	ms
t_{NRSTIN}	Input pulse required on the nRST pin to recognize a device reset (5)	See Figure 8-44	75	100	125	µs
t_{RSTTO}	Restart timer. Timer starts when VCC1 < UVCC1F. The device enters fail-safe mode (if enabled) or Sleep mode (fail-safe mode disabled) when the timer expires before the UVCC1 recovery. (5)	Measured from nRST active to LIMP active	120	150	180	ms

6.8 Timing Requirements (continued)

Over recommended operating range (unless otherwise noted)

Parameter		Test Condition	MIN	NOM	MAX	UNIT
t_{NRST_TOG}	Reset pulse duration due to watchdog error (5)	Register 8'h29[5] = 0, see Figure 8-25	1.5	2	2.5	ms
		Register 8'h29[5] = 1, see Figure 8-25	10	15	20	ms
t_{nINT_TI}	nINT output pulse width (low) when nINT_TOG_EN is enabled. (5)	Register 8'h1B[0] = 1b	75	100	125	µs
t_{nINT_TP}	nINT output pulse width (high) when nINT_TOG_EN is enabled (5)	Register 8'h1B[0] = 1b	75	100	125	µs
$t_{WK\_TIMEOUT}$	Bus wake-up timeout value	See Figure 8-29	0.8		2	ms
t_{WK_FILTER}	Bus time to meet filtered bus requirements for wake up request	See Figure 8-29	0.5		0.95	µs
$t_{WK\_WIDTH\_MIN}$	Minimum WAKE Pin pulse width(2) (3) (4) (5) See Figure 8-34	Register 8'h11[3:2] = 00b	10			ms
		Register 8'h11[3:2] = 01b	20			ms
		Register 8'h11[3:2] = 10b	40			ms
		Register 8'h11[3:2] = 11b	80			ms
$t_{WK\_WIDTH\_INVALID}$	Maximum WAKE Pin pulse width that is considered invalid (2) (3) (4) (5) See Figure 8-34	Register 8'h11[3:2] = 00b			5	ms
		Register 8'h11[3:2] = 01b			10	ms
		Register 8'h11[3:2] = 10b			20	ms
		Register 8'h11[3:2] = 11b			40	ms
$t_{WK\_WIDTH\_MAX}$	Maximum WAKE Pin pulse window (2) (3) (4) (5) See Figure 8-34	Register 8'h11[1:0] = 00b	750		950	ms
		Register 8'h11[1:0] = 01b	1000		1250	ms
		Register 8'h11[1:0] = 10b	1500		1875	ms
		Register 8'h11[1:0] = 11b	2000		2500	ms
t_{WK_CYC}	Sampling window for cyclic sensing; Standby or Sleep mode. (5) see Figure 8-37	Register 8'h12[5] = 0b	10	25	35	µs
		Register 8'h12[5] = 1b	55	75	85	µs
$t_{SILENCE\_CAN}$	Timeout for bus inactivity Timer is reset and restarted, when bus changes from dominant to recessive or inversely .(5)		0.6		1.2	s
$t_{INACTIVE}$	SWE timer used for fail-safe and mode inactivity	Can be programmed to different values using register 8'h1C[6:3]	4	5	6	min
t_{Bias}	Time from the start of a dominant-recessive-dominant sequence	Each phase 6 µs until Vsym ≥ 0.1. See Figure 7-10			250	µs
t_{SW}	SW pin filter time for a state change to be recognized (5)		130			µs
t_{INITWD}	Initial long window for watchdog (5) see Figure 8-62	WD_CONFIG_1 register 8'h13[1:0] = 00b	127	150	173	ms
		WD_CONFIG_1 register 8'h13[1:0] = 01b	255	300	345	ms
		WD_CONFIG_1 register 8'h13[1:0] = 10b (default)	510	600	690	ms
		WD_CONFIG_1 register 8'h13[1:0] = 11b	850	1000	1150	ms
$f_{PWM-ACC}$	HSS1-4 PWM Frequency accuracy(5)	HSS set to PWM and PWM frequency set to 200Hz or 400Hz per PWMx_FREQ bit	–10		10	%

6.8 Timing Requirements (continued)

Over recommended operating range (unless otherwise noted)

Parameter		Test Condition	MIN	NOM	MAX	UNIT
t_{WD-ACC}	Timeout watchdog timing accuracy(5)	Timeout watchdog enabled. Typical values for watchdog timer selected per Table 8-15	–15	tWD	15	%
	Window and Q&A watchdog timing accuracy(5)	Window watchdog or Q&A watchdog enabled. Typical values for watchdog timer selected per Table 8-15	–10	tWD	10	%
$t_{TMR-ACC}$	Timer1, Timer2 period/on-time accuracy OR SWE timer accuracy(5)	Typical value of Timer1 or Timer2 configured per register 8'h25 (TIMER1_CONFIG) or 8'h26 (TIMER2_CONFIG); Typical value of SWE timer configured per 8'h25 (SWE_TIMER_SET)	–15		15	%
t_{CTXD_DTO}	CAN TXD dominant time out(1) (5)	R_L = 60Ω, C_L = open; See Figure 7-7	1		5	ms
t_{LTXD_DTO}	LIN TXD dominant time out(5)		20	45	80	ms
t_{TOGGLE}	RXD pin toggle timing when programmed after a WUP (5)	See Figure 8-29	5	10	15	µs
$F_{OSC-16M}$	16 MHz clock frequency		15.36	16	16.64	MHz
F_{OSC-1M}	1 MHz clock frequency		0.94	1.04	1.14	MHz
$F_{OSC-10k}$	10 kHz clock frequency		8.8	10.4	12	kHz

(1) The CTXD dominant time out (t_{CTXD_DTO}) disables the driver of the transceiver once the CTXD has been dominant longer than t_{CTXD_DTO}, which releases the CAN bus lines to recessive, preventing a local failure from locking the bus dominant. The driver can only transmit dominant again after CTXD has been returned HIGH (recessive). The dominant timeout feature protects the CAN bus from locking the bus dominant but limits the minimum data rate possible. The CAN protocol allows a maximum of eleven successive dominant bits (on CTXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the t_{CTXD_DTO} minimum, limits the minimum bit rate. The minimum bit rate can be calculated by: Minimum Bit Rate = 11/ t_{CTXD_DTO} = 11 bits / 1.2ms = 9.2kbps.

(2) This parameter is valid only when register 11h[7:6] = 11b
(3) This is the minimum pulse width for a WAKE pin input that device will detect as a good pulse. Value between the min $t_{WK\_WIDTH\_MIN}$ and max $t_{WK\_WIDTH\_INVALID}$ is indeterminate and is sometimes but is not always considered valid.
(4) This parameter is set based upon the programmed value for $t_{WK\_WIDTH\_INVALID}$ register 11h[3:2]
(5) Specified by design and characterization

6.9 Switching Characteristics

Over recommended operating range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Transmitter and Receiver Timing (CAN FD SIC)						
$t_{prop(TxD-busrec)}$	Propagation delay time, low-to-high TXD edge to driver recessive (dominant to recessive)	45Ω ≤ R_L ≤ 65Ω, C_L = 100pF, R_{CM} = open; See Figure 7-4		55	80	ns
$t_{prop(TxD-busdom)}$	Propagation delay time, high-to-low TXD edge to driver dominant (recessive to dominant)	45Ω ≤ R_L ≤ 65Ω, C_L = 100pF, R_{CM} = open; See Figure 7-4		55	80	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{pHR} - t_{pLD} \rvert$)	45Ω ≤ R_L ≤ 65Ω, C_L = 100pF, R_{CM} = open; See Figure 7-4		15	25	ns
t_R	Differential output signal rise time:	45Ω ≤ R_L ≤ 65Ω, C_L = 100pF, R_{CM} = open; See Figure 7-4		20	55	ns
t_F	Differential output signal fall time:	45Ω ≤ R_L ≤ 65Ω, C_L = 100pF, R_{CM} = open; See Figure 7-4		30	55	ns
$t_{prop(busrec-RXD)}$	Propagation delay time, bus recessive input to RXD high output (dominant to recessive)	45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF, R_{CM} = open; C_{CRXD} = 15pF; see Figure 7-5		65	110	ns
$t_{prop(busdom-RXD)}$	Propagation delay time, bus dominant input to RXD low output (recessive to dominant)	45Ω ≤ R_L ≤ 65Ω, C_L = 100pF, R_{CM} = open; C_{CRXD} = 15pF; see Figure 7-5		60	110	ns
t_{LOOP}	Loop Delay(1)	45Ω ≤ R_L ≤ 65Ω, C_L = 100pF, C_{CRXD} = 15pF, 4.5V ≤ VCAN ≤ 5.5 V, VCC1 ± 2%, see Figure 7-6			190	ns
CAN FD SIC Switching Characteristics						
$t_{PAS\_REC\_START}$	Signal improvement start time of passive recessive phase	Measured from rising TXD edge with < 5ns slope at 50% threshold, to the end of the signal improvement phase; See Figure 7-22 $R_{DIFF\_PAS\_REC}$ ≥ MIN $R_{DIFF\_ACT\_REC}$; $R_{SE\_CANH/L}$ ≥ MIN $R_{SE\_SIC\_REC}$			530	ns
$t_{ACT\_REC\_START}$	Start time of active signal improvement phase	Measured from rising TXD edge with < 5ns slope at 50% threshold. See Figure 7-22			120	ns
$t_{ACT\_REC\_END}$	End time of active signal improvement phase		355			ns
$t_{\Delta Bit(Bus)}$	Transmitted recessive bit width variation	Typical conditions: 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF, C_{CRXD} = 15pF; $t_{\Delta Bit(Bus)}$ = $t_{Bit(Bus)}$ -$t_{Bit(TXD)}$ See Figure 7-6	-10		10	ns
$t_{\Delta Bit(RXD)}$	Received recessive bit width variation at 5 Mbps(3)	Typical conditions: 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF, C_{CRXD} = 15pF; $t_{\Delta Bit(RXD)}$ = $t_{Bit(RXD)}$ -$t_{Bit(TXD)}$ See Figure 7-6	-30		20	ns
$t_{\Delta REC}$	Receiver Timing symmetry variation(2)	Typical conditions: 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF, C_{CRXD} = 15pF, $t_{\Delta REC}$ = $t_{Bit(RXD)}$ -$t_{Bit(Bus)}$, See Figure 7-6	-20		15	ns
Switching Characteristics (LIN)						
t_{rx_pdr} t_{rx_pdf}	Receiver rising/falling propagation delay time (ISO/DIS 17987 Param 31)	R_{LRXD} = 2.4kΩ, C_{RXD} = 20pF (See Figure 7-14)			6	µs
t_{rs_sym}	Symmetry of receiver propagation delay time Receiver rising propagation delay time (ISO/DIS 17987 Param 32)	Rising edge with respect to falling edge, (t_{rx_sym} = t_{rx_pdf} – t_{rx_pdr}), R_{RXD} = 2.4kΩ, C_{LRXD} = 20pF (Figure 7-14)	–2		2	µs
t_{LINBUS}	LIN wakeup time (minimum dominant time on LIN bus for wakeup)	See Figure 8-31	25	100	150	µs

6.9 Switching Characteristics (continued)

Over recommended operating range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{CLEAR}	Time to clear false wakeup prevention logic if LIN bus had a bus stuck dominant fault (recessive time on LIN bus to clear bus stuck dominant fault)	See Figure 8-31	10		60	µs
Fast Mode (LIN)						
DR	Data Rate	5.5V ≤ VSUP ≤ 18V, R_{LIN} = 500Ω and $C_{LIN(bus)}$ = 600pF			200	kbps
t_{rx_pdr} t_{rx_pdf}	Receiver rising/falling propagation delay time (ISO/DIS 17987 Param 31)	R_{LRXD} = 2.4kΩ, C_{LRXD} = 20pF (See Figure 7-14)			5	µs
$t_{txr/f}$	LIN transmitter rise and fall time	5.5V ≤ VSUP ≤ 18V, R_{LIN} = 500Ω and $C_{LIN(bus)}$ = 600pF			1.5	µs
SPI Switching Characteristics						
f_{SCK}	SCK, SPI clock frequency (2)	Normal and standby modes, Sleep mode - if VCC1 is present, if register BYTE_CNT, 09h[3]=1b (two-byte mode)			2	MHz
f_{SCK}	SCK, SPI clock frequency (2)	Normal and standby modes, Sleep mode - if VCC1 is present, if register BYTE_CNT, 09h[3]=0b (single byte mode)			4	MHz
t_{SCK}	SCK, SPI clock period (2)	Normal and standby modes, Sleep mode - if VCC1 is present; See Figure 7-17 if register BYTE_CNT, 09h[3]=0b (single byte mode)	250			ns
t_{SCK}	SCK, SPI clock period (2)	Normal and standby modes, Sleep mode - if VCC1 is present; See Figure 7-17 if register BYTE_CNT, 09h[3]=1b (two-byte mode)	500			ns
t_{SCKR}	SCK rise time (2)	Normal and standby modes, Sleep mode - if VCC1 is present; See Figure 7-16	40			ns
t_{SCKF}	SCK fall time (2)	Normal and standby modes, Sleep mode - if VCC1 is present; See Figure 7-17	40			ns
t_{SCKH}	SCK, SPI clock high (2)	Normal and standby modes, Sleep mode - if VCC1 is present; See Figure 7-17 if register BYTE_CNT, 09h[3]=1b (two-byte mode)	250			ns
t_{SCKH}	SCK, SPI clock high (2)	Normal and standby modes, Sleep mode - if VCC1 is present; See Figure 7-17 if register BYTE_CNT, 09h[3]=0b (single byte mode)	125			ns
t_{SCKL}	SCK, SPI clock low (2)	Normal and standby modes, Sleep mode - if VCC1 is present; See Figure 7-17 if register BYTE_CNT, 09h[3]=1b (two-byte mode)	250			ns
t_{SCKL}	SCK, SPI clock low (2)	Normal and standby modes, Sleep mode - if VCC1 is present; See Figure 7-17 if register BYTE_CNT, 09h[3]=0b (single byte mode)	125			ns

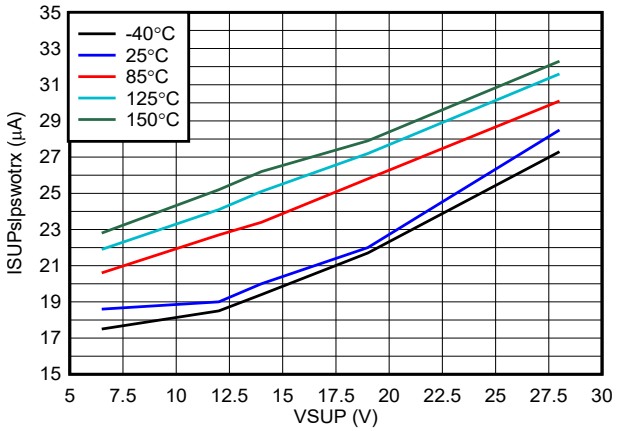
6.9 Switching Characteristics (continued)

Over recommended operating range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{nCSS}	nCS chip select setup time (2)	Normal and standby modes, Sleep mode - if VCC1 is present; See Figure 7-16			100	ns
t_{nCSH}	nCS chip select hold time (2)	Normal and standby modes, Sleep mode - if VCC1 is present; See Figure 7-16			100	ns
t_{nCSD}	nCS chip select disable time, 1-byte mode OR 2-byte mode with f_{SCK} ≤ 2 MHz (3)	Normal and standby modes, Sleep mode - if VCC1 is present; 1-byte mode OR 2-byte mode with f_{SCK} ≤ 2MHz See Figure 7-17	50			ns
t_{SISU}	Data in setup time (2)	Normal and standby modes, Sleep mode - if VCC1 is present; See Figure 7-17	50			ns
t_{SIH}	Data in hold time (2)	Normal and standby modes, Sleep mode - if VCC1 is present; See Figure 7-17	50			ns
t_{SOV}	Data out valid (2)	Normal and standby modes, Sleep mode - if VCC1 is present; See Figure 7-17			80	ns
t_{RSO}	SO rise time (2)	Normal and standby modes, Sleep mode - if VCC1 is present; See Figure 7-17			40	ns
t_{FSO}	SO fall time (2)	Normal and standby modes, Sleep mode - if VCC1 is present; See Figure 7-17			40	ns

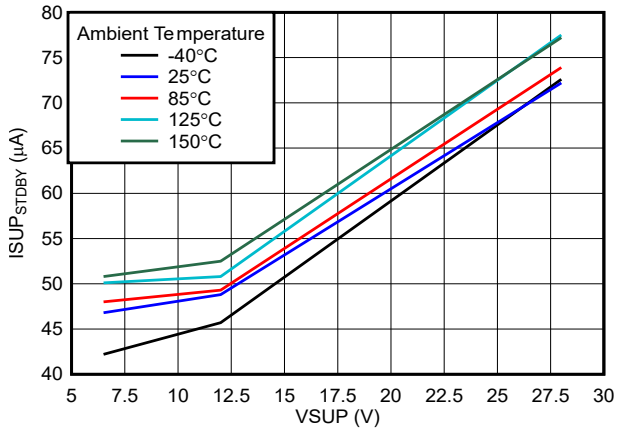
(1) Time span from signal edge on TXD input to next signal edge with same polarity on RXD output, the maximum of delay of both signal edges is to be considered.
(2) Specified by design
(3) For two byte SPI reads and writes, SPI_CONFIG register 8'h09[3] = 1b, the maximum SPI clock is 2MHz and what is shown here is for one byte reads and writes.

6.10 Typical Characteristics



A. SBC Mode: Sleep | CAN, LIN - Off | One wake pin enabled but floating | VCC1, VCC2, VEXCC = Off | HSSx = Off

Figure 6-1. Sleep Mode Current Consumption (ISUP) versus VSUP and Temperature



SBC Mode: Standby | CAN, LIN = Wake capable | All wake pins disabled | VCC2, VEXCC = Off | HSSx = Off | Watchdog = Off

Figure 6-2. Standby Mode Current Consumption (ISUP) versus VSUP and Temperature

7 Parameter Measurement Information

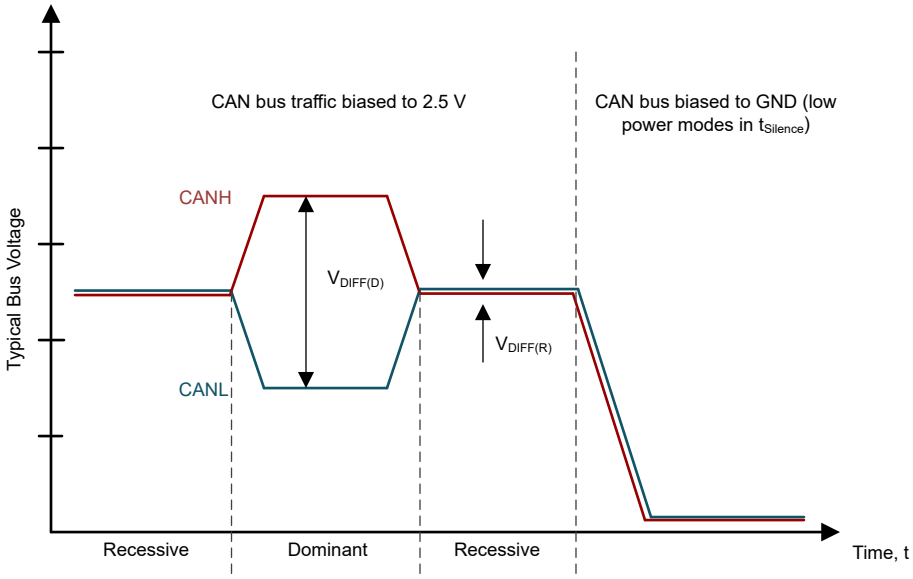
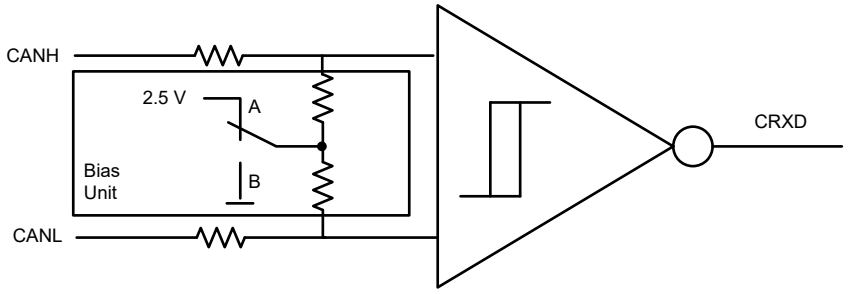


Figure 7-1. Bus States (Physical Bit Representation)



Note

A: Selective Wake, Normal, Listen Modes

B: Standby and Sleep Modes (Low Power)

Figure 7-2. Simplified Recessive Common Mode Bias Unit and Receiver

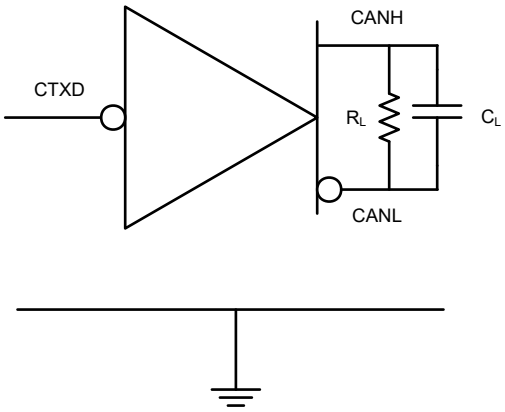


Figure 7-3. Supply Test Circuit

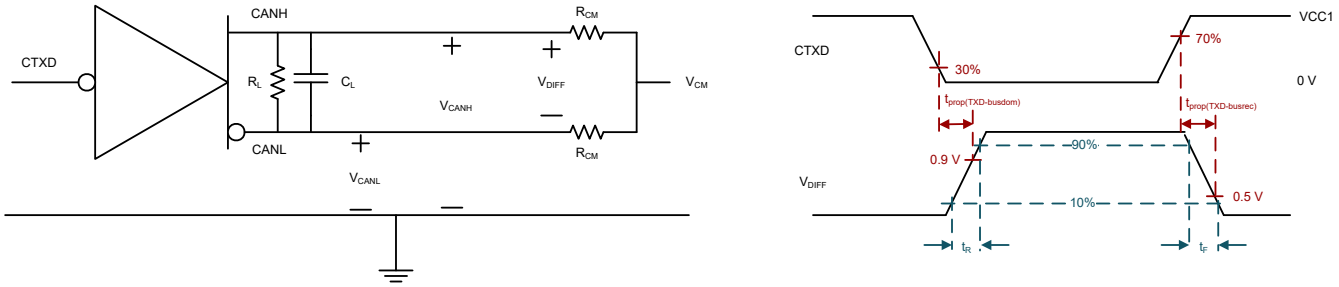


Figure 7-4. Driver Test Circuit and Measurement

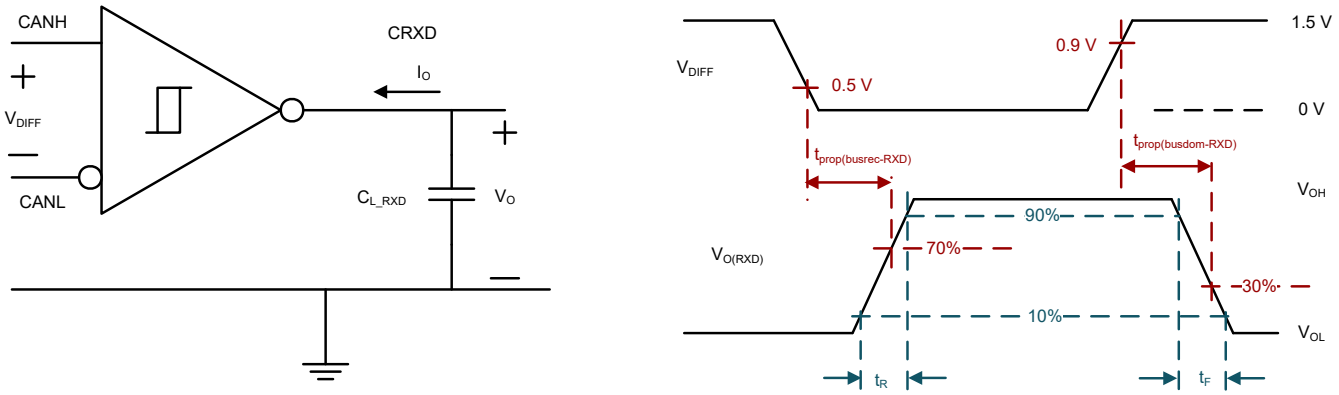


Figure 7-5. Receiver Test Circuit and Measurement

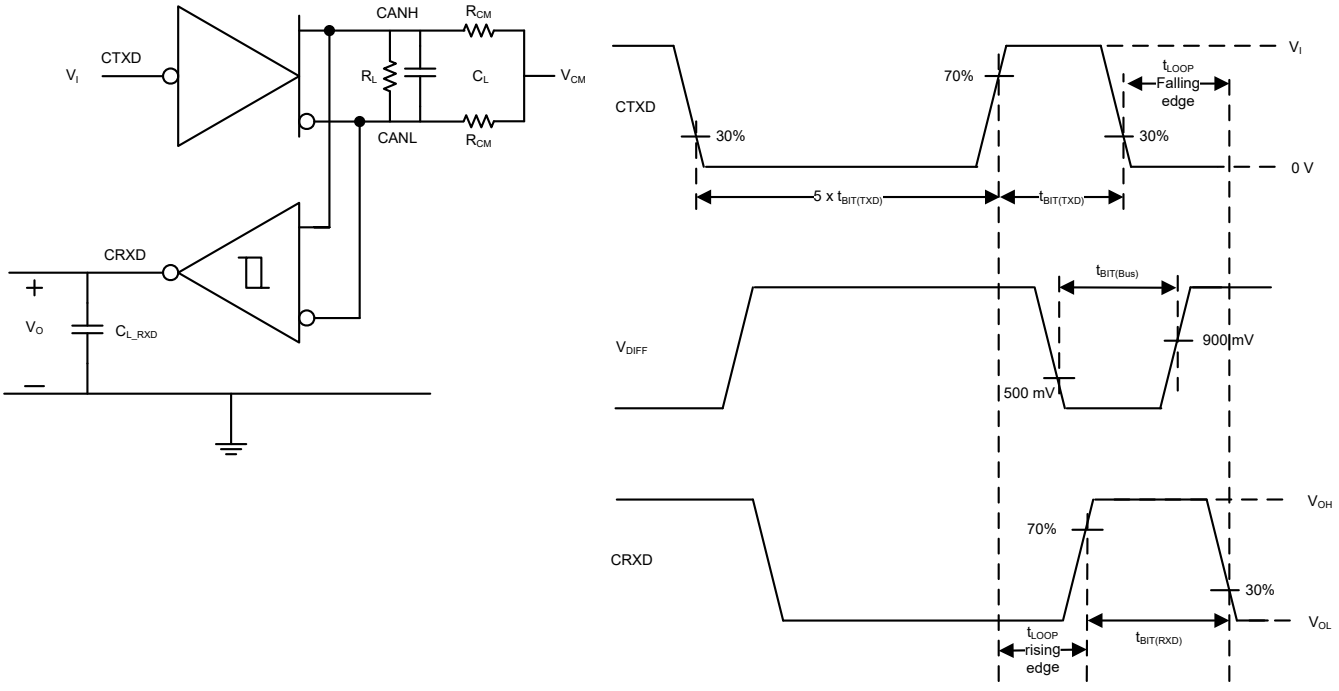


Figure 7-6. Transmitter and Receiver Timing Behavior Test Circuit and Measurement

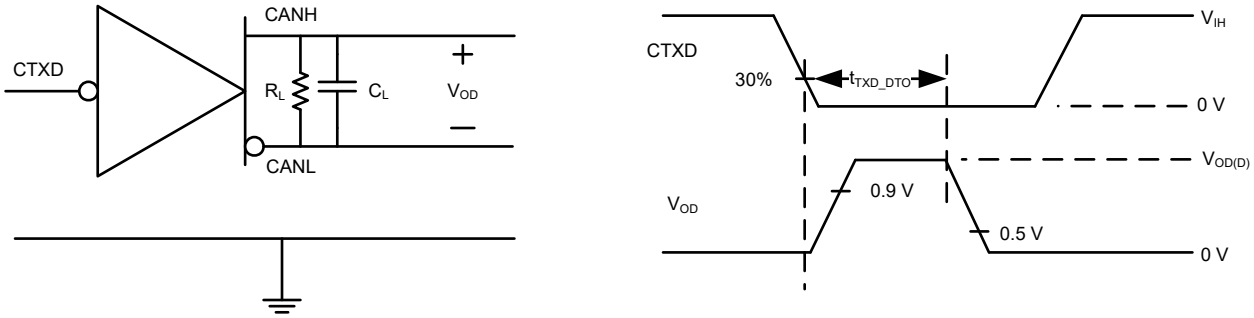


Figure 7-7. TXD Dominant Time Out Test Circuit and Measurement

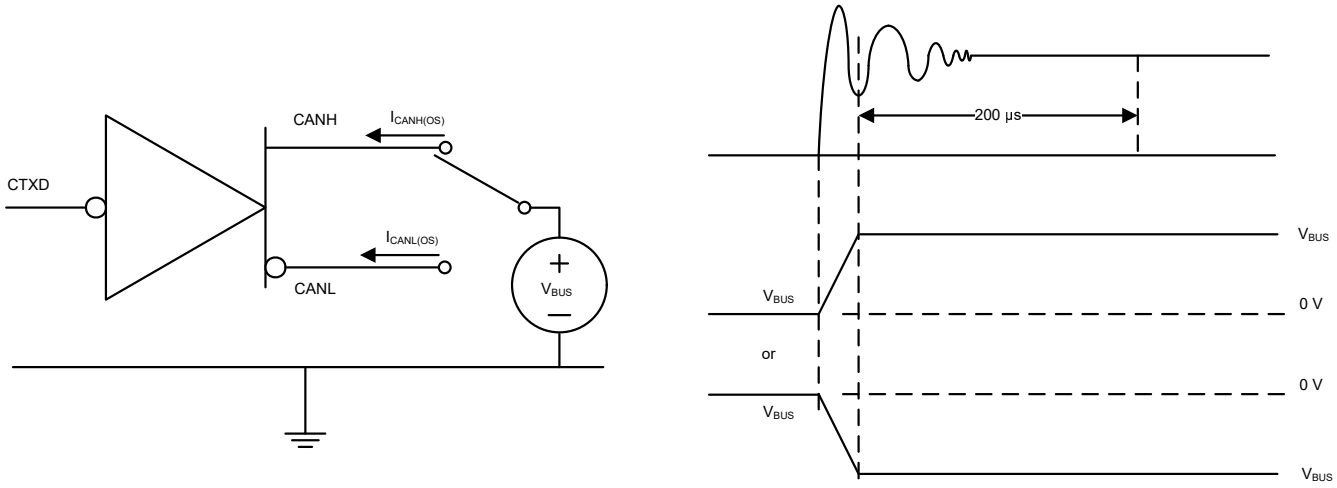


Figure 7-8. Driver Short-Circuit Current Test and Measurement

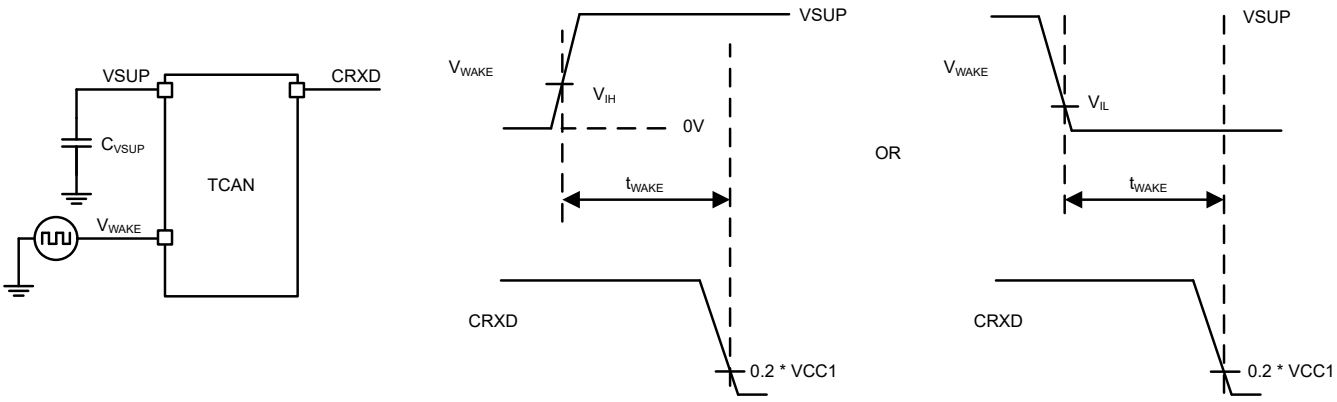


Figure 7-9. t_{WAKE} While Monitoring RXD Output

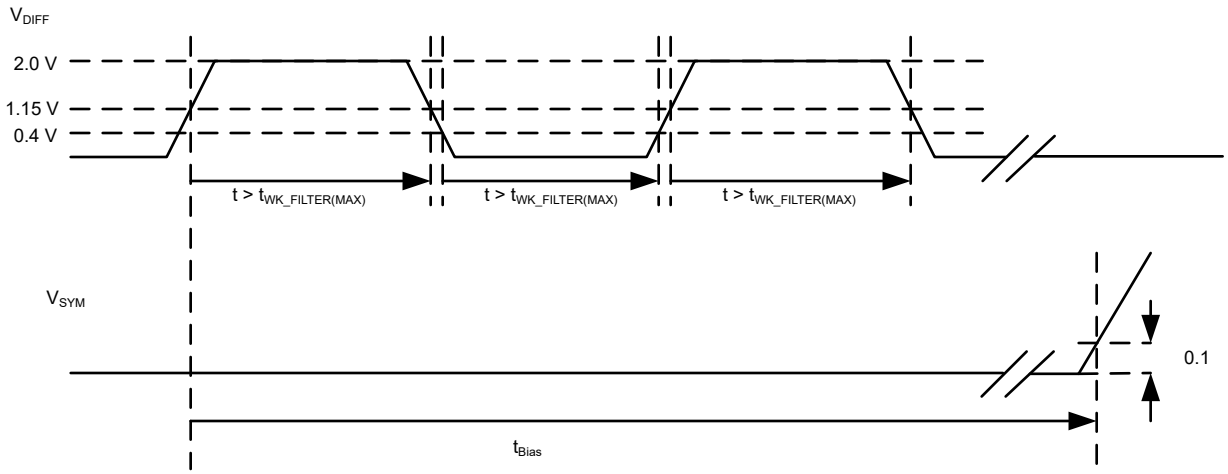


Figure 7-10. Test Signal Definition for Bias Reaction Time Measurement

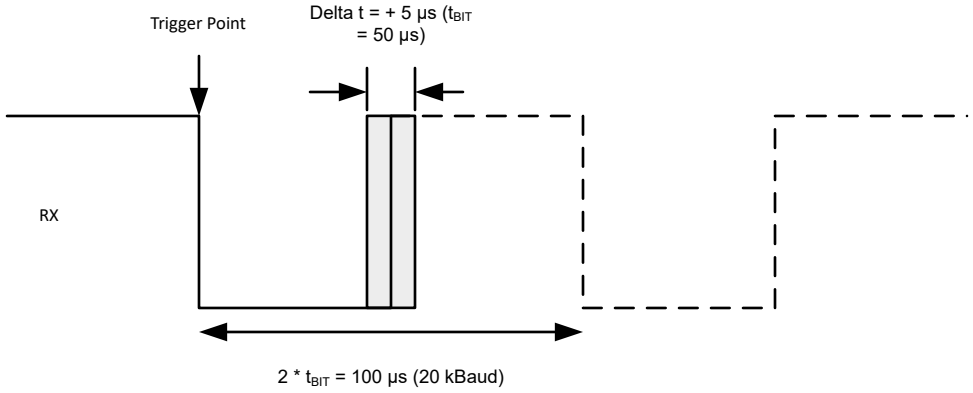


Figure 7-11. LIN RX Response: Operating Voltage Range

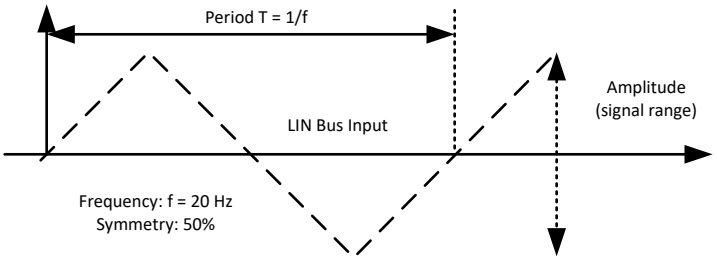


Figure 7-12. LIN Bus Input Signal

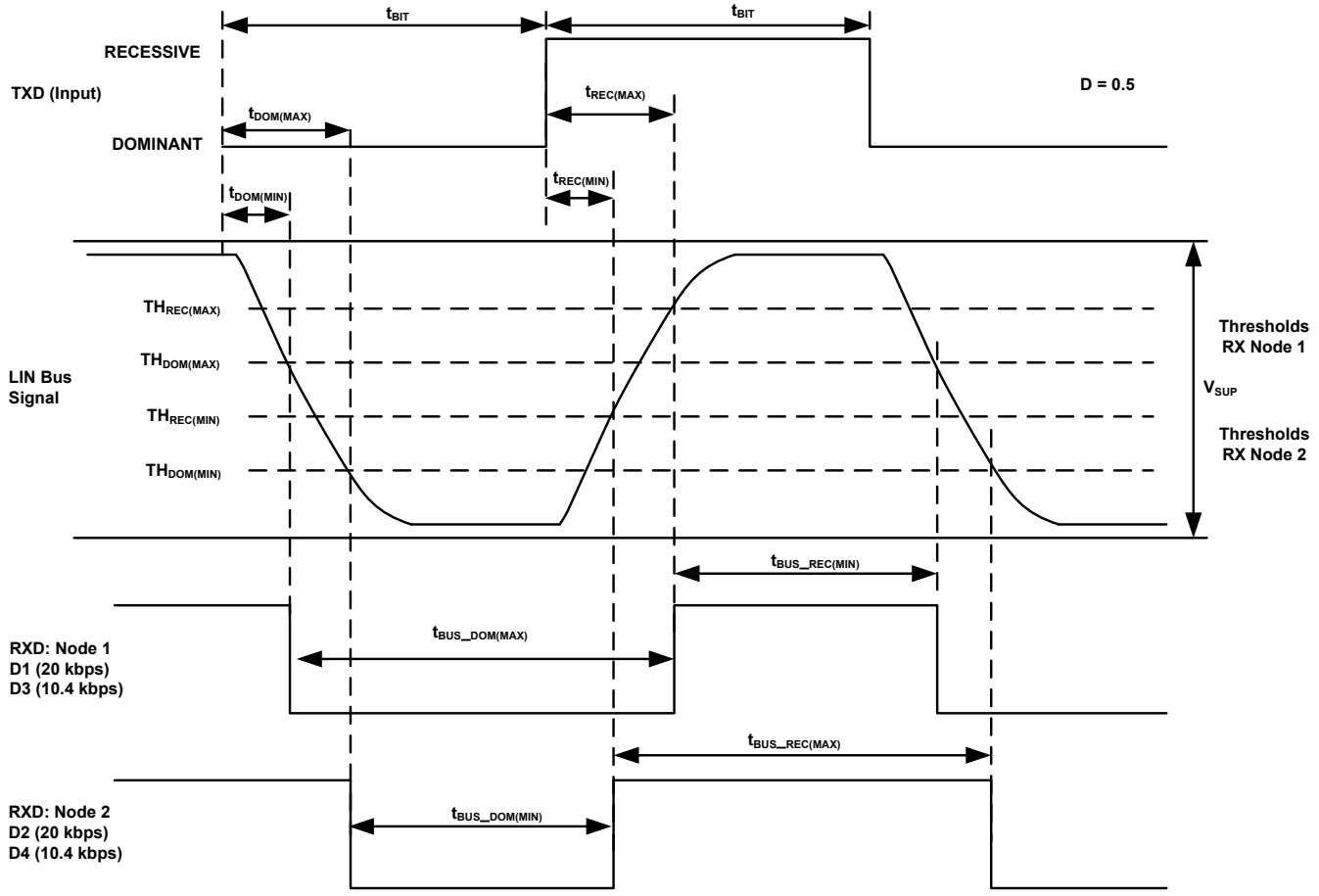


Figure 7-13. Definition of LIN Bus Timing

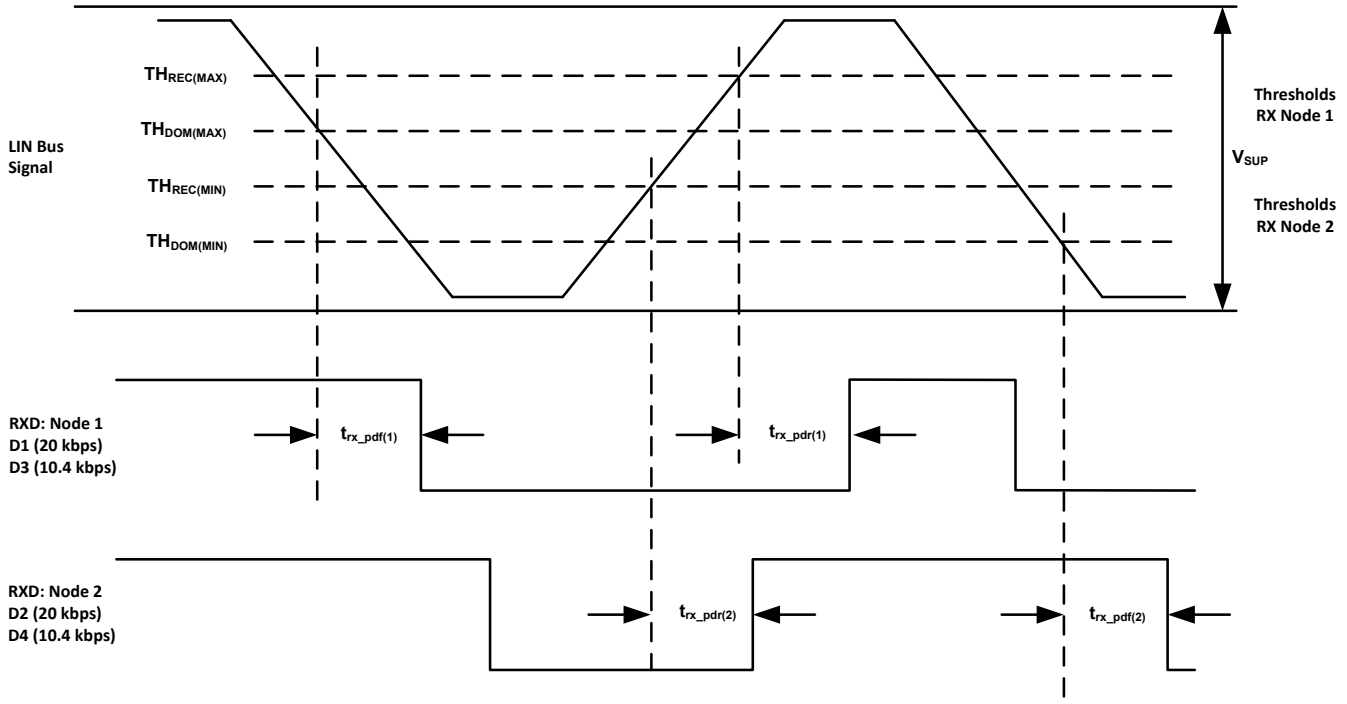


Figure 7-14. LIN Propagation Delay

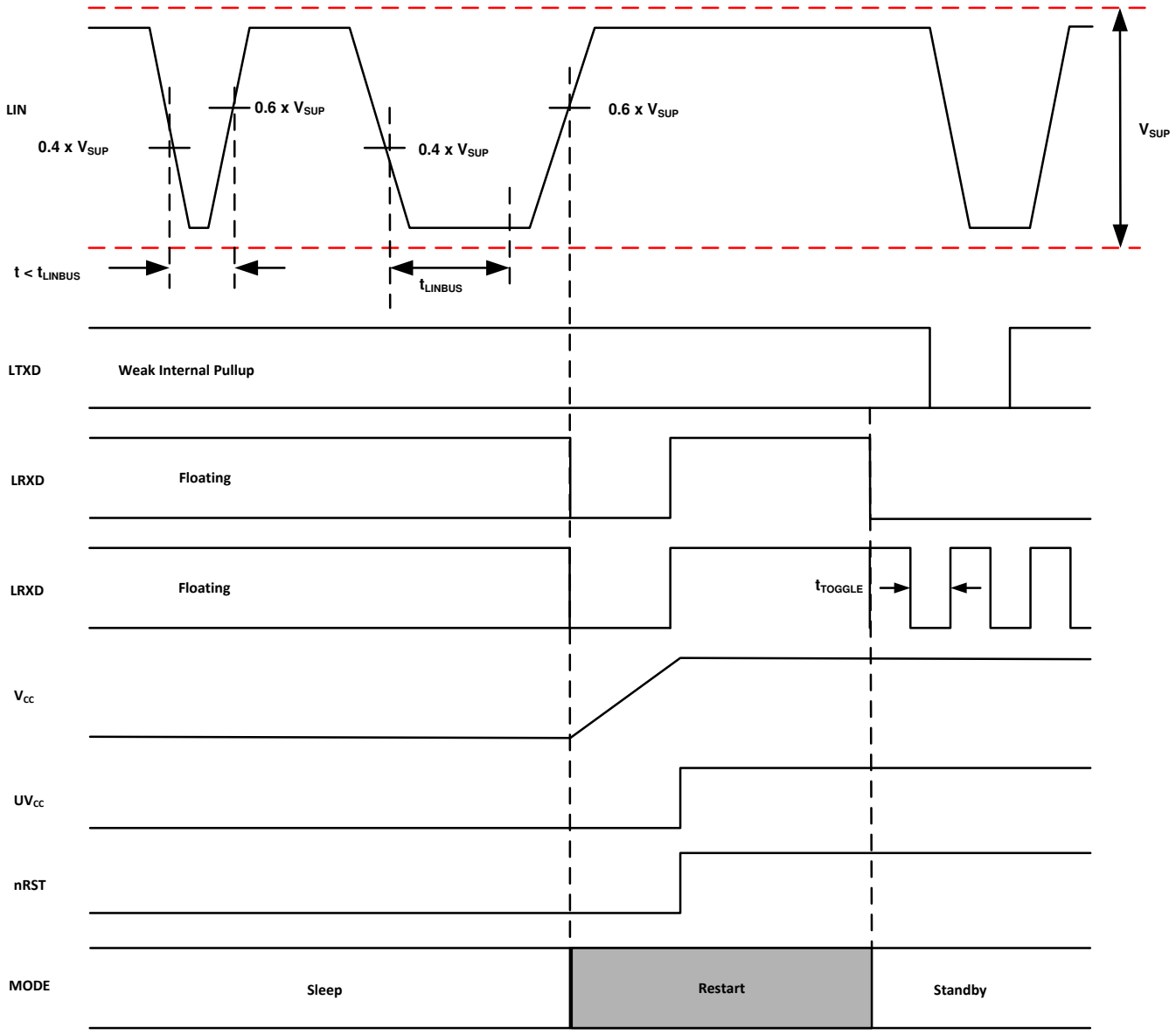


Figure 7-15. Wakeup through LIN Bus

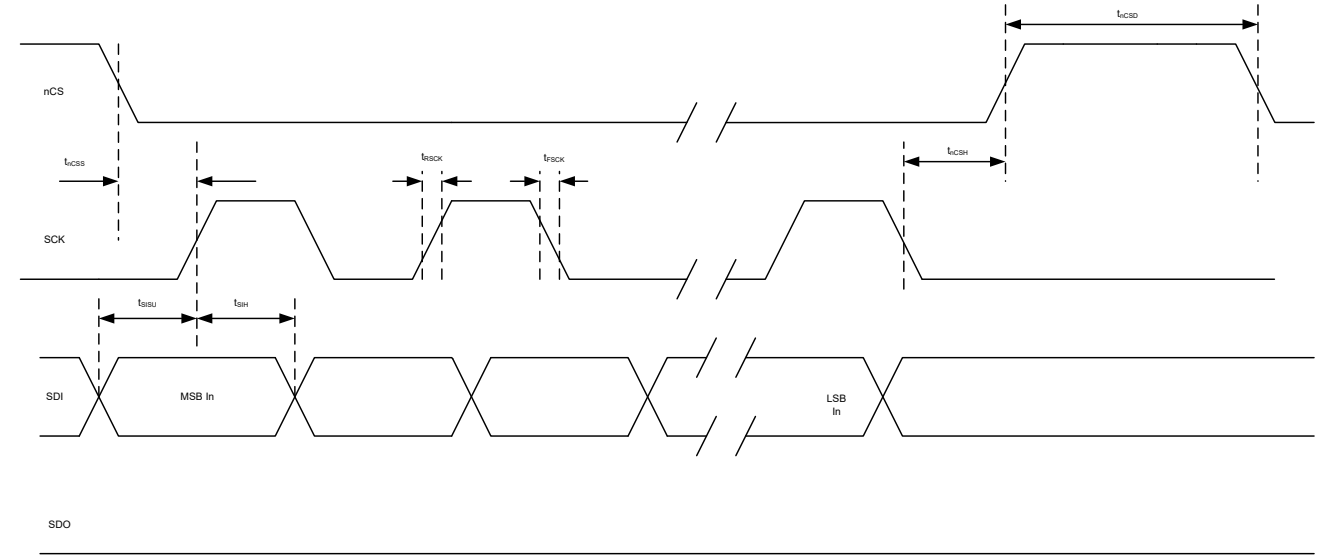


Figure 7-16. SPI AC Characteristic Write

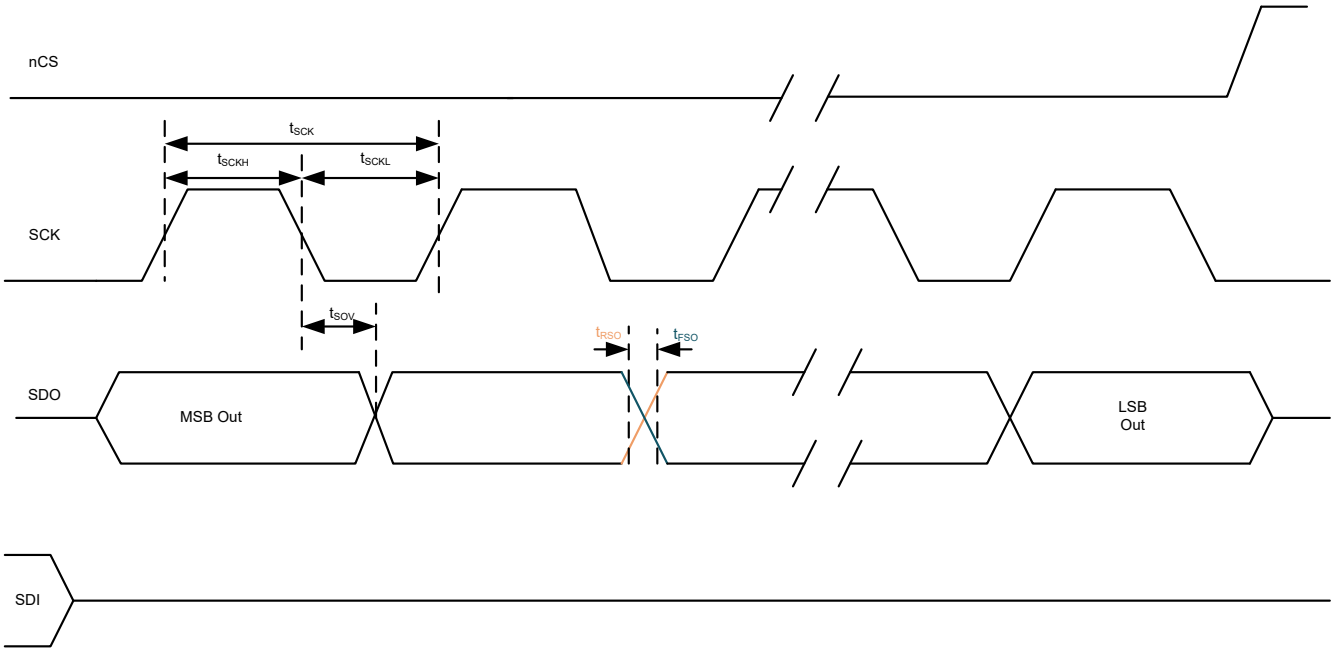


Figure 7-17. SPI AC Characteristic Read

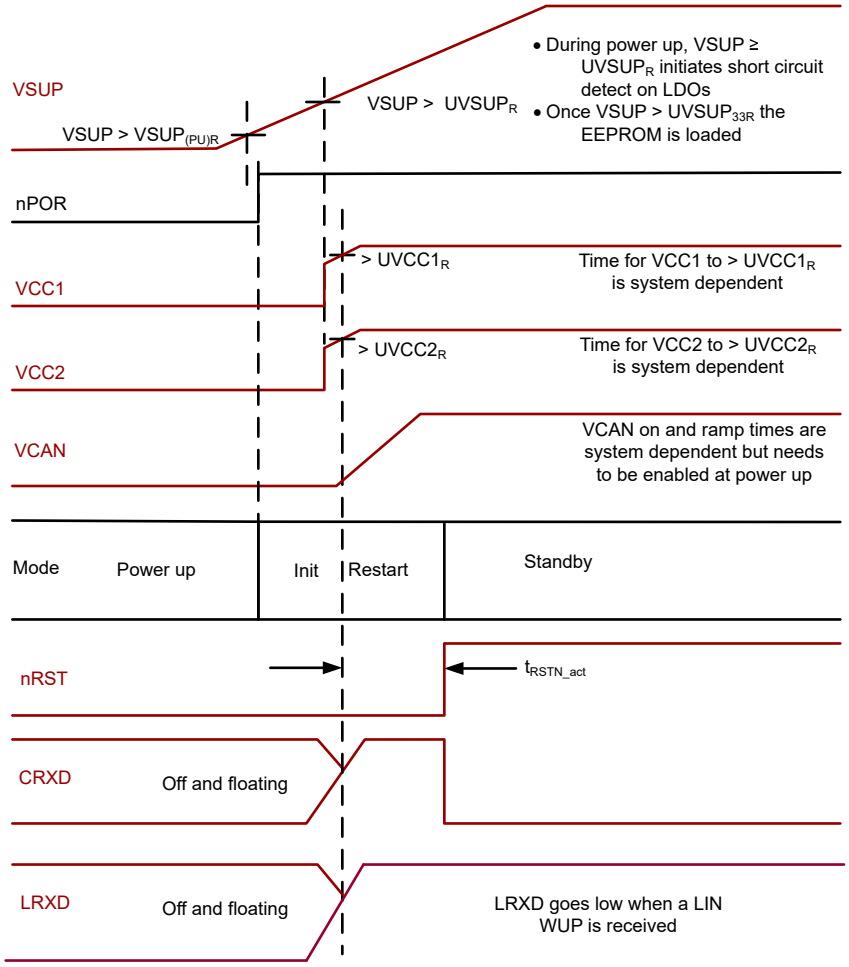


Figure 7-18. Power Up Timing

Note

On initial power up, VEXCC does not turn on if not programmed. After programming and the configuration is saved to EEPROM. VEXCC powers up as programmed after EEPROM has been loaded.

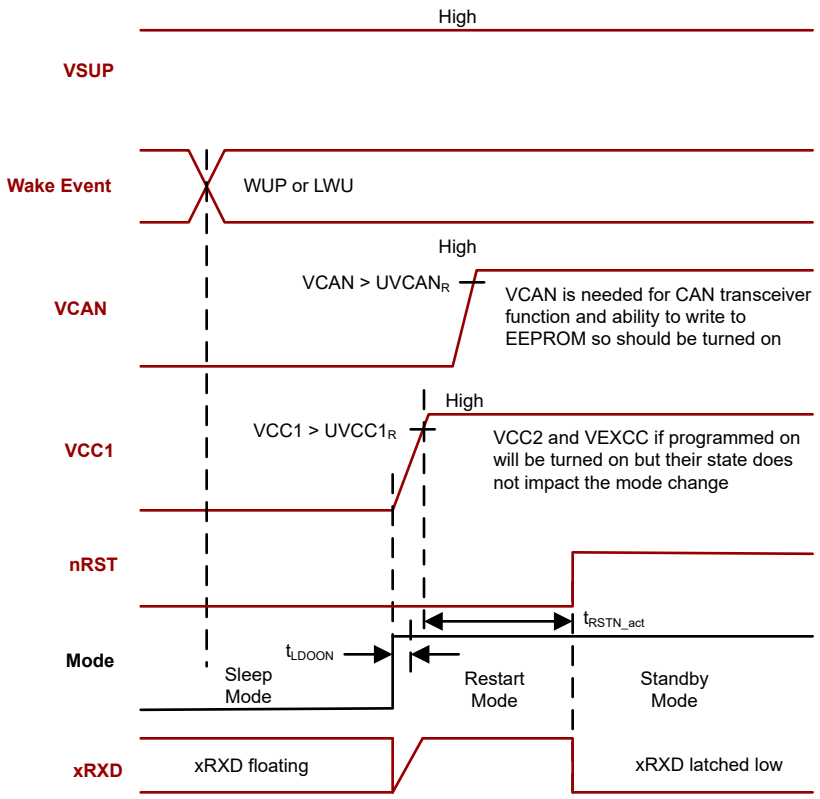


Figure 7-19. Sleep to Restart Timing

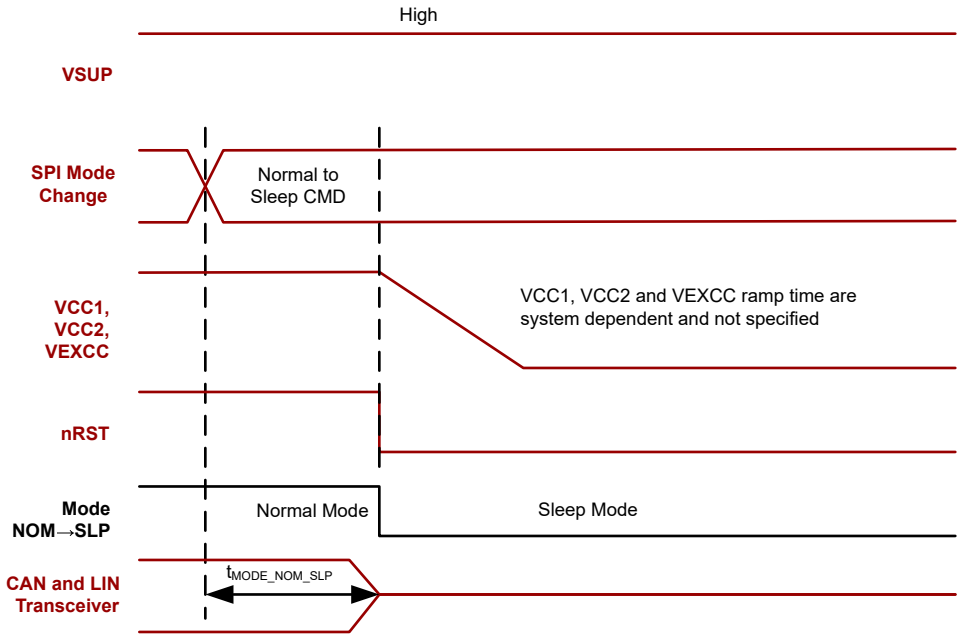


Figure 7-20. Normal to Sleep Timing

Note

The CAN and LIN transceiver is independently controlled. The timing diagram shown shows the transceivers configured to change states based upon the mode.

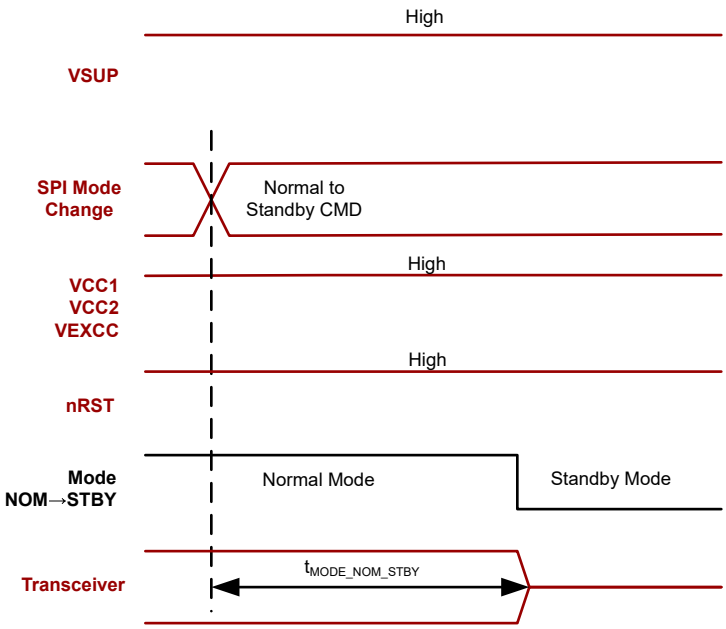


Figure 7-21. Normal to Standby Timing

Note

The CAN and LIN transceiver is independently controlled. The timing diagram shown shows the transceivers configured to change states based upon the mode.

Note

The red signals are input or output of the TCAN285x-Q1 and the black signals are internal to the TCAN285x-Q1. This is for any timing diagram in the data sheet that has red and black colors.

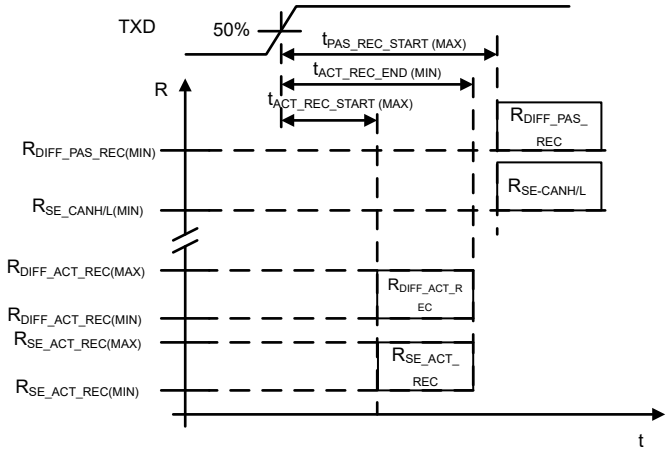


Figure 7-22. Signal Improvement Capability (SIC) Timing Diagram

8 Detailed Description

8.1 Overview

The TCAN285x-Q1 is a family of system basis chips (SBC) that integrate the CAN FD transceiver. The CAN FD transceiver supports data rates up to 8Mbps while meeting the high-speed CAN physical layer standards: ISO 11898-2:2024. The TCAN2857-Q1 integrate a LIN transceiver that supports data rates up to 200kbps when slope control is disabled and programmed for fast mode. The LIN transceiver physical layer transceiver is compliant to LIN 2.2A and ISO/DIS 17987–4 and SAE J2602 standards. These data rates support end of line programming. The TCAN2855-Q1 and TCAN2857-Q1 supports selective wake up on dedicated CAN-frames. The device can also wake up via remote wake up using CAN bus implementing the ISO 11898-2:2024 Wake Up Pattern (WUP). The TCAN285x-Q1 supports 3.3V and 5V processors based upon VCC1 voltage. The device has a Serial Peripheral Interface (SPI) that connects to a local microprocessor for configuration. The TCAN285x-Q1 provide a software development pin to help implementer with development. In this mode, the watchdog is still active but only sets a flag.

The TCAN285x3 variant of the devices provide a VCC1 of 3.3V output and the TCAN285x5 variant of the device provides a VCC1 of 5V output. These devices have a separate 5V LDO, VCC2. The ability to control an external PNP power transistor is provided to support output voltages of 1.8V, 2.5V, 3.3V or 5V at the VEXCC pin. VCC2 and VEXCC are short to battery protected. A 5V input supply is needed at the VCAN pin for the CAN FD transceiver.

The CAN bus has two logical states during operation: recessive and dominant. See Figure 7-1 and Figure 7-2.

Recessive bus state is when the bus is biased to a common mode of about 2.5V via the high resistance internal input resistors of the receiver of each node on the bus across the termination resistors. Recessive is equivalent to logic high and is typically a differential voltage on the bus of almost 0V. Recessive state is also the idle state.

Dominant bus state is when the bus is driven differentially by one or more drivers. Current is induced to flow through the termination resistors and generate a differential voltage on the bus. Dominant is equivalent to logic low and is a differential voltage on the bus greater than the minimum threshold for a CAN dominant. A dominant state overwrites the recessive state.

During arbitration, multiple CAN nodes can transmit a dominant bit at the same time. The differential voltage of the bus is greater than the differential voltage of a single driver.

Transceivers with low power Standby Mode have a third bus state where the bus terminals are weakly biased to ground via the high resistance internal resistors of the receiver. See Figure 7-1 and Figure 7-2.

8.2 Functional Block Diagram

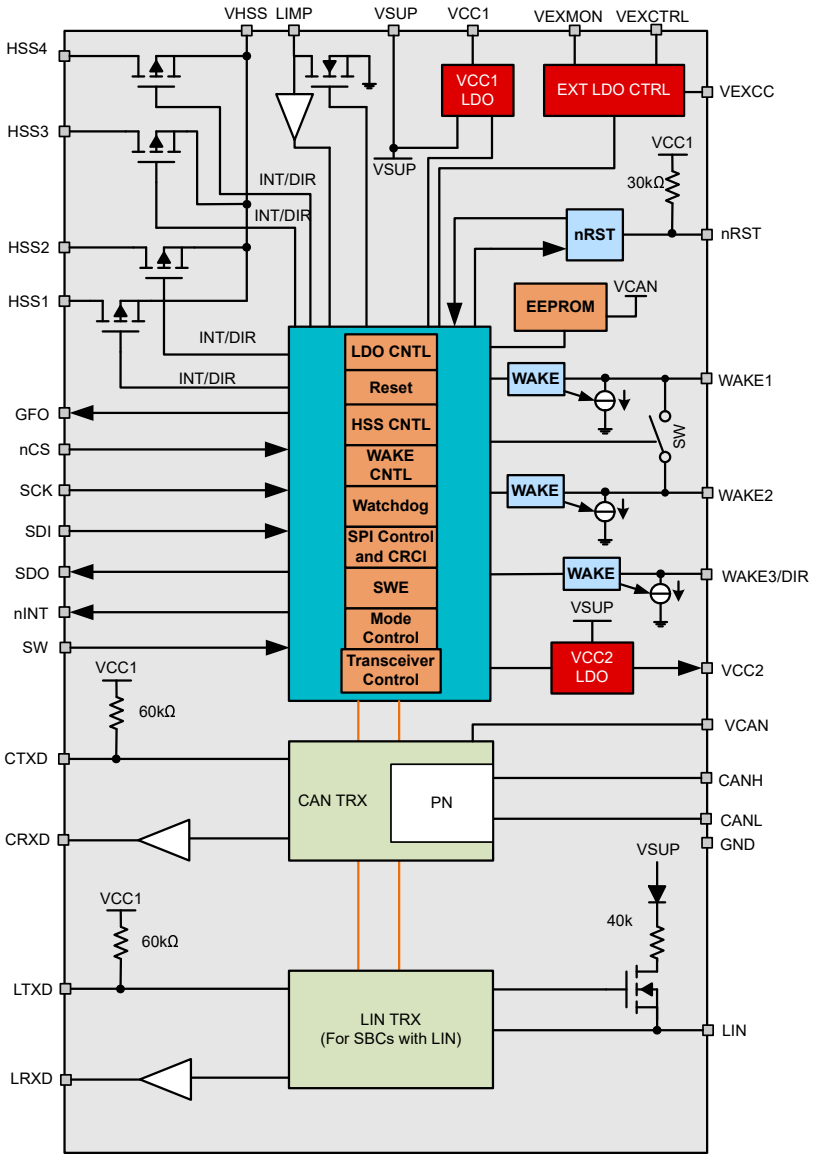


Figure 8-1. TCAN285x-Q1 Functional Block Diagram

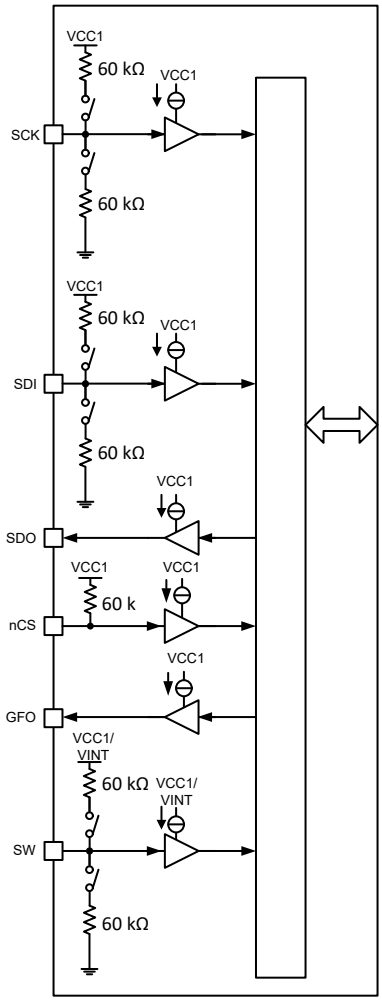


Figure 8-2. Digital Input and Output Block Diagram

8.3 Feature Description

8.3.1 VSUP Pin

VSUP is the high-voltage-tolerant power supply pin. VSUP is connected to the battery through an external reverse battery-blocking diode. If there is a loss of power at the ECU level, the device has a low leakage from the CAN and LIN pins, which does not load the bus down. This is designed for systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

There are three VSUP voltage levels monitored by the device, power on reset ($VSUP_{(PU)R/F}$) and undervoltage ($UVSUP_{33R/F}$ and $VSUP_{5R/F}$), where both ramping up and down values are monitored. UVSUP is also broken down to two different thresholds depending upon VCC1 voltage level. UVSUP is covered in Section 8.4.8.8. For power up, Figure 8-3 provides information on what voltage levels and functions are available and when.

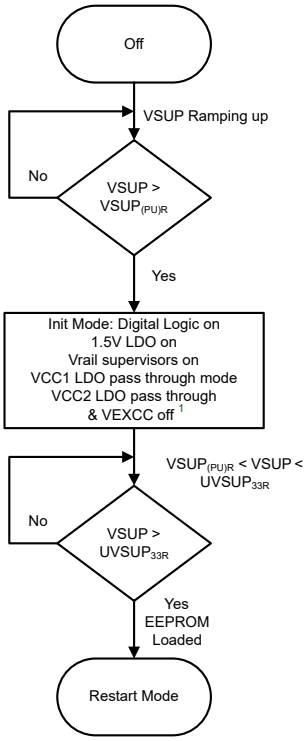


Figure 8-3. Power Up State Diagram

Note

- After initial power up and configuration are saved to EEPROM, the LDOs does not always perform as shown, an example is that these are programmed off
- VEXCC is always off until EERPOM has been loaded, and then behaves as configured
- VCAN must be > UVCAN to write to EEPROM and not considered here

8.3.2 VCC1 Regulator

The VCC1 regulator output pin sources either 3.3V or 5V to with up to 250mA of load current. The VCC1 pin is capable of sinking a current, $ICC1_{SINK}$, depending upon the setting of register VCC1_SINK at 8'h0D[3] and is active when VCC1 is enabled. Refer to Table 9-1 for the external capacitance requirement on this pin. There are three monitors on VCC1, under-voltage (UVCC1), over-voltage (OVCC1) and short to ground ($VCC1_{SC}$). When load sharing with VEXCC, VCC1 fault monitors are used for both. VCC1 is the main LDO output and sets the digital IO voltage levels. Any fault on VCC1 causes a state change.

8.3.3 VCC2 Regulator

The VCC2 pin provides 5V output with up to 200mA load current. Refer to Table 9-1 for the external capacitance requirement on this pin. This pin is short to battery protected and if connected to VCAN or another CAN transceiver in the ECU, VCC2 must not be taken off board where a short to battery can take place. There are three monitors on VCC2, under-voltage (UVCC2), over-voltage (OVCC2) and short to ground ($VCC2_{SC}$). When these faults are detected, an interrupt is provided and the LDO can be turned off. No mode change takes place. When VCC2 is on and not in a fault state, register 8'h4F[2], VCC2_STATUS is set to 1b.

8.3.3.1 V_{CC2} Short to Battery Protection

The output stage of V_{CC2} is short to battery protected. No inverse current flow if external voltage is at or above OVCC2. This protection is for up to the rated Absolute Maximum Rating for this pin. If the device powers up with a short to battery that is above the rated voltage, the device can be damaged or reliability issues can occur.

8.3.4 nRST Pin

The nRST pin is a bi-directional open-drain low side driver that serves several functions, an LDO monitor output for under-voltage events, an indicator to the processor that restart has been entered and a device input reset.

nRST is connected to VCC1 through a pullup resistor, see Figure 8-4. When a VCC1 under-voltage (UVCC1) event takes place, the device transitions to restart mode and nRST pin is latched low. nRST pin behavior is shown in Figure 8-5 based upon the SBC mode of operation and the mode is entered.

When the device enters restart mode this pins behavior depends upon the method of entry. If entering restart mode turns on the LDO the nRST is latched low until the device enters standby mode. This is t_{RSTN_act} after the LDOs exceed the rising under-voltage level. If the LDO is already on when entering restart mode (e.g. watchdog failure), the pin is pulled low for t_{NRST_TOG}. After this time the device transitions to standby mode and nRST returns to high.

The pin can determine when an input pulse of t_{NRSTIN} is applied causing the device to reload EEPROM, set other registers to factory default and enters restart mode.

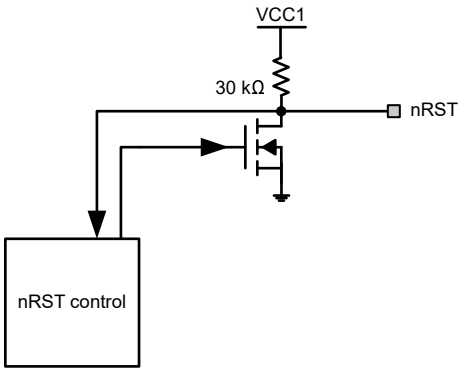


Figure 8-4. nRST Block Diagram

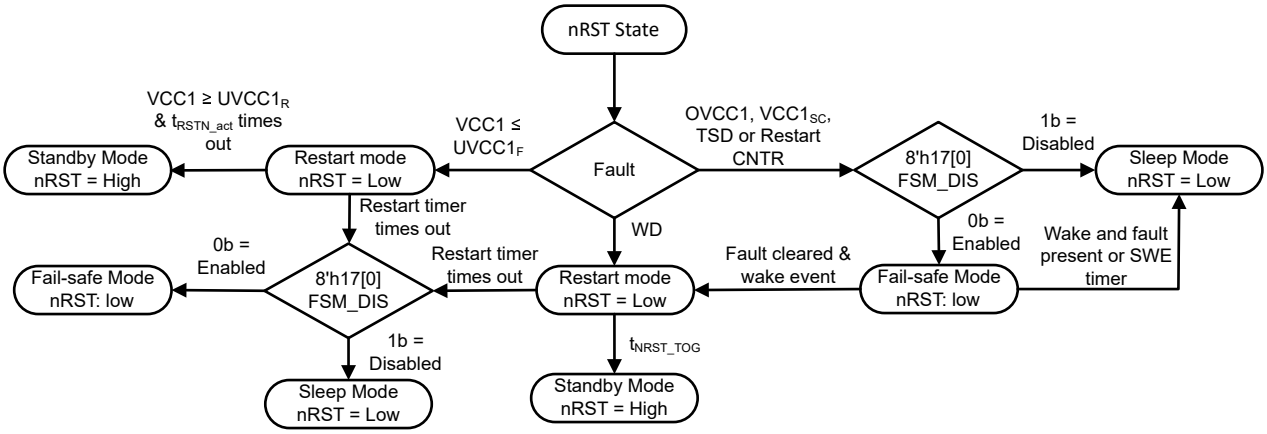


Figure 8-5. nRST State Diagram

8.3.5 VEXCC Regulator

TCAN285x-Q1Can control an external PNP power transistor with β between 50 and 500 to support higher currents and wider voltage needs with the VEXCC output. The TCAN285x-Q1 can support 1.8V, 2.5V, 3.3V and 5V output. The voltage is selected using SPI register 8'h0D[2:0] and defaults to 1.8V. There are three monitors on VEXCC, under-voltage (UVEXCC), over-voltage (OVEXCC) and short to ground ($VEXCC_{SC}$). The external PNP does not be turned on until register 8'h0D[5:4] is configured and is default off. When VEXCC is on and not in a fault state, register 8'h4F[3], VEXCC_STATUS, indicates this by being set to 1b. When load sharing is selected, the device automatically configures the voltage level to match the VCC1 voltage and follow the programming state of VCC1.

The shunt resistor, Rshunt, is between VSUP and VEXMON and serves two purposes depending upon configuration. When used as an stand-alone configuration, see Figure 8-6, Rshunt sets the current limit for the PNP FET. The value for Rshunt must be chosen based on the current limit requirement for the application. The value of this resistor is determined by the VSHUNTH threshold divided by the required current limit, meaning VSHUNTH/$I_{VEXCC-LIM}$ where $I_{VEXCC-LIM}$ is the required current limit value.

When configured for load sharing with VCC1, see Figure 8-7, the resistor Rshnut sets the ratio of current between VEXCC and VCC1. See Equation 1 and Equation 2 to determine how to calculate the Rshunt value.

If the TCAN285x-Q1 is not already programmed for VEXCC load sharing with VCC1 using end-of-line programming, the device can be programmed for load sharing using the following sequence of steps:

1. Power-up the device with VCC1 shorted to EXVCC on the board; the device powers-up into Standby mode
2. Set VEXCC voltage configuration register, 8'h0D[2:0], to the correct voltage setting. This must be the same as VCC1 setting (3.3V or 5V only)
3. Set the VEXT_CFG, VEXCC configuration register, 8'h0D[5:4] to match the VCC1_CFG setting
4. Wait 5ms for output to settle, read VEXCC_STATUS, 8'h4F[3], to confirm VEXCC is in regulation
5. Enable Load Sharing for VEXCC with register 8'h0D[2:0] = 100b
6. If the Load Sharing configuration is not saved to EEPROM and the device experiences POR event, repeat the steps 1-5.

$$Ratio = \left(\frac{IVEXCC}{IVCC1}\right) \quad (1)$$

$$Rshunt = \left(\frac{8.824}{Ratio}\right) - \left(\left(\frac{1 + Ratio}{Ratio}\right) \times \left(\frac{0.8}{Iload}\right)\right) \quad (2)$$

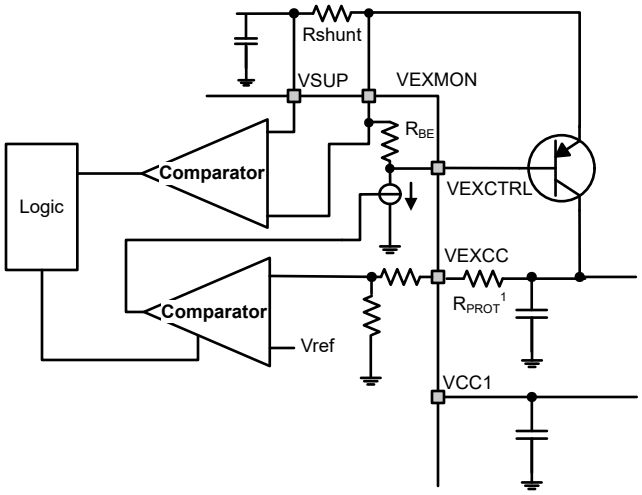


Figure 8-6. Stand-alone External PNP Example

Note

1. A series resistance of R_{PROT} = 100Ω is recommended when supplying ECU-external loads for EMC robustness

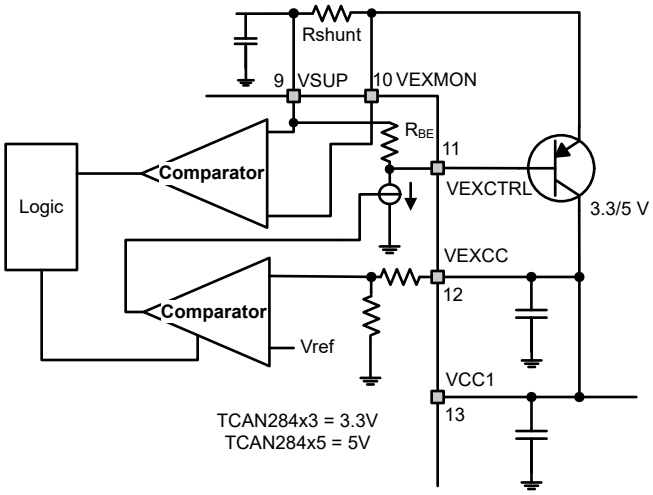


Figure 8-7. External PNP Example With Load Sharing

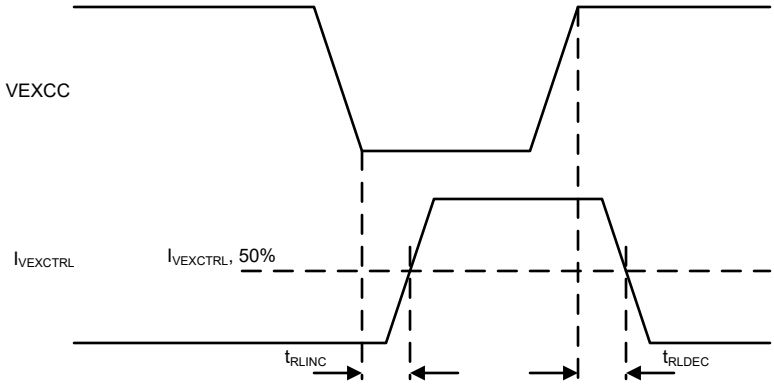


Figure 8-8. VEXCC versus $I_{VEXCTRL}$ Timing Diagram

Note

- The external PNP transistor power handling capabilities are application specific and must therefore be designed according to the selected PNP device along with the PCB properties to prevent thermal damage as the SBC is not able to make sure the thermal protection of the external PNP transistor.
- For limiting current through the external PNP transistor, connect VEXMON pin to the same power rail that connects to VSUP pin of the device using Rshunt as shown in Figure 8-6.
- If the external PNP collector is being connected to a different voltage rail, the device is not able to provide current limit capability. To avoid issues, the current limit must be disabled by using SBC_CONFIG register 8'h0C[6] VEXCC_ILIM_DIS = 1b. Disabling the current limit does not disable over-voltage, under-voltage, or short circuit detection.

8.3.6 CAN FD Transceiver

Figure 8-9 shows the block diagram for the CAN FD Transceiver.

The CTXD is the input to the CAN FD transmitter from the processor that controls the state of the CAN FD bus. When CTXD is low, the bus output is dominant. When CTXD is high, the bus output is recessive which is a logic 0. The CTXD input structure is compatible with processors with 3.3V to 5V V_O. CTXD has an internal pullup resistor to VCC1. The bus is protected from being stuck dominant through a system failure driving CTXD low through the dominant state time-out timer.

CRXD is the output of the CAN FD receiver. When a CAN wake event takes place the CRXD pin is latched low. CRXD also indicates the local wake up (LWU) from the high voltage WAKE pins. The CRXD is a push-pull output buffer and as such an external pull-up is not needed. In restart mode, the RXD pins are driven high. When VCC1 is > UVCC1 for t_{RSTN_act}, the device automatically transition to standby mode. The CRXD pin is then pulled low to indicate a wake up request. The CRXD pin can be programmed to toggle low/high with a pulse width of t_{TOGGLE}, see Section 8.4.7.3.1 as an example of this feature.

The VCAN pin is the 5V supply input for the CAN FD transceiver. VCAN is monitored for under-voltage events, UVCAN. When VCAN is present and not in a fault state, register 8'h4F[1], VCAN_STATUS, is set to 1b. For the CAN FD transceiver to be available, VCAN must be present. This pin is also used for EEPROM writing so must be on for this function to happen.

The CAN FD transceiver can be separately programmed outside of the SBC mode control or tied to the SBC mode control. When tied to the SBC mode control, changing the SBC mode to normal mode automatically changes the transceiver to ON and transceiver is wake capable in all other modes. When programmed separately than the SBC modes, there are certain states that the transceivers cannot be in for the mode.

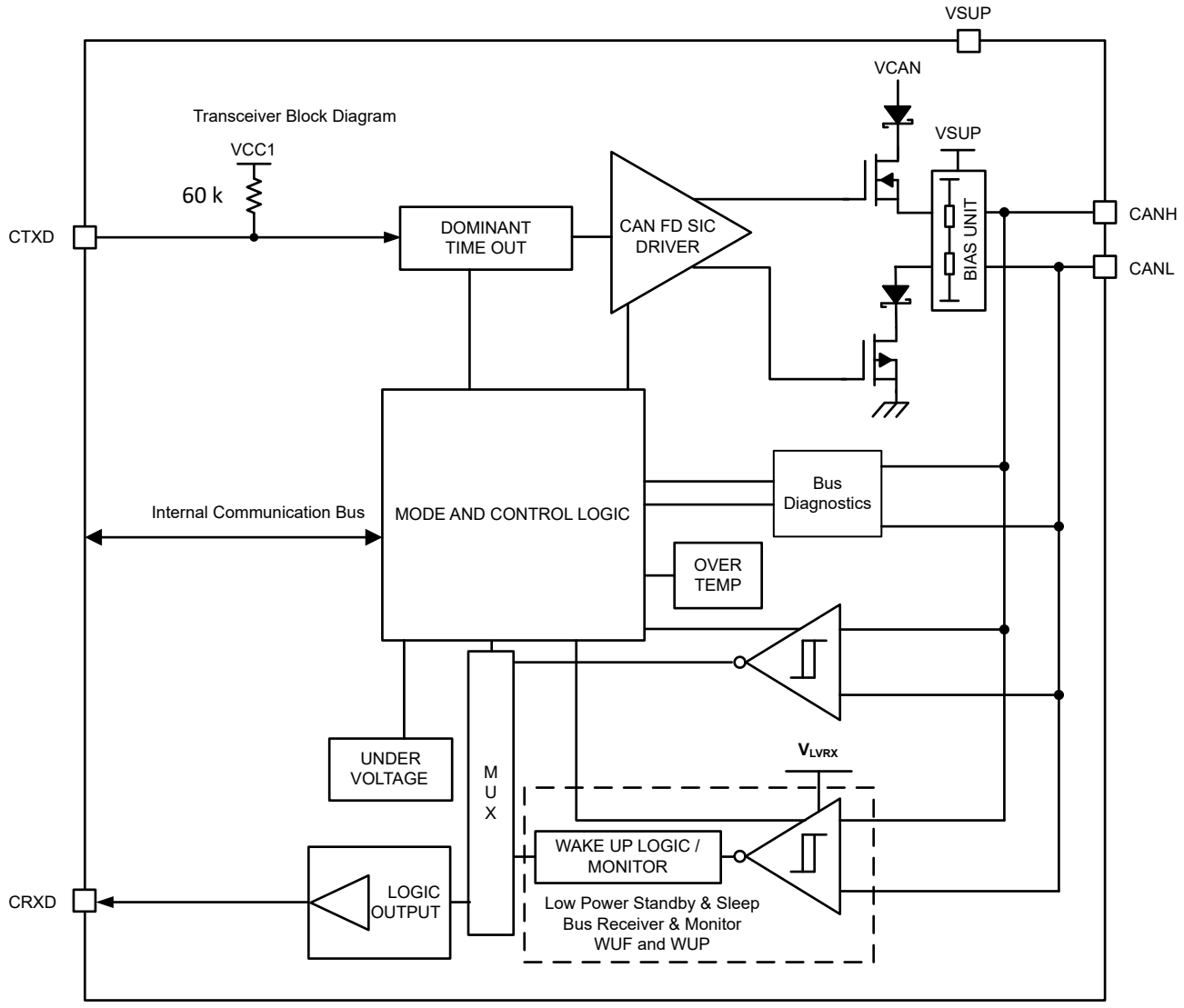


Figure 8-9. CAN Transceiver Block Diagram

Note

If a mode change is initiated and the transceiver is not in an allowed state, the mode change does not take place. The MODE_ERR interrupt at 8'h5A[3] is set to 1b.

This includes changing the transceiver configuration to a disallowed state while in the current SBC mode. See Table 8-1 and Table 8-1 for allowed transceiver configurations for each SBC mode. Here are a few specific cases for consideration:

- A transceiver in Normal mode configured for listen, wake capable and off can transition to standby mode and the state are the same.
- Transitioning to restart mode is wake capable unless the transceiver is programmed off.
- Transitioning from restart mode to standby mode is wake capable unless the transceiver is programmed off.
- When using the SWE timer and the timer times out, the transceivers automatically becomes wake capable when entering sleep mode or fail-safe mode.

Note

If the device is in SBC normal mode and the transceivers are programmed on, the TXD pin is checked. If the TXD pin is dominant, the transceiver does not turn on the transmitter until the TXD pin has transitioned to recessive.

The CAN FD transceiver supports off, on, listen and wake capable. The state of the transceiver is programmed using register 8'h10[2:0]. On represents what is normal mode for a stand-alone transceiver. The CAN transceiver defaults to wake capable when entering fail-safe mode but can be disabled for this mode by using CAN1_FSM_DIS at register 8'h10[3] = 1b.

Table 8-1. CAN FD Transceiver Programmable State by SBC Mode

SBC Mode	On	Listen	Wake Capable	Off	SBC Mode Control
Normal	✓	✓	✓	✓	On
Standby		✓	✓	✓	Wake Capable
Sleep			✓ default	✓	Wake Capable
Restart			✓ default	✓	Wake Capable
Fail-safe			✓ default	✓	Wake Capable

Note

- When entering SBC restart mode, the transceiver changes wake capable
- When entering SBC fail-safe mode, the transceiver defaults to wake capable.

8.3.6.1 Driver and Receiver Function

The TXD and RXD pins are input and output between the processor and the CAN FD and LIN physical layer transceivers. The digital logic input and output levels for these devices are TTL levels with respect to VCC1 for compatibility with protocol controllers having 3.3V or 5V logic. Table 8-2 and Table 8-3 provides the states of the CAN driver and CAN receiver in each mode.

Table 8-2. Driver Function Table

Transceiver State	TXD Input	Bus Outputs		Driven Bus State
		CANH	CANL	
CAN On	L	H	L	Dominant
	H or Open	Z	Z	Biased Recessive
Wake capable	X	Z	Z	Weak Pull to GND
Off	X	Z	Z	

Table 8-3. CAN Receiver Function Table

Transceiver State	CAN Differential Inputs $V_{ID} = V_{CANH} – V_{CANL}$	Bus States	RXD Terminal
On/Listen	$V_{ID} \geq 0.9V$	Dominant	L
	$0.5V < V_{ID} < 0.9V$	Undefined	Undefined
	$V_{ID} \leq 0.5V$	Recessive	H
Wake capable	$V_{ID} \geq 1.15V$	Dominant	See Section 8.4.7
	$0.4V < V_{ID} < 1.15V$	Undefined	
	$V_{ID} \leq 0.4V$	Recessive	
Off	Open ($V_{ID} \approx 0V$)	Open	H

8.3.6.2 CAN Bus Biasing

Bus biasing can be normal biasing, active in normal mode and inactive in low-power mode. Automatic voltage biasing is where the bus is active in normal mode but is controlled by the voltage between CANH and CANL in lower power modes. See Figure 8-10 for the state diagram on how the TCAN285x-Q1 performs automatic biasing.

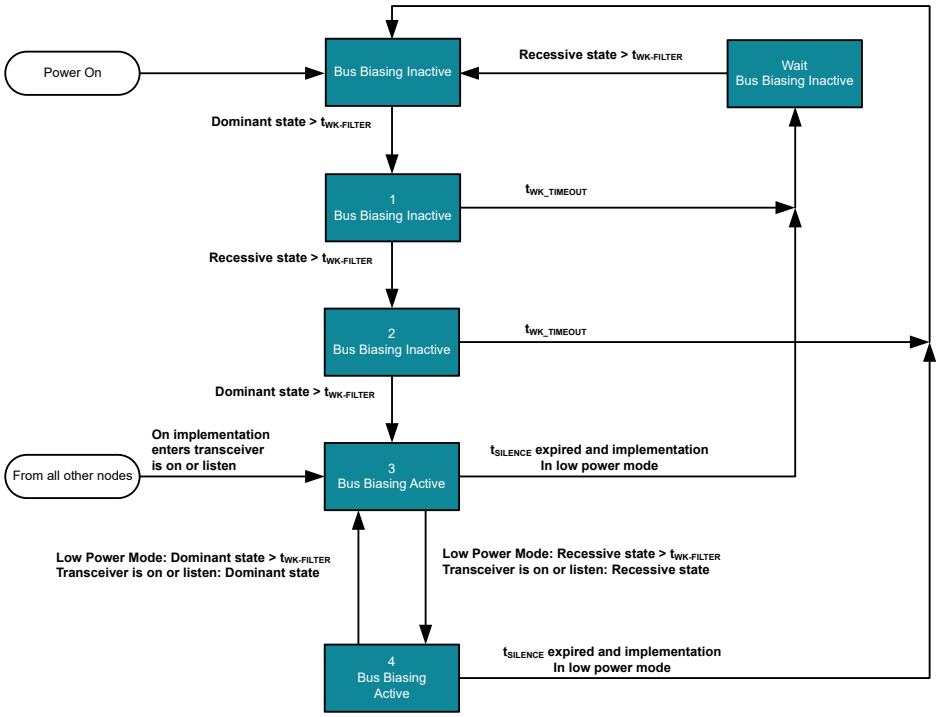


Figure 8-10. Automatic bus biasing state diagram

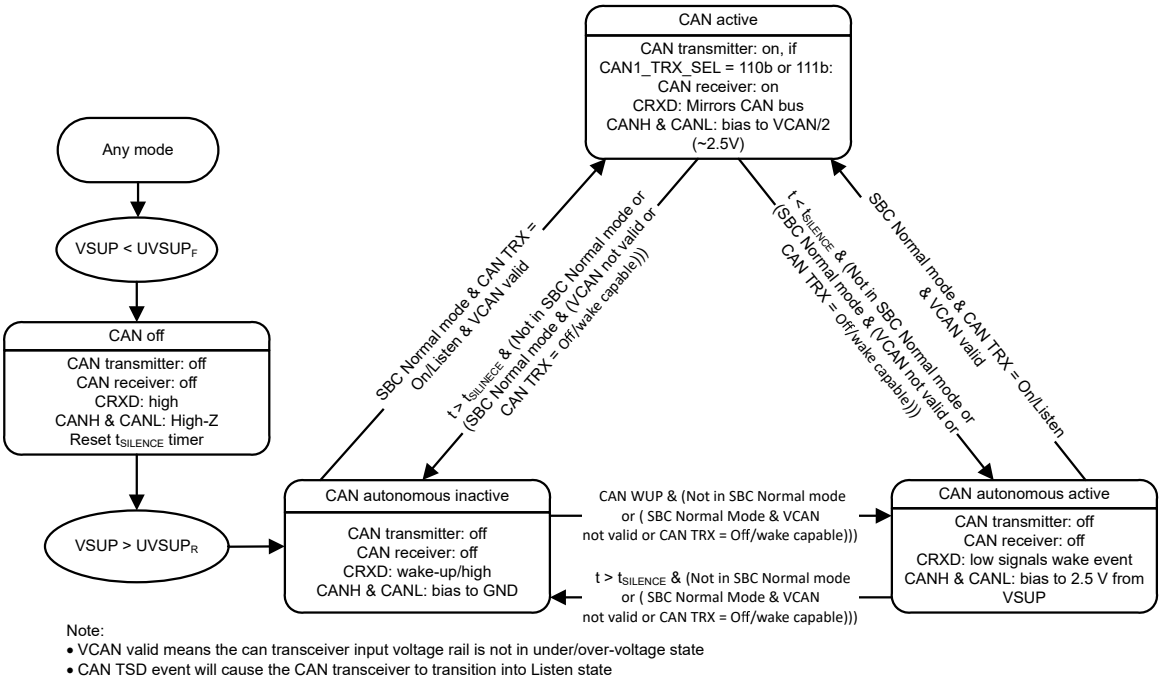


Figure 8-11. Bus biasing

8.3.7 LIN Transceiver

The TCAN2857-Q1 provides a LIN transceiver. The block diagram is as shown in Figure 8-12.

The LTXD pin is the input to the LIN transmitter that controls the state of the LIN bus. When LTXD is low, the bus output is dominant. When LTXD is high, the bus output is recessive which is a logic 0. The LTXD input structure is compatible with processors with 3.3V to 5V V_O. LTXD has an internal pullup resistor to VCC1. The bus is protected from being stuck dominant through a system failure driving TXD low through the dominant state time-out timer.

LRXD is the output of the LIN receiver. When a LIN wake event takes place, the LRXD is latched low. LRXD pin is a push-pull output buffer and as such an external pull-up is not needed. In restart mode, the LRXD pin is driven high. When VCC1 is > UVCC1 for t_{RSTN_act}, the device automatically transition to standby mode. The LRXD pin is then pulled low to indicate a wake up due to LIN WUP.

For the TCAN2855-Q1, the LRXD and LTXD pins are not used and must not be connected on the board.

LIN transceiver supports on, fast, listen, off and wake capable states. The state of this transceiver is programmed using register 8'h1D[7:5]. The LIN transceiver defaults to wake capable when entering fail-safe mode but can be disabled for this mode by using LIN1_FSM_DIS at register 8'h1C[1] = 1b.

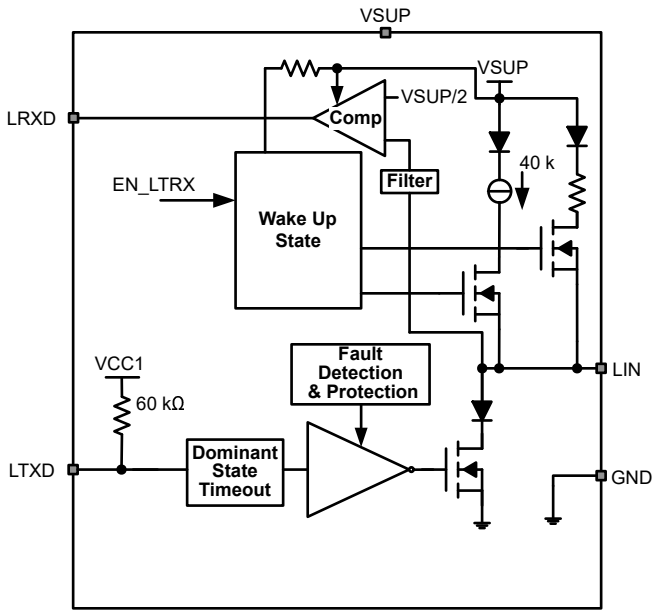


Figure 8-12. LIN Transceiver Block Diagram

Table 8-4. LIN Transceiver Programmable State by SBC Mode

SBC Mode	On	Fast	Listen	Wake Capable	Off	SBC Mode Control
Normal	✓	✓	✓	✓	✓	On
Standby			✓	✓	✓	Wake Capable
Sleep				✓ default	✓	Wake Capable
Restart				✓ default	✓	Wake Capable
Fail-safe				✓ default	✓	Wake Capable

Note

- When entering SBC restart mode, the transceiver changes to wake capable
- When entering SBC fail-safe mode, the transceiver defaults to wake capable

For the TCAN2855-Q1, the LIN pin is not present and is NU for not used. This pin must not be connected on the board.

8.3.7.1 LIN Transmitter Characteristics

The transmitter meets thresholds and AC parameters according to the LIN specification. The transmitter is a low side transistor with internal current limitation and thermal shutdown. During a thermal shutdown condition, the transmitter is disabled to protect the device. There is an internal pullup resistor with a serial diode structure to VSUP, so no external pull-up components are required for the LIN peripheral node applications. An external pullup resistor and series diode to VSUP must be added when the device is used for a controller node application. In fast mode the transmitter can support 200kbps data rates.

Table 8-5. LIN Driver Function Table

Transceiver State	TXD Input	LIN Bus Output	Driven Bus State
LIN On	L	L	Dominant
	H or Open	H	Biased Recessive
Wake capable	X	H	
Off	X	Z	

8.3.7.2 LIN Receiver Characteristics

The receiver characteristic thresholds are ratio-metric with the device supply pin according to the LIN specification.

The receiver is capable of receiving higher data rates (> 100kbps) than supported by LIN or SAEJ 2602 specifications. This allows the TCAN2857-Q1 to be used for high speed downloads at the end-of-line production or other applications. The actual data rate achievable depends on system time constants (bus capacitance and pull-up resistance) and driver characteristics used in the system. In fast mode the receiver can support 200kbps.

8.3.7.3 LIN Termination

There is an internal pullup resistor with a serial diode structure to VSUP, so no external pull-up components are required for the LIN responder node applications. An external pullup resistor (1kΩ) and a series diode to VSUP must be added when the device is used for commander node applications as per the LIN specification.

Figure 8-13 shows a commander node configuration and how the voltage levels are defined.

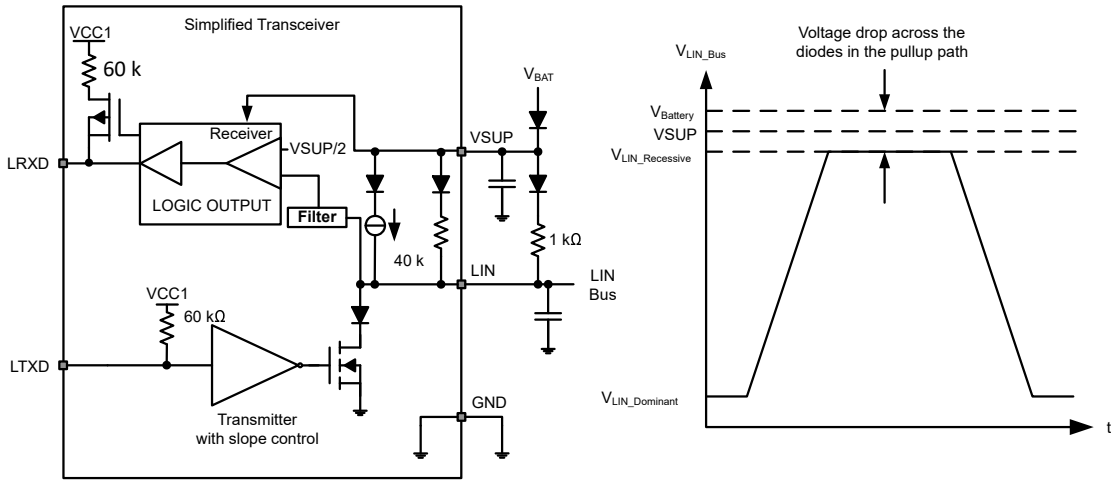


Figure 8-13. Commander node configuration with voltage levels

8.3.8 GND

GND is the device ground connection. The device can operate with a ground shift as long as the ground shift does not reduce the VSUP below the minimum operating voltage. If there is a loss of ground at the ECU level, the device has extremely low leakage from the CANL/H and LIN pins, which does not load the bus down. This is best for CAN and LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

8.3.9 LIMP Pin

The LIMP pin is for the limp home function and is an open-drain, active low, output. The pin is used for a limp home mode if the watchdog has timed out causing a reset. The pin must be pulled up with an external resistor connected to the battery supply, VSUP. For the LIMP pin to be turned off, the watchdog error counter must reach zero from correct input triggers. If programmed any event that triggers the fail-safe mode also turns on the LIMP pin. The state of this pin can be read back by setting DEVICE_CONFIG register 8'h1A[6] LIMP_RD_EN to 1b. The state of the LIMP pin active (on) or inactive (off) can be read back from LIMP_STATE at 8'h1A[5].

8.3.10 High-side Switches (HSS1- HSS4)

These pins are based upon a high-side switch configuration supporting load current up to $I_{OC(HSS)}$. The control method for each HSSx is accomplished by programming the HSS_CNTL (8'h1E) and HSS_CNTL2 (8'h4D). This control includes any of four PWM settings, two timers, always on/off or direct drive from the WAKE3/DIR pin. The four 10-bit PWMs support 200Hz or 400Hz and can be assigned to any HSSx. To configure PWM3 and PWM4 SBC_CONFIG0 register 8'h0C[5:4] needs to be set to 01b. Once this is set, use the PWM1 and

PWM2 configuration registers for programming PWM3 and PWM4. This changes the PWM1 control registers to PWM3 and the PWM2 control registers to PWM4. After configuring the registers, change 8'h0C[5:4] = 00b; thus, converting the PWM registers back to PWM1 and PWM2. The timers are configured using TIMERx_CONFIG registers 8'h25 and 8'h26.

Any HSS can be connected to any other HSS and synchronized by assigning them the same control mechanism. This allows higher current loads to be used. Assigning PWM1 to HSS1 - HSS4 synchronizes all four high-side switches. Timer1 and Timer2 can be used the same way. For the ability of the MCU to drive the HSSx directly, a direct drive capability using WAKE3/DIR pin is used. The high-side switches can be synchronized using direct drive by programming 1000b to the appropriate HSSx_CNTL fields.

When programing the high-side switches, the following procedure must be used:

- Make sure the selected timer, PWM or direct drive value is at 0
- Program the selected high-side switches to the desired timer, PWM or direct drive
  - If multiple HSSx need to be synchronized, program the desired HSSx to the same control mechanism (timer/PWM/direct drive)
- For using the timer, program the desired timer period and the ON time.

  HSSx starts as soon as the on-time is programmed.
- To program the PWM, follow these steps:
  - Program the PWMx_FREQ
  - Program the PWMx_DC_MSB
  - Program the PWMx_DC (LSB bits of duty cycle). **Only after this step, the PWM is programmed.**
    - Any changes to the PWMx_FREQ or PWMx_DC_MSB **must include** programming the PWMx_DC (LSB bits) as the last step for the updates to be implemented.
- For direct drive, the recommendation is to configure WAKE3_LEVEL at 8'h2B[1:0] to 00b for VCC1 levels to match the processor.

The high side switches are monitored for open loads and over-current faults. When an over-current is detected through an HSS, there is a filter time, t_{OCFLTR}, to determine if over-current is valid. If valid, a corresponding HSSx over-current interrupt flag is set in the INT_7 register 8'h55. If the over-current condition persists for t_{OCOFF}, the HSS is turned off and HSSx_CNTL register is reset to 000b. HSS is not turned back ON automatically. HSS can be turned ON again after another t_{OCOFF} period by writing into the corresponding HSSx_CNTL register. If the over-current fault is cleared, HSS stays ON. If the over-current fault exists, HSS is shutoff after t_{OCOFF}. When an open load fault is detected at an HSS, an interrupt flag is set in the INT_7 register 8'h55. HSS is not turned off due to open load fault. Please note that HSSx over-current or open load fault interrupt flags are not automatically cleared after the fault is cleared.

The VHSS pin is also monitored for a high-side switch over-voltage condition based upon OVHSS thresholds. If VHSS exceeds this threshold the high-side switches are turned off. When VHSS drops below this threshold the high-side switches is automatically enabled to the previous state. Register 8'h4F[7:6] disables the high-side switches from automatically shutting down due to an OVHSS or UVHSS event. HSS_OV_UV_REC, register 8'h4F[5] = 1b enables the high-side switches to go back to the programmed state. If HSS_OV_UV_REC = 0b, the high-side switches stay off due to an over-voltage or under-voltage event on VHSS.

HSS4 can be configured to use one of two timers that allows HSS4 to work with WAKE1, WAKE2 and WAKE3 pins supporting cyclic sensing. Cyclic sensing can be used in standby or sleep mode thus reducing mode current due to the HSS being constantly on.

Note

- For resistive loads an external capacitor to ground in not required.
- For inductive loads an external 100nF capacitor to ground is needed.
- When using the 10-bit PWM with the HSS, selecting values that are unrealizable due to the on and off times of the switch is possible. An example of this is 00 0000 0001b

8.3.11 WAKE1, WAKE2 and WAKE3/DIR Pins

WAKE1, WAKE2 and WAKE3/DIR pins are ground biased local wake up (LWU) input pins that are high voltage tolerant. This function is explained further in Section 8.4.7.3. The pins can be both rising and falling edge trigger, meaning the pins recognizes a LWU on either edge of WAKE pin transition. The pin can be configured to accept a pulse, see Figure 8-34 for timing diagram of this behavior. The WAKE pins are default enabled but can be disabled by using register 8'h2A[7:5], WAKE_PIN_SET, to turn off individual ones. Register 8'h11[7:6] sets the method the pins uses to register a wake event. These pins can be configured for cyclic sensing wake, see Section 8.4.7.3.2, or static wake.

The WAKE pins have four individual thresholds that can be set for a state change.

- Register 8'h12[1:0], WAKE1_LEVEL
- Register 8'h2B[5:4], WAKE2_LEVEL
- Register 8'h2B[1:0], WAKE3_LEVEL

Note

If WAKEx_LEVEL = 10b or 11b is selected and uses static wake, the system designer needs to make sure that VSUP does not cross the wake pin threshold; otherwise, a false wake up can take place. Normal undervoltage events on VSUP does not cause this to take place.

If WAKEx_LEVEL = 00b and the device enters Fail-safe mode or Sleep mode where VCC1 is off, the WAKEx pin becomes disabled and CAN and LIN are set wake-capable.

Register 8'h2A[4:0], MULTI_WAKE_STAT, provides which WAKE pin or combination of WAKE pins caused the LWU event. The individual status of the pins, low or high, can be read via SPI in any mode that SPI is available.

- Register 8'h11[5], WAKE1_STAT
- Register 8'h2B[6], WAKE2_STAT
- Register 8'h2B[2], WAKE3_STAT

8.3.11.1 WAKE Pins Alternate Configurations

WAKEx pins can be programmed to provide alternate features. When these pins are configured for the alternate functionality, the local wake up functionality is not available.

8.3.11.1.1 V_{BAT} monitoring

WAKE1 and WAKE2 have an internal switch between them that allows a V_{BAT} monitoring capability. This is accomplished by programming the WAKE_PIN_CONFIG1 register 8'h11[4] WAKE_VBAT_MON to 1b = On, see Figure 8-14. This closes the switch and disables WAKE1 and WAKE2 functionality. Refer to Table 9-1 for the values of $R_{WK\text{-}BAT}$ and the resistors R_{DIV1} and R_{DIV2}.

The WAKE1 and WAKE2 pins are capable of working with voltages up to 40V, which allows a high enough voltage onto the WAKE2 pin that the processor pin connected to the WAKE2 pin can be damaged. To avoid this, the OVHSS parameter can be used to turn off the switch. The WAKE1_SENSE bit at WAKE_PIN_CONFIG2 register 8'h12[6] is a dual function register bit. When WAKE_VBAT_MON = 0b the WAKE1_SENSE bit determines whether WAKE1 pin is a static wake input or cyclic wake input. When WAKE_VBAT_MON = 1b the WAKE1_SENSE bit becomes OV_WAKE12SW_DIS. When OV_WAKE12SW_DIS = 0b, the TCAN285x-Q1 turns off the switch between WAKE1 and WAKE2 when VHSS reaches the OVHSS limit.

Refer to Table 9-1 for the recommended values of external components

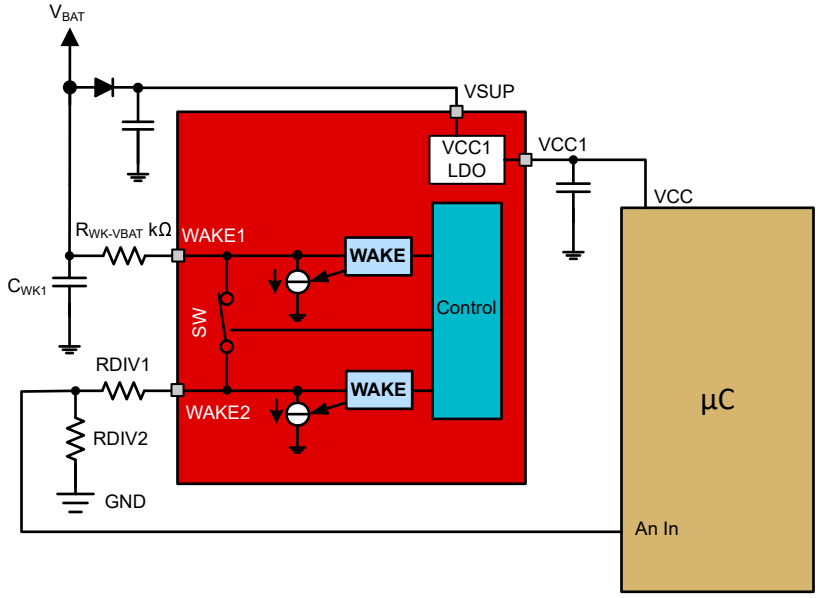


Figure 8-14. V_{BAT} Monitoring Circuit

8.3.11.1.2 Direct Drive

WAKE3/DIR pin can be programmed to directly control any or all of the high-side switches, HSSx, see Figure 8-15. This is accomplished by programming the HSS_CNTLx registers at 8'h1E and 8'h4D to 1000b = Direct Drive pin control for each selected HSSx. This disables the WAKE3 functionality. When using direct drive, there is an enable and disable time based upon the edge change on the WAKE3/DIR pin. This is a power savings feature and shown in Figure 8-16.

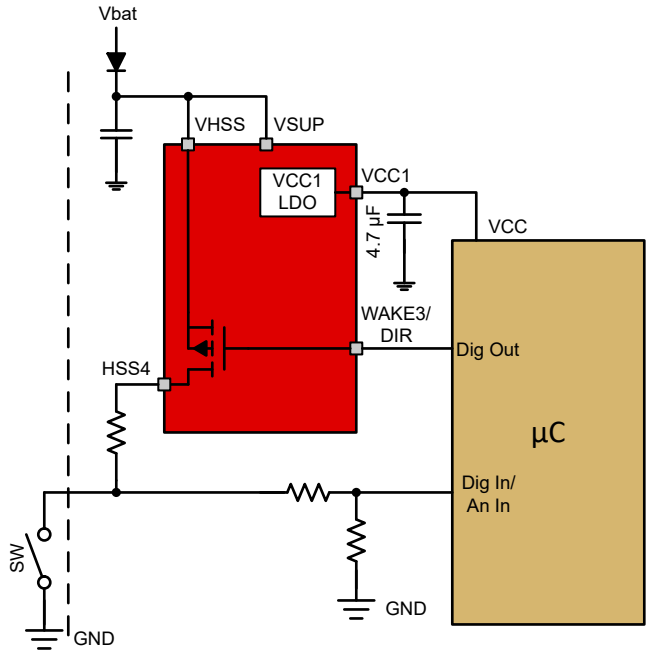


Figure 8-15. HSS4 Direct Drive Example

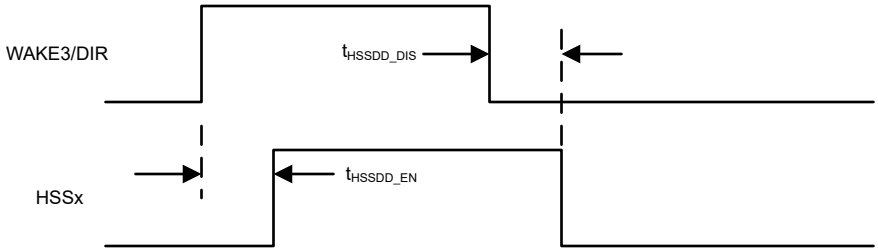


Figure 8-16. Direct Drive Enable and Disable Timing

8.3.12 SDO Pin

The SPI data output (SDO) function provides the requested data from the device to the processor. Upon nCS state changing states to low, the global interrupts information is placed SDO.

8.3.13 nCS Pin

The nCS pin is the SPI chip select pin. When pulled low and a clock is present, the device can be written to or read from.

8.3.14 SCK Pin

The SCK pin is the SPI clock to the TCAN285x-Q1. The SCK pin has both an internal pull-up and pull-down resistor. The resistor is selected based upon the SPI mode configuration. When mode 0 or 1 are selected, the resistor is a pull-down. When mode 2 or 3 is selected, the resistor is a pull-up.

8.3.15 SDI Pin

When nCS is low, this pin is the SPI data input pin used for programming the device or requesting data. The SDI pin has both an internal pull-up and pulldown resistor. The resistor is selected by programming the SDI_POL bit at SPI_CONFIG register 8'h09[2].

8.3.16 Interrupt Function (nINT)

The interrupt block is designed as a push-pull output stage referenced to VCC1 supply. When the TCAN285x-Q1 requires the attention of the processor due to any interrupt-generating event (any unmasked interrupt signalled in the interrupt registers), this pin is pulled low. After the interrupt is cleared the nINT pin is released back to high. A 1ms delay takes place before another interrupt can take place and latch the nINT pin low again. The nINT pin can be configured to toggle instead of being latched low by writing a 1b to nINT_TOG_EN bit at register 8'h1B[0], see Figure 8-17

By default, nINT pin is a global interrupt indicator and is activated for any enabled (unmasked) interrupt in the interrupt registers 8'h51-8'h55, 8'h5A and 8'h5C. If desired, specific interrupts can be masked such that those interrupts do not activate the nINT pin. The interrupts can be masked using the interrupt enable bits in the registers 8'h51-8'h55, 8'h5D and 8'h60. When masked, the interrupt bits are still set in the respective registers but nINT pin does not indicate the masked interrupt.

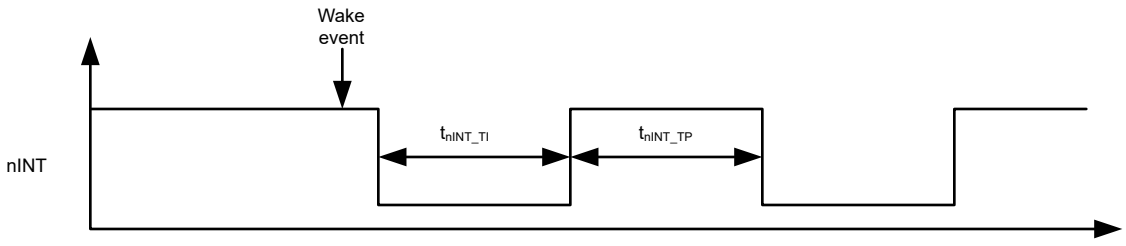


Figure 8-17. nINT Toggling Timing

All interrupts are stored in the respective interrupt registers until cleared by writing 1b (W1C) using SPI.

8.3.17 SW Pin

During debug or development this pin can be used to disable the watchdog actions. When the pin is active, the device expects normal WD triggers, but ignores any mode changes or actions outside of setting the watchdog failure interrupt flag and incrementing and decrementing the watchdog counter. When the pin is released, the flags self-clears, and the watchdog counter either goes back to default or programmed value. The pin is default active high but can be configured active low by using register 8'h0E[0] = 0b.

When the device is in sleep or fail-safe mode, this pin can be used as a digital wake up pin by enabling this feature using register 8'h0E[1] = 1b and 8'h0E[2] = 1b. When the device wakes up due to a SW pin state change, SWPIN interrupt at 8'h51[1] is set. If VCC1 is present in sleep mode, the thresholds are based on VCC1 levels. If VCC1 is not present, the levels are based off an internal voltage rail, $V_{IHSWINT}$ and $V_{ILSWINT}$. This pin can then be used to wake up when an external CAN FD or LIN transceiver is wake capable or MCU to wake up the device. This can be accomplished in several ways. If the external transceiver has an inhibit pin, external circuitry can be used to provide a wake input to this pin. The processor can connect directly to this pin and initiate the wake up without using a SPI command.

Figure 8-18 provides a state diagram on how the SW pin behaves.

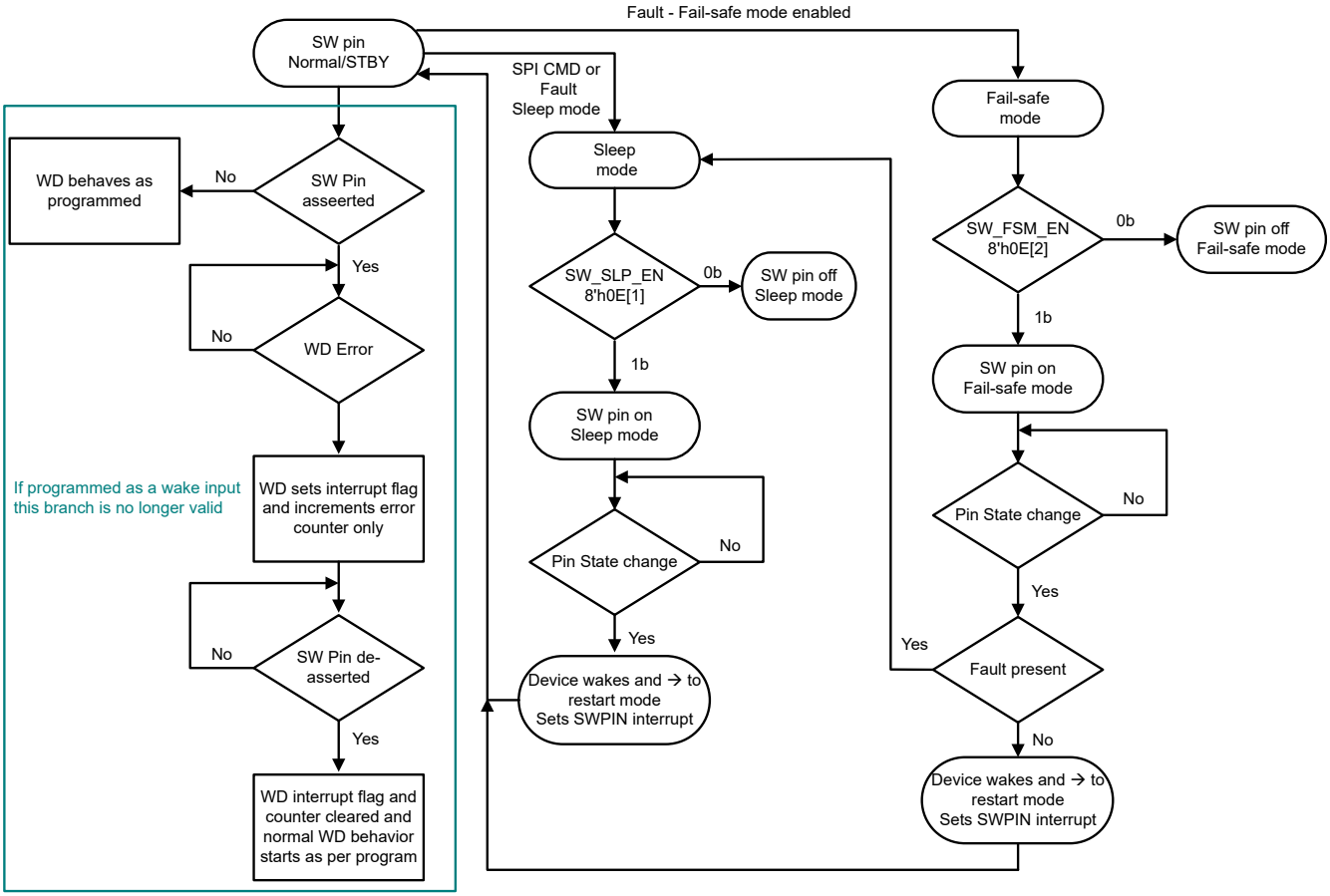


Figure 8-18. SW Pin State Diagram

Note

- The SW pin has a filter timer that the state change has to be at least t_{SW} = 140µs
- The pullup and pulldown resistor is self-configured based upon register 8'h0E[0] setting. Active high means pull-down active, active low means pull-up active.
- If the device is powered up with the SW pin connected high, the device treats this as no watchdog actions to take place.

8.3.18 GFO Pin

This pin is can be programmed to provide certain information back to the processor. These can be considered interrupts such as a UVCC1 or watchdog failures. The pin can be configured to state which wake event has taken place, bus or local via WAKE pin. Configurable to indicate device has entered fail-safe mode.

Pin can also be configured to act as an enable pin to control an external LIN or CAN transceiver. This is accomplished by configuring the pin to support the correct polarity and then programming the external device mode.

8.4 Device Functional Modes

The TCAN285x-Q1 has several SBC operating modes: normal, standby, sleep, restart and fail-safe. The first three mode selections are made by the SPI register, 8'h10[2:0]. Fail-safe mode if enabled is entered due to various fault conditions. The CAN FD and LIN transceivers are independently controlled. The TCAN285x-Q1 automatically goes from sleep to restart, and then to standby mode when receiving a WUP or LUP event. When selective wake is enabled, the device looks for a WUF and if not received the TCAN2855-Q1 and TCAN2857-Q1 remains in sleep mode. See Table 8-6 for the various modes and what parts of the device are active during each mode.

Table 8-6. Mode Overview

Block	Restart	Sleep	Standby	Normal	Fail-safe
nINT	High (VCC1 present) off others	High (VCC1 present) High-Z others	Active	Active	High-Z
GFO	Programmed active state (VCC1 present) off others	Programmed active state (VCC1 present); High-Z (VCC1 Off)	Active	Active	High-Z
SW	Off	Wake capable/Off	Active	Active	Wake capable/Off
HSSx	Off	Off (default); HSS4 can be on if WAKE pins setup for cyclic sensing; Any of the HSSx can be configured for direct drive	As Programmed	As Programmed	Off - HSS4 can be on if WAKE pins setup for cyclic sensing
LIMP (Open-drain active low)	Same as previous state: Low from fail-safe mode or from WD error	Previous state prior to entering sleep mode	Previous state prior to entering STBY	Previous state prior to entering normal mode	Low
WAKEx	Off	As Programmed	As Programmed	Off	Active
CRXD	High (VCC1 present)	High (VCC1 present); High-Z (VCC1 off)	Transceiver configuration dependent	Transceiver configuration dependent	High-Z
LRXD	High (VCC1 present)	High (VCC1 present); High-Z (VCC1 off)	Transceiver configuration dependent	Transceiver configuration dependent	High-Z
nRST	Low	Low (VCC1 off); High (VCC1 ON)	High	High	Off
SPI	Off	Active if VCC1 present	Active	Active	Off
Watchdog	Off	Off but can be programmed on with VCC1 present	Default on with long first pulse but programmable off	Active	Off

Table 8-6. Mode Overview (continued)

Block	Restart	Sleep	Standby	Normal	Fail-safe
Low Power CAN RX	Default on for Wake capable	Default on for Wake capable	On if Wake capable	On if Wake capable	Default on for Wake capable
CAN Transceiver	Off	Off	Programmable - Receiver only	Programmable	Off
Low Power LIN RX	Default on for Wake capable	Default on for Wake capable	On if Wake capable	On if Wake capable	Default on for Wake capable
LIN Transceiver	Off	Off	Programmable - Receiver only	Programmable	Off
LIN Bus Termination	Weak current pull-up	Weak current pull-up	35kΩ (typical)	35kΩ (typical)	Weak current pull-up
VCC1	Ramping	Off (default); programmable on	On	On	Off
VCC2	Ramping	Off (default); programmable on	On (default); programmable off	On (default); programmable off	Off
VEXCC	Ramping after initial configuration	Off (default); programmable on	Programmable	Programmable	Off

Note

When VCC1 is programmed on in sleep mode:

- nINT is high unless an interrupt takes place.
- GFO state is as programmed and can change state depending upon GFO pin programmed definition.
- CRXD and LRXD is high unless a wake event on bus takes place at which time these pins behave as programmed for a wake event.
- Watchdog can be programmed for timeout and if a watchdog failure takes place, the device transitions to restart mode.

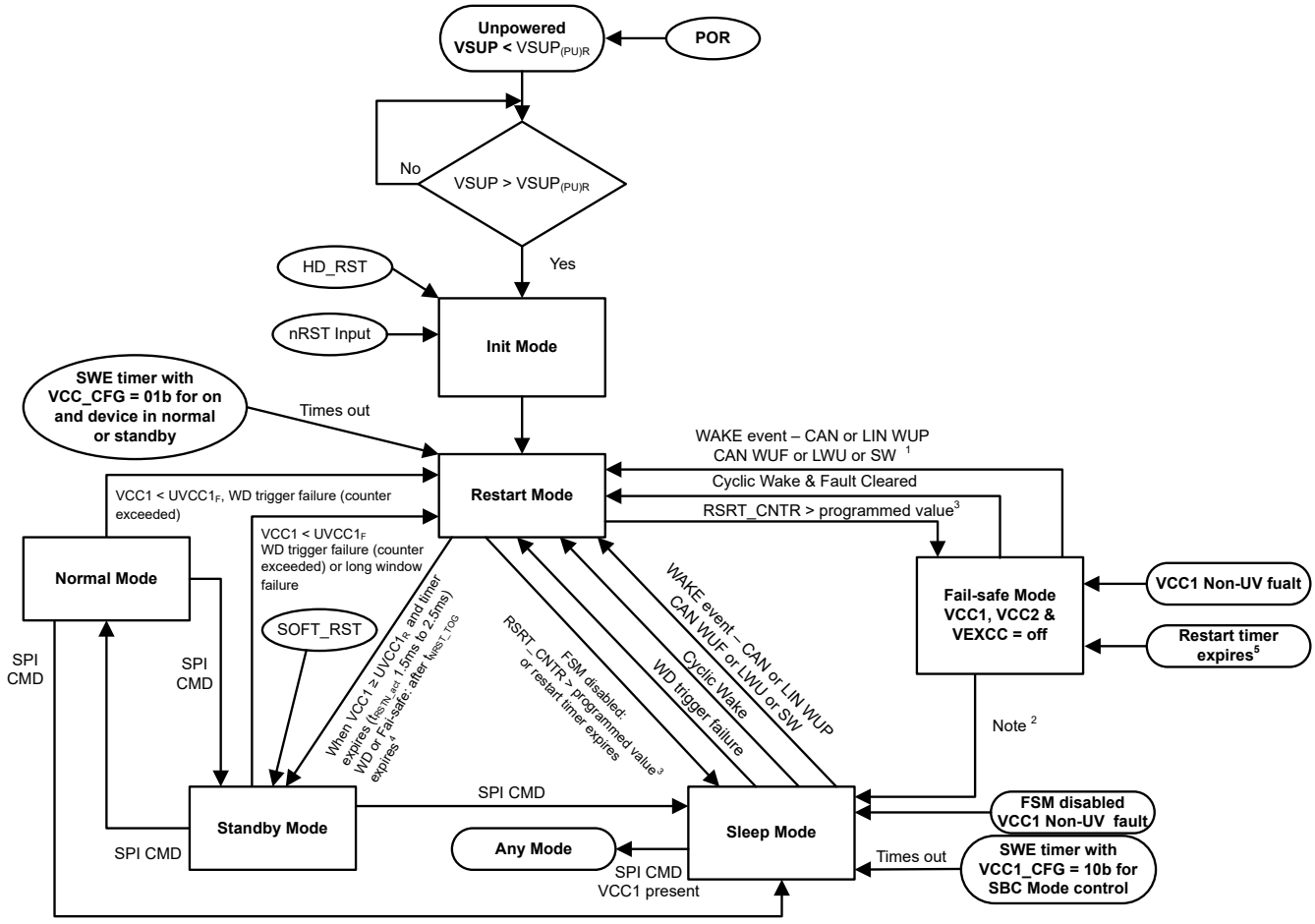


Figure 8-19. Device State Diagram

Note

Device state diagram figure notes

1. To exit fail-safe mode, the fault must be cleared and a wake event takes place
   - The exception to this is when fail-safe mode is entered due to a TSD event
2. If enabled, the SWE timer starts upon entering fail-safe mode and if timer times out the device transitions to sleep mode regardless of VCC1 configuration
3. Restart counter increments when entered from Normal or Standby modes
4. Exiting Restart mode to standby mode can take place due to these two actions
   - VCC1 must be > $UVCC1_R$
   - WD failure or FSM cause the device to enter Restart mode, pulling nRST low for t_{NRST_TOG}, and then transitions to standby mode releasing nRST
5. The restart timer can be configured to support either t_{RSTTO} or $t_{INACTIVE}$ (SWE) timers by configuring RSTRT_TMR_SEL at 8'h4F[0]; which determine the maximum allowed time that the device is in restart mode before exiting to fail-safe or sleep mode due to a fault. If the SWE timer is selected, the timer must be enabled.

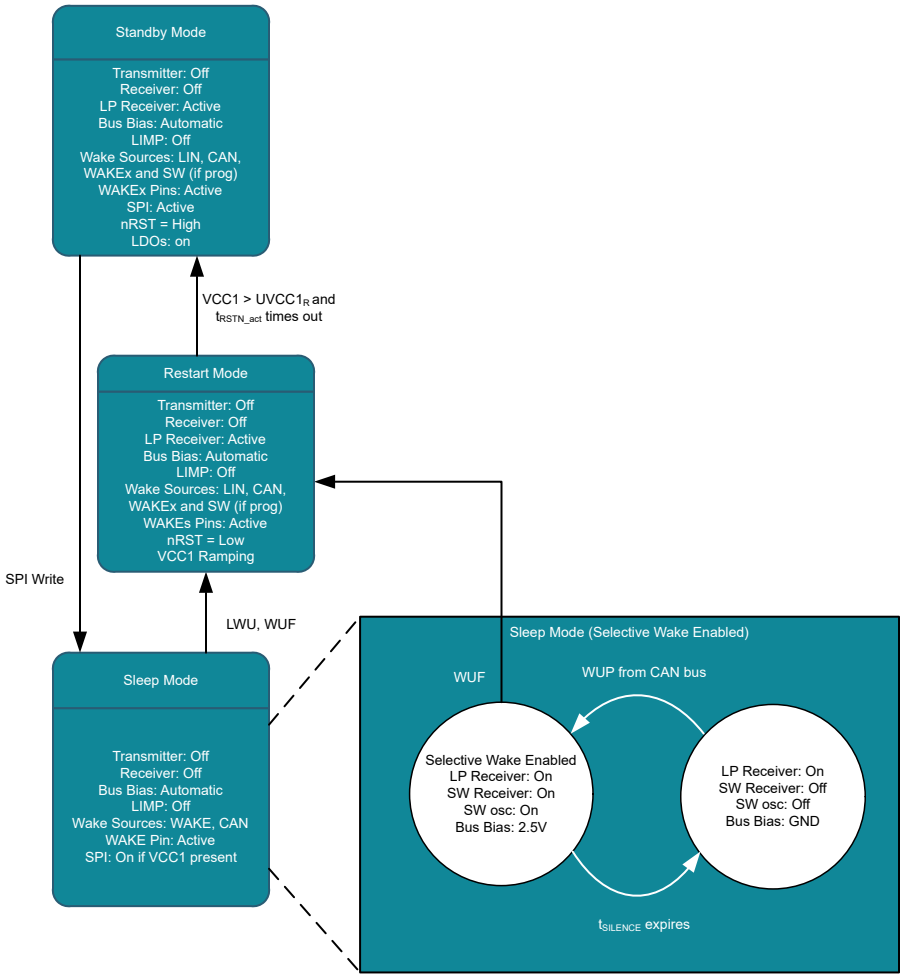


Figure 8-20. Selective Wake Enabled Sleep Mode

Note

For the state diagrams by default, SPI is off in sleep mode. SPI can be configured to work in sleep mode which includes selective wake sub state as shown in Figure 8-20.

8.4.1 Init Mode

This is the initial mode of operation upon powering up. This is a transitional mode that is entered once VSUP is above $VSUP_{(PU)R}$ threshold. The device transitions to restart mode once the device defaults are set.

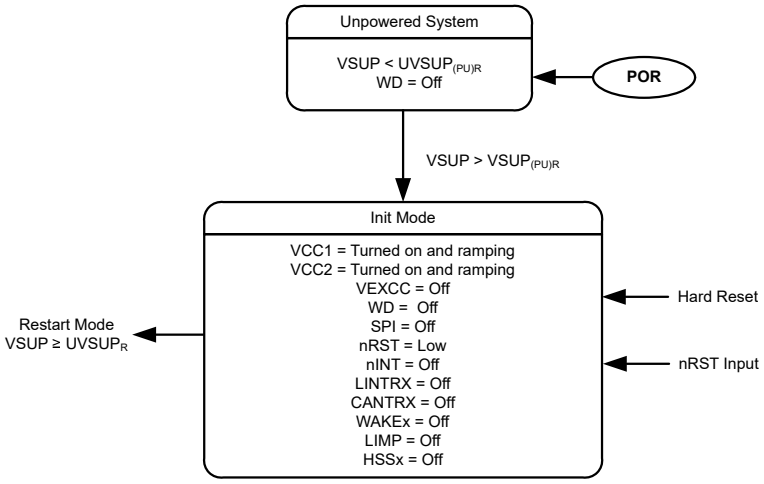


Figure 8-21. Init Mode

8.4.2 Normal Mode

In normal mode, the CAN FD transceiver can be configured as on, listen, wake capable or off. The LIN transceiver can be configured as on, fast, listen, wake capable or off. The transmitters are translating digital inputs on the LTXD and CTXD signals from the controller to LIN and or CAN signals on the bus. The receivers are translating signals from the bus to a digital output on the LRXD and CRXD to the processor. Normal mode is entered by a SPI command and does not change the programmed configuration of the transceivers.

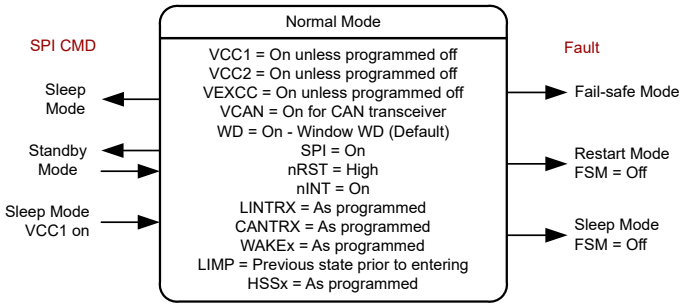


Figure 8-22. Normal Mode

8.4.3 Standby Mode

The device automatically enters standby mode from restart mode. Upon initial power up, this transition happens when VCC1 > UVCC1 and t_{RSTN_act} time has expired. VCC2 is turned on at power up but is not required to by greater than UVCC2 to transition to standby mode. The device can enter standby mode by writing a 00b to register 8'h0B[7:6] from normal mode. The watchdog function is default on in standby mode. Standby mode only supports timeout watchdog and automatically changes to this when entered. When WD_STBY_DIS, register 8'h14[0] = 0b (default value) entrance to standby mode has a long timeout window, t_{INITWD}, that a WD trigger event must take place when entered from restart mode. The watchdog can be disabled for standby mode by setting 8'h14[0] = 1b. In standby mode, the transceiver can be programmed to meet the applications requirements. There are several blocks that are active in this mode. In standby mode, the CAN FD transceiver can be configured as listen, wake capable or off. The LIN transceiver can be configured as listen, wake capable or off. If programmed as wake capable, the low power CAN and LIN receivers are actively monitoring the bus for the wake up pattern (WUP). The WAKEx pins monitor is active. The SPI is active so that the microprocessor can read and write registers in the memory for status and configuration. The device goes from sleep mode to restart mode to standby mode automatically upon a bus WUP event, WUF (if selective wake is enabled), or a local wake up from the WAKEx pins and when VCC1 > $UVCC1_R$. If VCC1 is disabled, the device enters standby mode after t_{RSTN_act} timer times out.

Upon entering standby mode, the SWE timer (if enabled), $t_{INACTIVE}$, starts and any SPI command from the processor clears the SWE timer. This feature makes sure the node is in the lowest power mode if the processor does not come up properly. To enable this feature register 8'h1C[7] (SWE_EN) must be set to 1b.

The following provides the description on how selective wake interacts between sleep and standby modes.

- At power up, the device is in standby. Clear all Wake flags (PWRON, WUP/LWU), configure the Selective Wake registers, and then set selective wake config (SWCFG = 1) and selective wake enable (SW_EN = 1).
- When SWCFG = 1 and the device is placed into sleep mode the low power WUP receiver is active and waiting for a WUP.
- Once a WUP is received the WUF receiver is active.
- The device receives the wake-up frame and determine if the frame is the node requested to wake up.
  - If the WUF address is correct, the device wakes up the node entering standby mode.
  - If the WUF is not address is incorrect, the device stays in sleep mode.
- A wake interrupt occurs from any type – WUF (CANINT), FRAME_OVF or LWU (if enabled), the device enters standby mode.

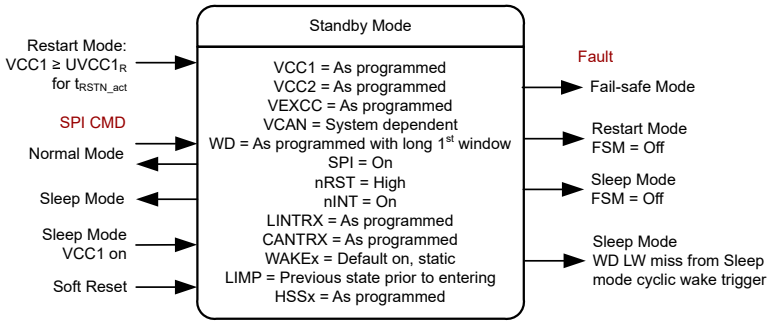


Figure 8-23. Standby Mode

8.4.4 Restart Mode

Restart mode is a transitional mode. This mode can be entered from any of the other modes depending upon whether fail-safe mode is disabled. In this mode the enabled LDOs are ramping or are on. At initial power up, once VCC1 ≥ $UVCC1_R$ for t_{RSTN_act} (approximately 2ms), the device transitions to standby mode. While in restart mode, nRST is latched low. When restart mode is entered, a restart timer is started. This timer can be selected between t_{RSTTO} and $t_{INACTIVE}$ (SWE) timer time by programming register 8'h4F[0], RSTRT_TMR_SEL. The default is t_{RSTTO}. If $t_{INACTIVE}$ (SWE) timer is selected, the SWE timer needs to be enabled be setting SWE_EN = 1b at SWE_TIMER register 8'h1C[7]. If the device has not exited restart mode prior to the timer timing out, the device transitions to fail-safe mode if enabled or sleep mode if fail-safe mode is disabled. Each time restart mode is entered from normal or standby modes, the restart mode counter, RSRT_CNTR, is incremented. The exception to this is if exceeding the restart counter caused the device to enter fail-safe or sleep mode. When re-entering restart mode due to this event, the counter is ignored and device enters standby mode. Once in standby mode, the counter must be cleared. This counter is programmable from register 8'h28[7:4], which sets the number of times restart can be entered before transitioning to sleep or fail-safe mode, up to 15 times. The default value is 4. Register 8'h16[3:0] is RSRT_CNTR. The counter can be disabled by programming the counter to 0000b. To prevent the transition to sleep or fail-safe mode, the counter must be cleared periodically.

Note

If the restart counter is disabled, configured to 0000b, a loop from restart to standby back to restart is possible due to a constant watchdog failure.

The nRST output pin behavior depends upon the reason the device entered restart mode.

When entered due a watchdog failure, from fail-safe mode or an external nRST toggle, the nRST pin is pulled low for t_{NRST_TOG} which defaults to 20ms. This pulse width can be configured to 2ms by changing register

8'h29[5] = 0. After this time, the device transitions to standby mode and release nRST pin to high. See Figure 8-25 on how restart mode is entered and exited after Watchdog failure.

When restart mode is entered from sleep mode or due to an under-voltage event, the device latches nRST low until VCC1 > $UVCC1_R$ for t_{RSTN_act}, and then transitions to standby mode and release nRST high. See Figure 8-24 on how restart mode is entered and exited.

The nRST pin is also reset input pin of the TCAN285x-Q1 which transitions the device into restart mode when the pin is pulled low for t_{nRSTIN}, see Figure 8-25

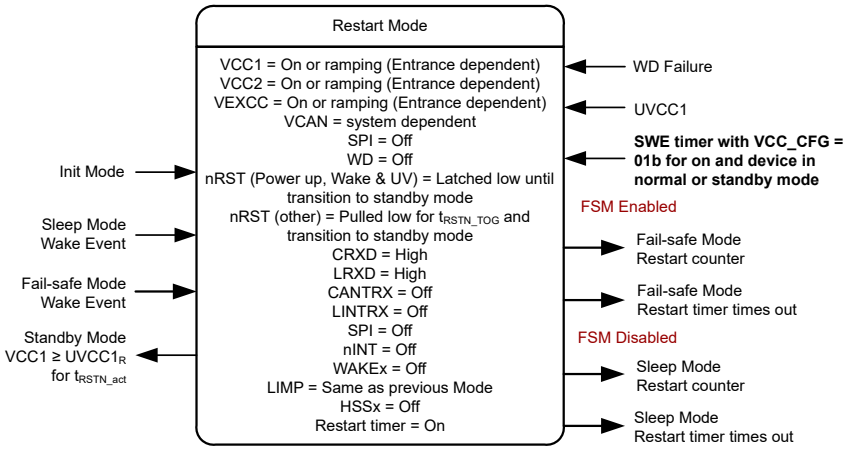


Figure 8-24. Restart Mode

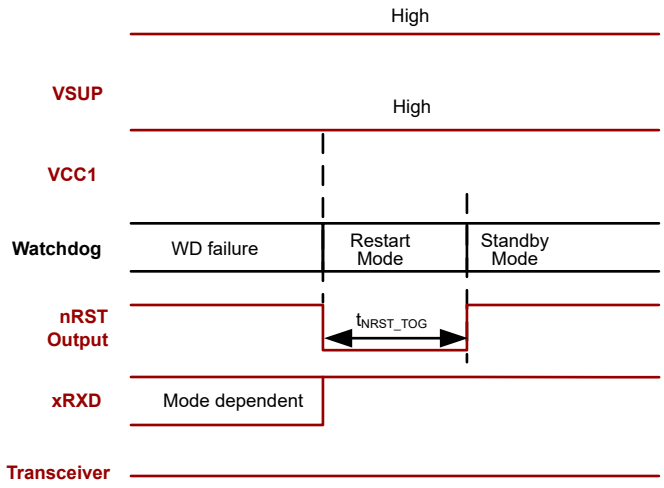


Figure 8-25. WD Failure to Restart Timing Diagram

8.4.5 Fail-safe Mode

The device has a fail-safe mode, default on, which is entered when certain fault events take place. When fail-safe mode is entered, a global interrupt is issued and the sleep wake error (SWE) timer, $t_{INACTIVE}$, if enabled starts and VCC1, VCC2 and VEXCC are turned off. The reason for entering fail-safe mode is provided by register 8'h17[3:1] and expanded further with other interrupt flags. This mode can be disabled by using register 8'h17[0], but the recommendation is to stay enabled as fault monitoring is active in fail-safe mode and not sleep mode. This mode turns on LIMP and brings other functions into lower power mode states. When entering fail-safe mode the LDOs are kept off for at least t_{LDOOFF}, approximately 300ms. During this time wake events are monitored and preserved. After t_{LDOOFF} times out wake events causes the device to transition to restart mode. If enabled and the SWE timer times out prior to faults being cleared and a wake event taking place, the device transitions to sleep mode. Figure 8-26 shows the various fault conditions that causes the device to enter fail-safe

mode. If the fault conditions are cleared and a wake event takes place, the device transitions to restart mode. Figure 8-27 provides a high level flow chart for fail-safe mode.

A fail-safe mode counter is available allowing a set number of fail-safe events in a row which then causes the device to perform the programmed action which can include going to sleep where a WUP, WUF or LWU event does not wake the device. A power on reset is required. The counter is default disabled and can be enabled at 8'h17[7:4] ≠ 0000b. The counter expiration action is at 8'h17[7:4]. The number of events before action is programmed is set at 8'h18[7:4] with a value up to 16 events. 8'h18[3:0] is the running up/down fail-safe event counter that can be read and cleared.

There are multiple ways to exit fail-safe mode depending upon the fault and programmed configuration.

- By default, the SWE timer is disabled. When enabled these are the transition paths out of fail-safe mode.
  - A wake event and cleared fault sends the device into restart mode.
  - If enabled, the SWE timer timing out causes the device to transition to sleep mode, and VCC1 remains off even if VCC1_CFG = 01b is on.
  - If FSM_CYC_WK_EN, 8'h1A[0] = 1b, the device wakes up during the on time of the selected timer and check to see if the fault has cleared. If so, the device transitions to restart mode.

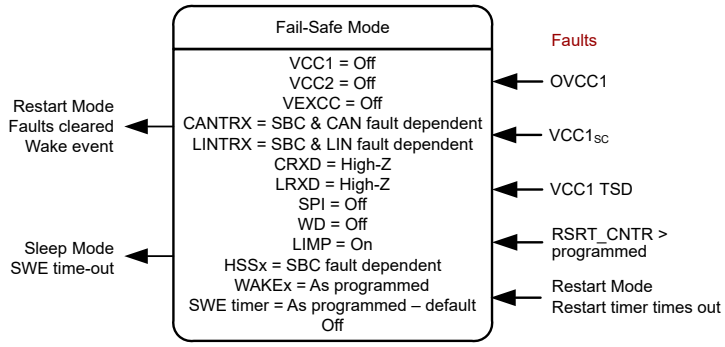


Figure 8-26. Fail-safe Mode

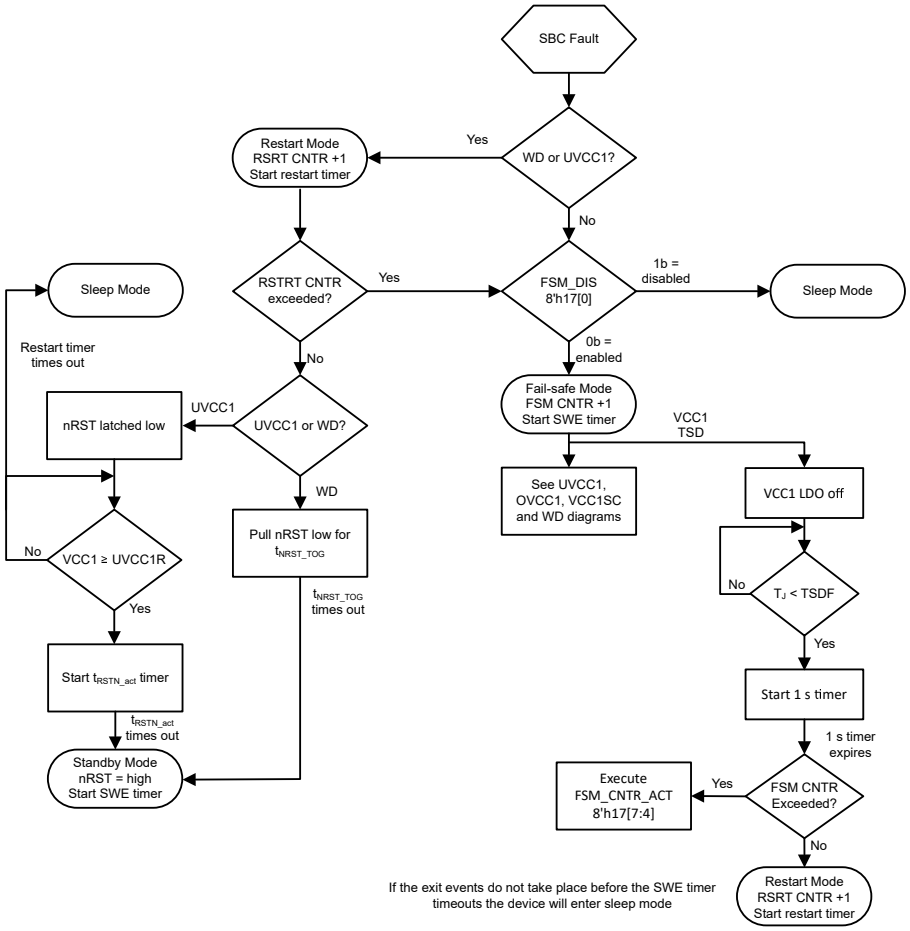


Figure 8-27. Fail-safe mode flow chart

Note

For the device to enter fail-safe mode, there has to be a method for the device to wake up. This can be by the communication bus or a WAKE pin. If these are all disabled for fail-safe mode, the device automatically makes the CAN FD and LIN transceivers wake capable.

When the device enters fail-safe mode, the SWE timer automatically starts, if enabled.

- If SWE timer times out the device enters sleep mode
- If a wake event takes place prior to the SWE timer timing out, the device determines if fault is still present.
  - If fault is present the device stays in fail-safe mode monitoring the fault.
  - If fault has cleared the device enters restart mode.

When fail-safe mode is entered due to any condition other than TSD the following takes place.

- The VCC1 LDO is turned off. If the fault impacts load sharing; both are turned off. If the device receives a wake event, the LDO is turned on for t_{LDOON} to determine if the short circuit event is still present.
  - At the end of t_{LDOON}, if a short circuit is detected the device turns off the LDO and wait for next wake event.
- Over-voltage is continuously monitored immediately enters sleep mode.
- If fault is cleared the device enters restart mode.

8.4.5.1 SBC Faults

SBC faults are faults that cause the device to change the mode of the device. If fail-safe mode is enabled, these faults cause the device to enter either restart or fail-safe mode. If fail-safe mode is disabled, the faults causes the device to enter either restart or sleep mode. SBC Faults are:

- Over-voltage for VCC1
- Under-voltage for VCC1
- Short circuit on VCC1
- Thermal Shutdown due to VCC1
- Watchdog failure
- Restart counter exceeds programmed value
- If enabled, SWE timer expires
- Under-voltage on VSUP is an SBC fault, but does not cause the device to enter fail-safe mode

8.4.5.2 CAN Transceiver Faults

CAN transceiver faults are ones that impact the transceiver and do not cause the device to enter fail-safe mode, but does turn off the CAN transmitter. CAN Transceiver Faults:

- VCC2 thermal shutdown
- CAN transceiver thermal shutdown
- CTXD pin stuck dominant - CTXD dominant timeout
- UVCAN

Note

If VCC2 is connected to VCAN, faults on VCC2 can cause a CAN fault.

8.4.5.3 LIN Transceiver Faults (TCAN2857-Q1)

LIN transceiver faults are ones that impact the transceiver, and do not cause the device to enter fail-safe mode. The faults include dominant state timeout and thermal shut down.

8.4.6 Sleep Mode

Sleep mode is the power saving mode for the device. In this mode, the device can wake up from the CAN bus, LIN bus, WAKEx pins or SW pin (if programmed). If VCC1 is present, SPI is available to change modes and nRST is high. If sleep mode is entered due to a fault condition, INT_2 register 8'h52[7] (SMS) is set to 1b. Figure 8-28 shows the various ways that sleep mode is entered and exited.

While the device is in sleep mode, the following conditions exist.

- The LIN bus driver is disabled and the internal LIN bus termination is switched off (to minimize power loss if LIN is short circuited to ground). However, the weak current pull-up is active to prevent false wake up events in case an external connection to the LIN bus is lost.
- The CAN bus driver is disabled and the internal CAN bus termination is switched to a weak ground.
- The CAN and LIN transceiver receivers are disabled.
- The CAN and LIN low power wake up receivers are as programmed.
- WAKE pins are as programmed.
- If cyclic sensing is enabled, HSS4 periodically turns on.
- If programmed as a digital wake input, the SW pin is on.
- If cyclic wake is enabled in sleep mode, the device wakes and transitions to restart mode and then standby mode once VCC1 > $UVCC1_R$. If a watchdog trigger does not take place during the long window or the fault is still present, the device transitions back to sleep mode.
- When VCC1 is configured on for sleep mode, consider the following:
  - The watchdog can be enabled as a timeout watchdog
  - A watchdog fault causes the device to enter restart mode and finally to standby mode. This also sets the SME interrupt

  - SBC faults are now monitored that can cause the device to change modes automatically which sets the sleep mode exit (SME) interrupt at INT_2 register 8'h52[0] is set to 1b
    - If Fail-safe mode is enabled, a TSD, OVCC1 or VCC1SC fault causes the device to transition to Fail-safe mode and turn off VCC1.
    - If Fail-safe mode is disabled, a TSD, OVCC1 or VCC1SC fault causes VCC1 to turn off for 300ms, and then turn back on. If the fault has cleared, the device transitions to restart and finally to standby mode.
  - If a UVCC1 event takes place, the device transitions to restart mode and finally to standby mode. This also sets the SME interrupt.

To enter sleep mode successfully, following conditions have to be met:

- All existing wake interrupts have to be cleared
  - Failure to do so results in an immediate wake-up from SBC Sleep Mode by going using SBC Restart to Standby Mode.
- At least one method to wake up has to be available
  - If all wake methods are disabled before entering Sleep mode, the device does not enter sleep mode and sets a MODE_ERR interrupt, 8'h5A[3].
  - If VCC1_CFG=10b (VCC1 is off in Sleep mode) and WAKEx pin threshold is set to be VCC1 based (WAKEx_LEVEL =00b), the device sets CAN and LIN to be wake capable before entering Sleep mode

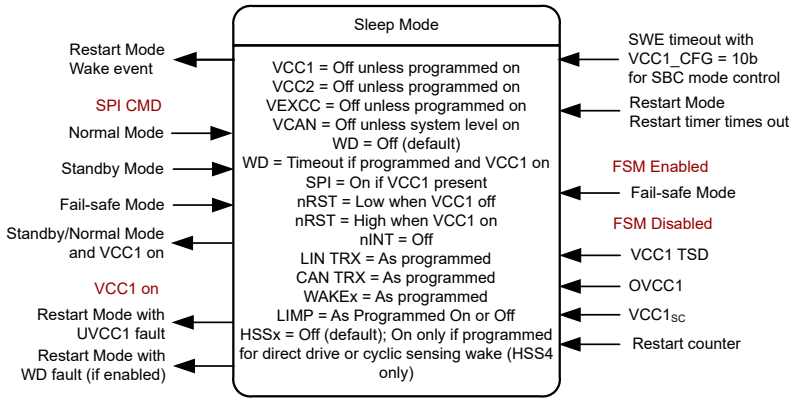


Figure 8-28. Sleep Mode

8.4.7 Wake Functions

There are multiple ways to wake up from sleep mode.

- CAN bus wake using BWRR
- CAN bus wake using selective wake
- LIN bus wake (TCAN2857Q1)
- Local wake up through the WAKEx pins
- SW pin if programmed as a digital wake input
- Cyclic wake enabled for sleep mode

Note

- A wake event that takes place prior to the device going to sleep is treated as a wake event. Preventing the device from entering sleep mode.
- When VCC1 is off in sleep mode, for a wake event, the device to follow the normal wake flow
- When VCC1 is on in sleep mode, for a wake event, the device sets an interrupt, pull RXD low, and perform the programmed VCC1_SLP_ACT at SBC_CONFIG1 register 8'h0E[5]. As SPI is available, changing modes without VCC2 or VEXCC being turned on is possible.
- For a cyclic wake event in Sleep mode, VCC1_SLP_ACT configuration has no effect. The device transitions to Standby mode via Restart mode irrespective of the VCC1_SLP_ACT configuration.

8.4.7.1 CAN Bus Wake Using CRXD Request (BWRR) in Sleep Mode

The TCAN285x-Q1 supports low power sleep and standby modes and uses a wake up from the CAN bus mechanism called bus wake using CRXD Request (BWRR). Once this pattern is received, the TCAN285x-Q1 automatically switches to standby mode from sleep mode and insert an interrupt onto the nINT pin, if enabled, to indicate to a host microprocessor that the bus is active, and the processor wakes up and services the TCAN285x-Q1. The low power receiver and bus monitor are enabled in sleep mode to allow for CRXD Wake Requests using the CAN bus. A wake-up request is output to the CRXD (driven low) as shown in Figure 8-29. The external CAN FD controller monitors CRXD for transitions (high to low) and reactivate the device to normal mode based on the CRXD Wake Request. The CAN bus terminals are weakly pulled to GND during this mode, see Figure 7-2.

This device uses the wake-up pattern (WUP) from ISO 11898-2: 2024 to qualify bus traffic into a request to wake the host microprocessor. The bus wake request is signaled to the integrated CAN FD controller by a falling edge and low corresponding to a “filtered” bus dominant on the CRXD terminal (BWRR).

The wake-up pattern (WUP) consists of

- A filtered dominant bus of at least t_{WK_FILTER} followed by
- A filtered recessive bus time of at least t_{WK_FILTER} followed by
- A second filtered dominant bus time of at least t_{WK_FILTER}
- A second filtered recessive bus time of at least t_{WK_FILTER}

Once the WUP is detected, the device starts issuing wake up requests (BWRR) on the CRXD pin. The behavior of this pin is determined by register 8'h12[2]. If 8'h12[2] = 0b the CRXD pin is pulled low once the WUP pattern has been received that meets the dominant, recessive, dominant filtered times. The first filtered dominant initiates the WUP and the bus monitor is now waiting on a filtered recessive, other bus traffic does not reset the bus monitor. Once a filtered recessive is received, the bus monitor is now waiting on a filtered dominant and again, other bus traffic does not reset the bus monitor. Immediately upon receiving of the second filtered dominant the bus monitor recognizes the WUP and transition to BWRR output. Immediately upon verification receiving a WUP the device transitions the bus monitor into BWRR mode. This is indicated on the CRXD pin by latching the pin low; thus, the CRXD output during BWRR matches the classical 8 pin CAN devices that used the single filtered dominant on the bus as the wake-up request mechanism from ISO 11898-2: 2024.

For a dominant or recessive to be considered “filtered”, the bus must be in that state for more than t_{WK_FILTER} time. Due to variability in the t_{WK_FILTER} the following scenarios are applicable.

- Bus state times less than $t_{WK\_FILTER(MIN)}$ are never detected as part of a WUP; thus, no BWRR is generated.
- Bus state times between $t_{WK\_FILTER(MIN)}$ and $t_{WK\_FILTER(MAX)}$ can be detected as part of a WUP and a BWRR can be generated.
- Bus state times more than $t_{WK\_FILTER(MAX)}$ is always detected as part of a WUP; thus, a BWRR is always generated.

See Figure 8-29 for the timing diagram of the WUP.

The pattern and t_{WK_FILTER} time used for the WUP and BWRR prevents noise and bus stuck dominant faults from causing false wake requests while allowing any CAN or CAN FD message to initiate a BWRR. If the device is switched to normal mode or an under-voltage event occurs on V_{CC}, the BWRR is lost. The WUP pattern must take place within the $t_{WK\_TIMEOUT}$ time; otherwise, the device is in a state waiting for the next recessive and then a valid WUP pattern.

If 8'h12[2] = 1b, the CRXD pin toggles low too high too low for t_{TOGGLE} = 10µS until the device is put into normal mode or listen mode. BWRR is active in standby mode upon power up and once coming out of sleep mode or certain fail-safe mode conditions. If a SPI write puts the device into standby mode, the CRXD pin is high until a wake event takes place. The CRXD pin then behaves as if in sleep mode.

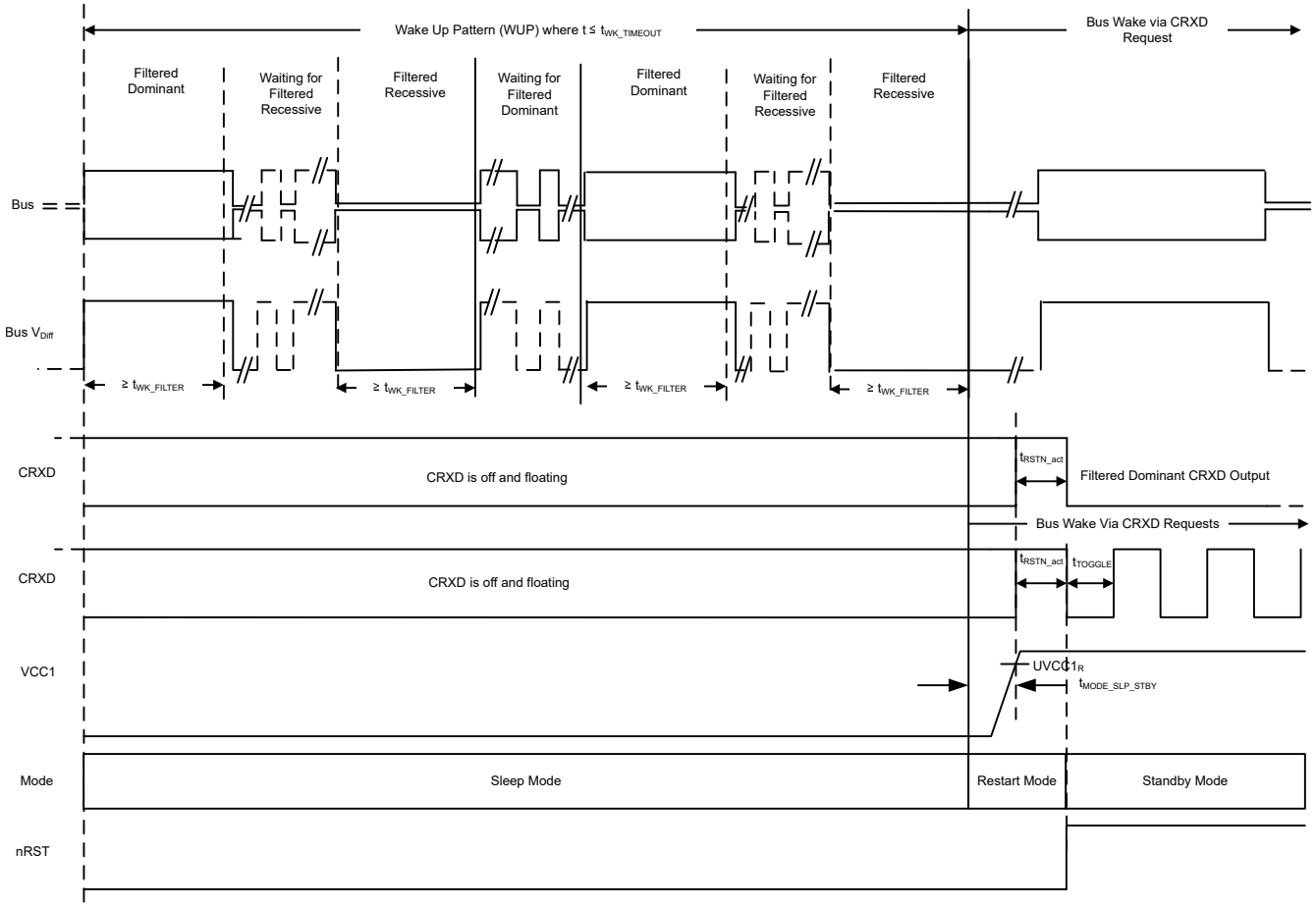


Figure 8-29. Wake Up Pattern (WUP) and Bus Wake Using CRXD Request (BWRR)

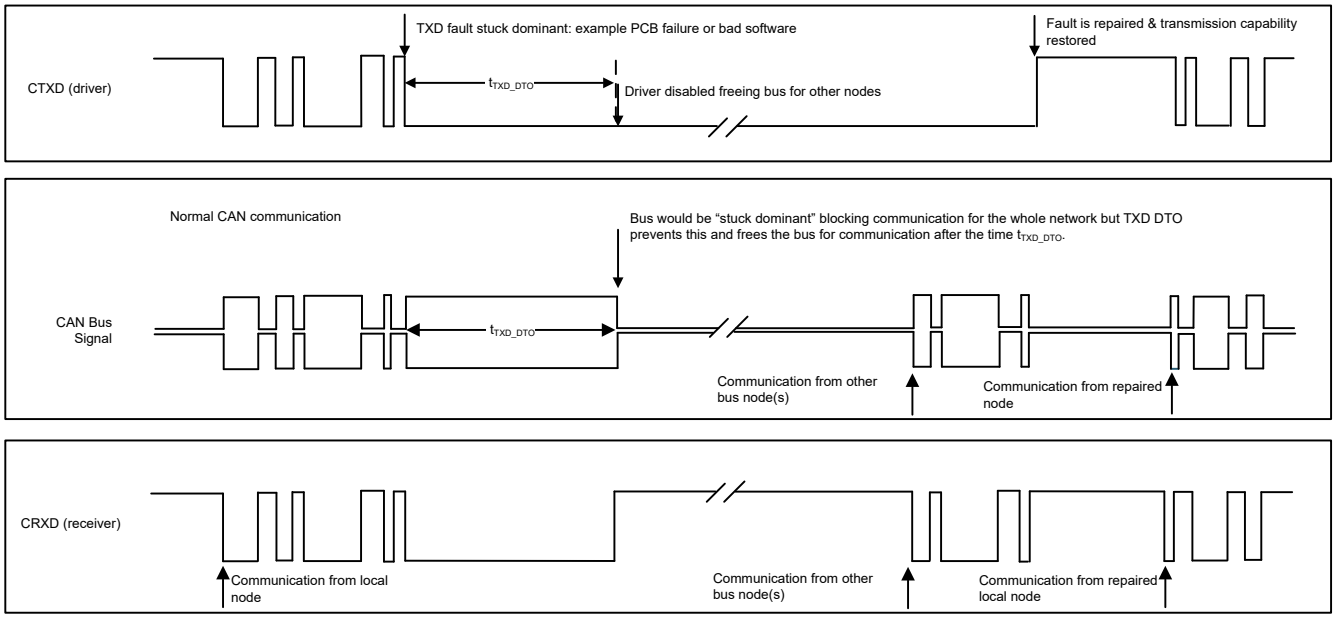


Figure 8-30. Example Timing Diagram With CTXD DTO

Note

CAN wake from WUP signal can be disabled by programming CAN1_TRX_SEL at register 8'h10[2:0] = 010b.

8.4.7.2 LIN Bus Wake

Remote wake up initiated by the falling edge of a recessive (high) to dominant (low) state transition on the LIN bus where the dominant state is held for the t_{LINBUS} filter time. After this t_{LINBUS} filter time has been met and a rising edge on the LIN bus going from dominant state to recessive state initiates a remote wake up event eliminating false wake ups from disturbances on the LIN bus or if the bus is shorted to ground. The LIN bus wake event is indicated by LRXD being pulled low once the device enters standby mode.

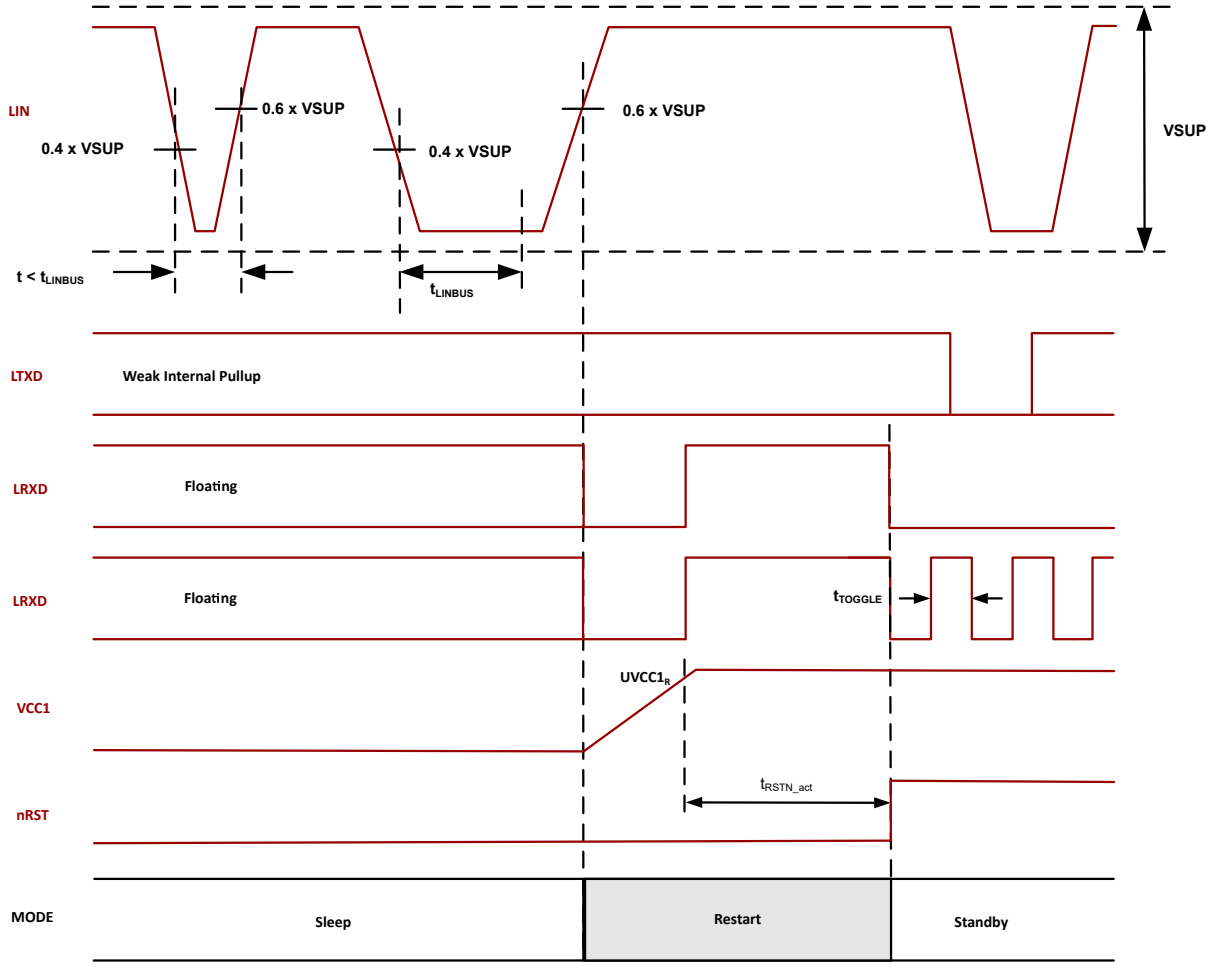


Figure 8-31. LIN bus wake

8.4.7.3 Local Wake Up (LWU) via WAKEx Input Terminal

The WAKEx terminals are a highly configurable ground based, high voltage capable inputs which can be used for local wake up (LWU) request via a voltage transition. There are two methods for this wake event. A static wake based on a level changed on the pin or a timing based, cyclic sensing where the WAKEx pin is periodically turned on and a change during this on time is the trigger event is checked.

The device provides a WAKE pin status change update using reg 2Ah[4:0] showing which WAKE pin has changed states.

There are two methods of using the WAKE pins:

- Static wake

- Cyclic sensing wake

The WAKE pins have a global control for which method a wake takes place, rising edge, falling edge, bi-directional, pulse or filtered pulse. The WAKE pins have programmable thresholds

8.4.7.3.1 Static Wake

The WAKEx pins default to bi-directional input but can be configured for rising edge and falling edge transitions, see Figure 8-32 and Figure 8-33, by using WAKE_CONFIG register 8'h11[7:6]. WAKE pins are ground based wake inputs and can be used with a switch to ground or V_{SUP}. The WAKEx pins input thresholds can be based on VCC1 levels which allows a direct connection to the processor or a switch to the VCC1 rail. If the terminal is not used, connect the terminal to ground to avoid unwanted parasitic wake up. Once the device enters sleep mode, the WAKEx terminals voltage level need to be at either a low state or high state for t_{WAKE} before a state transition for a WAKE input can be determined. A pulse width less than $t_{WAKE\_INVALID}$ is filtered out.

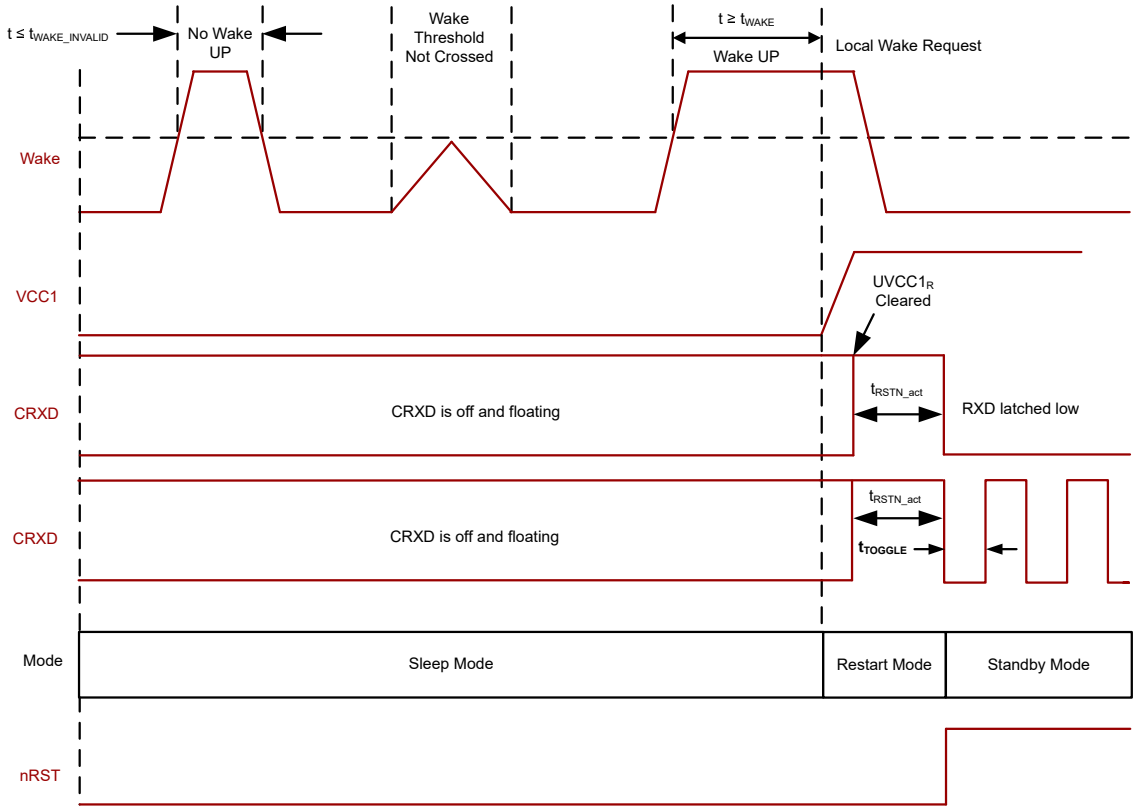


Figure 8-32. Local Wake Up – Rising Edge

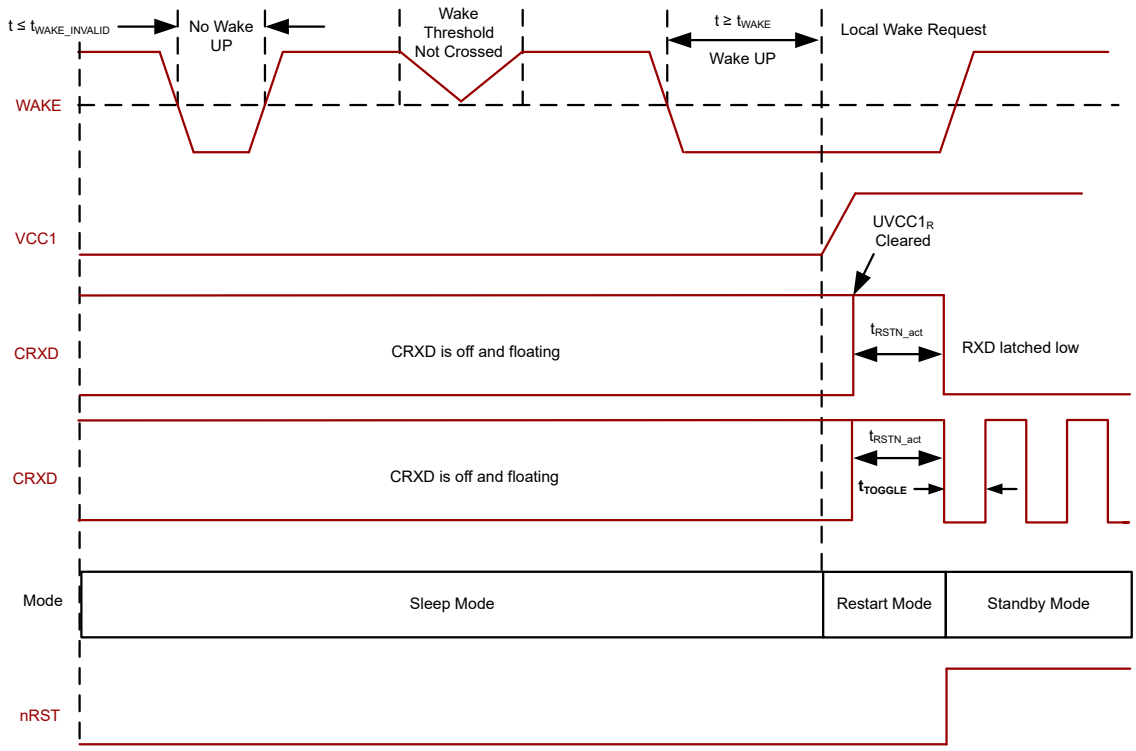


Figure 8-33. Local Wake Up – Falling Edge

Note

When either a rising or falling edge is selected for the WAKE pins the state prior to the edge requires a t_{WAKE} period of time.

- If a rising edge is selected and the device goes to sleep with WAKE high, a low of at least t_{WAKE} must be present prior to the rising edge wake event
- If a falling edge is selected and the device goes to sleep with WAKE low, a high of at least t_{WAKE} must be present prior to the falling edge wake event
- This requirement is not necessary for a bidirectional edge (default)
- Figure 8-32 and Figure 8-33 provide examples of a rising or falling edge WAKE input. RXD is pulled low once VCC1 > UVCC1 and standby mode is entered.

The WAKE terminal can be configured for a pulse, see Figure 8-34, by using WAKE_CONFIG register 8'h11[7:6]. The terminal can be configured to work off a pulse only. The pulse must be between $t_{WK\_WIDTH\_MIN}$ and $t_{WK\_WIDTH\_MAX}$. The figure provides three examples of pulses and whether the device wakes or does not wake. $t_{WK\_WIDTH\_MIN}$ is determined by the value for $t_{WK\_WIDTH\_INVALID}$ is set to in register 8'h11[3:2]. There are two regions where a pulse can be detected. By using register 8'h1B[1], WAKE_WIDTH_MAX_DIS, the pulse mode can be configured as a filtered wake input. Writing a 1 to this bit disables $t_{WK\_WIDTH\_MAX}$. The WAKE input is based upon the configuration of register 8'h11[3:2] which selects a $t_{WK\_WIDTH\_INVALID}$ and $t_{WK\_WIDTH\_MIN}$ value. A WAKE input of less than $t_{WK\_WIDTH\_INVALID}$ is filtered out and if longer than $t_{WK\_WIDTH\_MIN}$ the device enters restart mode and turn on the LDOs. The region between the two is not always counted, see Figure 8-35. Register 8'h12[7] determines the direction of the pulse or filter edge that is recognized. The status of the WAKE pin can be determined from register 8'h11[5:4]. When a WAKE pin change takes place, the device registers a rising edge or falling edge. This is latched until a 00 is written to the bits.

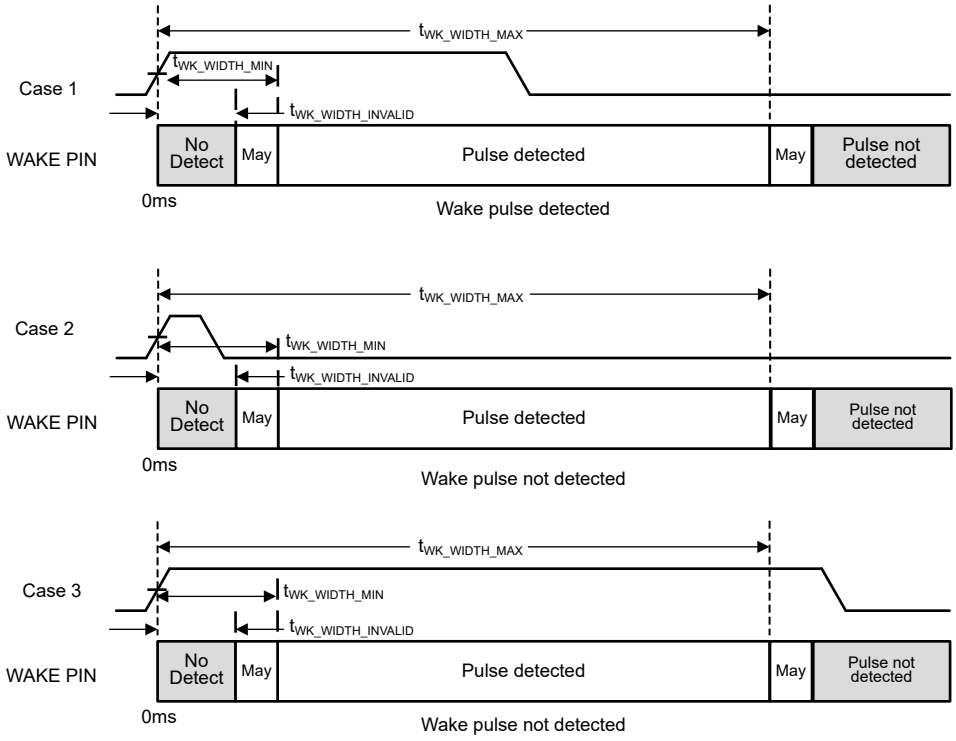


Figure 8-34. WAKE Pin Pulse Behavior

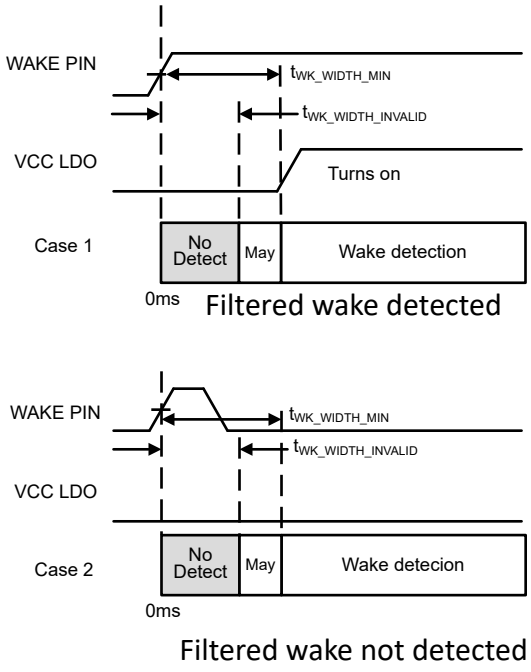


Figure 8-35. WAKE Pin Filtered Behavior

8.4.7.3.2 Cyclic Sensing Wake

When using cyclic sense WAKE, the quiescent current of the device in sleep mode is reduced as the WAKE circuitry is only active during the on time of the selected HSS4 pin, see Figure 8-36. Periodically the HSS4 pin turns on applying VSUP to the external local wake circuitry. Each time, WAKEx sets a bit stating the pin is high or low and compares the bit to the previous state. If there has been a change, the device wakes up;

otherwise, the device remains in sleep mode. See Figure 8-37 for a timing diagram. The wake pin filter time for the sampling window is based upon t_{WK_CYC} as shown in Figure 8-37. To enable cyclic sensing wake in Sleep mode, perform the following configurations before entering the Sleep mode.

- Connect the desired WAKE pins to HSS4 as shown in Figure 8-36
- Set the desired WAKEx pin to cyclic sensing mode
  - WAKE1: h’12[6] WAKE1_SENSE=1b
  - WAKE2: h’2B[7] WAKE2_SENSE=1b
  - WAKE3: h’2B[3] WAKE3_SENSE=1b
- Set the wake pin filter time for the sampling window, if a non-default setting is needed
  - Set the register bit 8'h12[5]
- Set HSS4 to the desired timer using HSS4_CNTL bits
  - h'4D[2:0] = Timer1 or Time2
- Set the selected timer configuration with the desired on-time and period

  (Note: do not set the cyclic wake bit in the timer configuration unless cyclic wake needs to be configured in addition to cyclic sensing wake)

  - Set h'25 for Timer1 period and on-time
  - Set h'26 for Timer2 period and on-time

Cyclic sensing wake is also supported in Standby mode. In Standby mode, the device only sets the corresponding wake pin interrupt. Cyclic sensing wake is not supported in Normal mode. Set the WAKEx_SENSE bit to 0b before entering Normal mode to operate HSS4 in the SBC Normal mode.

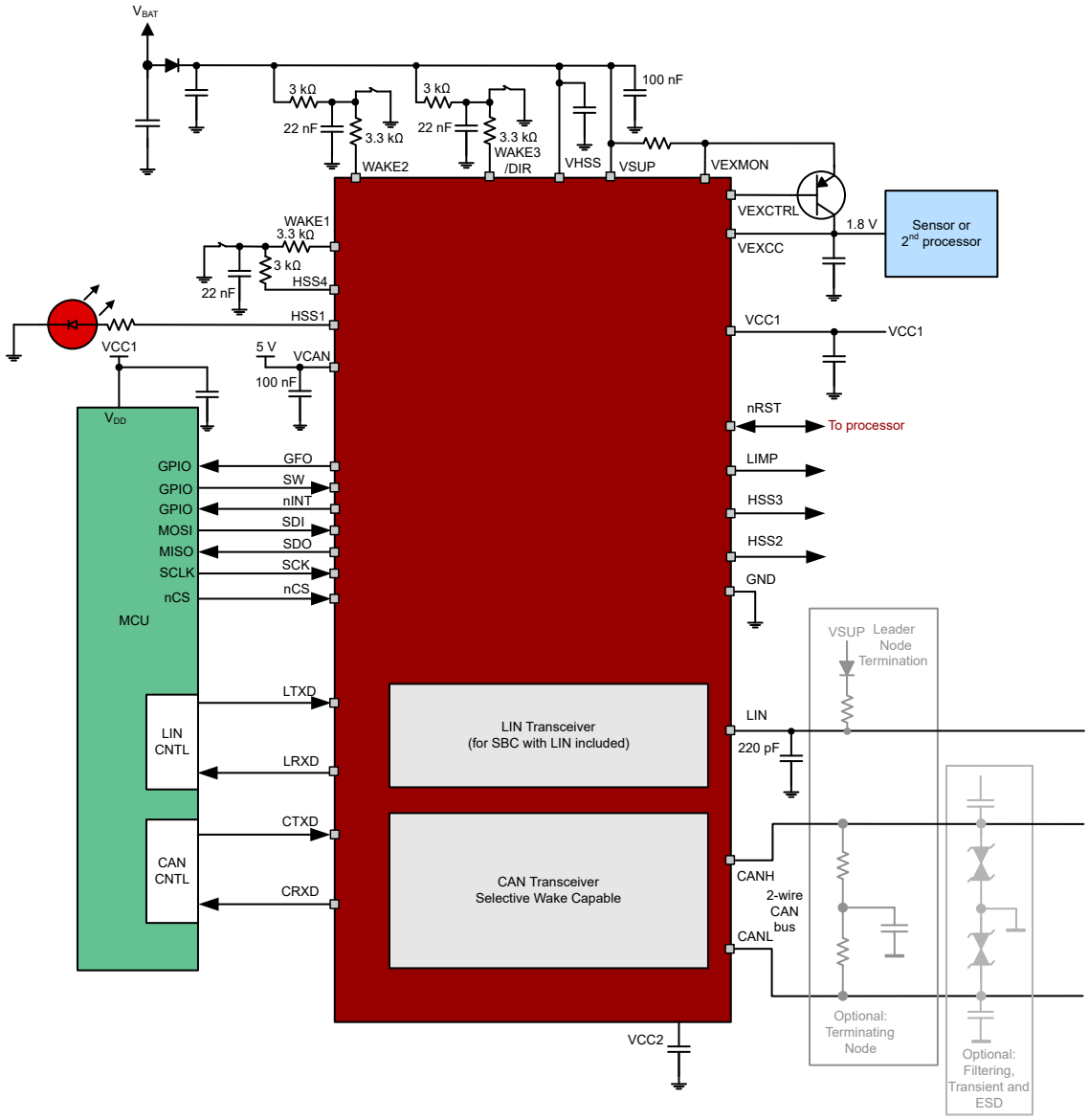


Figure 8-36. Application Drawing With Cyclic Sensing Configuration

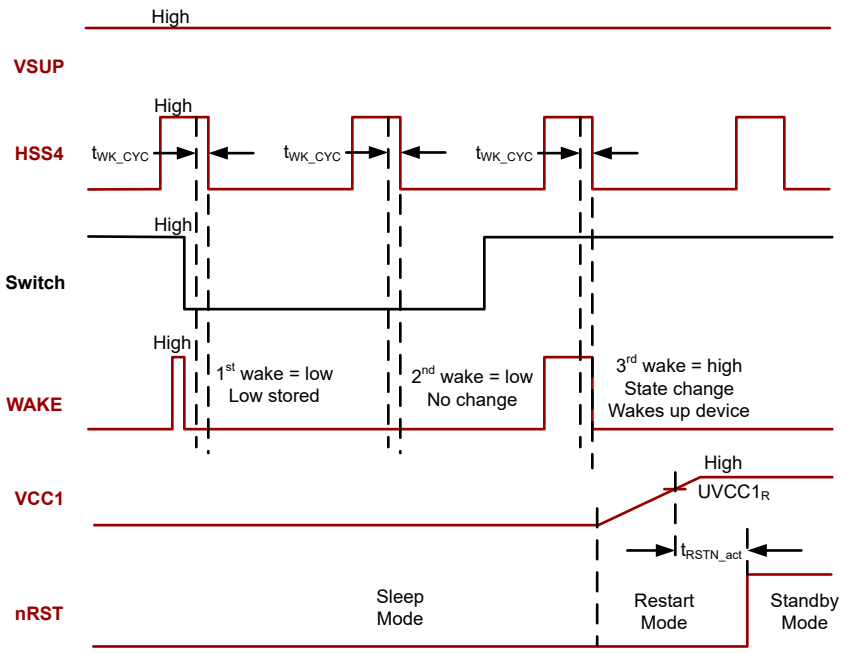


Figure 8-37. Cyclic Sensing Timing Diagram

8.4.7.4 Cyclic Wake

Cyclic Wake can be used to self-wake the device using timer1 or timer2 period without a need for an external wake event. This feature behaves in a specific manner depending upon the SBC mode the device is in and if enabled. This function is available in normal, standby, fail-safe and sleep modes.

In normal and standby Cyclic Wake, at the start of the programmed on time, the device pulls nINT low for programmed-on time and release. The first on time pulse is ignored but each on-time afterward causes the interrupt to pulse low. Cyclic wake is enabled by using register 8'h25[3] for timer1 or 8'h26[3] for timer2. See Table 8-7 for registers used to program cyclic wake feature. Timers are configured using the respective registers. For cyclic wake to work in Normal and Standby modes, all existing interrupts need to be cleared. Interrupts take priority over cyclic wake function in the Normal and Standby modes. Set nINT_TOG=0b (default setting) for cyclic wake configuration. Setting nINT_TOG=1b causes the nINT pin to toggle during the on-time of the timer.

Cyclic wake can be enabled in fail-safe mode by using register 8'h0E[6]=1b. As VCC1 is off in fail-safe mode, nINT pin is not used. When enabled, the period selected for the timer needs to be 500ms, 1s or 2s (longer than t_{LDOOFF}). When the on time takes place, the device determines if a fault is still present. If fault has not cleared, the device stays in fail-safe mode and repeats the process until the SWE timer times out at which time the device transitions to sleep mode. If fault has cleared, this is treated as a wake event and the device transitions to restart mode. Cyclic wake interrupt is reported at the CYC_WUP interrupt bit, INT_4[4].

Cyclic wake can be enabled in sleep mode by setting register 8'h4F[4]=1b and configuring the corresponding timer. After the configured timer period expires, the device wakes up and transition to restart mode where the LDOs are turned on. Cyclic wake interrupt is reported at the CYC_WUP interrupt bit, INT_4[4]. Once the device enters standby mode, the programmed long window starts and is expecting a WD trigger from the processor within this window. If this does not take place, the device considers this as a watchdog error and transition back to restart mode. Which then transition back to standby mode and expect a WD trigger within the long window. Even if VCC1 is on in sleep mode, this same procedure takes place.

Table 8-7. Cyclic Wake Registers

Address	Default	Field	Description
8'h0E[6]	0b	FSM_CYC_WK_EN	Setting to 1b enables the cyclic wake feature in fail-safe mode
8'h25[3]	0b	TIMER1_CYC_WK_EN	Setting to 1b associates the cyclic wake timer to timer1

Table 8-7. Cyclic Wake Registers (continued)

Address	Default	Field	Description
8'h26[3]	0b	TIMER2_CYC_WK_EN	Setting to 1b associates the cyclic wake timer to timer2
8'h4F[4]	0b	SLP_CYC_WK_EN	Setting to 1b enables cyclic wake feature in sleep mode.

Note

- By configuring Cyclic Wake to Timer1 or Timer2, the device performs the cycle wake function in Normal and Standby mode.

8.4.7.5 Direct Drive in Sleep Mode

Direct drive is where the high-side switch is controlled directly from the WAKE3/DIR pin of the device. This is configured by assigning direct drive to any combination of high-side switches. See Section 8.3.11.1 for how this feature is implemented. Direct drive does not wake the device, but methods to wake the device are provided.

- As VCC1 is on when using direct drive, SPI commands can be used to wake the device up from sleep mode.
- Configure SW pin as a digital wake input by setting SW_SLP_EN to 1b in register SBC_CONFIG1 8'h0E[1].
- An unused WAKE1 or WAKE2 pin can be used to wake the device by the processor. The pin thresholds have to be configured to meet the processor requirements.

8.4.7.6 Selective Wake-up

The TCAN285x-Q1 performs CAN communication according to ISO 11898-1 and Bosch CAN protocol specification 3.2.1.1.

8.4.7.6.1 Selective Wake Mode

This is the medium level of power saving mode of the device. The WUF receiver is turned on, and connected internally to the frame detection logic is looking for a Wake-Up Frame (WUF) as outlined in the Frame Detection section of the data sheet. The CAN bus data is not put on the RXD pin in this state. The device is supplied via the VSUP supply coming from the system battery.

The valid wakes up sources in selective wake mode are:

- Wake-Up Frame (WUF)
- WAKE pin local wake up (LWU). Event on WAKE pin must match the programmed requirements for WAKE pin in register 8'h11[7:6]
- Frame Overflow (FRAME_OVF)
- SPI command to another state

If a WUF and/or LWU event occurs, the corresponding wake event flag (CANINT1 and/or LWU) flag is set. At this point, an interrupt is provided to the MCU using the nINT pin if enabled or by pulling down the RXD pin.

To enter selective wake mode, the following conditions must be met:

- Selective Wake Configured, SWCFG, flag is set
  - All Selective Wake registers must be written followed by a read to make sure the registers are programmed correctly for the proper frame detection and selective wake configuration. Once configured, the SWCFG bit must be set to 1b.
- Selective Wake Error, SWERR, flag is cleared
- Set Selective Wake Enable (SW_EN) = 1b, register 8'h10[7] = 1b

If a frame is incoming during the transition, the frame can be lost and frame detection may not sync to the frames for an additional four incoming CAN frames.

Note

If a fault condition or FRAME_OVF forces the device into sleep mode, fail-safe mode disabled, or into fail-safe mode; SW_EN is disabled turning off selective wake function.

8.4.7.6.2 Frame Detection

The frame detection logic is what enables processing of serial data, or CAN frames, from the CAN bus. The device has Selective Wake Control Registers to set up the device to look for a programmed match using either the CAN ID (11 bit or 29 bit), or the CAN ID plus the data frame including data masking. If the detected CAN frame received from the bus matches the configured requirements in the frame detection logic, the detected CAN frame is called a Wake-Up Frame (WUF).

Before Frame Detection can be enabled or used the data needed for validation, or match, of the WUF needs to be correctly configured in the device registers. Once the device has been correctly configured to allow frame detection, or selective wake function the SWCFG (Selective Wake Configuration) must be set to load the parameters for WUF for the device. If a valid WUF is detected, the WUF is shown using the CANINT flag, including selective wake up.

When Frame Detection is enabled several other actions can take place as the logic is decoding the CAN frames the device receives on the bus. These include error detection and counting and the indication of reception of a CAN frame via the CAN_SYNC and CAN_SYNC_FD flags.

If a Frame Overflow (FRAME_OVF) occurs while in Frame Detection mode, the mode is disabled, clearing the SW_EN bit.

When Frame Detection is enabled transitioning from a mode where the receiver bias is not on up to four CAN frames for 500kbps and slower data rates and up to eight CAN frames for greater than 500kbps can be ignored by the device until the Frame Detection is stabilized.

The procedure to correctly configure the device to use frame detection and selective wake up is:

- Write all control registers for frame detection (selective wake), Selective Wake Config 1-4 (Registers 8'h44 through 8'h47), and ID and ID mask (Registers 8'h30 through 8'h38)
- Recommend reading all Selective Wake registers, allowing the software to confirm the device is written, and thus, configured properly
- Set Selective Wake Configured (SWCFG) bit to 1b, register 8'h4F[7] = 1b
- Set Selective Wake Enable = 1b, register 8'h10[7] = 1b
- Set device into standby mode by SPI write to 8'h10[2:0] =100b. Step must be done even if already in standby mode.

If a SWERR interrupt then occurs from the Frame Overflow flag, the Frame Overflow interrupt needs to be cleared, and then the SWCFG bit must be set again to 1b.

8.4.7.6.3 Wake-Up Frame (WUF) Validation

When the following conditions are all met the received frame shall be valid as a Wake-Up Frame (WUF):

- The received frame is a Classical CAN data frame when DLC (Data Length Code) matching is not disabled. The frame can also be a remote frame when DLC matching is disabled.
- The ID (as defined in ISO 11898-1:2015, 8.4.2.2) of the received Classical CAN frame is exactly matching a configured ID in the relevant bit positions. The relevant bit positions are given by an ID-mask illustrated in Section 8.4.7.6.5
- The DLC (as defined in ISO 11898-1:2015, 8.4.2.4) of the received Classical CAN data frame is exactly matching a configured DLC. See the mechanism illustrated in Section 8.4.7.6.6. Optionally, this DLC matching condition can be disabled by configuration in the implementation.
- When the DLC is greater than 0 and DLC matching is enabled, the data field (as defined in ISO 11898-1:2015, 8.4.2.5) of the received frame has at least one bit set in a bit position which corresponds to a set bit in the configured data mask. See the mechanism illustrated in Section 8.4.7.6.5.
- A correct cyclic redundancy check (CRC) has been received, including a recessive CRC delimiter, and no error (according to ISO 11898-1:2015, 10.11) is detected prior to the acknowledgment (ACK) Slot.

8.4.7.6.4 WUF ID Validation

The ID of the received frame matches the configured ID in all required bit positions. The relevant bit positions are determined by the configured ID in 8'h30 through 8'h33 and the programmed ID mask in 8'h34 and 8'h38. Classic Base Frame Format (CBFF) 11-bit Base ID and Classic Extended Frame Format (CEFF) 29-bit

Extended ID and ID masks are supported. All masked ID bits except "do not care" must match exactly the configured ID bits for a WUF validation. If the masked ID bits are configured as "do not care" then both "1" and "0" are accepted in the ID. In the ID mask register a 1 represents “do not care”.

Figure 8-38 shows an example for valid WUF ID and corresponding ID Mask register

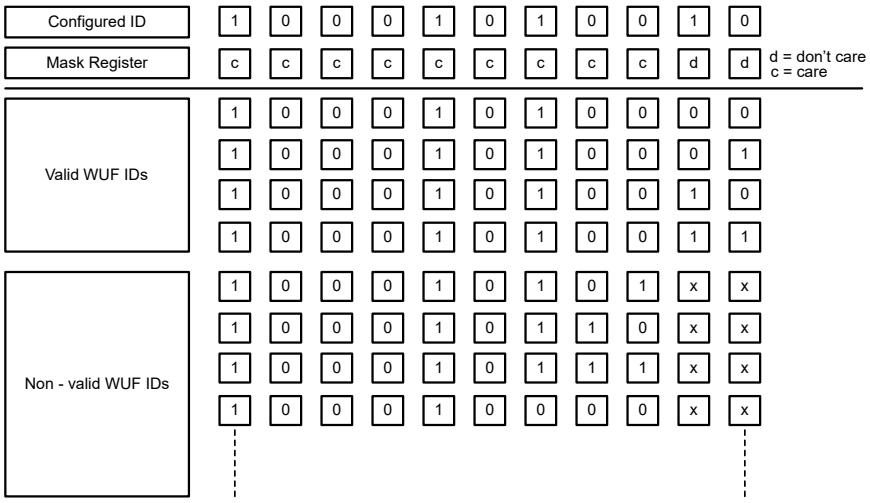


Figure 8-38. ID and ID Mask Example for WUF

8.4.7.6.5 WUF DLC Validation

The DLC (Data Length Code) of the received frame must match exactly the configured DLC if the data mask bit is set. The DLC is configured in 8'h38[4:1]. The data mask bit is set in 8'h38[0].

Table 8-8. DLC

Frames	Data Length Code				Number of Data Bytes
	DLC3	DLC2	DLC1	DLC0	
Classical Frames & FD Frames	0	0	0	0	0
	0	0	0	1	1
	0	0	1	0	2
	0	0	1	1	3
	0	1	0	0	4
	0	1	0	1	5
	0	1	1	0	6
	0	1	1	1	7
	1	0	0	0	8
Classical Frames	1	0 or 1	0 or 1	0 or 1	8

8.4.7.6.6 WUF Data Validation

When the Data mask is enabled using the data mask bit, the data of the received frame must match the configured Data where at least one logic high (1) bit within the data field of the received frame matches a logic high (1) of the data field within the configured data. The relevant bit positions are determined by the configured Data in 8'h39 through 8'h40 and enabled by Data mask enable in 8'h38[0]. An example of a matching and non-matching Data is shown in Figure 8-39

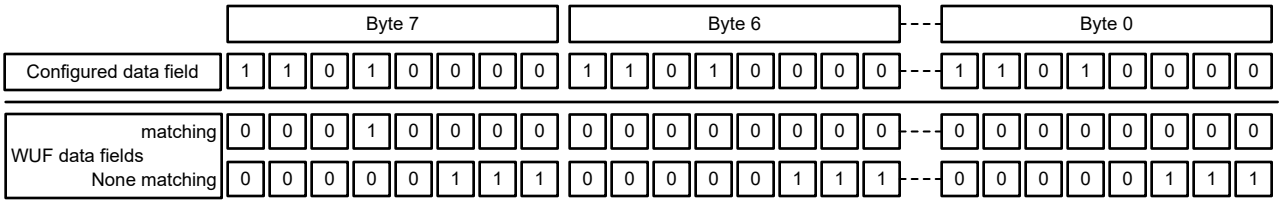


Figure 8-39. Data Field Validation for WUF Example

The selective wake data validation makes sure the last byte sent on the bus is interpreted as data mask byte 0. This means for 8 bytes of data, the first byte sent is interpreted as data mask byte 7. For a DLC of 3, the last byte sent on the bus is interpreted as data mask byte 0 and the first byte sent is interpreted as data mask byte 2. Figure 8-40 provides a few examples of which bytes is used for various bytes sent and received.

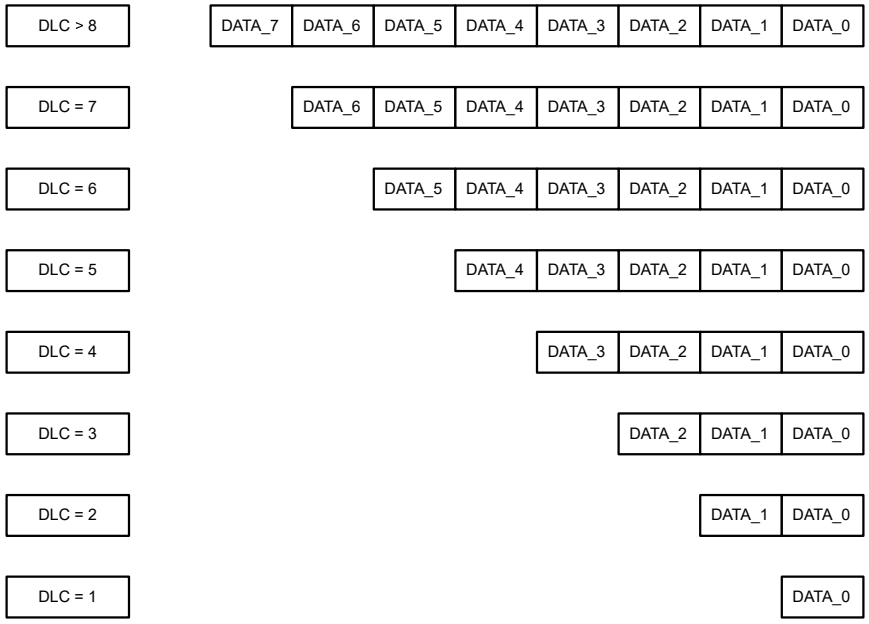


Figure 8-40. Data Register Mask Values for Different DLC Values

8.4.7.6.7 Frame Error Counter

Upon activation of the selective wake up function and upon the expiration of $t_{SILENCE}$ the CAN frame error counter is set to zero. This error counter determines the CAN frame errors detected by the device. In 8'h45 the error counter is called FRAME_CNTx.

The initial counter value is zero and is incremented by 1 for every received frame error detected (stuff bit, CRC or CRC delimiter form error). The counter is decremented by 1 for every correctly received CAN frame assuming the counter is not zero. If the device is set for passive on CAN with flexible data rate frames, any frame detected as a CAN FD frame has no impact on the frame error counter (no increment or decrement). If a valid Classical CAN frame has been received and the counter is not zero, the counter is decremented by one. Dominant bits between the CRC delimiter and the end of the intermission field does not increase the frame error counter.

On each increment or decrement of the error counter, the decoder unit waits for nBits_idle recessive bits before considering a dominant bit as a start of frame (SOF). See Figure 8-41 for the position of the mandatory start of frame detection when classic CAN frame is received and in case of error scenario.

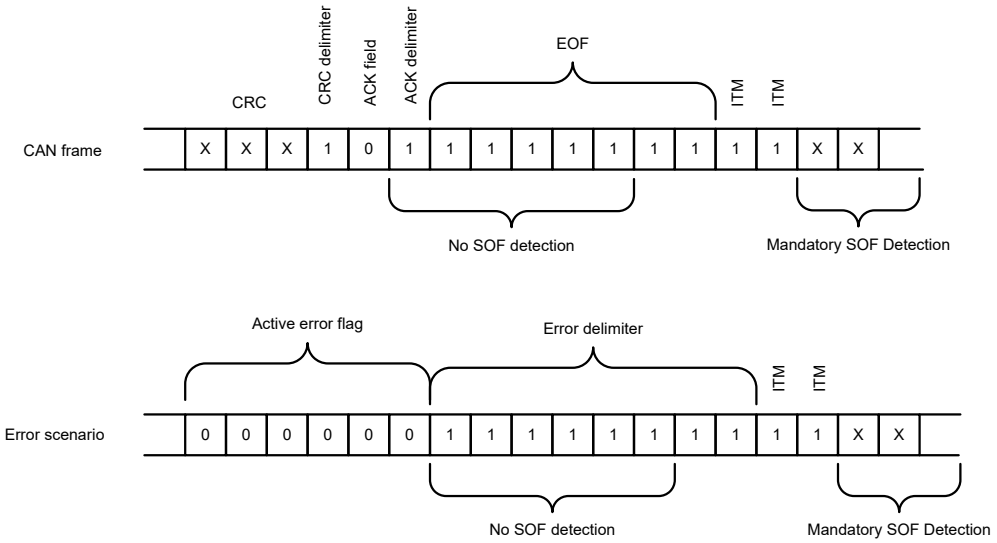


Figure 8-41. Mandatory SOF Detection After Classic CAN Frames and Error Scenarios

The default value for the frame error counter threshold is 31, so that on the 32nd error, the frame overflow flag (FRAME_OVF) is set.

Up to four (or eight when bit rate > 500kbps) consecutive Classic CAN data and remote frames that start after the bias reaction time, t_{Bias}, has elapsed can be either ignored, no error counter increase of failure, or judged as erroneous (error counter increases even in case of no error).

Received a frame in CEFF with non-nominal reserved bits (SRR, r0) are not led to an increase of the error counter.

The frame error counter is compared to the frame error counter threshold, FRAME_CNT_THRESHOLD in 8'h46. If the counter overflows the threshold the frame error overflow flag, FRAME_OVF, is set. The default value for the frame error counter threshold is 31 so that on the 32nd error the overflow flag is set. However, if the application requires a different frame error count overflow threshold the required value can be programmed into the FRAME_CNT_THRESHOLD register.

The counter is reset by the following: disabling the frame detection, CANSLNT flag set, and setting register 8'h51[2] = 1b.

The description for the errors detected:

- *Stuff bit error:* A stuff bit error is detected when the 6th consecutive bit of the same state (level) is received. CAN message coding must have had a stuff bit at this bit position in the data stream.
- *CRC error*: The CRC sequence consists of the result of the CRC calculation by the transmitting node. This device calculates the CRC with the same polynomial as the transmitting node. A CRC error is detected if the calculated result is not the same as the result received in the CRC sequence.
- *CRC delimiter error:* The CRC delimiter error is detected when a bit of the wrong state (logic low / dominant) is received in the CRC delimiter bit position which is defined as logic high (recessive).

8.4.7.6.8 CAN FD Frame Tolerance

After receiving a FD Format indicator (FDF) followed by a dominant res bit, the decoder unit waits for n_{Bits_idle} recessive bits before considering a further dominant bit as a SOF as per Figure 8-41. Table 8-9 defines n_{Bits_idle}.

Table 8-9. Number of Recessive Bits Prior to Next SOF

Parameter	Notation	Value	
		Min	Max
Number of recessive bits before a new SOF is accepted	n_{Bits_idle}	6	10

There are two bitfilter options available to support different combinations of arbitration and data phase bit rates. Register 8'h47[4] is where the $p_{Bitfilter}$ option is selected.

- Bitfilter 1: A data phase bit rate ≤ four times the arbitration rate or 2Mbps whichever is lower shall be supported
- Bitfilter 2: A data phase bit rate ≤ ten times the arbitration rate or 5Mbps whichever is lower shall be supported

Dominant signals ≤ the minimum pBitfilter, see Table 8-10, of the arbitration bit time in duration is not considered valid and does not restart the recessive bit counter. Dominant signals ≥ the maximum of pBitfilter of the arbitration bit time duration restart the recessive bit counter.

Table 8-10. Number of Recessive Bits Prior to Next SOF

Parameter	Notation	Value	
		Min	Max
CAN FD data phase bitfilter 1	pBitfilter1	5.00%	17.50%
CAN FD data phase bitfilter 2	pBitfilter2	2.50%	8.75%

8.4.7.6.9 8Mbps Filtering

- Bitfilter 3: A data phase bit rate ≤ 16 times the arbitration rate or 8Mbps whichever is lower shall be supported
- pBitffilter 3 Min 1.25% to Max 4.375%

8.4.8 Protection Features

The TCAN285x-Q1 has several protections features that are described as follows.

8.4.8.1 Fail-safe Features

The TCAN285x-Q1 has a fail-safe mode that can be used to reduce node power consumption for a node system issue. This can be separated into two operation modes, sleep and failsafe modes.

8.4.8.1.1 Sleep Mode Using Sleep Wake Error

The sleep wake error (SWE) timer ($t_{INACTIVE}$) is a timer used to determine if specific functions are not working or if communication between the device and processor is present. This feature is disabled by default. The SWE timer can be enabled by setting SWE_EN; 8'h1C[7] = 1b. See Figure 8-42 for information on which modes the SWE timer start in and when. When enabled, at power up with VCC1_CFG = 10b for SBC mode control, if the device has not had the PWRON flag cleared or been placed into normal mode, the device enters sleep mode when $t_{INACTIVE}$ times out. If VREG_CONFIG1 register 8'h0D[7:6], VCC1_CFG, has been set to 01b for always on and the SWE timer times out while the device is in normal or standby modes, the device transitions to restart mode.

The device wakes up if the CAN or LIN bus provides a WUP or a local wake event takes place thus entering standby mode. Once in standby mode, the $t_{SILENCE}$ and $t_{INACTIVE}$ timers start. If the $t_{INACTIVE}$ expires the device re-enter sleep mode. When the device receives a CANINT, LWU or FRAME_OVF such that the device leaves sleep mode, entering restart mode and then enters standby mode, the processor has the programmed SWE timer time to clear the flags or place the device into normal mode. If this does not happen, the device enters either restart mode or sleep mode depending upon the programmed value of VCC1_CFG. When in standby or normal mode and the CANSLNT flag persists for $t_{INACTIVE}$, the device enters sleep mode. Examples of events are the processor is no longer working and not able to exercise the SPI bus. A go to sleep command comes in, and the processor is not able to receive or respond to the command. See Figure 8-43 .

Note

- When VCC1 is enabled on for sleep mode a SWE timer time-out, in any mode other than FSM, causes the device to transition to restart mode instead of sleep mode. This causes the nRST pin to be pulled low to reset the processor and set the WKERR and SMS interrupt flags.
- A SWE timer time-out does not impact VCC2 or VEXCC if enabled on for sleep mode.

Note

The restart timer can be either t_{RSTTO} or $t_{INACTIVE}$ (SWE timer), and is selected using register 8'h4F[0], RSTRT_TMR_SEL. The SWE timer is default disabled and must be enabled if $t_{INACTIVE}$ is to be used.

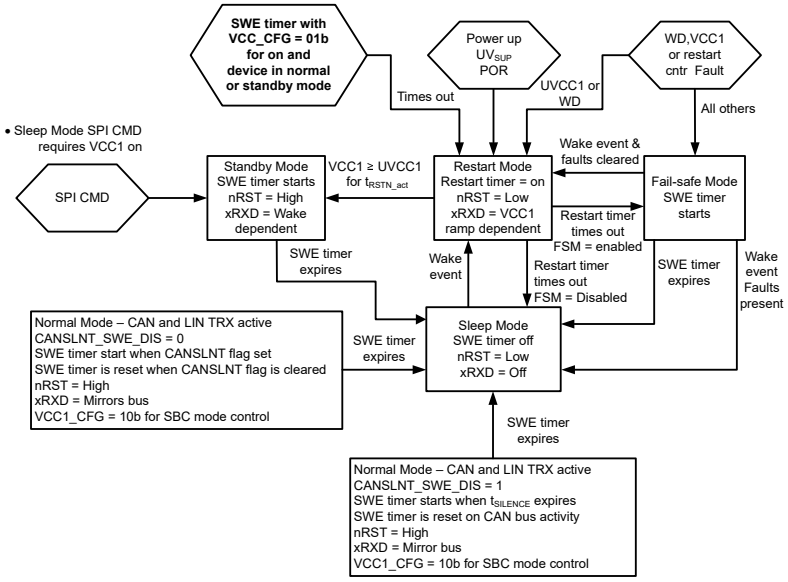
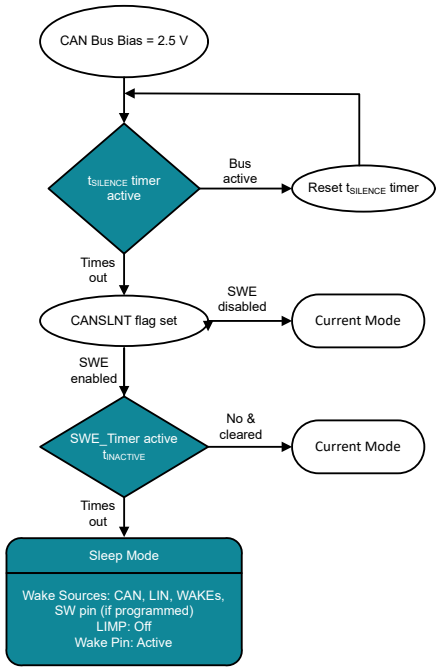


Figure 8-42. SWE Timer by Mode When Enabled



Note

This figure is based upon the CAN FD transceiver being on or in listen only states.

Figure 8-43. Normal and Standby to Sleep Mode

8.4.8.2 Device Reset

The TCAN285x-Q1 family has three methods to reset the device. Two are accomplished with SPI commands and are a soft reset and hard reset. Soft reset and hard reset are accomplished by writing a 1b to DEVICE_RST register 8'h19[1] for soft reset or to 8'h19[0] for hard reset.

Hard reset can also be performed by pulling nRST low for t_{NRSTIN}, see Figure 8-44.

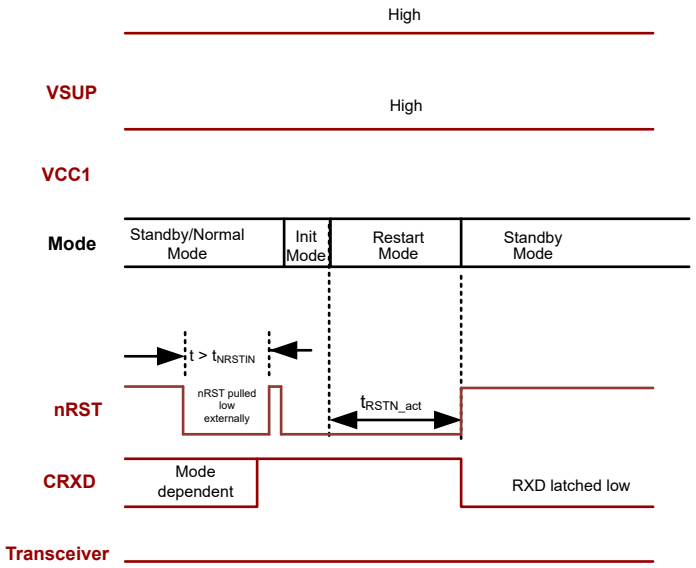


Figure 8-44. Performing Hard Reset with the nRST Pin

When performing a soft reset, the following takes place:

- Saved EEPROM registers are reloaded
- All other registers are reset to default values
- VCC1 and VCC2 do not change state
- Device transitions to standby mode

When performing a hard reset, the following takes place:

- Device transitions to Init mode
- Saved EEPROM registers are reloaded
- All other registers are reset to default values
- Most of the internal device logic is reset to default
- VCC1 and VCC2 do not change state
- Device then transitions to restart mode and finally to standby mode where the device can be reprogrammed

When pulling nRST pin low and releasing, the following takes place:

- Device transitions to Init mode
- Saved EEPROM registers are reloaded
- All other registers are reset to default values
- Most of the internal logic is reset to default
- VCC1 and VCC2 do not change state
- Device then transitions to restart mode and finally to standby mode where the device can be reprogrammed

Note

The recommended is for any changes to registers that are stored into EEPROM be saved to EEPROM. A reset causes these registers to be loaded from EEPROM. This overwrites unsaved changes with the last-saved register values from EEPROM.

8.4.8.3 Floating Terminals

There are internal pull ups and pull downs on critical terminals to place the device into known states if the terminal floats. See Table 8-11 for details on terminal bias conditions.

Table 8-11. Terminal Bias

TERMINAL	PULL-UP or PULL-DOWN	COMMENT
SW	60kΩ Pull-down or Pull-up	When SW pin is active high pin weakly biases input to GND. When SW pin is active low pin weakly biases input to either VCC1 or internal voltage rail
SCK	60kΩ Pull-down or Pull-up	Automatically configures to pull-up or pull-down based upon the SPI mode selected which weakly biases input • Mode 0 or 1 configures for pull-down • Mode 2 or 3 configures for pull-up
SDI	60kΩ Pull-down or Pull-up	Configured as either a pull-up or pull-down based upon SDI_POL configuration in SPI_CONFIG register 8'h09[2] which weakly biases input
nCS	60kΩ Pull-up	Weakly biases input so the device is not selected
nRST	30kΩ Pull-up	Pulled-up to VCC1
LIN	40kΩ Pull-up	Weakly biases
LTXD	60kΩ Pull-up	Weakly biases input
CTXD	60kΩ Pull-up	Weakly biases input

Note

The internal bias must not be relied upon as only termination, especially in noisy environments, but must be considered a fail-safe protection. Special care needs to be taken when the device is used with MCUs using open drain outputs.

8.4.8.4 TXD Dominant Time Out (DTO)

The TCAN285x-Q1 supports dominant state time out on both the LIN and CAN buses. This is an internal function based upon the TXD path. The TXD DTO circuit prevents the local node from blocking network communication in event of a hardware or software failure where TXD is held dominant (LOW) longer than the time out period t_{TXD_DTO}. The TXD DTO circuit is triggered by a falling edge on TXD. If no rising edge is seen before the time out constant of the circuit, t_{TXD_DTO}, the bus driver is disabled. This frees the bus for communication between other nodes on the network. The driver is re-activated when a recessive signal (HIGH) is seen on TXD terminal; thus, clearing the dominant time out. The receiver remains active and the RXD terminal reflects the activity on the CAN bus and the bus terminals is biased to recessive level during a TXD DTO fault. This feature can be disabled by using register 8'h10[6] TXD_DTO_DIS for CAN and 8'h1D[5] LIN1_TXD_DTO_DIS for LIN.

Note

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame.

8.4.8.5 LIN Bus Stuck Dominant System Fault: False Wake Up Lockout

The device contains logic to detect bus stuck dominant system faults and prevents the device from waking up falsely during the system fault. Upon entering sleep mode, the device detects the state of the LIN bus. If the bus is dominant, the wake-up logic is locked out until a valid recessive on the bus “clears” the bus stuck dominant, preventing excessive current use. Figure 8-45 and Figure 8-46 show the behavior of this protection.

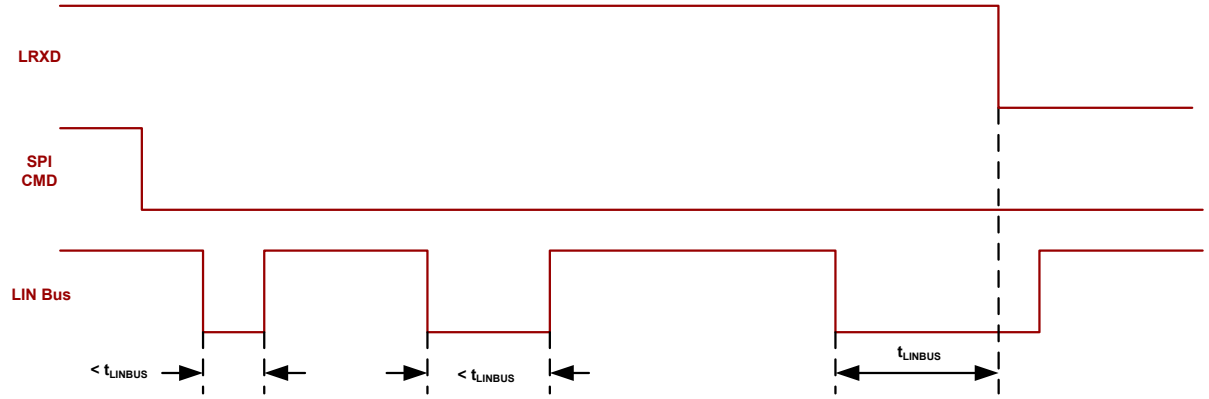


Figure 8-45. No Bus Fault: Entering Sleep Mode with Bus Recessive Condition and Wake Up

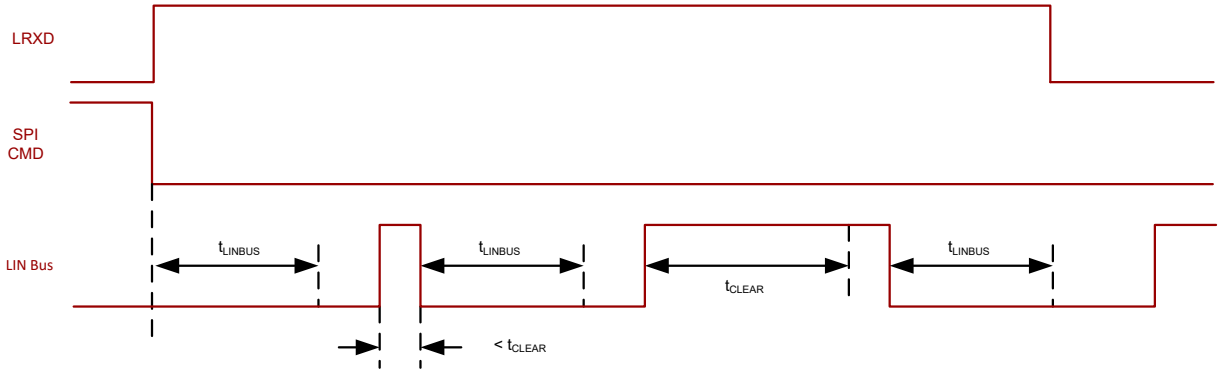


Figure 8-46. Bus Fault: Entering Sleep Mode with Bus Stuck Dominant Fault, Clearing, and Wake Up

8.4.8.6 CAN Bus Short Circuit Current Limiting

These devices have several protections features that limit the short circuit current when a CAN bus line is shorted. These include CAN driver current limiting (dominant and recessive). The device has TXD dominant time out which prevents permanently having the higher short circuit current of dominant state for a system fault. During CAN communication the bus switches between dominant and recessive states; thus, the short circuit current can be viewed either as the current during each bus state or as a DC average current. For system current and power considerations in the termination resistors and common mode choke ratings, the average short circuit current is used. The percentage dominant is limited by the TXD dominant time out and CAN protocol which has forced state changes and recessive bits such as bit stuffing, control fields, and inter frame space. These make sure there is a minimum recessive amount of time on the bus even if the data field contains a high percentage of dominant bits.

Note

The short circuit current of the bus depends on the ratio of recessive to dominant bits and the respective short circuit currents. The average short circuit current can be calculated using Equation 3.

$$I_{OS(AVG)} = \%Transmit \times [(\%REC\_Bits \times IOS(SS)\_REC) + (\%DOM\_Bits \times IOS(SS)\_DOM)] + [\%Receive \times IOS(SS)\_REC] \quad (3)$$

Where

- $I_{OS(AVG)}$ is the average short circuit current.
- %Transmit is the percentage the node is transmitting CAN messages.
- %Receive is the percentage the node is receiving CAN messages.
- %REC_Bits is the percentage of recessive bits in the transmitted CAN messages.
- %DOM_Bits is the percentage of dominant bits in the transmitted CAN messages.

- IOS(SS)_REC is the recessive steady state short circuit current and IOS(SS)_DOM is the dominant steady state short circuit current.

Note

The short circuit current and possible fault cases of the network must be taken into consideration when sizing the power ratings of the termination resistance, other network components, and the power supply used to generate VSUP.

8.4.8.7 Thermal Shutdown

The device has two thermal sensors in the device to monitor the junction temperature of the die.

1. Covers VCC1 LDO and external PNP control, VEXCC
2. Covers VCC2 LDO, CAN transceiver and LIN transceiver

There is a thermal shutdown pre-warning provided that is set when the junction temperature of VCC1 LDO,and external PNP control, VEXCC, hits the warning temperature level. When this temperature sensor reaches the pre-warning rising, TSDWR, an interrupt is set for pre-warning. There are three interrupts a thermal event. The behavior of the device depends upon which sensor hits the thermal event. This is a device preservation feature.

- INT_6 register 8'h5C[7] is TSDW interrupt
- INT_2 register 8'h52[1] is TSD_VCC1_VEXCC interrupt
- INT_3 register 8'h53[1] is TSD_CAN_LIN interrupt which includes VCC2 LDO

Exceeding the maximum junction temperature for > t_{TSD} causes interrupt flags to be set and is indicated by pulling nINT low. If VCC1 or VEXCC causes the TSD event; the device turns off these LDOs and enter either fail-safe mode (if enabled) or sleep mode. The nRST pin is pulled to ground during this TSD event. Once the over temperature fault condition has been removed and the junction temperature has cooled beyond the TSDF temperature for 1s, the device transitions from fail-safe mode to restart mode and turn on VCC1 and VEXCC (if enabled). A thermal shut down interrupt flag is set but not indicated on nINT pin as VCC1 is off. This event turns off the high side switches by resetting the HSS1-4_CNTL registers. If thermal shutdown event happens while the device is in fail-safe or sleep mode and cyclic sensing is enabled, the cyclic sensing function is lost as HSS4 is turned off.

If TSD is detected by the second sensor which covers the transceivers and VCC2. Both CAN and LIN transmitters is disabled placing them into listen mode. VCC2 LDO is disabled and the interrupt flag is set. This does not cause an SBC state change. Once the over temperature fault condition has been removed and the junction temperature has cooled beyond the TSDF temperature, the CAN and LIN transmitters is re-enabled. After 1s of further wait time, VCC2 LDO is turned on. Note that UVCC2 is not set because the LDO has been disabled. Read VCC2_STATUS at register 8'h4F[2] to determine when VCC2 has been re-enabled. If VCC2 is used in the system as the supply source for VCAN, then the VCC2 off condition creates a UVCAN condition. The CAN transceiver changes to wake capable, and cannot be re-enabled until VCC2 is fully powered again. VCC2_STATUS is also indicating the status of VCAN. When VCC2_STATUS=1b, the CAN transceiver is re-enabled and UVCAN interrupt flag can be cleared.

8.4.8.8 Under and Over Voltage Lockout and Unpowered Device

The device monitors all of the supply rails of the device, both input (VSUP, VHSS and VCAN) and output (VCC1, VCC2 and VEXCC). For the input supply rails, all are monitored for under voltage and VHSS can be monitored for over voltage. For the output supply rails, all are monitored for under voltage, over-voltage and short circuit failures. Each of these fault events have a corresponding interrupt with VSUP and VCC1 faults causing device SBC mode changes. See Table 8-12 for the relationship between VSUP, VCC1, VCC2 and VEXCC faults.

The device monitors VCC1, VCC2 and VEXCC for over-voltage condition. Over-voltage is represented by OVCC1, OVCC2 and OVEXCC. The TCAN285x-Q1 monitors VCC1, VCC2 and VEXCC for short to ground conditions. Short to ground is represented by $VCC1_{33SC}$, $VCC1_{5SC}$, $VCC2_{SC}$ and $VEXCC_{SC}$.

The device monitors the high-side switches supply voltage, VHSS, for over-voltage events (OVHSS) and disables the high-side switches due to OVHSS. To keep the high-side switches operating under OVHSS condition, write 1b to 8'h4F[7], HSS_OV_SD_DIS. Under-voltage is monitored on the VHSS supply, UVHSS and disables the high-side switches due to UVHSS. To keep the high-side switches operating under UVHSS condition, write 1b to 8'h4F[6], HSS_UV_SD_DIS. If the HSS switches are disabled due to OVHSS or UVHSS, they automatically recover when OVHSS or UVHSS are cleared, unless disabled by writing 1b to 8'h4F[5], HSS_OV_UV_REC.

Table 8-12. VSUP, VCC1, VCC2 and VEXCC Faults and Device Mode

VSUP	VCC1	VCC2	VEXCC	Device Mode
> UVSUP	> UVCC1	> UVCC2	NA	Normal or Standby
> UVSUP	< $UVCC1_{PR}$	> UVCC2	NA	Previous Mode
> UVSUP	< UVCC1	> UVCC2	NA	Restart
> UVSUP	> UVCC1	< UVCC2	NA	Previous Mode
> UVSUP	> UVCC1	> UVCC2	< UVEXCC	Previous Mode
> UVSUP	> OVCC1	NA	NA	Fail-safe or Sleep
> UVSUP	> UVCC1	> OVCC2	NA	Previous Mode
> UVSUP	> UVCC1	NA	< OVEXCC	Previous Mode
> UVSUP	< $VCC1_{SC}$	NA	NA	Fail-safe or Sleep
> UVSUP	> UVCC1	< $VCC2_{SC}$	NA	Previous Mode
> UVSUP	> UVCC1	NA	< $VEXCC_{SC}$	Previous Mode

Note

If a permanent fault on VCC1 takes place and fail-safe mode is disabled, getting into a loop between restart and sleep mode due to wake events and VCC1 SBC fault is possible.

- Enable fail-safe mode when VCC1 is programmed on for sleep mode.
- To avoid the loop situation for a permanent fault with fail-safe mode enabled, the recommendation is to use FSM_CONFIG register 8'h17[7:4] = 0100b which is FSM_CNTR_ACT and places the device into sleep mode with LDOs off until a power cycle reset takes place.

8.4.8.8.1 Under-voltage

The device monitors VSUP, VHSS, VCAN, VEXCC, VCC1 and VCC2 for under-voltage events. Under-voltage events are represented by $UVSUP_{xR/F}$, $UVHSS_{R/F}$, $UVCAN_{R/F}$, $VCC1_{xR/F}$, $UVCC2_{R/F}$ and $UVEXCC_{xR/F}$. The x represents the voltage level, R is when voltage level is ramping up and F is when voltage level is ramping down. Behavior of the device is dependent upon when supply rail is in under-voltage.

VCC1 is the LDO that provides power for the digital input/output pins and is expected to be connected to the node processor. VCC1 has a under-voltage pre-warning threshold and four programmable under-voltage threshold. When the under-voltage pre-warning event takes place an interrupt is set, INT_6 register 8'h5C[6] and the nINT pin is pulled low. Once VCC1 reaches one of the programmed thresholds, SBC_CONFIG1 register 8'h0E[4:3], the device to transition to restart mode and latch nRST low until the LDO voltage exceeds the under-voltage rising threshold. nRST remains latched low and the device stays in restart mode for t_{RSTN_act} after clearing the UV threshold. For UVCC1, there is a filter time, t_{UVFLTR}, that under-voltage event must last longer than for the device to enter restart mode.

8.4.8.8.1.1 VSUP and VHSS Under-voltage

VSUP is the primary input supply rail required for the device to function properly. There are three voltage levels monitored by the device, power on reset and two under-voltage level. For all functions and output voltage rails to be in regulation the device must exceed $UVSUP_{5R}$. If VSUP is in under-voltage, the device loses the supply

source needed to keep the internal regulators in regulation. This causes the device to go into a state where communication between the microprocessor and the TCAN285x-Q1 is disabled. In this mode, the device is still active but VCC1, VCC2 and VEXCC can be experiencing under voltage events and other functions is not active, like watchdog. No mode change can take place. The device is not able to receive information from the bus; thus, does not pass any signals from the bus, including any Bus Wake using BWRR signals to the microprocessor. VCC1 determines which UVSUP level, $UVSUP_{33R/F}$ or $UVSUP_{5R/F}$. If VSUP keeps ramping down and drops below $VSUP_{(PU)F}$, the device enters powered off state. When VSUP returns, the device comes up as if there is an initial power on. All registers are cleared and the device has to be reconfigured from the stored EEPROM values that are retained. During an UVSUP event, the device has some functionality. The LDOs are in pass through mode until VSUP ≥ $UVSUP_{xxR}$ and VCC1 exceeds the $UVCC1_{xxR}$ level. The device transitions to restart mode if VCC1 < $UVCC1_{xxF}$ and stays in restart mode until $UVCC1_{xxR}$ is cleared (the restart timer, $t_{RSTTO,}$ is ignored).

For devices where VCC1 is 5V, $UVSUP_{5R/F}$ is the only VSUP under-voltage rail monitored. When VSUP drops below $UVSUP_{5F}$, The CAN and LIN transceivers are turned off and LDOs are in pass thru mode. See Table 8-13 for relationship between VSUP, $VCC1_5$, VCAN, device mode and transceivers.

When VCC1 is 3.3V, both $UVSUP_{33R/F}$ and $UVSUP_{5R/F}$ are monitored. When powering up, VSUP has to exceed $UVSUP_{33R}$ for VCC1 to be in regulation and above $UVSUP_{5R}$ for VCC2 and other functions of the device to work properly. When VSUP is ramping down, $UVSUP_{5F}$ is the first UVSUP level that sets an UVSUP5 interrupt flag, register 8'h52[4], and turns off the CAN transceiver. The LIN transceiver is still functioning, but does not always meet the data sheet electrical and timing specifications. If VSUP keeps dropping, the next level is $UVSUP_{33F}$. When this is reached, the $UVSUP_{33}$ interrupt flag is set, register 8'h52[3]. When this level is reached, the LIN transceiver is turned off. See Table 8-14 for relationship between VSUP, $VCC1_{33}$, VCAN, device mode and transceivers.

Under-voltage on the high-side switches power, VHSS, is indicated by interrupt INT_4 register 8'5A[0] UVHSS. How the high-side switches behave due to an UVHSS event is determined by HSS_CNTL3 register 8'h4F[6:5].

Table 8-13. Under-voltage Events for $VCC1_5$, Device State and Transceiver State

VSUP	VCC1	VCAN	DEVICE STATE	CAN TRANSCEIVER	LIN TRANSCEIVER
> $UVSUP_5$	> $UVCC1_5$	> UVCAN	Normal or Standby	As Programmed	As Programmed
> $UVSUP_5$	< $UVCC1_5$	NA	Restart	Wake capable or off	Wake capable or off
> $UVSUP_5$	> $UVCC1_5$	> UVCAN	Previous State	As Programmed	As Programmed
> $UVSUP_5$	> $UVCC1_5$	> UVCAN	Previous State	As Programmed	As Programmed
> $UVSUP_5$	> $UVCC1_5$	< UVCAN	Previous State	Listen, Wake capable or off	As Programmed

Table 8-14. Under-voltage Events for $VCC1_{33}$, Device State and Transceiver State

VSUP	VCC1	VCAN	DEVICE STATE	CAN TRANSCEIVER	LIN TRANSCEIVER
> $UVSUP_5$	> $UVCC1_{33}$	> UVCAN	Normal or Standby	As Programmed	As Programmed
> $UVSUP_5$	< $UVCC1_{33}$	NA	Restart	Wake capable or off	Wake capable or off
> $UVSUP_5$	> $UVCC1_{33}$	> UVCAN	Previous State	As Programmed	As Programmed
< $UVSUP_5$ > $UVSUP_{33}$	> $UVCC1_{33}$	NA	Normal or Standby	Off	As Programmed
< $UVSUP_5$ > $UVSUP_{33}$	< $UVCC1_{33}$	NA	Restart	Off	Off
> $UVSUP_5$	> $UVCC1_{33}$	< UVCAN	Normal or Standby	Listen, Wake capable or off	As Programmed

Note

- If a thermal shut down or short circuit event takes place while the regulator is in UV, the device transitions to sleep mode (fail-safe mode disabled) or fail-safe mode if enabled.
- When UVCC1 does not clear by the time the restart timer expires, the device enters the fail-safe mode, if enabled (except in an UVSUP event). If not enabled the device transitions to sleep mode and turn off VCC1. When VCC1 is enabled on for sleep mode, an UVCC1 event proceeds in the same manner. In an UVSUP event, the device stays in Restart mode due to UVCC1 and the restart timer is ignored.
- OV/UVHSS is not shown in the table as OV/UVHSS only impacts the high-side switches.

8.4.8.8.1.2 VCC1 Under-voltage

VCC1 is the LDO that provides power for the digital input/output pins and is expected to be connected to the node processor. VCC1 is monitored for under-voltage and has two levels that are monitored, pre-warning ($UVCC1_{xPR}$) and under-voltage ($UVCC1_{XXR/FX}$). The under-voltage has one of four levels that can be programmed using register 8'h0E[4:3], UVCC1_SEL. Of the supply rails providing external power, VCC1 is the only one considered an SBC fault which causes a state change. When the under-voltage pre-warning event takes place an interrupt is set, INT_6 register 8'h5C[6] and the nINT pin is pulled low. Once VCC1 reaches one of the programmed thresholds, SBC_CONFIG1 register 8'h0E[4:3], the device transitions to restart mode and latches nRST low until VCC1 exceeds the under-voltage rising threshold. nRST remains latched low and the device stays in restart mode for t_{RSTN_act} after clearing the UV threshold. For UVCC1, there is a filter time, $t_{UVFLTR,}$ that the under-voltage event must last longer than for the device to enter restart mode, See Figure 8-47 for UVCC1 behavior.

Note

When VCC1_CFG = 01b for VCC1 always on, or FSM CNTR exceeded, a wake event is not needed to exit the fail-safe mode. The device exits the fail-safe mode after t_{LDOOFF} timer expires.

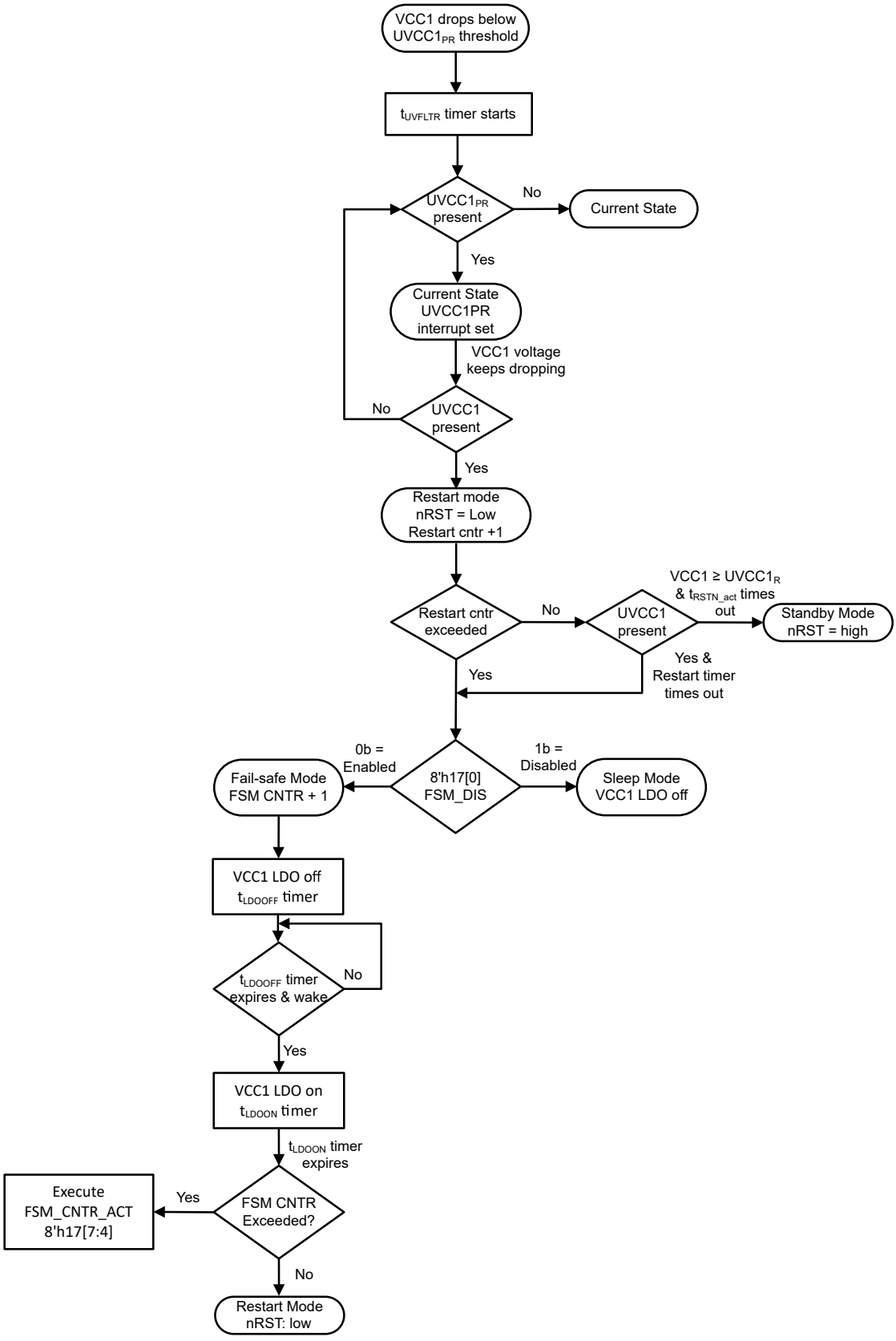


Figure 8-47. UVCC1 State Diagram

8.4.8.8.1.3 VCC2 and VEXCC Under-voltage

A UVCC2 or UVEXCC sets interrupt flags, but do not cause a mode change. See Figure 8-48 and Figure 8-49 for under-voltage behavior

- Register INT_6; 8'h5C[5] is the interrupt for UVEXCC
- Register INT_6; 8'h5C[2] is the interrupt for UVCC2

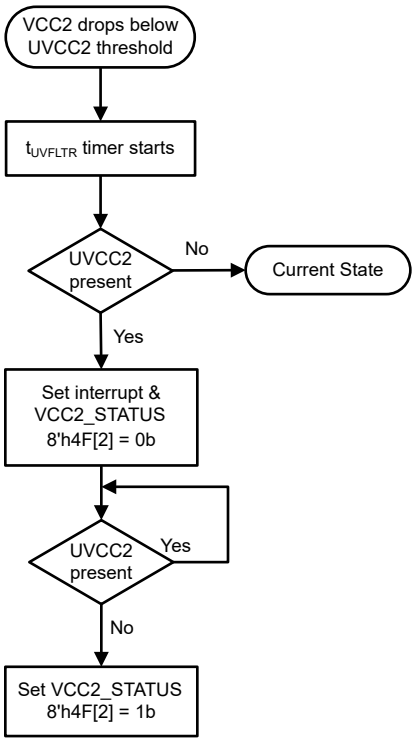


Figure 8-48. UVCC2 State Diagram

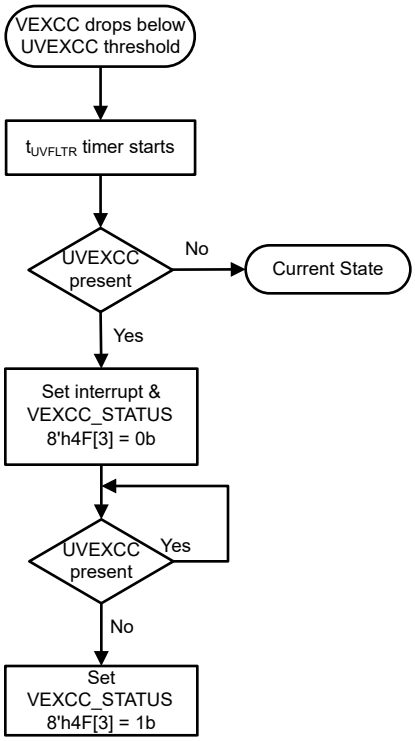


Figure 8-49. UVEXCC State Diagram

8.4.8.8.1.4 VCAN Under-voltage

If VCAN drops below UVCAN under-voltage detection, the CAN transmitter switches off and disengage from the bus until VCAN has recovered. The CAN receiver is still active. See Figure 8-50 on how the device behaves. The device is designed to be an "passive" or “no load” to the CAN bus if the device is unpowered. The bus terminals (CANH, CANL) have extremely low leakage currents when the device is unpowered, which does not load the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains operational. Logic terminals also have low leakage currents when the device is unpowered, so the terminals do not load other circuits which can remain powered.

The UVLO circuit monitors both rising and falling edge of a power rail when ramping and declining.

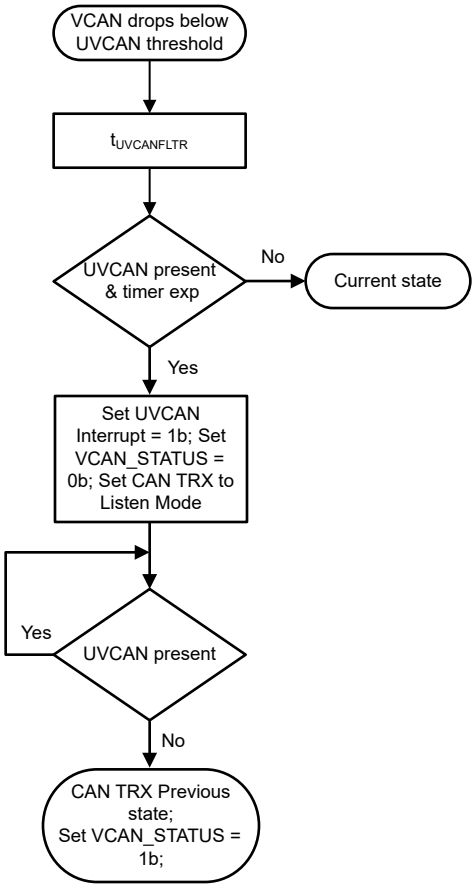


Figure 8-50. UVCAN State Diagram

Note

- UVCAN comparator is enabled in SBC Normal and Standby modes.
- VCAN is required for EEPROM writes so VCAN_STATUS = 1b at register 8'h4F[1] needs to be checked before writing to the EEPROM.

8.4.8.8.2 VCC1, VCC2 and VEXCC Over-voltage

TCAN285x-Q1 monitors VCC1, VEXCC and VCC2 for over-voltage condition. Over-voltage is represented by OVCC1, OVCC2 and OVEXCC. When OVCC1 occurs, the device enters either fail-safe mode, if enabled, or sleep mode. When OVCC2 or OVEXCC takes place, the LDOs are turned off and an interrupt flag is set but no mode change takes place. When entering fail-safe mode, the device turns off all the LDOs and starts the t_{LDOOFF} timer. After this timer times out, OVCC1 is checked for over-voltage. If the OV event has cleared, and a wake event has taken place, the device enters restart mode. If OVCC1 is still present, the device enters sleep mode. Wake events are monitored but not acted upon until t_{LDOOFF} time out. If no wake event has taken place and the OV event has cleared. the device is still in fail-safe mode until the SWE timer times out or a wake event takes place. See Figure 8-51, Figure 8-52 and Figure 8-53 for device behavior during an over-voltage event.

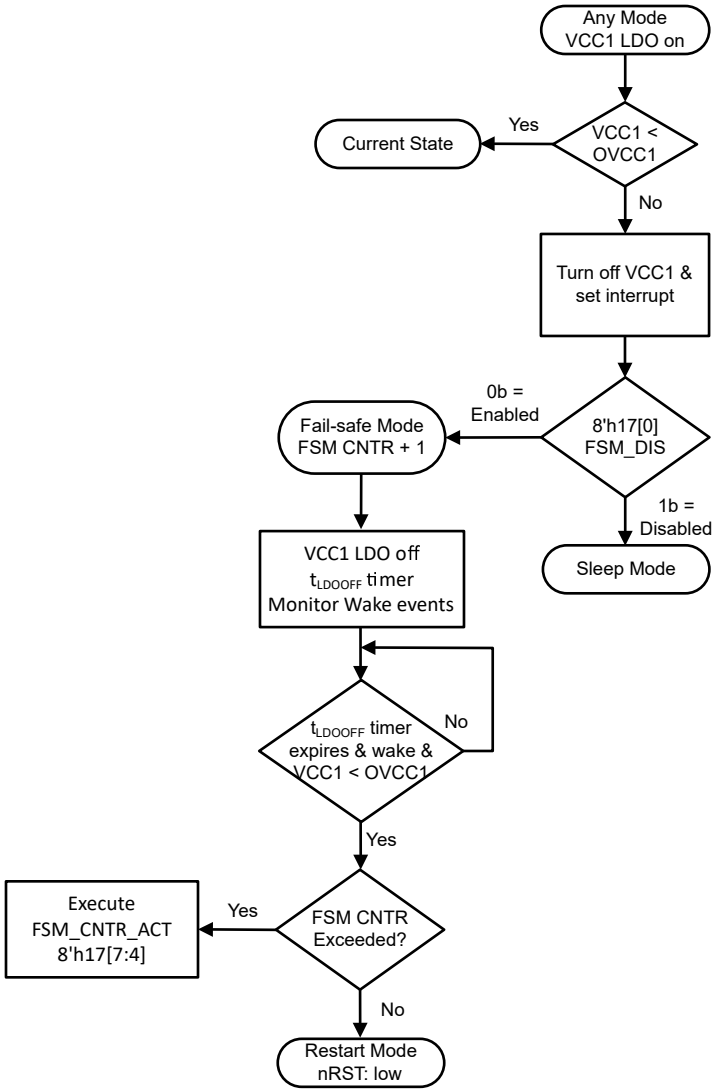


Figure 8-51. OVCC1 State Diagram

Note

When VCC1_CFG = 01b for VCC1 always on, or FSM CNTR exceeded, a wake event is not needed to exit the fail-safe mode. The device exits the fail-safe mode after t_{LDOOFF} timer expires.

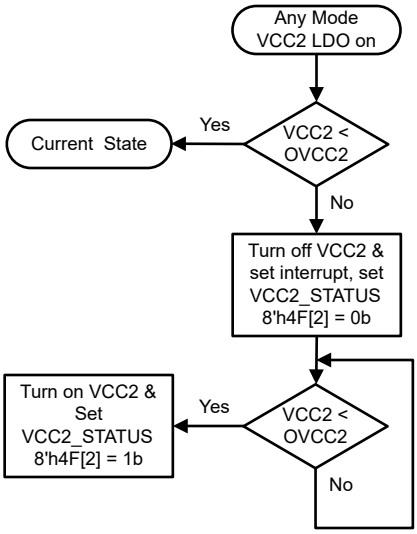


Figure 8-52. OVCC2 State Diagram

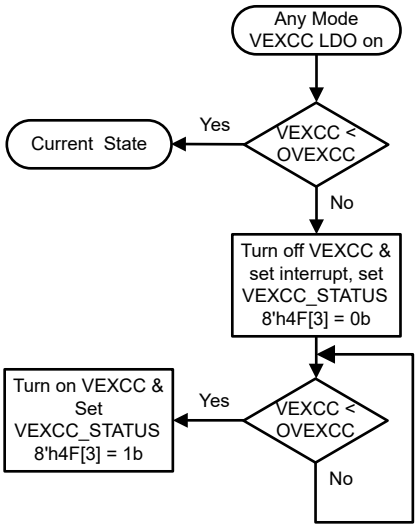


Figure 8-53. OVEXCC State Diagram

8.4.8.8.3 VCC1, VCC2 and VEXCC Short Circuit

The TCAN285x-Q1 monitors VCC1, VEXCC and VCC2 (CAN LDO) for short to ground conditions. Short to ground is represented by $VCC1_{33SC}$, $VCC1_{5SC}$, $VCC2_{SC}$ and $VEXCC_{SC}$. A short to ground turns off the LDO. When a $VCC1_{SC}$ occurs, VCC1 is turned off for a minimum of t_{LDOOFF}, and the device enters fail-safe mode (if enabled) or sleep mode. During this time, wake events are monitored and preserved. A short circuit event cannot be monitored while the LDO is off. A wake event causes VCC1 to be turned on for t_{LDOON} to see if the SC event is still present. If still present, the device transitions to sleep mode. If not present, the device transitioned to restart mode. While in fail-safe mode, the SWE timer starts and if the fault is not cleared and a wake event has not taken place before the timer times out the device transitions to sleep mode. If fail-safe mode is disabled, the device transitions to sleep mode. See Figure 8-54, Figure 8-55 and Figure 8-56 for device behavior during a short to ground event.

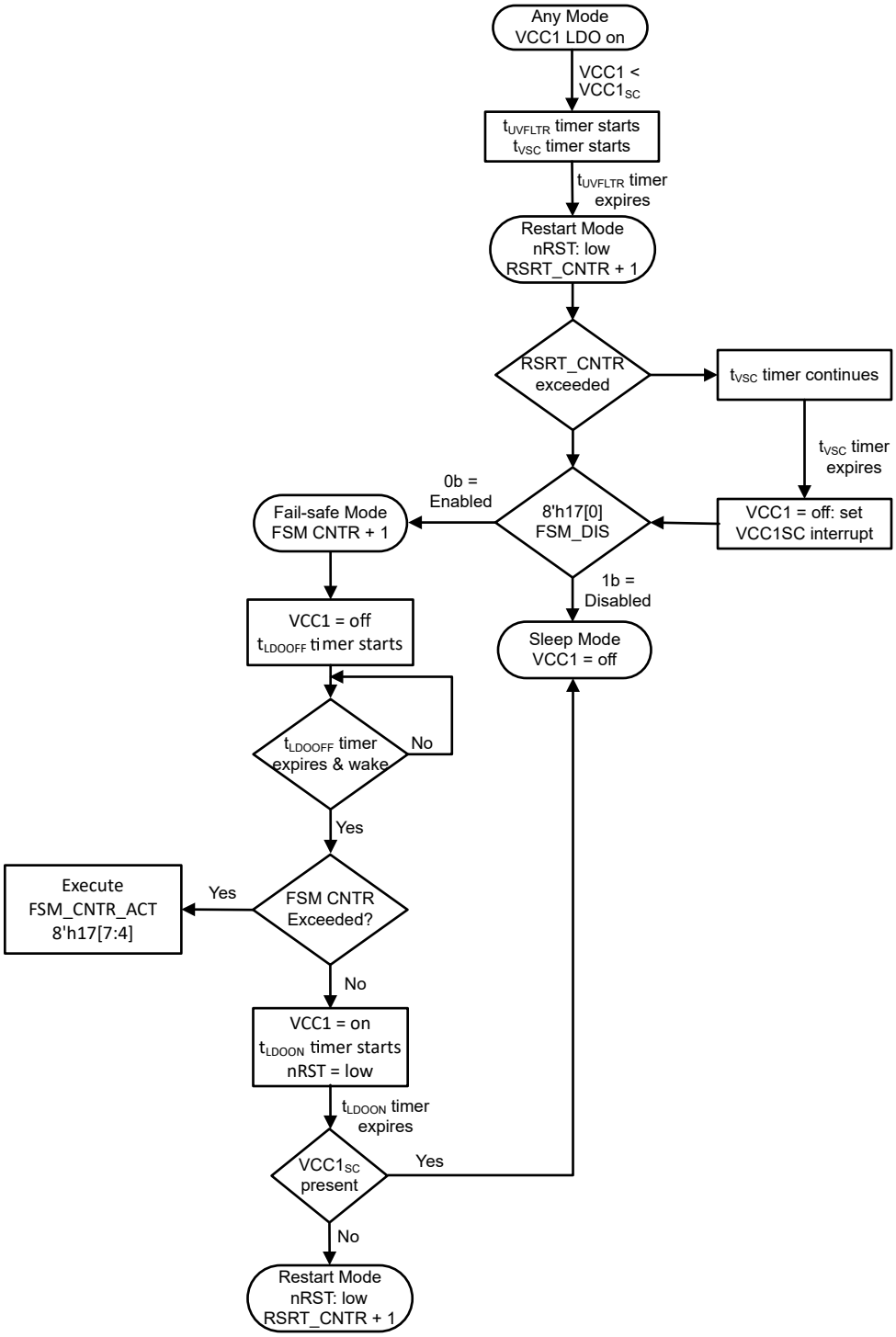


Figure 8-54. $VCC1_{SC}$ State Diagram

Note

When VCC1_CFG = 01b for VCC1 always on, or FSM CNTR exceeded, a wake event is not needed to exit the fail-safe mode. The device exits the fail-safe mode after t_{LDOOFF} timer expires.

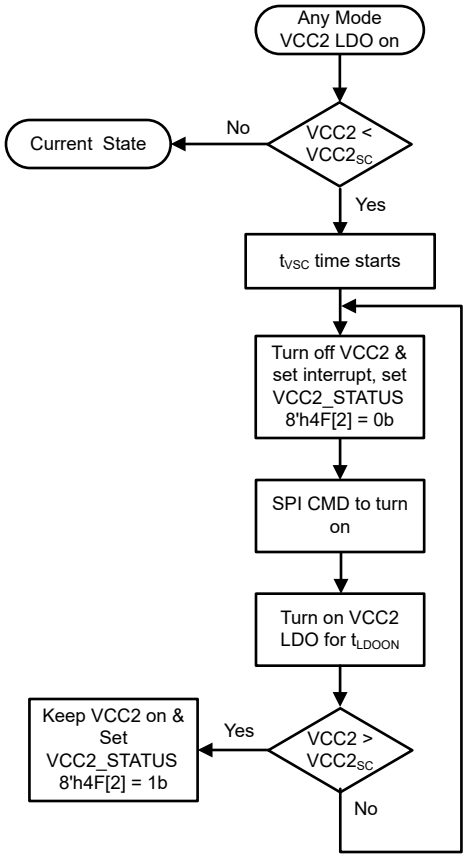


Figure 8-55. $VCC2_{SC}$ State Diagram

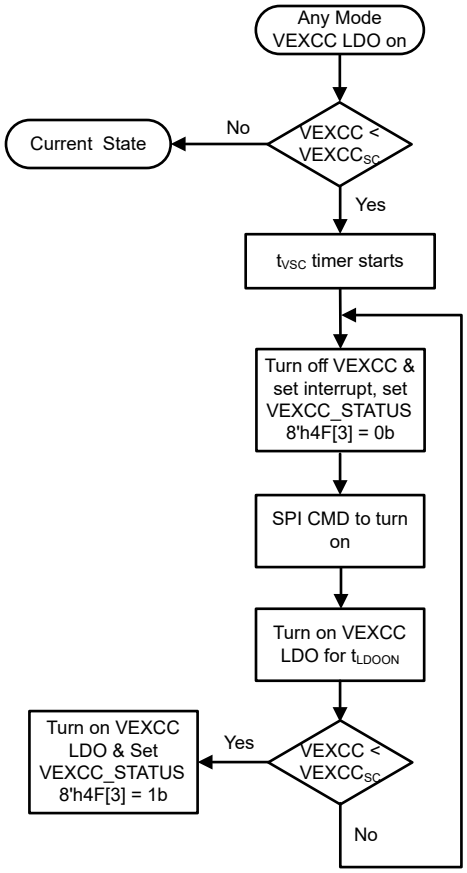


Figure 8-56. $VEXCC_{SC}$ State Diagram

8.4.8.9 Watchdog

The device has an integrated watchdog function. The device provides a default window based, time-out and question and answer (Q&A) watchdog using SPI programming at WD_CONFIG_1 register 8'h13[7:6], WD_CONFIG. The watchdog configuration and type can only be programmed when the device is in standby mode. Normal mode supports all three watchdog configurations while standby mode defaults to timeout. When the device enters standby mode, the watchdog configuration automatically changes to a timeout watchdog. The standby mode watchdog can be configured to the same type as normal mode by programming register 8'h13[2] = 1b. The watchdog is default off in sleep mode but can be configured to be active as a timeout watchdog by programming WD_SLP_EN at register 8'h13[3] = 1b.

When entering standby mode from restart mode, there is a nRST transition from low to high. This transition starts the t_{INITWD} timer, and includes the t_{RSTN_act} timer in restart mode. A WD trigger input must take place prior to this initial long window times out. The initial long window defaults to 600ms but can be programmed to other values, WD_LW_SEL at register 8'h13[1:0]. See Figure 8-57 for the timing diagram. Once the long window watchdog is served, the watchdog configured in the Standby mode starts immediately.

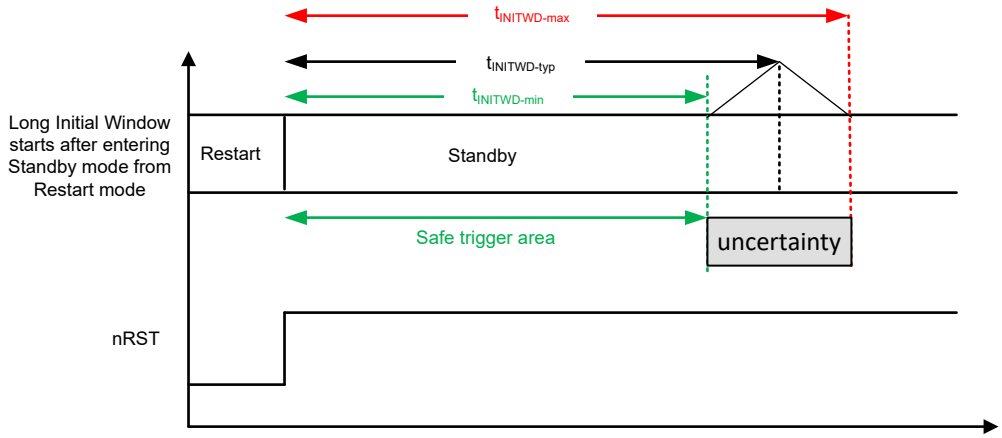


Figure 8-57. Long Window Watchdog Timing Diagram

When entering normal mode, the programmed watchdog timer starts based upon the programmed configuration. The watchdog timer is off in sleep, restart and fail-safe modes. The LIMP pin provides a limp home capability. When in sleep mode, the LIMP pin is off. When the error counter exceeds the watchdog trigger event level, the LIMP pin turns pulling the LIMP pin to ground as described in the LIMP pin section.

The watchdog has extensive configurable including the ability to select the time-out or Q&A watchdog. Watchdog is default enabled for standby mode, but can be disabled by setting register 8'h14[0] = 1b. Register 8'h13[7:6] can be set to 00b to disable the WD. There is a WD error counter available, see Section 8.4.8.9.1 for description of this counter. Figure 8-58 provides a flow chart on the watchdog in standby mode. Watchdog can be enabled in sleep mode, but only behaves as a time-out watchdog. VCC1 must be enabled for sleep mode. Figure 8-59 flow chart provides the behavior of the device when the watchdog is enabled or disabled in sleep mode.

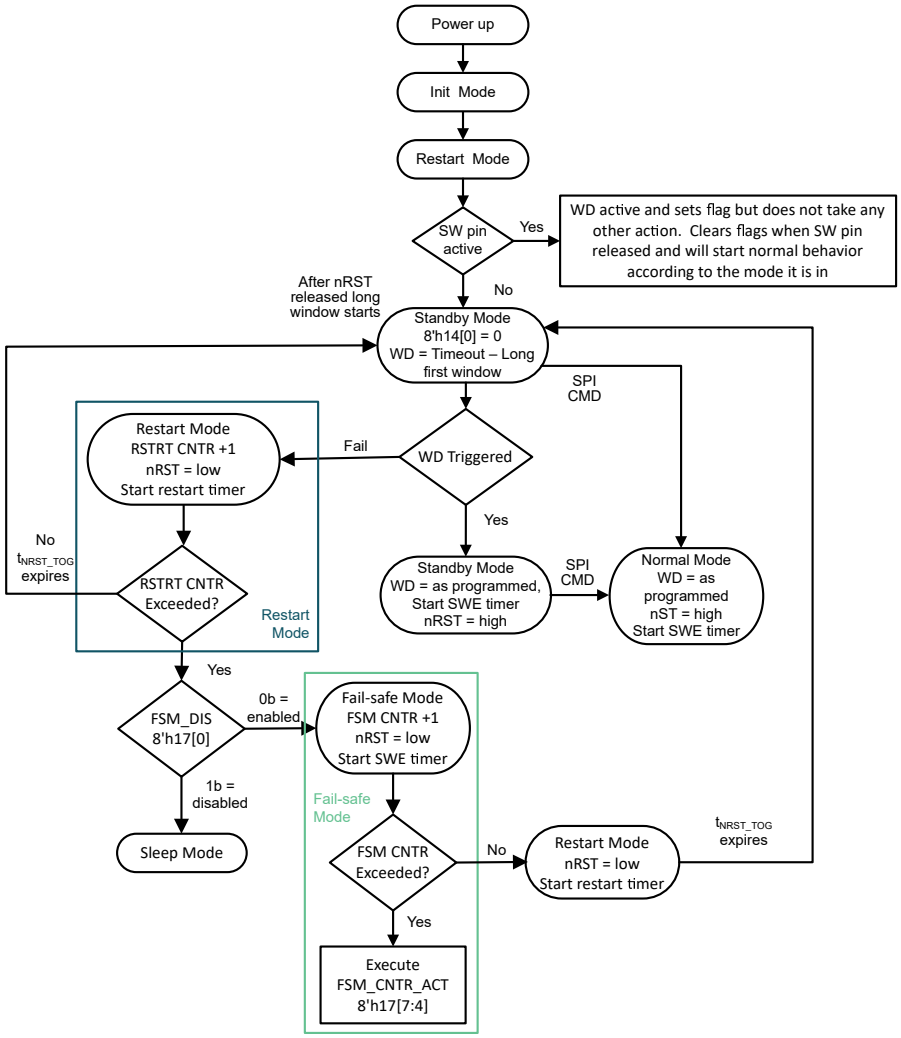


Figure 8-58. Watchdog in Standby Mode

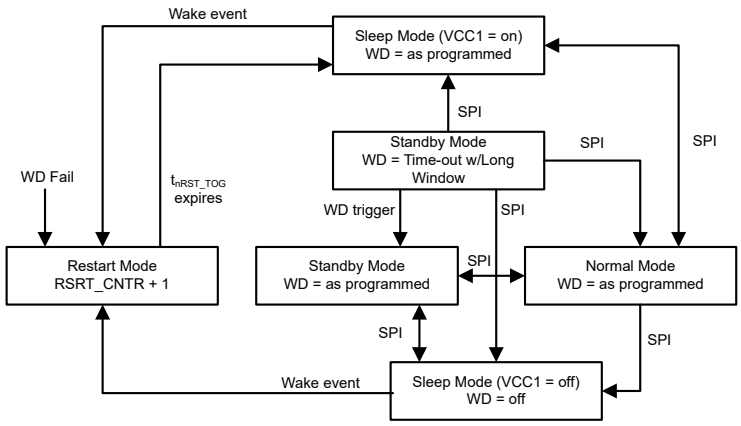


Figure 8-59. Watchdog in Sleep Mode

Note

- When the mode is changed the watchdog timer does not restart. If standby mode is configured for timeout and the Q&A watchdog is enabled, the recommendation is to trigger the watchdog in standby mode prior to changing to normal mode to avoid a watchdog error by missing answers due to limited window time.
- When changing the WD timer value from a longer value to a shorter value, provide a WD trigger before programing the shorter value to avoid a WD error.

8.4.8.9.1 Watchdog Error Counter and Action

The device has a watchdog error counter. This counter is an up down counter that increments for every missed window or incorrect input watchdog trigger event. For every correct input trigger, the counter decrements but does not drop below zero. The default trigger for this counter is to trigger a watchdog event is for every event. This counter can be configured at register 8'h16[7:4] which sets the limit for incorrect input triggers up to 15. The error counter can be read at register 8'14[4:1].

Once the programmed WD error counter limit has been exceeded, the device transitions to restart mode which pulls nRST low for t_{NRST_TOG}. The error counter resets back to 0 at this point. Once t_{NRST_TOG} times out the device transitions back to standby mode releasing nRST high. If the WD failure causes the restart counter to exceed the programmed limit, the device transitions to either fail-safe mode if enabled or to sleep mode.

8.4.8.9.2 Watchdog SPI Programming

Registers 8’h13, 8'h14, and 8’h16 configure the watchdog function. The TCAN285x-Q1 watchdog can be set as a timeout, window, or Q&A watchdog by setting 8’h13[6] to the method of choice. The timer, t_{WD}, for each of these watchdog configurations is based upon registers 8’h13[5:4] WD prescaler and 8’h14[7:5] WD timer and is in ms. See Table 8-15 for the achievable times and more detail. If using smaller time windows, use the timeout version of the watchdog, but not required. This is for times between 4ms and 64ms. The programmed time is also used for the Q&A watchdog which is programmed at registers 8'h2D through 8'h2F where 8'h2D is the configuration register.

Table 8-15. Timeout, Window, and Q&A Watchdog Timer (t_{WD}) Configuration (ms)

WD_TIMER	8'h13[5:4] WD_PRE			
8'h14[7:5]	**00 (default)**	01	10	11
000	4	8	12	16
001	32	64	96	128
010	128	256	384	512
011 (default)	**256**	384	512	768
100	512	1024	1536	2048
101	2048	4096	6144	8192
110	10240	20240	RSVD	RSVD
111	RSVD	RSVD	RSVD	RSVD

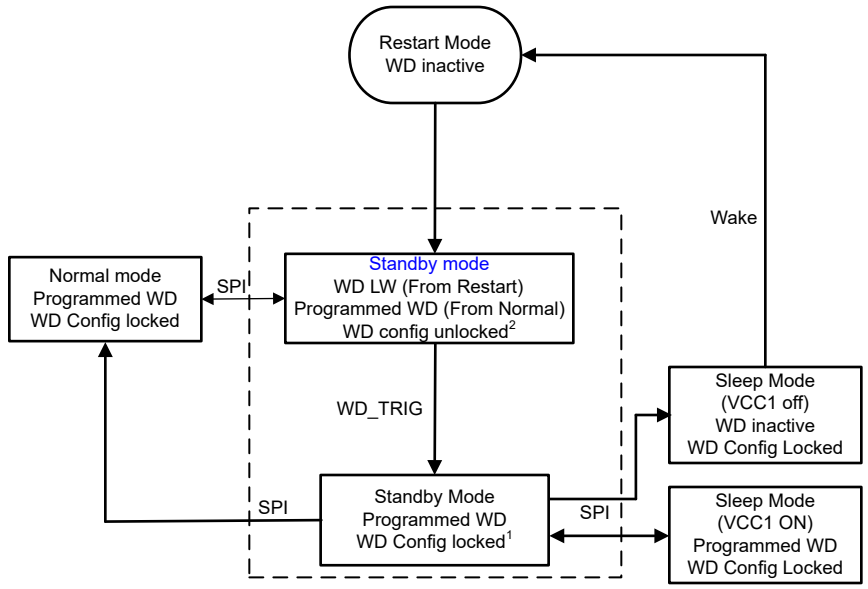
Note

The watchdog timing can only be configured in standby mode if unlocked.

8.4.8.9.2.1 Watchdog Configuration Registers Lock and Unlock

To avoid inadvertent watchdog configuration changes, the TCAN285x-Q1 family implements a watchdog configuration register locking and unlocking mechanism. Registers 8'h13, 8'h14, 8'16 and 8'h2D are only programmable in standby mode and are the registers that become locked. These registers automatically lock with the first WD input trigger event or when transitioning to normal mode via SPI command. The unlocking mechanism is transitioning to standby mode; which allows one write to each of the four registers. If the registers are locked while in standby mode, the device must transition to normal mode and then back to standby mode.

The WD can be enabled in sleep mode and is only capable of timeout and the configuration registers are locked. See Figure 8-60;which shows the described behavior.



1 As long as SW pin is active in Standby mode, WD is unlocked for programming in Standby mode
2 Allows one write to registers 8'h13, 8'h14, 8'h16 and 8'h2D before WD trigger.

Figure 8-60. Watchog Configuration Registers Locking and Unlocking Flow Chart

8.4.8.9.3 Watchdog Timing

The TCAN285x-Q1 provides three methods for setting up the watchdog, window, timeout and question and answer. Question and Answer watch dog is covered in Question and Answer Watchdog. Refer to Figure 8-61 for the Timeout watchdog timing diagram. Timeout watchdog has an internal accuracy of ±15%.

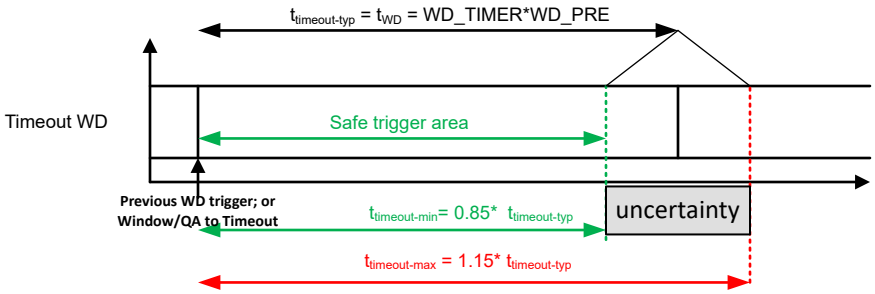


Figure 8-61. Timeout Watchdog Timing Diagram

When using the window watchdog, understanding the closed and open window aspects is important. The device is set up with a 50%/50% open and closed window, and is based on an internal oscillator with a ±10% accuracy range. To determine when to provide the input trigger, the variance needs to be considered. Using the 64ms nominal total window, t_{WINDOW}, provides a closed and open window that are each 32ms. Taking the ±10% internal oscillator into account means t_{WINDOW} can be between 57.6ms and 70.4ms. The closed, t_{CLOSED}, and open window, t_{OPEN}, are between 28.8ms and 35.2ms. Using $t_{OPEN-MIN}$ of 57.6ms and $t_{CLOSED-MAX}$ of 35.2ms, the available safe trigger window is 22.4ms long. The safe trigger area needs to happen at the 46.4ms ± 11.2ms which is half the t_{OPEN} min + t_{CLOSED} max. The same method is used for the other window values. Figure 8-62 provides the above information graphically. This also describes the response 1 and response 2 windows for the Q&A watchdog.

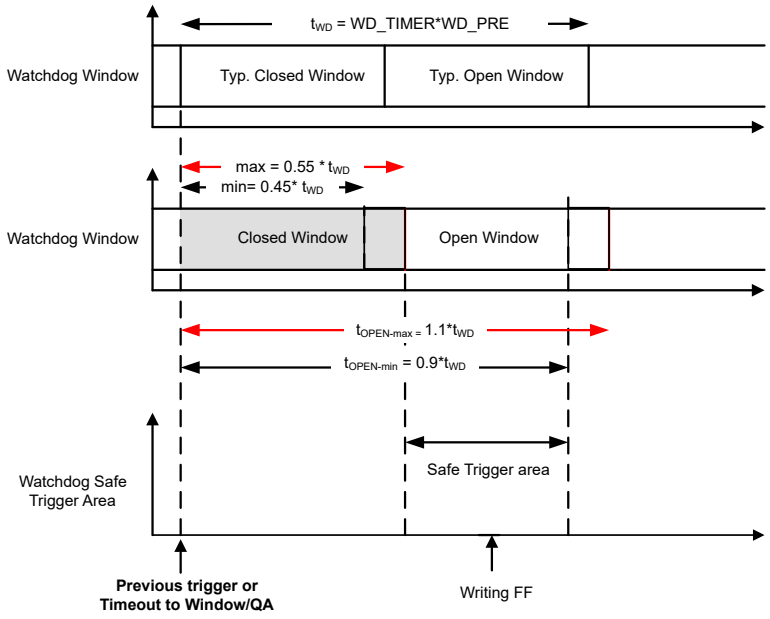


Figure 8-62. Window Watchdog Timing Diagram

8.4.8.9.4 Question and Answer Watchdog

The devices include a question and answer watchdog selectable from SPI. Device defaults to window watchdog.

Question and Answer WD Example explains the WD initialization events.

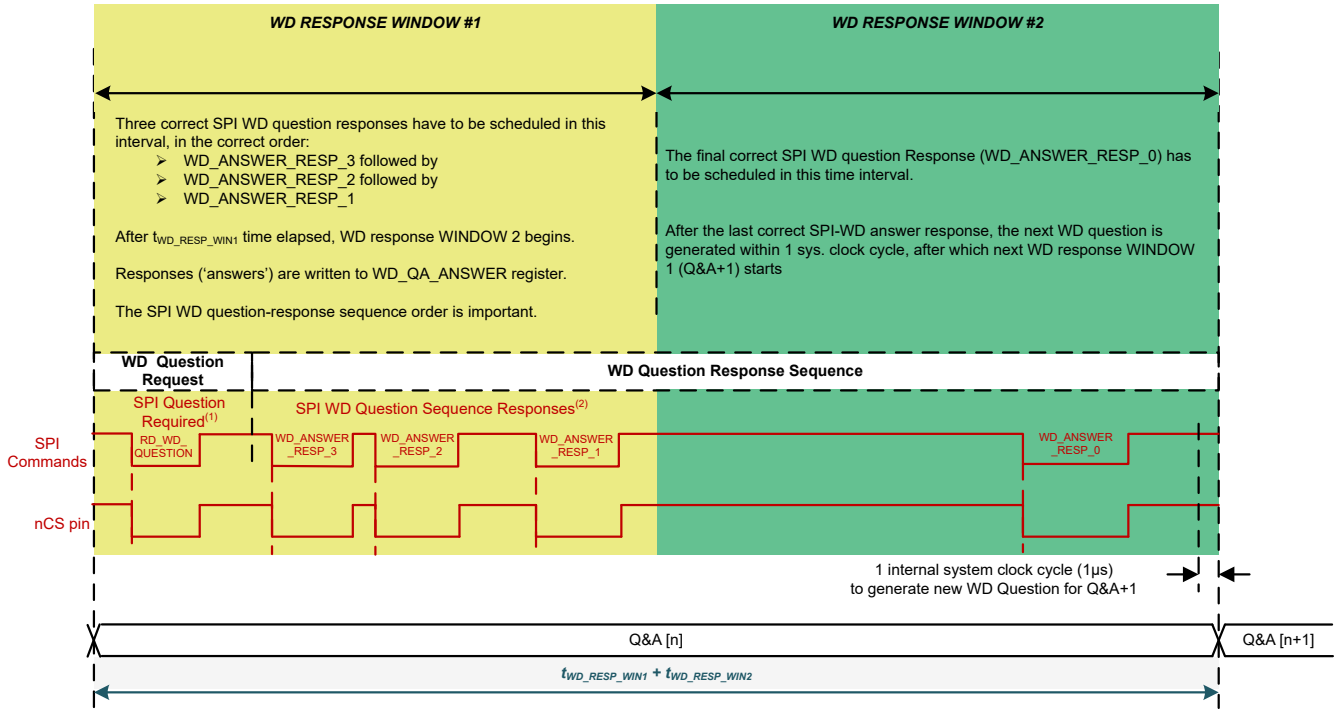
8.4.8.9.4.1 WD Question and Answer Basic Information

A Question and Answer (Q&A) watchdog is a type of watchdog where instead of simply resetting the watchdog via a SPI write, the MCU must read a 'question' from the device, do math based on the question, and then write the computed answers back to the device. The correct answer is a 4-byte response. Each byte must be written in order, and with the correct timing to have a correct answer.

There are 2 watchdog windows, referred to as WD Response window #1 and WD Response window #2 (Figure 8-63 WD QA Windows as example). The size of each window is 50% of the total watchdog window time, $t_{WD\_RESP\_WIN1}$ + $t_{WD\_RESP\_WIN2}$, which is selected from the WD_TIMER and WD_PRE register bits.

Each watchdog question and answer is a full watchdog cycle. The general process is that the MCU reads the question during WD Response Window #1. The CPU must perform a mathematical function on the question, resulting in 4 bytes of answers. 3 of the 4 answer bytes must be written to the answer register within the WD Response Window #1, in correct order. The last answer must be written to the answer register after the first response window, inside of WD Response Window #2. If all 4 answer bytes are correct and in the correct order, then the response is considered good, the error counter is decremented and a new question is generated, starting the cycle over again. Once the fourth answer is written into WD Response Window #2, that window is terminated and a new WD Response Window #1 is started.

If anything is incorrect or missed, the response is considered bad and the watchdog question does NOT change. In addition, an error counter is incremented. Once this error counter exceeds the threshold (defined in the WD_ERR_CNT_SET register field), the watchdog failure action is performed. Examples of actions are an interrupt, or reset toggle, and so on.



A. The MCU is not required to request the WD question. The MCU can start with correct answers, WD_ANSWER_RESP_x bytes anywhere within RESPONSE WINDOW 1. The new WD question is always generated within one system clock cycle after the final WD_ANSWER_RESP_0 answer during the previous WD Q&A sequence run.

B. The MCU can schedule other SPI commands between the WD_ANSWER_RESPx responses (even a command requesting the WD question) without any impact to the WD function as long as the WD_ANSWER_RESP_[3:1] bytes are provided within the RESPONSE WINDOW 1 and WD_ANSWER_RESP_0 is provided within the RESPONSE WINDOW 2.

Figure 8-63. WD Q&A Sequence Run

8.4.8.9.4.2 Question and Answer Register and Settings

There are several registers used to configure the watchdog registers, see Table 8-16.

Table 8-16. List of Watchdog Related Registers

Register Address	Register Name	Description
0x13	WD_CONFIG_1	Watchdog configuration and action in event of a failure
0x14	WD_CONFIG_2	Sets the time of the window, and shows current error counter value
0x15	WD_INPUT_TRIG	Register to reset or start the watchdog
0x16	WD_RST_PULSE	Sets error counter threshold
0x2D	WD_QA_CONFIG	Configuration related to the QA configuration
0x2E	WD_QA_ANSWER	Register for writing the calculated answers
0x2F	WD_QA_QUESTION	Reading the current QA question

The WD_CONFIG_1 and WD_CONFIG_2 registers primarily handle setting up the watchdog window time length. Refer to Table 8-15 to see the options for window sizes, and the required values for the WD_TIMER values and WD_PRE values. Take note that each of the 2 response windows are half of the selected value. Due to the need for several bytes of SPI to be used for each watchdog QA event, the windows must be greater than 64ms be used when using the QA watchdog functionality.

There are also different actions that can be performed when the watchdog error counter exceeds the error counter threshold.

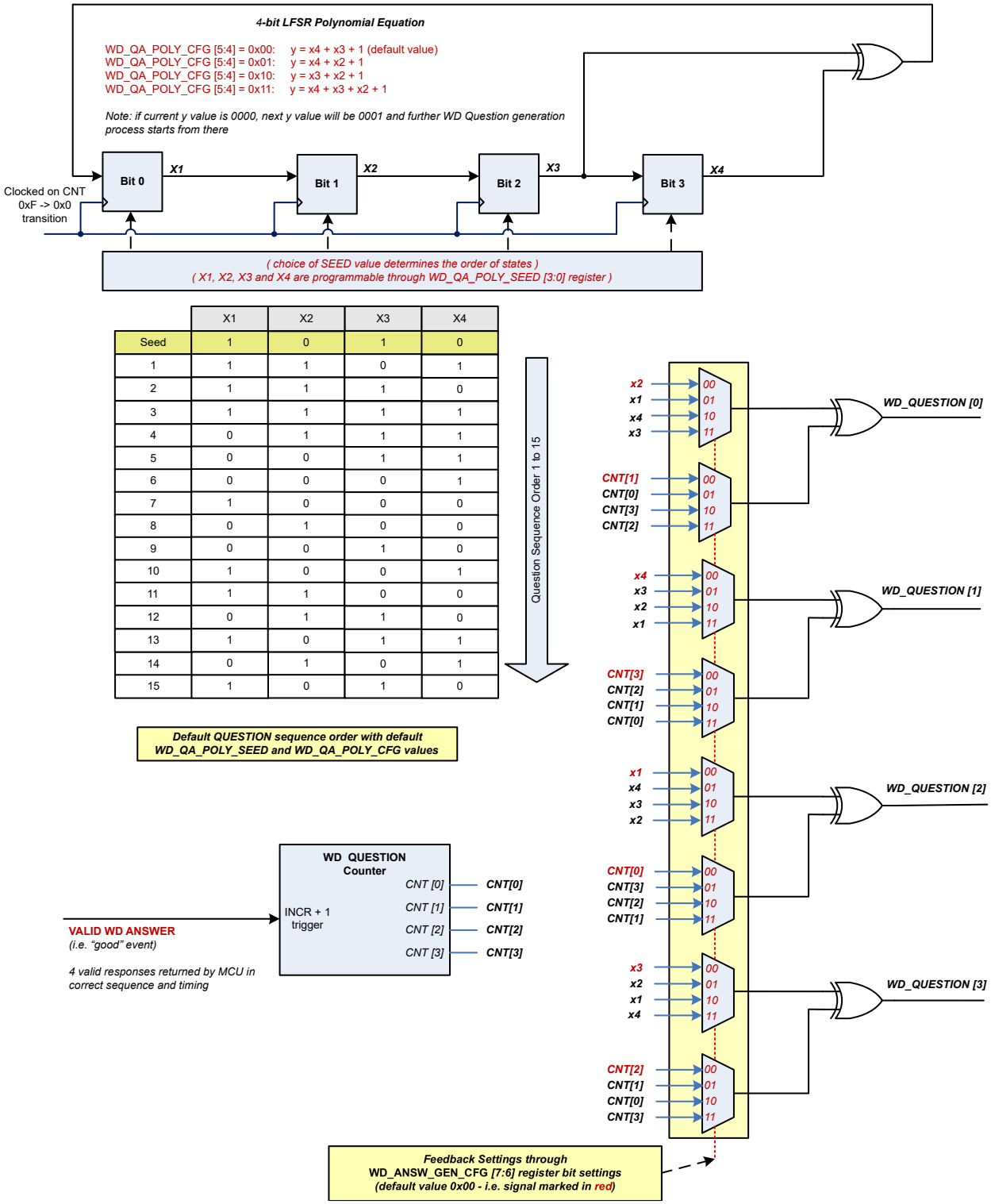
8.4.8.9.4.3 WD Question and Answer Value Generation

The 4-bit WD question, WD_QA_QUESTION[3:0], is generated by 4-bit Markov chain process. A Markov chain is a stochastic process with Markov property, which means that state changes are probabilistic, and the future state depends only on the current state. The valid and complete WD answer sequence for each WD Q&A mode is as follows:

- WD Q&A mode expectations:
  1. Three correct SPI WD answers are received during RESPONSE WINDOW 1.
  2. One correct SPI WD answer is received during RESPONSE WINDOW 2.
  3. In addition to the previously listed timing, the sequence of four responses shall be correct.

The WD question value is latched in the WD_QUESTION bits of the WD_QA_QUESTION register and can be read out at any time.

The Markov chain process is clocked by the 4-bit Question counter at the transition from 1111b to 0000b. This includes the condition of a correct answer (correct answer value and correct timing response). The logic combination of the 4-bit questions WD_QA_QUESTION [3:0] generation is given in Figure 8-64. The question counter is reset to default value of 0000b and the Markov chain is re-initialized to programmed register value when a watchdog fail puts the device in restart mode.



	X1	X2	X3	X4
Seed	1	0	1	0
1	1	1	0	1
2	1	1	1	0
3	1	1	1	1
4	0	1	1	1
5	0	0	1	1
6	0	0	0	1
7	1	0	0	0
8	0	1	0	0
9	0	0	1	0
10	1	0	0	1
11	1	1	0	0
12	0	1	1	0
13	1	0	1	1
14	0	1	0	1
15	1	0	1	0

A. • Register 8'h2D[3:0] WD_QA_POLY_SEED maps as bit 3 = X1, bit 2 = X2. bit 1 = X3 and bit 0 = X4.
• If the current *y* value is 0000, the next *y* value is 0001. The next watchdog question generation process starts from that value. Any changes to WD_QA_CONFIG register in Standby mode re-initializes the Markov chain to the current register value. The question counter is not affected.

Figure 8-64. Watchdog Question Generation

8.4.8.9.4.3.1 Answer Comparison

The 2-bit, watchdog-answer counter, WD_ANSW_CNT[1:0], counts the number of received answer-bytes and controls the generation of the reference answer-byte as shown in Figure 8-65. At the start of each watchdog sequence, the default value of the WD_ANSW_CNT[1:0] counter is 11b to indicate that the watchdog expects the MCU to write the correct Answer-3 in WD_QA_ANSWER[7:0].

The device sets the WD_QA_ERR status bit as soon as one answer byte is not correct. The device clears this status bit only if the MCU writes a '1' to this bit.

8.4.8.9.4.3.2 Sequence of the 2-bit Watchdog Answer Counter

The sequence of the 2-bit, watchdog answer-counter is as follows for each counter value:

- WD_ANSW_CNT[1:0] = 11b:
  1. The watchdog calculates the reference Answer-3.
  2. A write access occurs. The MCU writes the Answer-3 byte in WD_QA_ANSWER[7:0].
  3. The watchdog compares the reference Answer-3 with the Answer-3 byte in WD_QA_ANSWER[7:0].
  4. The watchdog decrements the WD_ANSW_CNT[1:0] bits to 10b and sets the WD_QA_ERR status bit to 1 if the Answer-3 byte is incorrect.
- WD_ANSW_CNT[1:0] = 10b:
  1. The watchdog calculates the reference Answer-2.
  2. A write access occurs. The MCU writes the Answer-2 byte in WD_QA_ANSWER[7:0].
  3. The watchdog compares the reference Answer-2 with the Answer-2 byte in WD_QA_ANSWER[7:0].
  4. The watchdog decrements the WD_ANSW_CNT[1:0] bits to 01b and sets the WD_QA_ERR status bit to 1 if the Answer-2 byte is incorrect.
- WD_ANSW_CNT[1:0] = 01b:
  1. The watchdog calculates the reference Answer-1.
  2. A write access occurs. The MCU writes the Answer-1 byte in WD_QA_ANSWER[7:0].
  3. The watchdog compares the reference Answer-1 with the Answer-1 byte in WD_QA_ANSWER[7:0].
  4. The watchdog decrements the WD_ANSW_CNT[1:0] bits to 00b and sets the WD_QA_ERR status bit to 1 if the Answer-1 byte is incorrect.
- WD_ANSW_CNT[1:0] = 00b:
  1. The watchdog calculates the reference Answer-0.
  2. A write access occurs. The MCU writes the Answer-0 byte in WD_QA_ANSWER[7:0].
  3. The watchdog compares the reference Answer-0 with the Answer-0 byte in WD_QA_ANSWER[7:0].
  4. The watchdog sets the WD_QA_ERR status bit to 1 if the Answer-0 byte is incorrect.
  5. The watchdog starts a new watchdog sequence and sets the WD_ANSW_CNT[1:0] to 11b.

The MCU needs to clear the bit by writing a '1' to the WD_QA_ERR bit

Table 8-17. Set of WD Questions and Corresponding WD Answers Using Default Setting

QUESTION IN WD_QA_QUESTION REGISTER	WD ANSWER BYTES (EACH BYTE TO BE WRITTEN INTO WD_QA_ANSWER REGISTER)			
	WD_ANSWER_RESP_3	WD_ANSWER_RESP_2	WD_ANSWER_RESP_1	WD_ANSWER_RESP_0
WD_QUESTION	WD_ANSW_CNT[1:0] 11b	WD_ANSW_CNT[1:0] 10b	WD_ANSW_CNT[1:0] 01b	WD_ANSW_CNT[1:0] 00b
0x0	FF	0F	F0	00
0x1	B0	40	BF	4F
0x2	E9	19	E6	16
0x3	A6	56	A9	59
0x4	75	85	7A	8A
0x5	3A	CA	35	C5
0x6	63	93	6C	9C
0x7	2C	DC	23	D3
0x8	D2	22	DD	2D
0x9	9D	6D	92	62
0xA	C4	34	CB	3B
0xB	8B	7B	84	74
0xC	58	A8	57	A7
0xD	17	E7	18	E8
0xE	4E	BE	41	B1
0xF	01	F1	0E	FE

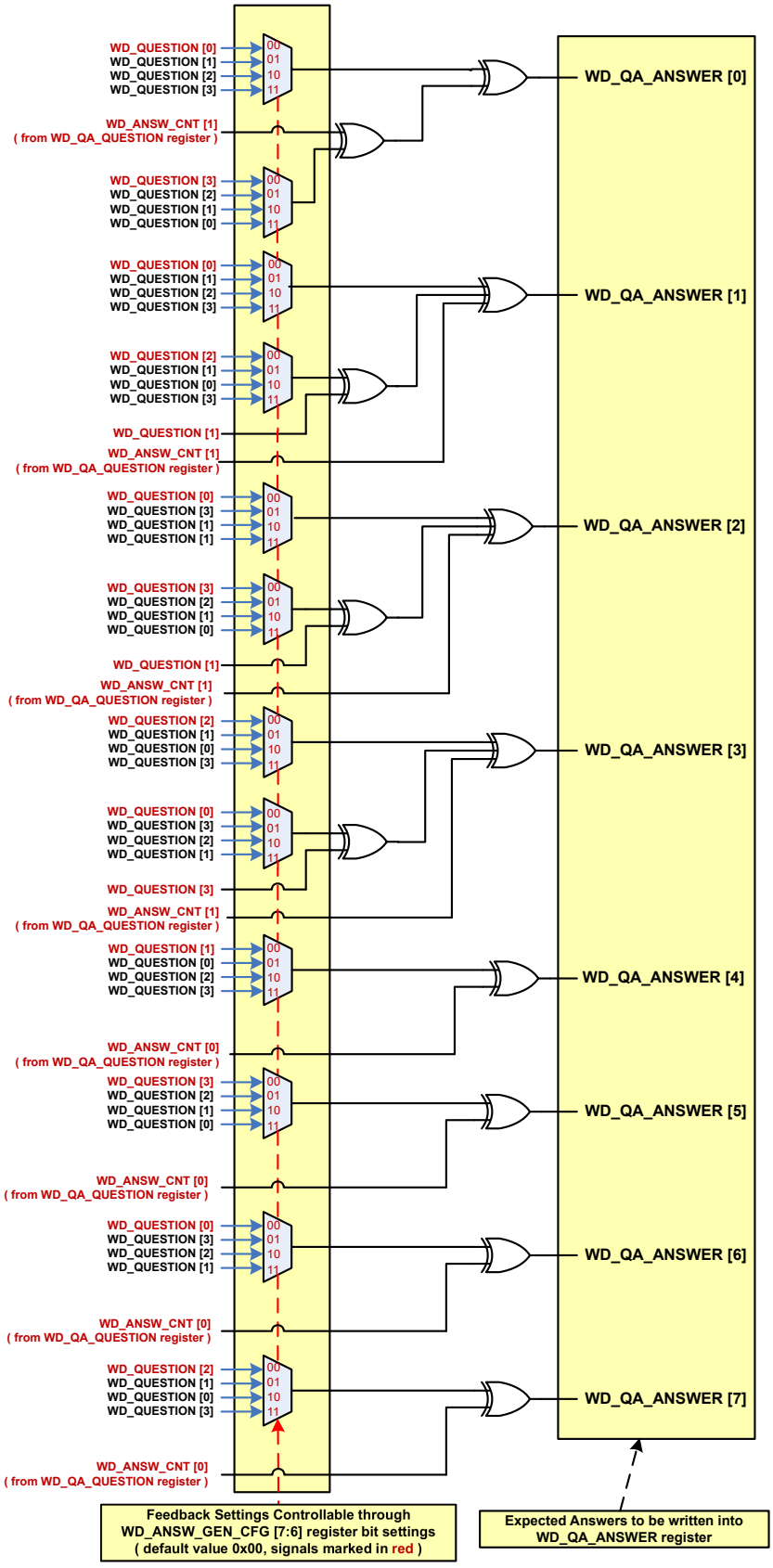


Figure 8-65. WD Expected Answer Generation

Table 8-18. Correct and Incorrect WD Q&A Sequence Run Scenarios

NUMBER OF WD ANSWERS		ACTION	WD_QA_ERR (in WD_QA_QUESTION Register)[1]	COMMENTS
RESPONSE WINDOW 1	RESPONSE WINDOW 2			
0 answer	0 answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	No answer
0 answer	4 INCORRECT answers	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Total Answers Received = 4
0 answer	4 CORRECT answers	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Total Answers Received = 4
0 answer	1 CORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Less than 3 CORRECT ANSWERS in RESPONSE WINDOW 1 and 1 CORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
1 CORRECT answer	1 CORRECT answer			
2 CORRECT answers	1 CORRECT answer			
0 answer	1 INCORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Less than 3 CORRECT ANSWERS in RESPONSE WINDOW 1 and 1 INCORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
1 CORRECT answer	1 INCORRECT answer			
2 CORRECT answers	1 INCORRECT answer			
0 answer	4 CORRECT answers	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Less than 3 CORRECT ANSWERS in WIN1 and more than 1 CORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] = 4)
1 CORRECT answer	3 CORRECT answers			
2 CORRECT answer	2 CORRECT answers			
0 answer	4 INCORRECT answers	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Less than 3 CORRECT ANSWERS in RESPONSE WINDOW 1 and more than 1 INCORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] = 4)
1 CORRECT answer	3 INCORRECT answers			
2 CORRECT answers	2 INCORRECT answers			
0 answer	3 CORRECT answers	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Less than 3 INCORRECT ANSWERS in RESPONSE WINDOW 1 and more than 1 CORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
1 INCORRECT answer	2 CORRECT answers	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	
2 INCORRECT answers	1 CORRECT answer			
0 answer	3 INCORRECT answers	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Less than 3 INCORRECT ANSWERS in RESPONSE WINDOW 1 and more than 1 INCORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
1 INCORRECT answer	2 INCORRECT answers			
2 INCORRECT answers	1 INCORRECT answer			
0 answer	4 CORRECT answers	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Less than 3 INCORRECT ANSWERS in RESPONSE WINDOW 1 and more than 1 CORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] = 4)
1 INCORRECT answer	3 CORRECT answers		1b	
2 INCORRECT answers	2 CORRECT answers			
0 answer	4 INCORRECT answers	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Less than 3 INCORRECT ANSWERS in RESPONSE WINDOW 1 and more than 1 INCORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] = 4)
1 INCORRECT answer	3 INCORRECT answers			
2 INCORRECT answers	2 INCORRECT answers			
3 CORRECT answers	0 answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD Question	1b	Less than 4 CORRECT ANSWERS in RESPONSE WINDOW 1 and more than 0 ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
2 CORRECT answers	0 answer		1b	
1 CORRECT answer	0 answer			
3 CORRECT answers	1 CORRECT answer	-New WD cycle starts after the 4th WD answer -Decrement WD failure counter -New WD cycle starts with a new WD question	0b	CORRECT SEQUENCE
3 CORRECT answers	1 INCORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Total Answers Received = 4
3 INCORRECT answers	0 answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Total Answers Received < 4
3 INCORRECT answers	1 CORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Total Answers Received = 4

Table 8-18. Correct and Incorrect WD Q&A Sequence Run Scenarios (continued)

NUMBER OF WD ANSWERS		ACTION	WD_QA_ERR (in WD_QA_QUESTION Register)(1)	COMMENTS
RESPONSE WINDOW 1	RESPONSE WINDOW 2			
3 INCORRECT answers	1 INCORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Total Answers Received = 4
4 CORRECT answers	Not applicable	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	
3 CORRECT answers + 1 INCORRECT answer	Not applicable	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	4 CORRECT or INCORRECT ANSWERS in RESPONSE WINDOW 1
2 CORRECT answers + 2 INCORRECT answers	Not applicable			
1 CORRECT answer + 3 INCORRECT answers	Not applicable			

(1) WD_QA_ERR is the logical OR of all QA watchdog errors

8.4.8.9.4.4 Question and Answer WD Example

For this example, see the single sequence with the following configuration settings, Table 8-19.

Table 8-19. WD Function Initialization

Item	Value	Description
Watchdog window size	1024ms	Window size of 1024ms
Answer Generation Option	0 (default)	Answer generation configuration
Question Polynomial	0 (default)	Polynomial used to generate the question
Question polynomial seed	A (default)	Polynomial seed used to generate questions
WD Error Counter Limit	15	On the 15th fail event, do the watchdog action

8.4.8.9.4.4.1 Example Configuration for Desired Behavior

Table 8-20 configures the part for the example behavior. Most of the settings are power on defaults.

Table 8-20. Example Register Configuration Writes

Step	Register	Data
1	WD_CONFIG_1 (0x13)	[W] 0b11010000 / 0xD0
2	WD_CONFIG_2 (0x14)	[W] 0b10000000 / 0x80
3	WD_RST_PULSE (0x16)	[W] 0b11110000 / 0xF0
4	WDT_QA_CONFIG (0x2D)	[W] 0b00001010 / 0x0A

8.4.8.9.4.4.2 Example of Performing a Question and Answer Sequence

The normal sequence summary is as follows:

1. Read the question
2. Calculate the 4 answer bytes
3. Send 3 of them within the first response window
4. Wait and send the last byte in the second response window

See Table 8-21 for an example of the first loop sequence.

Table 8-21. Example First Loop

Step	Register	Data	Description
1	WD_QA_QUESTION (0x2F)	[R] 0x0C	Read the question. Question is 0x0C
2	WD_QA_ANSWER (0x2E)	[W] 0x58	Write answer 3 (See Table 8-17 Example answers to questions with default settings to see answers)
3	WD_QA_ANSWER (0x2E)	[W] 0xA8	Write answer 2
4	WD_QA_ANSWER (0x2E)	[W] 0x57	Write answer 1
5	WD_QA_ANSWER (0x2E)	[W] 0xA7	Write answer 0 once window 2 has started

At this point, the user can read the WD_QA_QUESTION[6] (0x2F) register to determine if WD_QA_ERR is set.

8.4.8.10 Bus Fault Detection and Communication

The TCAN285x-Q1 provides advanced bus fault detection. The device can determine certain fault conditions and set a status or interrupt flag so that the MCU can understand what the fault is. As with any bus architecture where termination resistors are at each end not every fault can be specified to the lowest level, meaning exact location. The fault detection circuitry is monitoring the CANH and CANL pins (currents) to determine if there is

a short to battery, short to ground, short to each other or opens. From a system perspective the location of the device also determines what can be detected. See Figure 8-66 as an example of node locations and how the nodes can impact the ability to determine the actual fault location. Figure 8-67 through Figure 8-71 show the various bus faults based upon the three-node configuration. Table 8-22 shows what can be detected and by which device.

Bus fault detection is a system level situation. If the fault is occurring at the ECU then the general communication of the bus is compromised. For complete coverage of a node a system level diagnostic step is needed for each node and the ability to communicate this back to a central point.

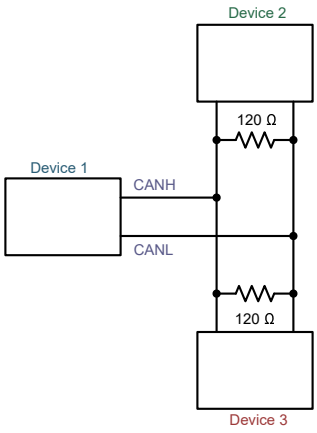


Figure 8-66. Three Node Example

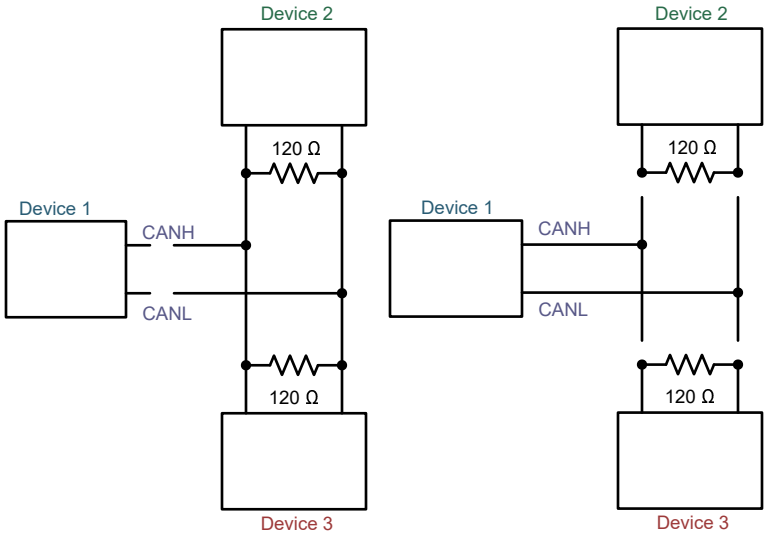


Figure 8-67. Open Fault Examples

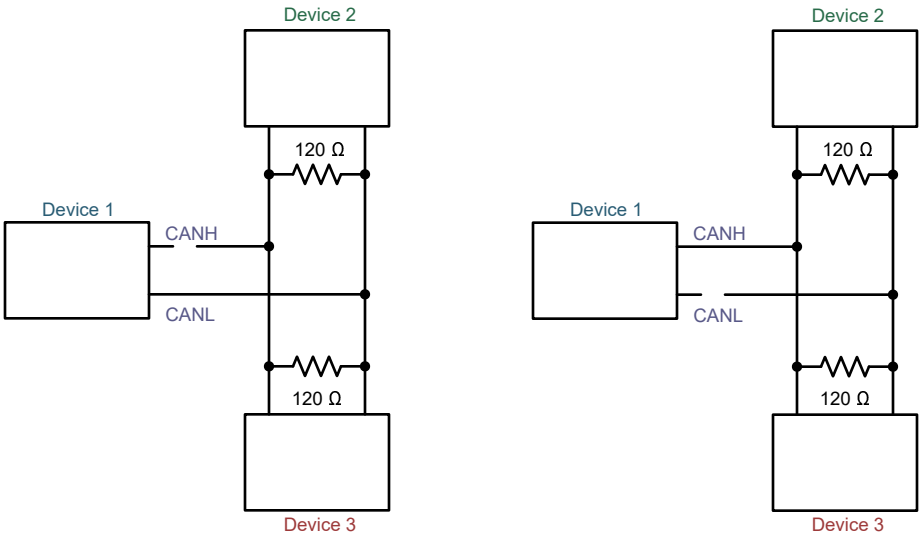


Figure 8-68. Open Faults 3 and 4 Examples

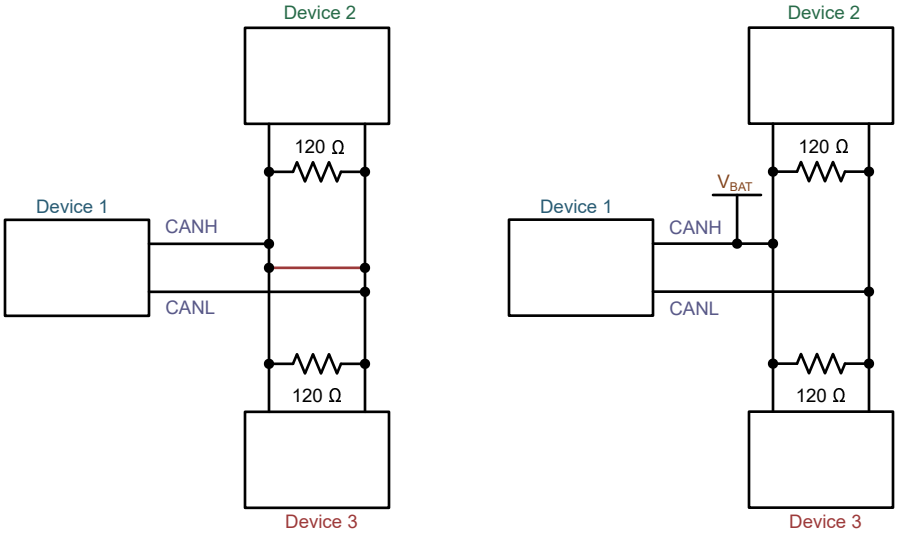


Figure 8-69. Short Faults 5 and 6 Examples

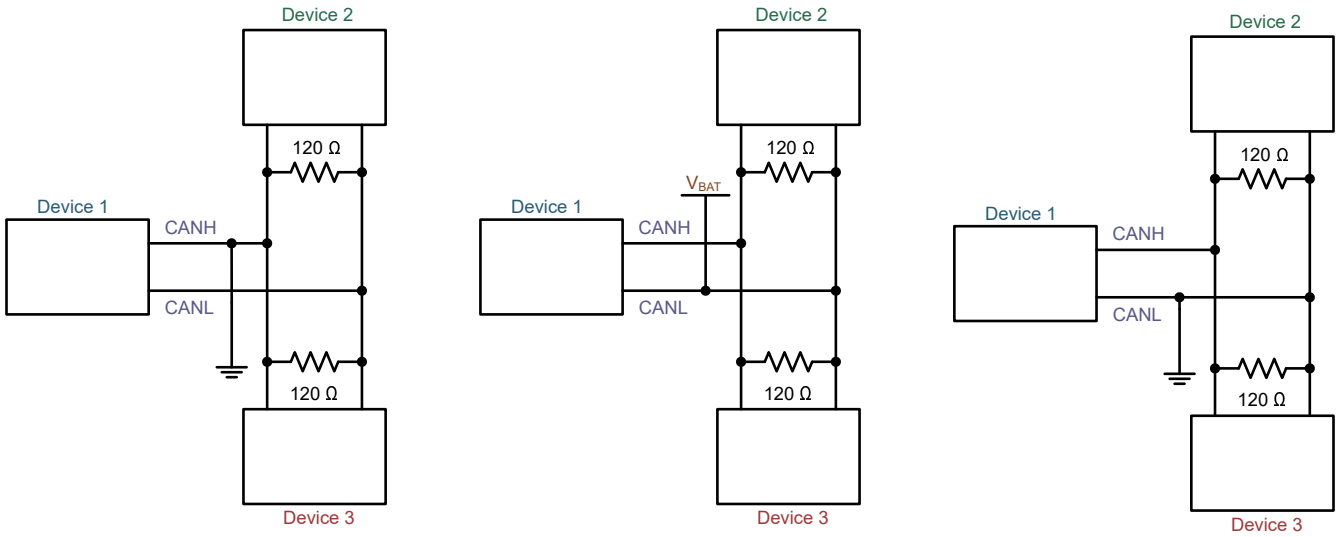


Figure 8-70. Short Faults 7, 8 and 9 Examples

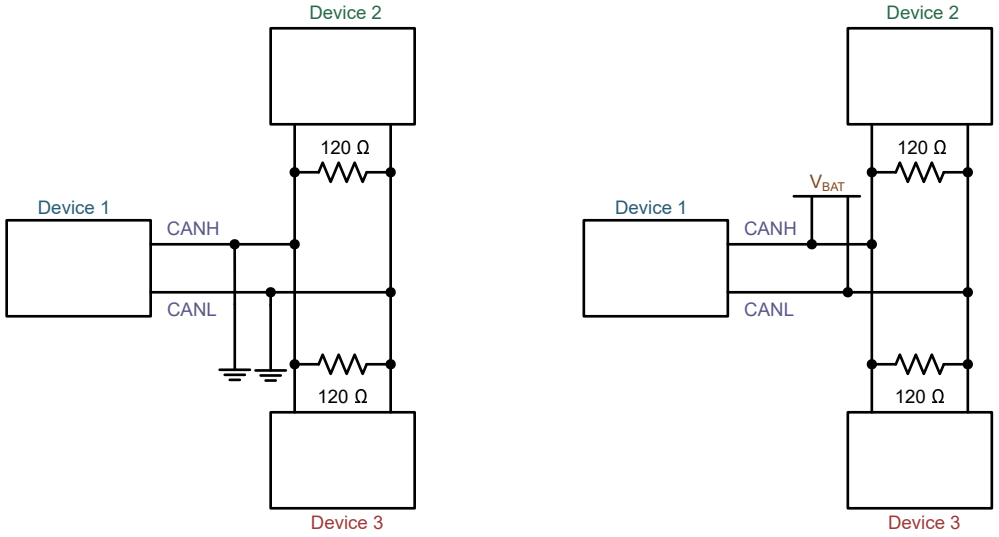


Figure 8-71. Short Faults 10 and 11 Examples

Table 8-22. Bus Fault Pin State and Detection Table

Fault #	CANH	CANL	Fault Detected
2	Open	Open	Depending upon open location the device detects this as no termination.
3	Open	Normal	Yes, but cannot tell the difference between the state and Fault 2 and 4; Device 2 and Device 3 does not see this fault
4	Normal	Open	• Device 1 detects this fault but cannot tell the difference between the state and Fault 2 and 5 • Device 2 and Device 3 does not see this fault
5	Shorted to CANL	Shorted to CANH	Yes, but not location
6	Shorted to V_{bat}	Normal	Yes, but not location
7	Shorted to GND	Normal	Yes, but cannot tell the difference between this and Fault 10
8	Normal	Shorted to V_{bat}	Yes, but cannot tell the difference between this and Fault 11
9	Normal	Shorted to GND	Yes, but not location
10	Shorted to GND	Shorted to GND	Yes, but cannot tell the difference between this and Fault 7

Table 8-22. Bus Fault Pin State and Detection Table (continued)

Fault #	CANH	CANL	Fault Detected
11	Shorted to V_{bat}	Shorted to V_{bat}	Yes, but cannot tell the difference between this and Fault 8

Table 8-23. Bus Fault Interrupt Flags Mapping to Fault Detection Number

Address	BIT(S)	DEFAULT	FLAG	DESCRIPTION	FAULT DETECTED	ACCESS
8'h54	7	1'b0	UVCAN	VCAN under-voltage interrupt	Normal Operation	R/W1C
	6	1'b0	RSVD	Reserved	NA	R
	5	1'b0	CANHCANL	CANH and CANL Shorted Together	Fault 3	R/W1C
	4	1'b0	CANHBAT	CANH Shorted to V_{bat}	Fault 6	R/W1C
	3	1'b0	CANLGND	CANL Shorted to GND	Fault 9	R/W1C
	2	1'b0	CANBUSOPEN	CAN Bus Open (One of three possible places)	Faults 2, 4 and 5	R/W1C
	1	1'b0	CANBUSGND	CANH Shorted to GND or Both CANH & CANL Shorted to GND	Faults 7 and 10	R/W1C
	0	1'b0	CANBUSBAT	CANL Shorted to Vbat or Both CANH & CANL Shorted to Vbat	Faults 8 and 11	R/W1C

8.5 Programming

The TCAN285x-Q1 is a 7-bit address access SPI communication port.

8.5.1 SPI Communication

The SPI communication uses a standard SPI. Physically the digital interface pins are nCS (Chip Select Not), SDI (SPI Data In), SDO (SPI Data Out) and SCK (SPI Clock). Each SPI transaction is initiated by a seven bit address with a R/W bit. The TCAN285x-Q1 can be configured for one data byte or two date bytes per transaction depending upon the value of the BYTE_CNT bit at SPI_CONFIG register 8'h09[3]. The default is one byte. When two byte is selected, the second data byte is for address + 1.

The data shifted out on the SDO pin for the transaction always starts with the register 8'h50[7:0] which is the global interrupt register. This register provides the high-level interrupt status information about the device. The data byte which are the 'response' to the address and R/W byte are shifted out next. See Figure 8-72 and Figure 8-73 for read and write method when cyclic redundancy (CRC) is disabled. For two byte read see Figure 8-75. When a two byte SPI write takes place, the current information in the address and address + 1 is fed back out on the SDO pin, see Figure 8-74.

The device defaults to mode 0 where SPI data input data on SDI is sampled on the low to high edge of SCK. The SPI output data on SDO is changed on the high to low edge of SCK. The device can be configured to support Mode 1 - 3 by using MODE_SEL in SPI_CONFIG register 8'h09[1:0]. SPI communication figures are based upon Mode 0.

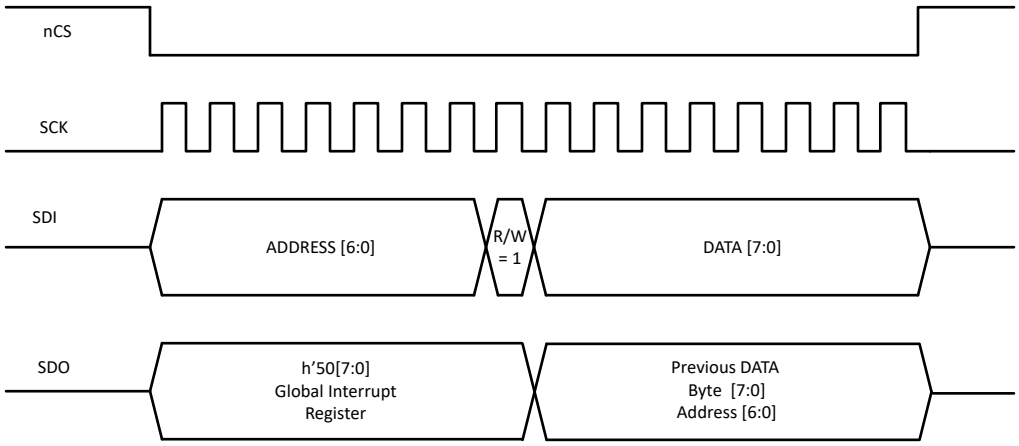


Figure 8-72. SPI Write

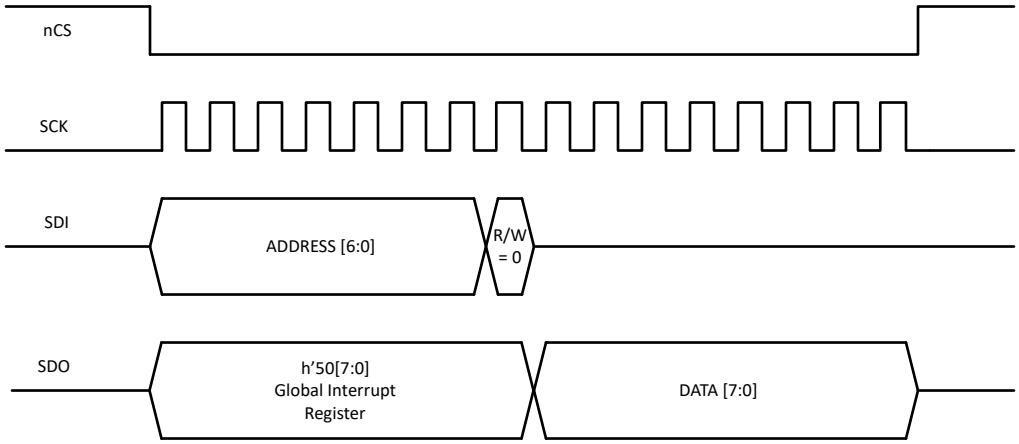


Figure 8-73. SPI Read

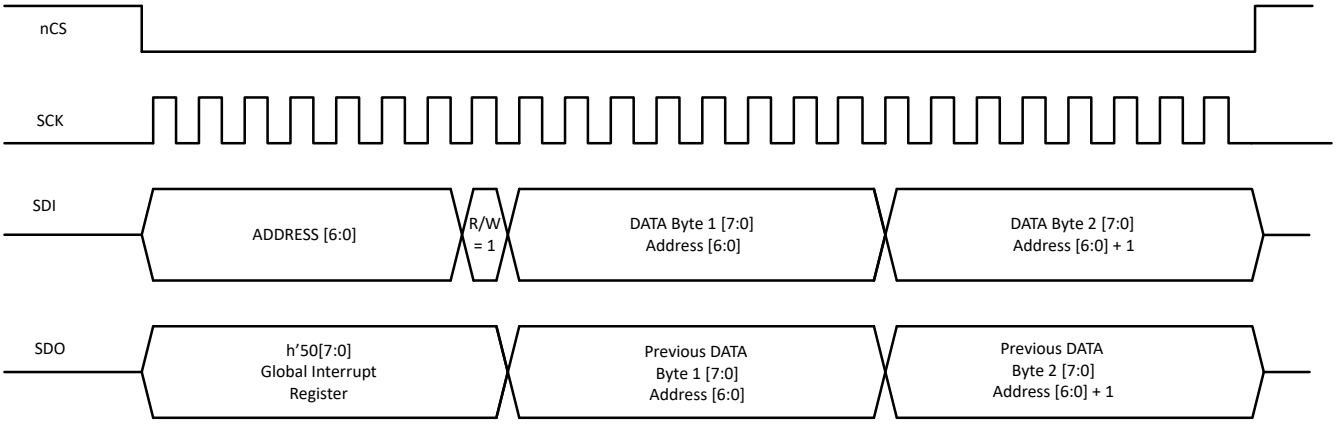


Figure 8-74. Two Byte SPI Write

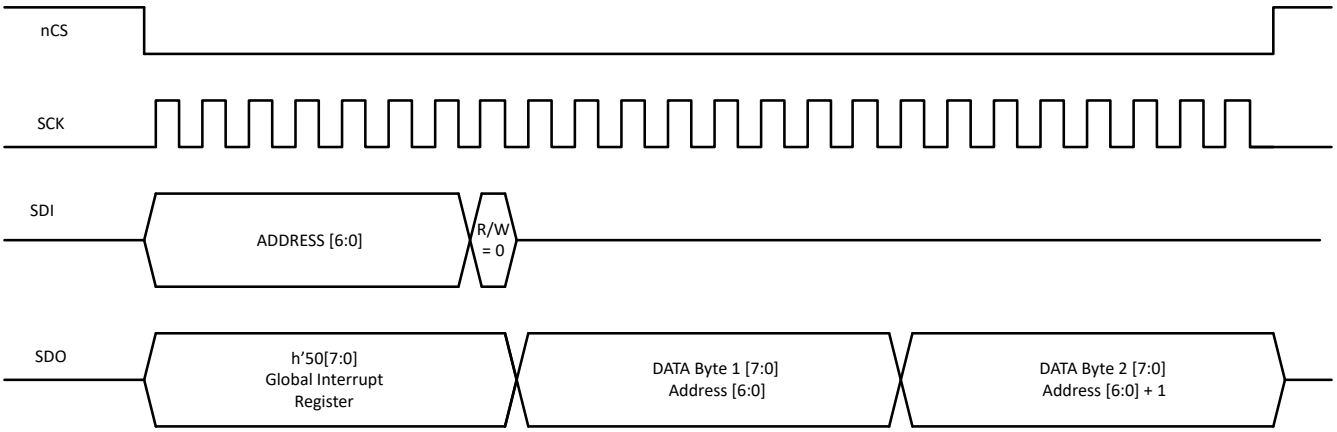


Figure 8-75. Two Byte SPI Read

8.5.1.1 Cyclic Redundancy Check

The TCAN285x-Q1 family cyclic redundancy check (CRC) for SPI transactions, default disabled. Register 'h0A[0] can be used to enable this feature. The default polynomial supports AutoSAR CRC8H2F, $X^8 + X^5 + X^3 + X^2 + X + 1$, see Table 8-24. CRC8 according to SAE J1850 is also supported and can be selected at register 8'h0B[0]. When CRC is enabled, the a filler byte of 00h is used to calculate the CRC value during a read/write operation, see Figure 8-76 and Figure 8-77 for one byte data that includes CRC.

Note

CRC is not implemented when two byte data is configured. Enabling CRC in two-byte mode prevents SPI communication and requires a device reset to recover from the SPI communication loss.

Table 8-24. CRC8H27

SPI Transactions	
CRC result width	8 bits
Polynomial	2Fh
Initial value	FFh
Input data reflected	No
Result data reflected	No
XOR value	FFh
Check	DFh

Table 8-24. CRC8H27 (continued)

SPI Transactions	
Magic Check	42h

Table 8-25. CRC8 SAE J1850

SPI Transactions	
CRC result width	8 bits
Polynomial	1Dh
Initial value	FFh
Input data reflected	No
Result data reflected	No
XOR value	FFh
Check	4Bh
Magic Check	C4h

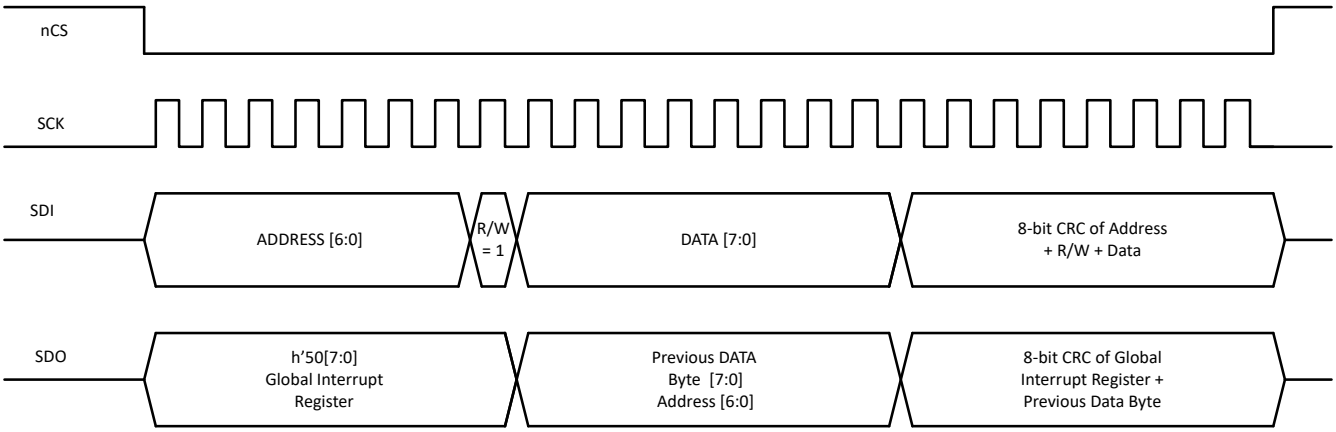


Figure 8-76. One Byte CRC SPI Write

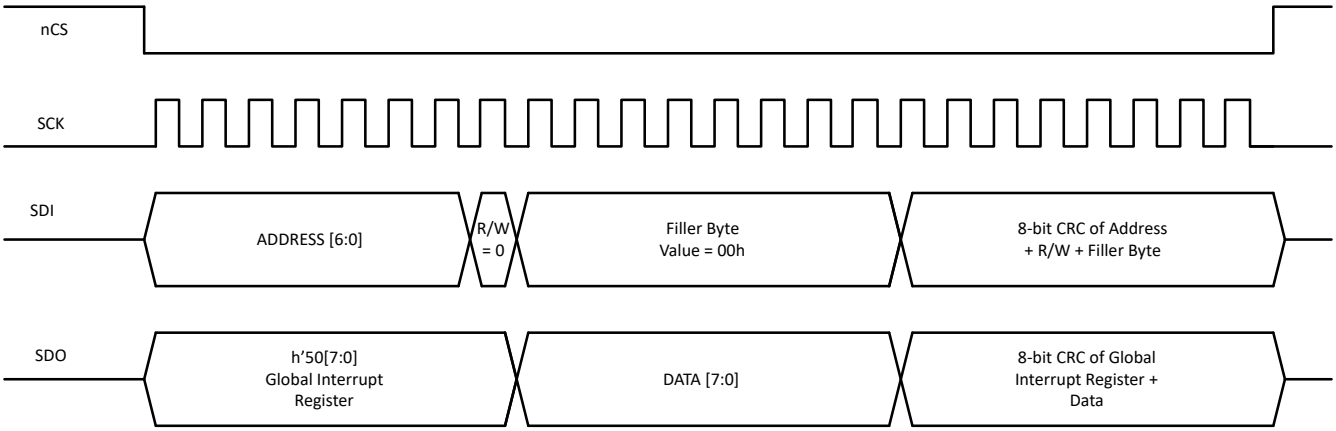


Figure 8-77. One Byte CRC SPI Read

8.5.1.2 Chip Select Not (nCS):

This input pin is used to select the device for a SPI transaction. The pin is active low, so while nCS is high the SPI Data Output (SDO) pin of the device is high impedance allowing an SPI bus to be designed. When nCS is low the SDO driver is activated and communication can be started. The nCS pin is held low for a SPI transaction. A special feature on this device allows the SDO pin to immediately show the Global Fault Flag on a falling edge of nCS.

8.5.1.3 SPI Clock Input (SCK):

This input pin is used to input the clock for the SPI to synchronize the input and output serial data bit streams. The default SPI mode 0 is where data input is sampled on the rising edge of SCK and the SPI data output is changed on the falling edge of the SCK. See Figure 8-78. Figure shown provides the timing based upon Mode 0 which is the default. Table 8-26 provides the configurable modes with the clock phase.

Table 8-26. SPI Modes

Mode	CPOL	CPHA	Clock Phase
0	0	0	Data sampled on rising edge and shifted on falling edge
1	0	1	Data sampled on falling edge and shifted on rising edge
2	1	0	Data sampled on falling edge and shifted on rising edge
3	1	1	Data sampled on rising edge and shifted on falling edge

Note

- CPOL is the clock polarity where 0 = logic low and 1 = logic high
- CPHA is the clock phase

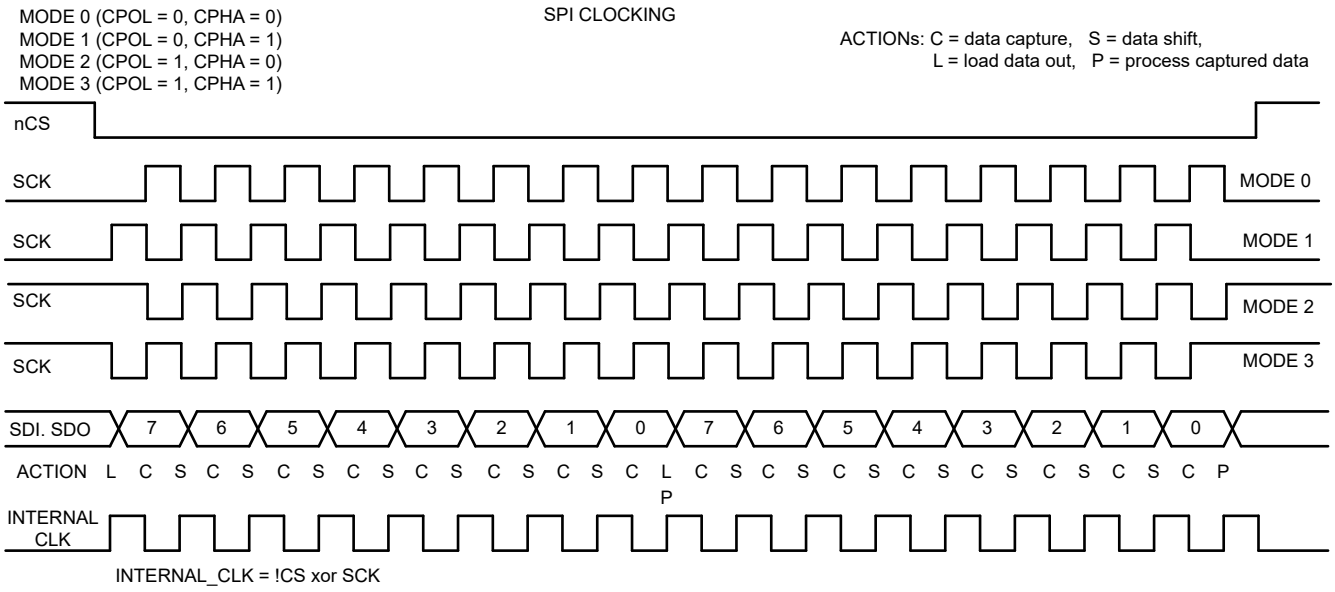


Figure 8-78. SPI Clocking

8.5.1.4 SPI Data Input (SDI):

This input pin is used to shift data into the device. Once the SPI is enabled by a low on nCS, the SDI samples the input shifted data on each rising edge of the SPI clock (SCK). The data is shifted into an 8-bit shift register. After eight (8) clock cycles and shifts, the addressed register is read giving the data to be shifted out on SDO. After eight clock cycles, the shift register is full and the SPI transaction is complete. If the command code is a write, the new data is written into the addressed register only after exactly 8 bits have been shifted in by SCK and the nCS has a rising edge to deselect the device. If there are not exactly 8 bits shifted in to the device during one SPI transaction (nCS low), the SPI command is ignored, the SPIERR flag is set and the data is not written into the device preventing any false actions by the device.

8.5.1.5 SPI Data Output (SDO):

This pin is high impedance until the SPI output is enabled via nCS. Once the SPI is enabled by a low on nCS, the SDO is immediately driven high or low showing the Global Fault Flag status which is also the first bit (bit 7)

to be shifted out if the SPI is clocked. On the first falling edge of SCK, the shifting out of the data continues with each falling edge on SCK until all 8 bits have been shifted out the shift register.

8.5.2 EEPROM

The TCAN285x-Q1 family uses EEPROM for two purposes. The first is for device trimming and is not accessible. This portion of EEPROM is monitored and loaded upon power and when exiting sleep mode, checking for a valid CRC. If the CRC is not valid, this process is performed a total of eight times. If still not valid, INT_3 register 8'h53[0] is set to 1b. This means the device has an issue that can impact the performance and functionality.

The second use of the EEPROM is to allow the user to store specific device configurations. The configuration bits saved are provided in each register. To save the configuration to SPI CRC must be enabled for the save function at a minimum. Saving the configuration to EEPROM is accomplished by writing a 1b to register 8'h4E[7] and default code Ah to 8'h4E[3:0] followed by the CRC byte.

When in one-byte mode, see Table 8-27 for the procedure if the processor does not support CRC. Register 8'h4E[3:0] reads back 0h. Once the configuration bits have been stored to EEPROM, a 0b is read back from 8'h4E[7]. If a power on reset takes place the configuration of the device is reloaded from EEPROM. Table 8-29 provides the list of registers and the bits saved to EEPROM if used.

When two-byte mode needs to be programmed into EEPROM for the first time, or if the device is already in two-byte mode and the device configuration needs be saved in EEPROM, follow the procedure outlined in Table 8-28.

Note

The EEPROM can be reprogrammed a maximum of 500 times.

Table 8-27. Process for non-CRC capable processors (one-byte mode)

Step	Description	Register	Data	Second Data Byte
1	Configure device	See Table 8-29		N/A
2	Set CRC Polynomial • 0x2F AutoSar (00h) • 0X1D SAE J1185 (01h)	8'h0B[0]	• 00h, OR • 01h	N/A
3	Enable SPI CRC if not enable	8'h0A	01h	N/A
4	Save to EERPOM	8'h4E	8Ah	• 36h (CRC POLY_8_SET = 00h) • 0Ch (CRC POLY_8_SET = 01h)
5	Disable SPI CRC if not supported	8'h0A	00h	• Eh (CRC POLY_8_SET = 00h) • 6Bh (CRC POLY_8_SET = 01h)

Table 8-28. Process for Non-CRC Capable Processors (Two-byte Mode)

Step	Description	Register	Data	Second Data Byte
1	Configure the device into two-byte mode (skip this step if a;ready in two-byte mode)	8h'09	80h	N/A
2	Perform any other configurations that need to be saved into EEPROM (Use two-byte SPI writes)	See Table 8-29		
3	Readback register 8h'09/0A to confirm two-byte mode. This step is critical for saving to EEPROM.	8h'09	80h	00h
4	Save to EERPOM	8'h4E	8Ah	36h

The saved configuration can be forced to check if the saved configuration CRC is valid but using register 8'h4E[6], EEPROM_CRC_CHK, = 1b. This takes approximately 200µs to complete. If CRC is valid then no action is taken, If CRC is not valid the device attempts this action eight times. If still not valid afterward the device sets an interrupt indicating there is an issue are INT_4 register 8'h5A[1], EEPROM_CRC_INT.

The following are power and reset scenarios and how the EEPROM is used.

- UVSUP event; no action as registers are not lost
- Power on reset event; EEPROM is read and registers restored in Init mode once VSUP > $UVSUP_{33R}$
- Soft reset; EEPROM is read and registers restored and device transitions to standby mode
- Hard reset; EERPOM is read and registers restored and device transitions to Init mode
- nRST input; EEPROM is read and register restored and device transitions to restart mode

Table 8-29. EEPROM Saved Registers and Bits

Register	Bits Saved
SPI_CONFIG Register (Address = 09h)	0-3
SBC_CONFIG (Address = Ch)	0-1, 6, 7
VREG_CONFIG1 (Address = Dh)	0-7
SBC_CONFIG1 Register (Address = Eh)	0, 3-5, 7
WAKE_PIN_CONFIG1 Register (Address = 11h)	0-4
WAKE_PIN_CONFIG2 Register (Address = 12h)	0-1, 5 , 6
WD_CONFIG_1 Register (Address = 13h)	0-7
WD_CONFIG_2 Register (Address = 14h)	0, 5-7
WD_RST_PULSE Register (Address = 16h)	4-7
DEVICE_CONFIG1 (Address = 1Ah)	0, 4, 7
DEVICE_CONFIG2 (Address = 1Bh)	0
SWE_TIMER (Address = 1Ch)	3-7
nRST_CNTL (Address = 29h)	5
WAKE_PIN_CONFIG4 Register (Address = 2Bh)	0-1, 3, 4-5, 7
WD_QA_CONFIG Register (Address = 2Dh)	0-7
HSS_CNTL3 Register (Address = 4Fh)	0, 4

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TCAN285x-Q1 family supports CAN FD communication while certain device also supports LIN communication

9.1.1 CAN BUS Loading, Length and Number of Nodes

The ISO 11898-2:2024 standard specifies a maximum bus length of 40m and maximum stub length of 0.3m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A high number of nodes require a transceiver with high input impedance such as this transceiver family.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2:2024 standard. These organizations made system level trade off decisions for data rate, cable length, and parasitic loading of the bus. Examples of these CAN systems level specifications are ARINC825, CANopen, DeviceNet, SAEJ2284, SAEJ1939, and NMEA200.

A CAN network system design is a series of tradeoffs. In ISO11898-2 the driver differential output is specified with a 60Ω bus load (the two termination resistors in parallel) where the differential output must be greater than 1.5V. The TCAN285x-Q1 is specified to meet the 1.5V requirement with a across this load range and is specified to meet 1.4V differential output at 45Ω bus load. The differential input resistance of this family of transceiver is a minimum of 30kΩ. If 167 of these transceivers are in parallel on a bus, this is equivalent to an 180Ω differential load in parallel with the 60Ω from termination gives a total bus load of 45Ω. Therefore, this family theoretically supports over 167 transceivers on a single bus segment with margin to the 1.2V minimum differential input voltage requirement at each receiving node. However, for CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is much lower. Bus length can also be extended beyond the original ISO 11898-2:2024 standard of 40m by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths, allowing for the system level network extensions and additional standards to build on the original ISO11898-2 CAN standard. However, when using this flexibility, the CAN network system designer must take the responsibility of good network design for robust network operation.

9.1.2 CAN Termination

The ISO 11898-2:2024 standard specifies the interconnection to be a single twisted pair cable (shielded or unshielded) with 120Ω characteristic impedance (Z_O).

9.1.2.1 Termination

Resistors equal to the characteristic impedance of the line must be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop-lines (stubs) connecting nodes to the bus must be kept as short as possible to minimize signal reflections. The termination can be in a node, but is generally not recommended, especially if the node can be removed from the bus. Termination must be carefully placed, so that the termination is not removed from the bus. System level CAN implementations such as CANopen allow for different termination and cabling concepts for example to add cable length.

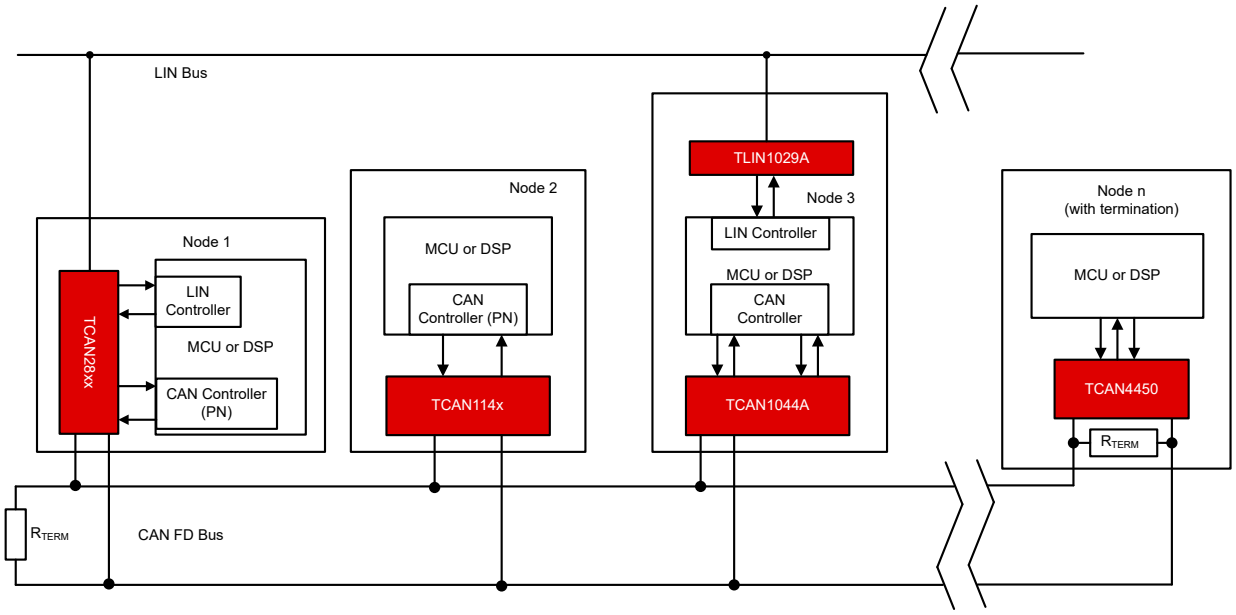


Figure 9-1. Typical CAN FD and LIN Bus

Termination can be a single 120Ω resistor at the end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common mode voltage of the bus is desired then “split termination” can be used, see Figure 9-2. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common mode voltage levels at the start and end of message transmissions.

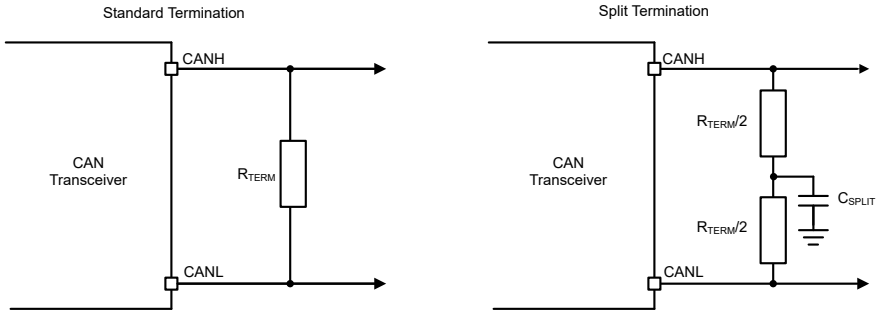


Figure 9-2. CAN Bus Termination Concepts

9.1.3 Channel Expansion

The devices have the ability to control an external LIN or CAN FD transceiver or even other LIN and CAN FD SBCs. The processor controls the mode of the transceiver with the GFO pin as an EN/STB/nSTB/S pin. This capability allows the system implementer the ability to have many different configurations.

- Two CAN FD transceivers by using the TCAN2855-Q1 with an eight pin CAN FD transceiver
- Two CAN FD transceivers and a LIN transceiver by using the TCAN2857-Q1 with an eight pin CAN FD transceiver, see Figure 9-6
- On CAN FD transceiver and two LIN transceivers by using the TCAN2857-Q1 with a LIN transceiver, see Figure 9-4
- A second SBC with a LIN transceiver can be implemented by using the TCAN2857-Q1 and the TLIN1028x, see Figure 9-5
- A second SBC with a CAN transceiver can be implemented by using the TCAN2857-Q1and the TCAN1162x, see Figure 9-7

9.1.3.1 Channel Expansion for LIN

Figure 9-3 and Figure 9-4 show high level diagrams on how the TCAN2855-Q1 or TCAN2857-Q1 can control an external LIN transceiver. Both of these show a high side switch (HSS) providing the power to the transceiver. When the TCAN285x-Q1 goes to sleep mode the HSS is turned off thus turning off the power to the transceiver. If this is not desired the transceiver VSUP can be connected to the same VSUP power as the device. To configure the device to control the LIN transceivers the following register and bits need to be configured.

- Register 29h[3:1] = 110b sets the GFO pin a general purpose output pin
- Register 29h[4] sets the level of the GFO pin, high or low to control the EN pin of a LIN transceiver or LIN SBC
- To use the HSS as the power to the transceiver, turn on the selected HSS

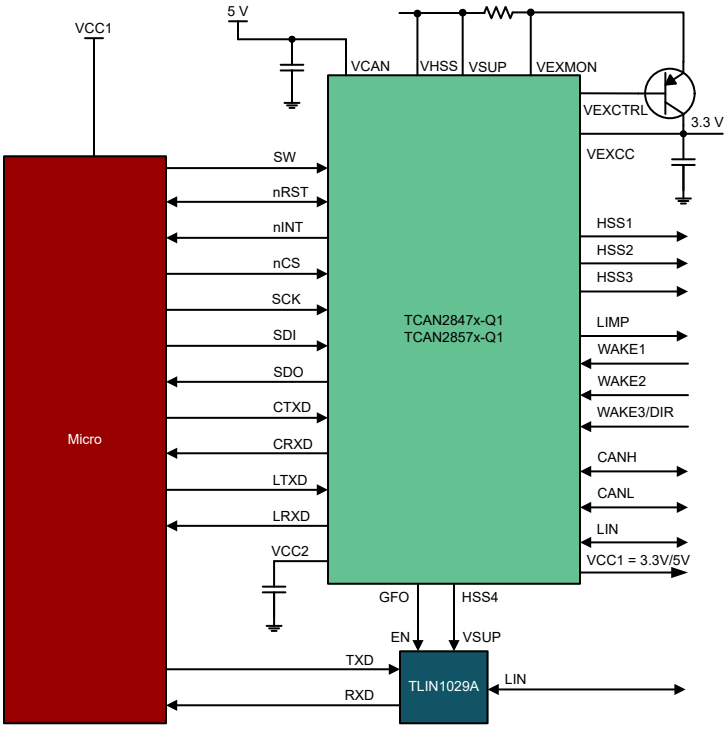


Figure 9-3. Channel Expansion Simple LIN Transceiver

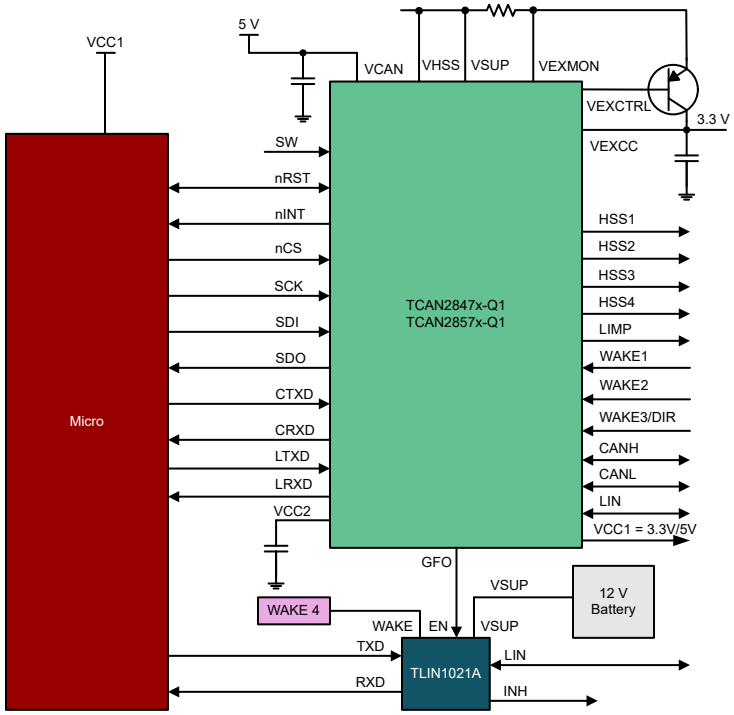


Figure 9-4. Channel Expansion Enhanced LIN Transceiver

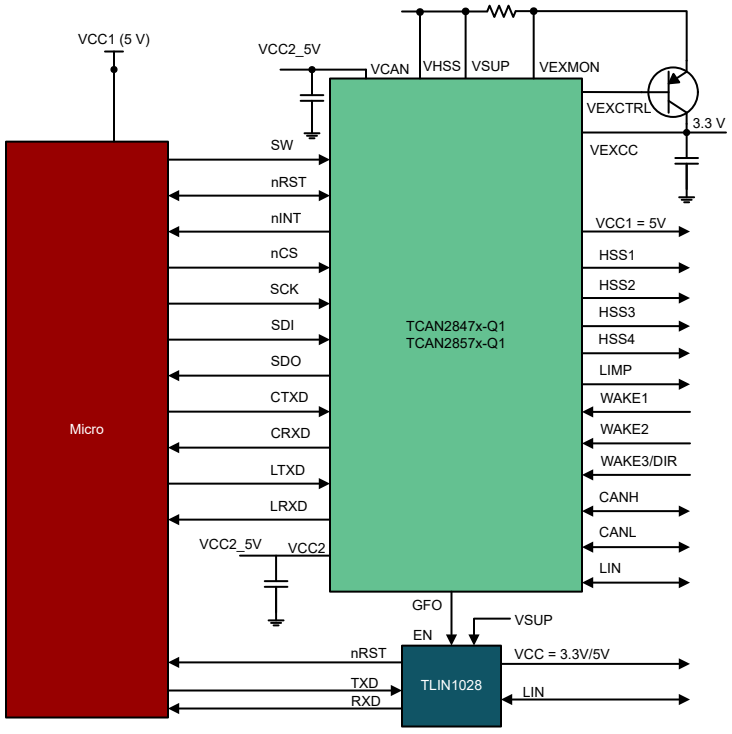


Figure 9-5. Channel Expansion with LIN SBC

9.1.3.2 Channel Expansion for CAN FD

Section 9.1.3.2 show high level diagrams on how the TCAN2854-Q1 can control an external CAN FD transceiver. As the LDO turns off in sleep mode or in various fault conditions like thermal shut down, the CAN FD transceiver has the power shut off. To configure the TCAN285x-Q1 to control the CAN FD transceivers the following register and bits need to be configured. If the 5V variant shows VCC2 is used to power the CAN FD transceiver but VCC1 can also be used. A simple CAN SBC can also provide a second CAN transceiver as shown in Figure 9-7

- Register 29h[3:1] = 110b sets the GFO pin to a general purpose output pin
- Register 29h[4] sets the level of GFO pin to support an external CAN transceiver or SBC STB/nSTB/S pin.

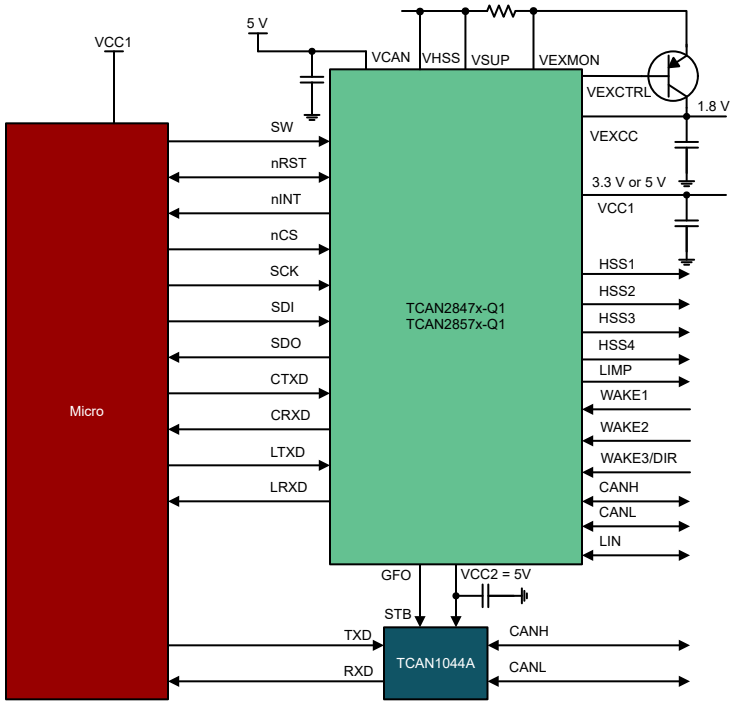


Figure 9-6. Channel Expansion with a CAN FD Transceiver

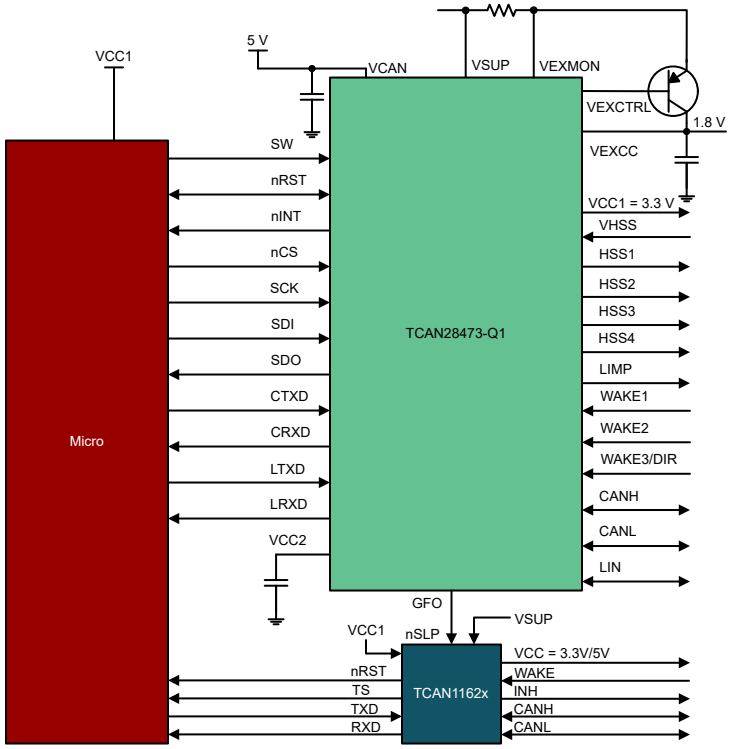


Figure 9-7. Channel Expansion with a CAN FD SBC

9.1.4 Device Brownout information

The brownout behavior of the device depends upon VCC1 and whether VSUP drops below $VSUP_{(PU)F}$. For devices where VCC1 = 5V, the device behaves as per Figure 9-8. When VSUP continues to fall to below $VSUP_{(PU)F}$, the device behaves as a power on reset as per Figure 9-9. $UVSUP_{5F}$ is used for turning off VEXCC and UVSUP5R is used to turn on VEXCC is programmed to be on.

When VCC1 = 3.3V, Both $UVSUP_{5R/F}$ and $UVSUP_{33R/F}$ are used. The device behaves as per Figure 9-10 when VSUP drops below $UVSUP_{33F}$ but stays above $VSUP_{(PU)F}$. When VSUP continues to fall to below $VSUP_{(PU)F}$, the device behaves as a power on reset as per Figure 9-11.

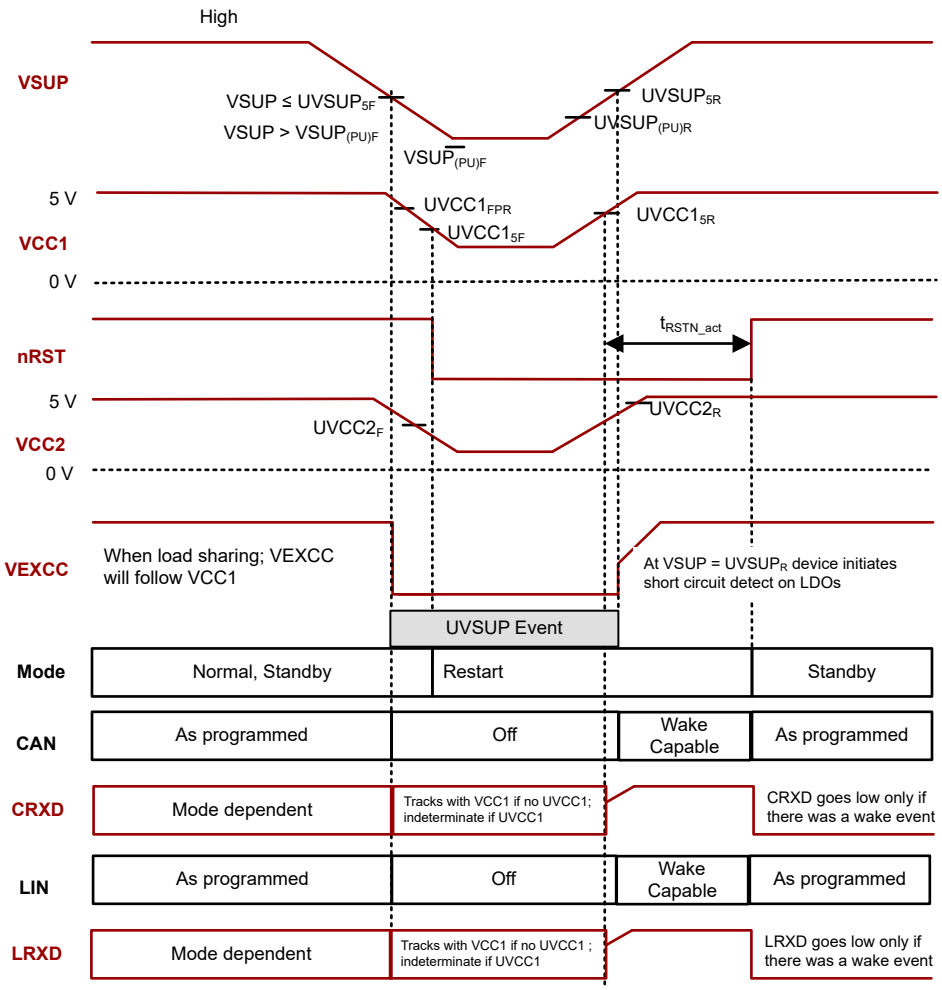


Figure 9-8. Brownout Above $VSUP_{(PU)F}$ for VCC1 = 5V

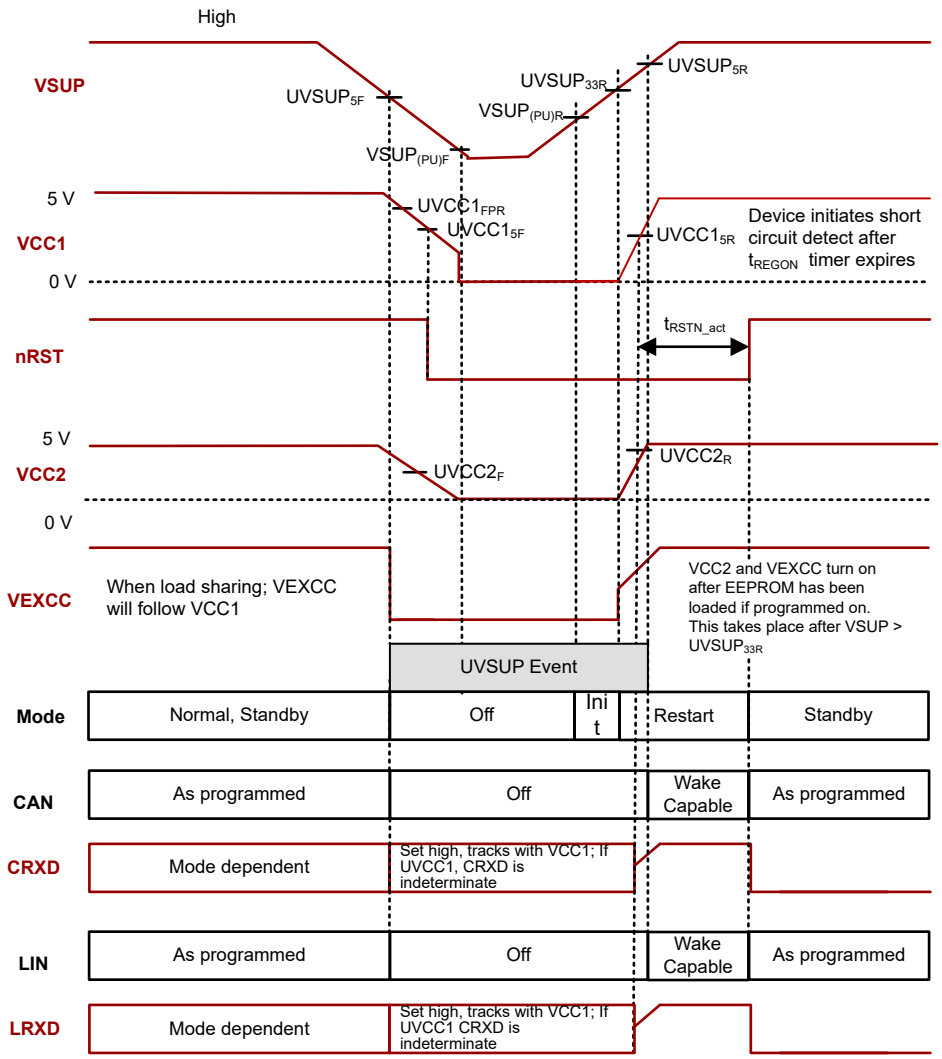


Figure 9-9. Brownout Below $VSUP_{(PU)F}$ for VCC1 = 5V

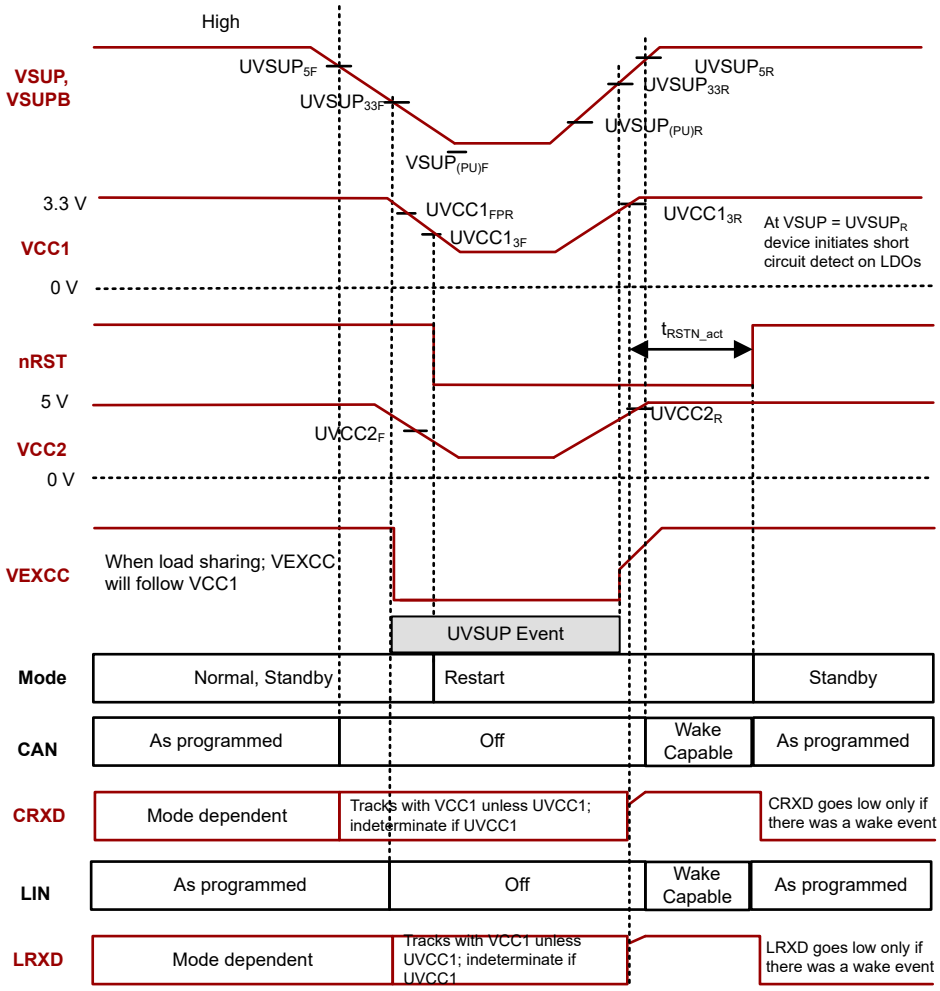


Figure 9-10. Brownout Above $VSUP_{(PU)F}$ for VCC1 = 3.3V

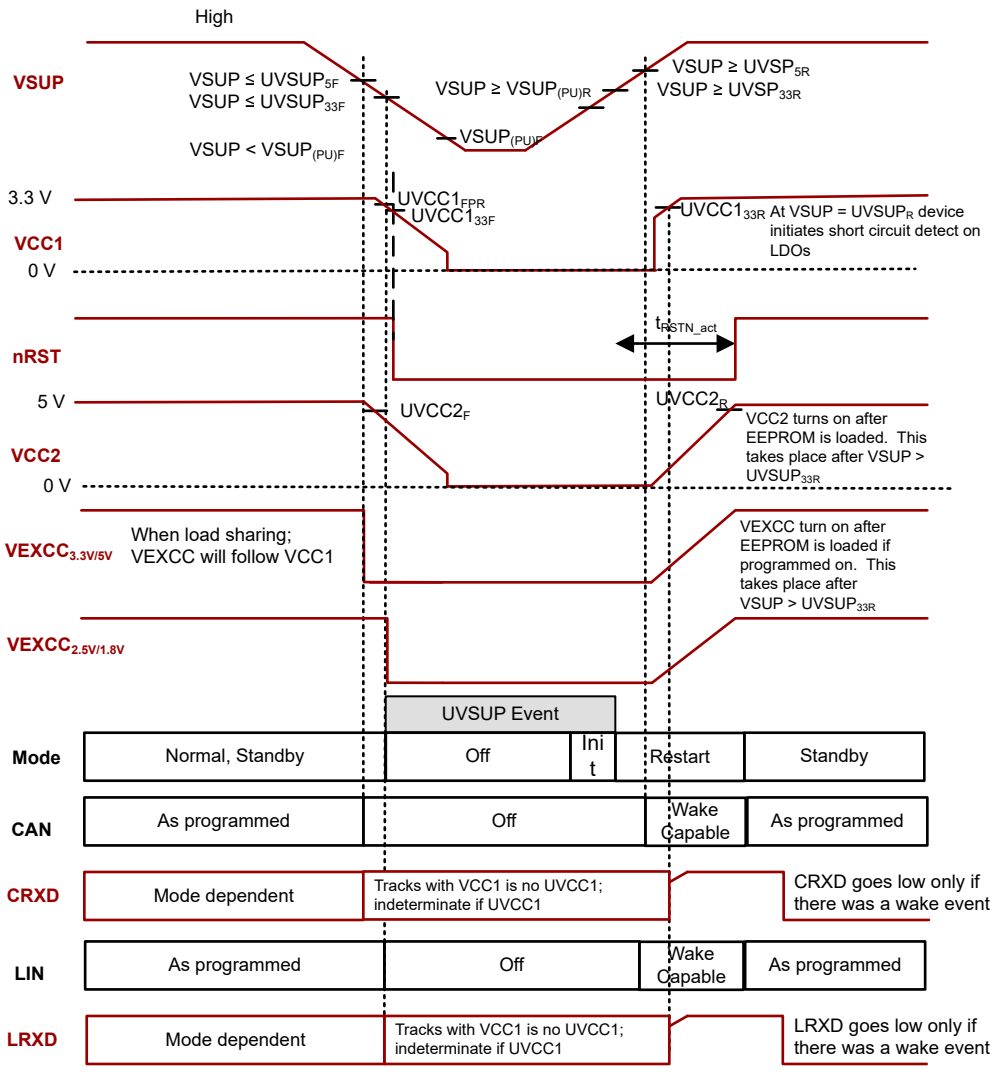


Figure 9-11. Brownout Below $VSUP_{(PU)F}$ for VCC1 = 3.3V

9.1.5 Typical Application

The TCAN285x-Q1 SBC family is typically used in applications with a host microprocessor or FPGA that requires CAN FD and LIN support while using the devices many features like its watchdog, advanced bus fault diagnostics for CAN FD bus and high side switches. Below are typical applications configuration for 3.3V microprocessor applications. These devices work with 3.3V and 5V microprocessors depending upon the value of VCC1. The bus termination is shown for illustrative purposes.

Figure 9-12 shows the TCAN2857-Q1 with different functions than the previous application.

- VCC1 providing power to MCU
- External PNP providing power to a system sensor or second MCU
- HSS1 and HSS2 connected together to provide higher current to an external component.
- Cyclic sensing with the WAKE pin and HSS4

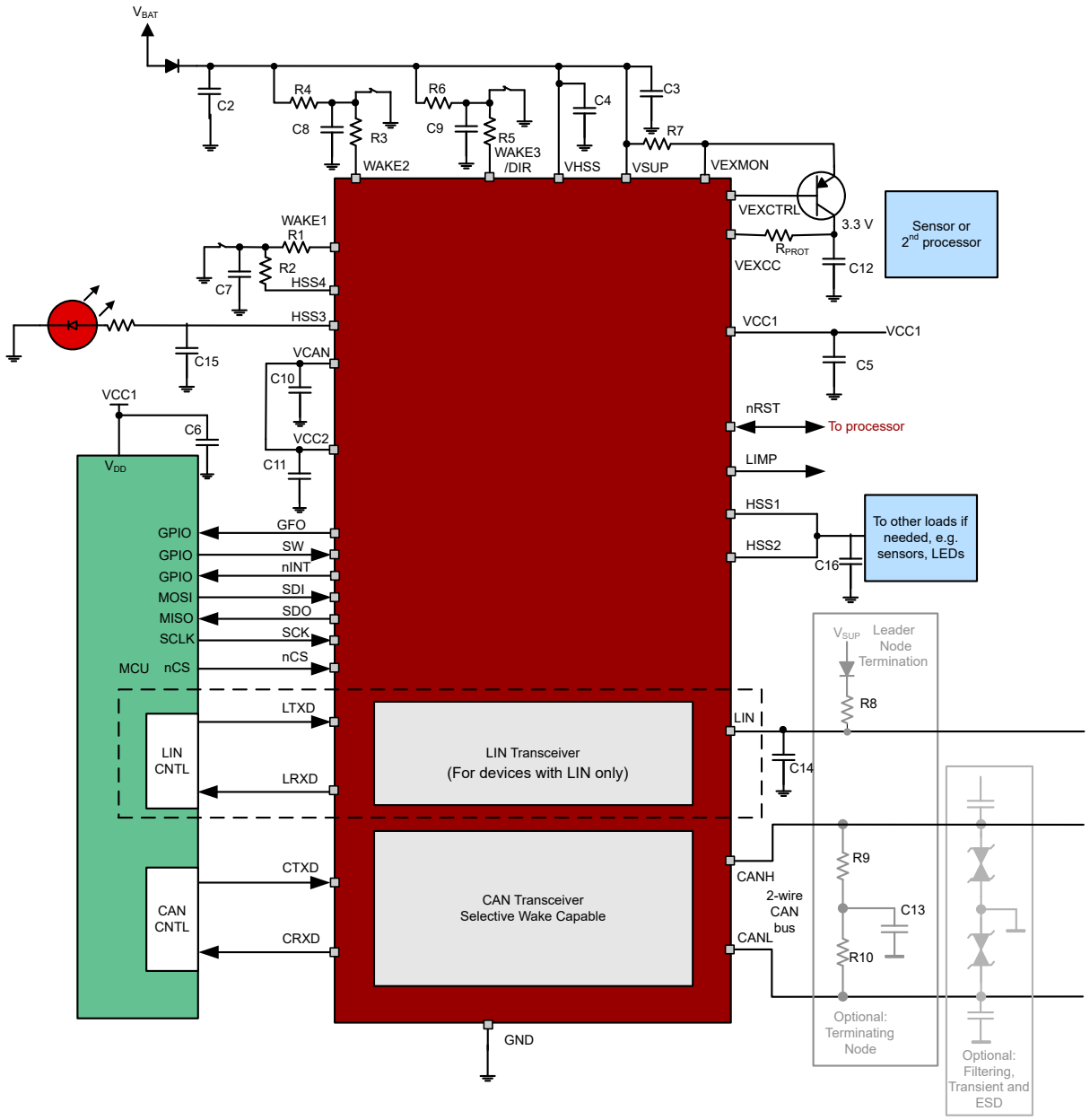


Figure 9-12. Typical CAN and LIN Applications for TCAN2857-Q1 with Synchronized High Side Switch

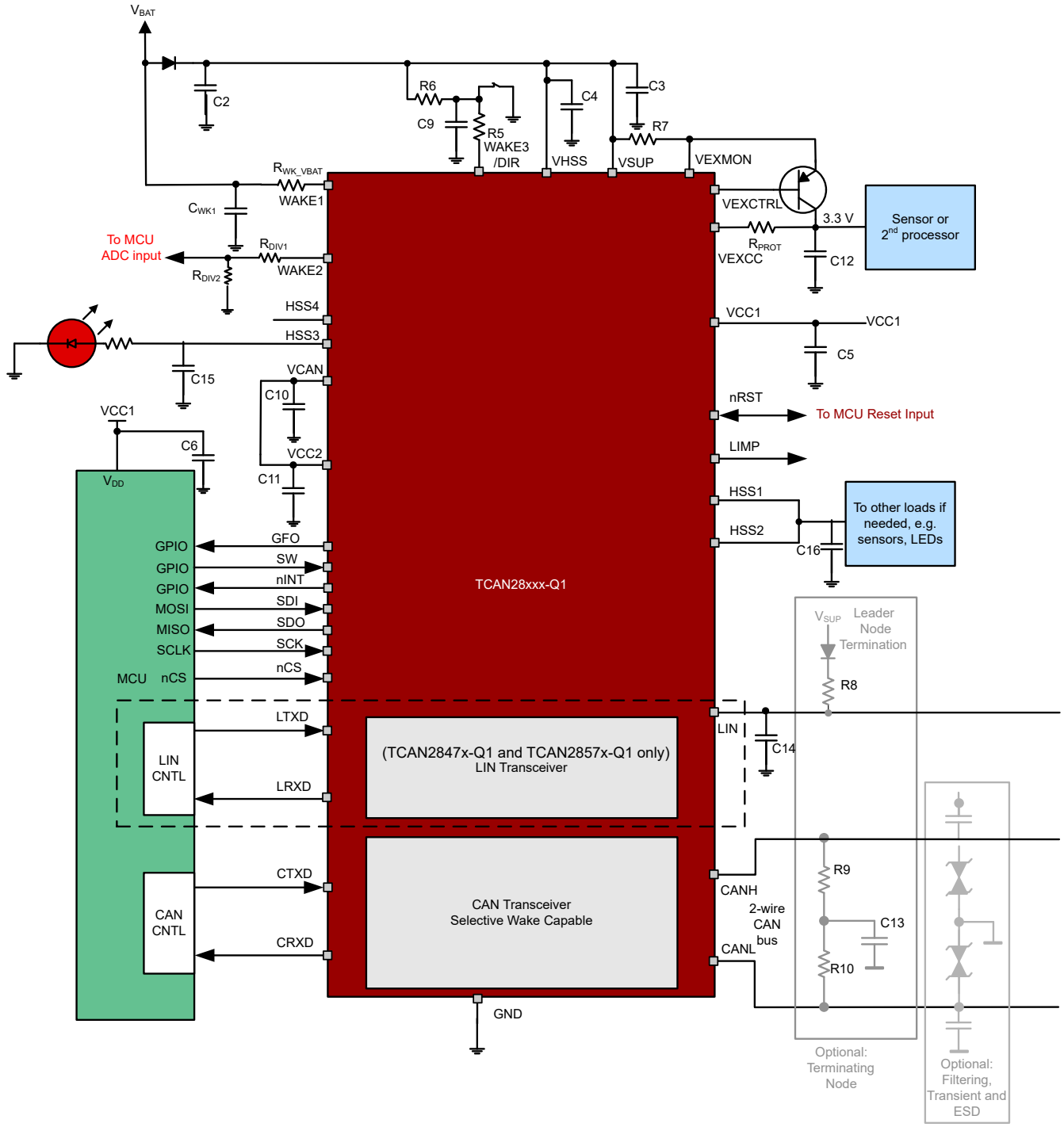


Figure 9-13. Typical Application Diagram with VBAT monitoring function enabled between WAKE1 and WAKE2 pins

Table 9-1. External Component Values

Component	Typical Value	Comments
Capacitance		
C2	22µF	Decoupling capacitance to cut-off battery spike, protect from ISO pulses. Can require higher capacitance per application requirements
C3, C4	100nF, low ESR	Decoupling capacitance, place the capacitance close to the pin of the IC to help with EMC robustness
C5	4.7µF, low ESR	Per application requirements. Min. 1µF required for LDO stability; higher capacitance value recommended here for EMC robustness and help with load transients
C6	Refer to microcontroller manual for capacitance requirement per application.	To improve stability of supply for microcontroller, not needed for SBC.
C7, C8, C9, C_{WK1}	22nF	Required for EMC robustness; only needed if WAKE pins are connected to ECU pins
C10	100nF, low ESR	Needed for VCAN supply stability, place close to the pin of the IC
C11	4.7µF, low ESR	Per application requirements. Min. 1µF required for LDO stability; higher capacitance value recommended here for EMC robustness and help with load transients
C12	4.7µF, low ESR	Per application requirements. Min. 1µF required for LDO stability; higher capacitance value recommended here for EMC robustness and help with load transients
C13	4.7nF	If CAN split termination is needed, per OEM requirement
C14	220pF	LIN termination capacitance
C15, C16	100nF	Only needed if HSS is driving ECU-external loads; for EMC protection
Resistances		
R1, R3, R5	3.3kΩ	Series resistance to limit the current into WAKE pin and protect from ISO pulses
R2, R4, R6	3kΩ	Sets the wetting current needed for the switch, as required by the application
R7	Vshunt/I_limit Ω	Shunt resistance to set the current limit on VEXCC, as required by the application
R8	1kΩ	LIN leader node termination, if used as a leader node
R9, R10	60Ω	CAN termination, if needed, per OEM requirement
$R_{WK-VBAT}$	5.1kΩ	To limit the current through the battery monitoring switch
R_{DIV1}, R_{DIV2}	To limit the voltage at the MCU ADC pin below the Abs Max or ADC input range	Per the MCU ADC pin requirement and max battery voltage requirement
R_{PROT}	100Ω	Only if VEXCC is used to power ECU-external sensors (as a global pin): a series resistance, R_{PROT}, is recommended for EMC robustness

9.1.5.1 Design Requirements

The ISO 11898-2:2024 Standard specifies a maximum bus length of 40m and maximum stub length of 0.3m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A large number of nodes requires transceivers with high input impedance such as the TCAN285x-Q1. Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2:2024. These organizations have made system-level trade-offs for data rate, cable length, and parasitic loading of the bus. The device is specified to meet the 1.5V requirement with a 50Ω load, incorporating the worst case including parallel transceivers. The differential input resistance of the device is a minimum of 30kΩ. If 100 of the devices are in parallel on a bus, this is equivalent to a 300Ω differential load worst case. That transceiver load of 300Ω in parallel with the 60Ω gives an equivalent loading of 50Ω. Therefore, the TCAN285x-Q1 theoretically supports up to 100 transceivers on a single bus segment. However, for CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is typically much lower. Bus length can also be extended beyond the original ISO 11898-2:2024 standard of 40m by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate. This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898-2:2024 CAN standard. In using this flexibility comes the responsibility of good network design and balancing these tradeoffs.

9.1.5.1.1 LTXD Dominant State Timeout Application Note

The maximum dominant LTXD time allowed by the TXD dominant state time out limits the minimum possible data rate of the device. The LIN protocol has different constraints for controller and peripheral node applications. Thus, there are different maximum consecutive dominant bits for each application case and thus different minimum data rates.

9.1.5.2 Detailed Design Procedures

9.1.5.2.1 CAN Detailed Design Procedure

The ISO 11898 standard specifies the interconnect to be a twisted pair cable (shielded or unshielded) with 120Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line must be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop lines (stubs) connecting nodes to the bus must be kept as short as possible to minimize signal reflections. The termination can be on the cable or in a node, but if nodes can be removed from the bus, the termination must be carefully placed so that two terminations always exist on the network. Termination can be a single 120Ω resistor at the end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common mode voltage of the bus is desired, then split termination can be used. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltages at the start and end of message transmissions.

9.1.5.2.2 LIN Detailed Design Procedures

The TCAN2857-Q1 LIN transceiver has been developed with the internal LIN responder pullup resistor to meet ISO 17987-4:2023. This tightening of the pull-up and designing the network with lower bus capacitance allows longer network lengths or more LIN nodes on the bus. Controller node applications require and external 1kΩ pullup resistor and serial diode.

9.1.5.3 Application Curves

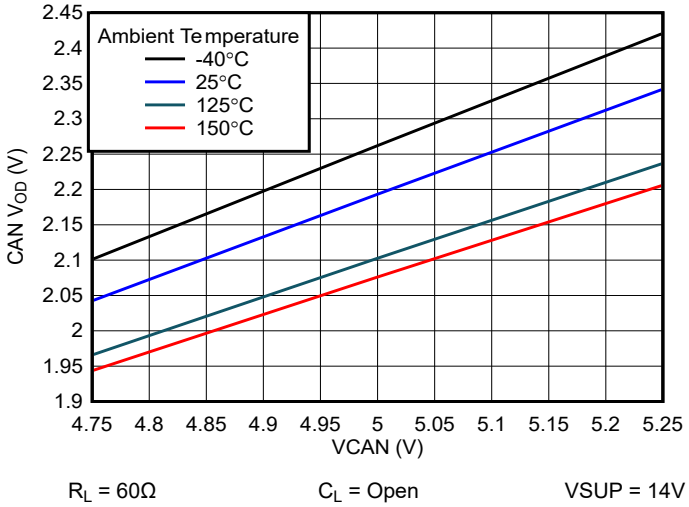


Figure 9-14. CAN Driver Differential Output Voltage versus VCAN and Temperature

9.2 Power Supply Recommendations

The TCAN285x-Q1 is designed to operate off of the battery VSUP and VCAN. To support a wide range of microprocessors the logic I/O and SPI are powered off of VCC1 which supports levels 3.3V and 5V. The CAN FD transceiver 5V supply is powered from VCAN input. As VCAN is used for the CAN transceiver and needed for EEPROM writes, do not use VCC2 to provide the 5V if VCC2 is providing power off board. Refer to Table 9-1 for the recommended values of the external components required on the input and output supply terminals.

9.3 Layout

Robust and reliable bus node design often requires the use of external transient protection device to protect against EFT and surge transients that can occur in industrial environments. Because ESD and transients have a wide frequency bandwidth from approximately 3MHz to 3GHz, high-frequency layout techniques must be applied during PCB design. The family comes with high on-chip IEC ESD protection, but if higher levels of system level immunity are desired external TVS diodes can be used. TVS diodes and bus filtering capacitors can be placed

as close to the on-board connectors as possible to prevent noisy transient events from propagating further into the PCB and system.

9.3.1 Layout Guidelines

Place the protection and filtering circuitry as close to the bus connector, J1, to prevent transients, ESD and noise from propagating onto the board. The layout example provides information on components around the device. A series common mode choke (CMC) is placed on the CANH and CANL lines between and connector J1.

Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device. Use supply and ground planes to provide low inductance.

Note

High-frequency currents follows the path of least impedance and not the path of least resistance.

Use at least two vias for supply and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

- Bypass and bulk capacitors must be placed as close as possible to the supply terminals of transceiver, examples are 100nF capacitors on VCC1, VCC2 and VCAN; C_{OUT} VCC1 and C_{VCC2} on VCC2
- Bus termination: this layout example shows split termination. This is where the termination is split into two resistors, R_{TERM}, with the center or split tap of the termination connected to ground using capacitor C_{SPLIT}. Split termination provides common mode filtering for the bus. When bus termination is placed on the board instead of directly on the bus, additional care must be taken to make sure the terminating node is not removed from the bus thus also removing the termination.

9.3.2 Layout Example

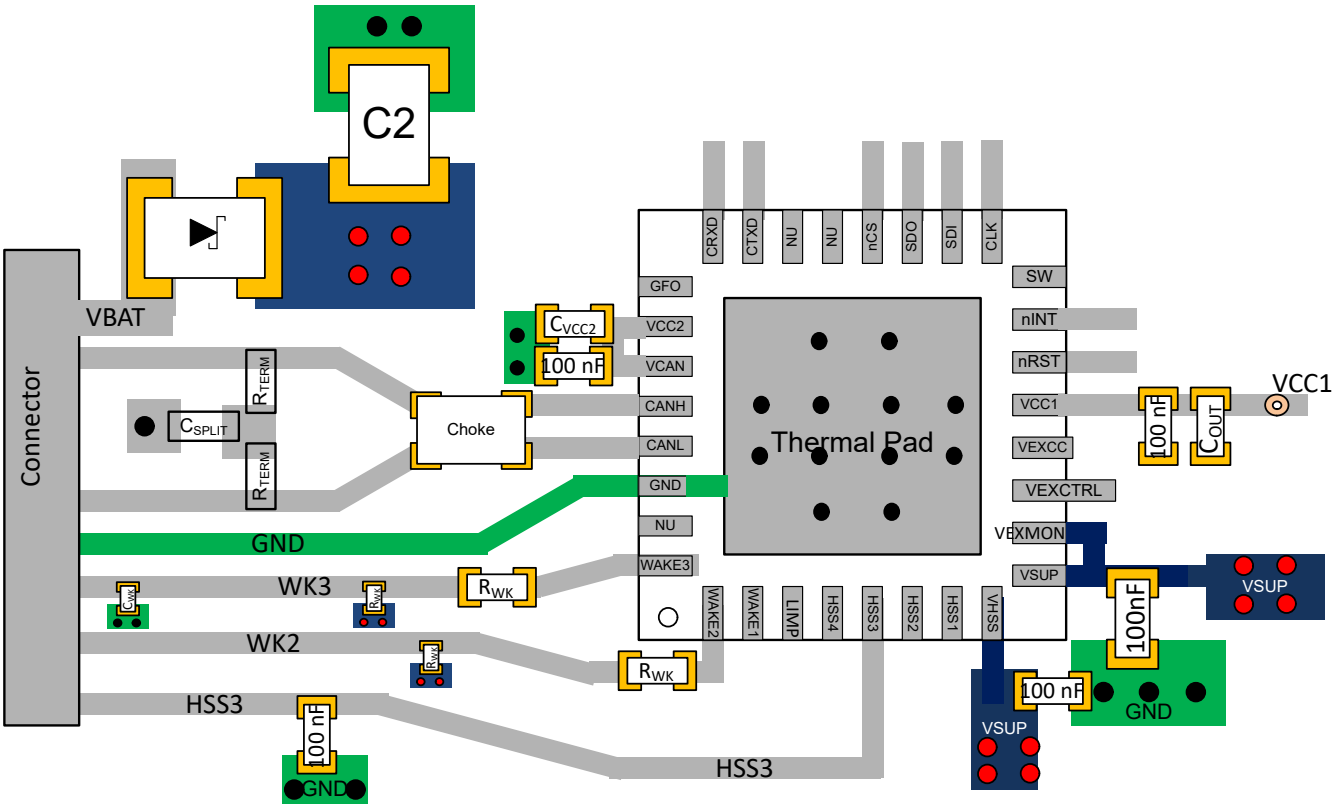


Figure 9-15. Example Layout

10 Registers

10.1 Registers

Table 10-1 lists the memory-mapped registers for the Device registers. All register offset addresses not listed in Table 10-1 should be considered as reserved locations and the register contents should not be modified.

Table 10-1. Device Registers

Address	Acronym	Register Name	Section
0h + formula	DEVICE_ID_y	Device Part Number	Section 10.1.1
8h	REV_ID	Major and Minor Revision	Section 10.1.2
9h	SPI_CONFIG	SPI mode configuration	Section 10.1.3
Ah	CRC_CNTL	SPI CRC control	Section 10.1.4
Bh	CRC_POLY_SET	Sets SPI CRC polynomial	Section 10.1.5
Ch	SBC_CONFIG	SBC, HSS and VCC2 select	Section 10.1.6
Dh	VREG_CONFIG1	Configures VCC1 and VEXCC regulators	Section 10.1.7
Eh	SBC_CONFIG1	SBC Configuration	Section 10.1.8
Fh	Scratch_Pad_SPI	Read and Write Test Register SPI	Section 10.1.9
10h	CAN_CNTRL_1	CAN transceiver 1 control	Section 10.1.10
11h	WAKE_PIN_CONFIG1	WAKE pin configuration 1	Section 10.1.11
12h	WAKE_PIN_CONFIG2	WAKE pin configuration 2	Section 10.1.12
13h	WD_CONFIG_1	Watchdog configuration 1	Section 10.1.13
14h	WD_CONFIG_2	Watchdog configuration 2	Section 10.1.14
15h	WD_INPUT_TRIG	Watchdog input trigger	Section 10.1.15
16h	WD_RST_PULSE	Watchdog output pulse width	Section 10.1.16
17h	FSM_CONFIG	Fail safe mode configuration	Section 10.1.17
18h	FSM_CNTR	Fail safe mode counter	Section 10.1.18
19h	DEVICE_CONFIG0	Device configuration 0	Section 10.1.19
1Ah	DEVICE_CONFIG1	Device configuration 1	Section 10.1.20
1Bh	DEVICE_CONFIG2	Device configuration 2	Section 10.1.21
1Ch	SWE_TIMER	Sleep wake error timer configuration	Section 10.1.22
1Dh	LIN_CNTL	LIN transceiver control	Section 10.1.23
1Eh	HSS_CNTL	High side switch 1 and 2 control	Section 10.1.24
1Fh	PWM1_CNTL1	Pulse width modulation frequency select	Section 10.1.25
20h	PWM1_CNTL2	Pulse width modulation duty cycle two MSB select	Section 10.1.26
21h	PWM1_CNTL3	Pulse width modulation duty cycle eight LSB select	Section 10.1.27
22h	PWM2_CNTL1	Pulse width modulation frequency select	Section 10.1.28
23h	PWM2_CNTL2	Pulse width modulation duty cycle two MSB select	Section 10.1.29
24h	PWM2_CNTL3	Pulse width modulation duty cycle eight LSB select	Section 10.1.30
25h	TIMER1_CONFIG	High side switch timer 1 configuration	Section 10.1.31
26h	TIMER2_CONFIG	High side switch timer 2configuration	Section 10.1.32
28h	RSRT_CNTR	Restart counter configuration	Section 10.1.33

Table 10-1. Device Registers (continued)

Address	Acronym	Register Name	Section
29h	nRST_CNTL	nRST and GFO pin control	Section 10.1.34
2Ah	WAKE_PIN_CONFIG3	Multi wake input configuration and reporting for WAKE pin	Section 10.1.35
2Bh	WAKE_PIN_CONFIG4	Multi wake input configuration and reporting for WAKE pin	Section 10.1.36
2Dh	WD_QA_CONFIG	Q and A Watchdog configuration	Section 10.1.37
2Eh	WD_QA_ANSWER	Q and A Watchdog answer	Section 10.1.38
2Fh	WD_QA_QUESTION	Q and A Watchdog question	Section 10.1.39
30h	SW_ID1	Selective wake ID 1	Section 10.1.40
31h	SW_ID2	Selective wake ID 2	Section 10.1.41
32h	SW_ID3	Selective wake ID 3	Section 10.1.42
33h	SW_ID4	Selective wake ID 4	Section 10.1.43
34h	SW_ID_MASK1	Selective wake ID mask 1	Section 10.1.44
35h	SW_ID_MASK2	Selective wake ID mask 2	Section 10.1.45
36h	SW_ID_MASK3	Selective wake ID mask 3	Section 10.1.46
37h	SW_ID_MASK4	Selective wake ID mask 4	Section 10.1.47
38h	SW_ID_MASK_DLC	ID Mask, DLC and Data mask enable	Section 10.1.48
39h + formula	DATA_y	CAN data byte 7 through 0	Section 10.1.49
41h + formula	SW_RSVD_y	SW_RSVD0 through SW_RSVD2	Section 10.1.50
44h	SW_CONFIG_1	CAN and CAN FD DR and behavior	Section 10.1.51
45h	SW_CONFIG_2	Frame counter	Section 10.1.52
46h	SW_CONFIG_3	Frame counter threshold	Section 10.1.53
47h	SW_CONFIG_4	Mode configuration	Section 10.1.54
48h + formula	SW_CONFIG_RSVD_y	SW_CONFIG_RSVD0 through SW_CONFIG_RSVD5	Section 10.1.55
4Dh	HSS_CNTL2	HSS3 and HSS4 control registers	Section 10.1.56
4Eh	EEPROM_CONFIG	EEPROM accessibility	Section 10.1.57
4Fh	HSS_CNTL3	COnfigures HSS behavior due to OV/UV and provides VCC2/ VEXCC status	Section 10.1.58
50h	INT_GLOBAL	Global Interrupts	Section 10.1.59
51h	INT_1	Interrupts	Section 10.1.60
52h	INT_2	Interrupts	Section 10.1.61
53h	INT_3	Interrupts	Section 10.1.62
54h	INT_CANBUS_1	CAN transceiver 1 Bus fault interrupts	Section 10.1.63
55h	INT_7	Interrupts for high side switches	Section 10.1.64
56h	INT_EN_1	Interrupt mask for INT_1	Section 10.1.65
57h	INT_EN_2	Interrupt mask for INT_2	Section 10.1.66
58h	INT_EN_3	Interrupt mask for INT_3	Section 10.1.67
59h	INT_EN_CANBUS_1	Interrupt mask for INT_CANBUS	Section 10.1.68
5Ah	INT_4	Interrupts	Section 10.1.69
5Ch	INT_6	Interrupts	Section 10.1.70
5Eh	INT_EN_4	Interrupt mask for INT_4	Section 10.1.71
60h	INT_EN_6	Interrupt mask for INT_6	Section 10.1.72

Table 10-1. Device Registers (continued)

Address	Acronym	Register Name	Section
62h	INT_EN_7	High side switch interrupt mask	Section 10.1.73

Complex bit access types are encoded to fit into small table cells. Table 10-2 shows the codes that are used for access types in this section.

Table 10-2. Device Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RH	H R	Set or cleared by hardware Read
Write Type		
H	H	Set or cleared by hardware
W	W	Write
W1C	1C W	1 to clear Write
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, the variables refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address the variable refers to the value of a register array.

10.1.1 DEVICE_ID_y Register (Address = 00h + formula) [reset = xxh]

DEVICE_ID_y is shown in Table 10-3 and described in Table 10-4.

Return to Table 10-1.

Device Part Number, the xxh reset value depends upon device part number and register as shown in description table.

Offset = 00h + y; where y = 0h to 7h

Table 10-3. DEVICE_ID_y Register

7	6	5	4	3	2	1	0
DEVICE_ID							
R-xxh							

Table 10-4. DEVICE_ID_y Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DEVICE_ID	R	xxh	The DEVICE_ID[1:8] registers determine the part number of the device. The reset values and value of each DEVICE_ID register are listed for the corresponding register address: Address 00h = 54h = T Address 01h = 43h = C Address 02h = 41h = A Address 03h = 32h = 2 Address 04h = 38h = 8 Address 05h = 35h = 5 Address 06h = 35h = 5 for TCAN2855Q1 Address 06h = 37h = 7 for TCAN2857Q1 Address 07h = 33h = 3 for 3.3V VCC1 Address 07h = 35h = 5 for 5V VCC1

10.1.2 REV_ID Register (Address = 08h) [reset = 2Xh]

REV_ID is shown in Table 10-5 and described in Table 10-6.

Return to Table 10-1.

Major and Minor Revision

Table 10-5. REV_ID Register

7	6	5	4	3	2	1	0
Major_Revision				Minor_Revision			
R-2h				R-xh			

Table 10-6. REV_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Major_Revision	R	02h	Major die revision 0001b = 1 0010b = 2
3-0	Minor_Revision	R	xh	Minor die revision 0000b = 0 0001b = 1 0010b = 2

10.1.3 SPI_CONFIG Register (Address = 09h) [reset = 00h]

SPI_CONFIG is shown in Table 10-7 and described in Table 10-8.

Return to Table 10-1.

Serial Peripheral Interface configuration register

Bits 0-3 are saved to EEPROM if used.

Table 10-7. SPI_CONFIG Register

7	6	5	4	3	2	1	0
RSVD				BYTE_CNT	SDI_POL	SPI_MODE	
R-0000b				R/W-0b	R/W-0b	R/W-00b	

Table 10-8. SPI_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RSVD	R	0000b	Reserved
3	BYTE_CNT	R/W	0b	Selects the data byte count for a read or write operation 0b = One byte 1b = Two byte
2	SDI_POL	R/W	0b	Selects the idle polarity of the SDI input pin by configuring the internal pullup or pulldown resistor configuration 0b = Pull_down 1b = Pull_up
1-0	SPI_MODE	R/W	00b	Configures the SPI mode 00b = Mode 0 (CPOL = 0, CPHA = 0) 01b = Mode 1 (CPOL = 0, CPHA = 1) 10b = Mode 2 (CPOL = 1, CPHA = 0) 11b = Mode 3 (CPOL = 1, CPHA = 1)

10.1.4 CRC_CNTL Register (Address = 0Ah) [reset = 00h]

CRC_CNTL is shown in Table 10-9 and described in Table 10-10.

Return to Table 10-1.

SPI CRC register controls the CRC function. CRC_EN bit can enable the CRC function.

Table 10-9. CRC_CNTL Register

7	6	5	4	3	2	1	0
CRC_CNTL_RSVD							CRC_EN
R-0000000b							R/W-0b

Table 10-10. CRC_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	CRC_CNTL_RSVD	R	0000000b	CRC control reserved bits
0	CRC_EN	R/W	0b	CRC enable 0b = Disable 1b = Enable

10.1.5 CRC_POLY_SET (Address = 0Bh) [reset = 00h]

CRC_POLY_SET is shown Table 10-11 and described in Table 10-12.

Return to Table 10-1.

This register sets which polynomial is set for CRC. Defaults to AutoSAR 8-bit 0x2F.

Table 10-11. CRC_POLY_SET

7	6	5	4	3	2	1	0
RSVD							POLY_8_SET
R-0000000b							R/W-1b

Table 10-12. CRC_POLY_SET Register Field Description

Bit	Field	Type	Reset	Description
7-1	RSVD	R	0000000b	Reserved
0	POLY_8_SET	R/W	0b	8 bit CRC polynomial set 0b = X^8 + X^5 + X^3 + X^2 + X + 1 (0x2F) 1b = X^8 + X^4 + X^3 + X^2 + 1 (0x1D SAE J1850)

10.1.6 SBC_CONFIG (Address = 0Ch) [reset = 06h]

SBC_CONFIG is shown Table 10-13 and described in Table 10-14.

Return to Table 10-1.

The register programs which mode the SBC is in and which high side switches are being programmed. Configures VCC2 operation.

Bits 0, 1, 6 and 7 are saved to EEPROM if used

Table 10-13. SBC_CONFIG

7	6	5	4	3	2	1	0
VCC1_OV_SEL	VEXCC_ILIM_DIS	PWM_SEL	RSVD	SBC_MODE_SEL		VCC2_CFG	
R/W-0b	R/W-0b	R/W-0b	R-0b	R/W/H-01b		R/W-10b	

Table 10-14. SBC_CONFIG Register Field Description

Bit	Field	Type	Reset	Description
7	VCC1_OV_SEL	R/W	0b	OVCC1 Threshold selection 0b = Lower threshold 1b = Higher threshold
6	VEXCC_ILIM_DIS	R/W	0b	VEXCC current limit disable 0b = Enabled 1b = Disabled
5	PWM_SEL	R/W	0b	PWM select 0b = PWM1 and PWM2 1b = PWM3 and PWM4
4	RSVD	R	0b	Reserved
3-2	SBC_MODE_SEL	R/W/H	01b	SBC mode select 00b = Sleep mode 01b = Standby mode 10b = Normal mode 11b = Reserved
1-0	VCC2_CFG	R/W	10b	VCC2 voltage regulator configuration 00b = Off in all SBC modes 01b = On in all SBC modes except Fail-safe mode 10b = On in all SBC modes except Sleep and Fail-safe modes 11b = RSVD

10.1.7 VREG_CONFIG1 (Address = 0Dh) [reset = 80h]

VREG_CONFIG1 is shown Table 10-15 and described in Table 10-16.

Return to Table 10-1.

This register controls VCC1 and the external PNP configurations.

Bits 0-7 are saved to EEPROM if used

Table 10-15. VREG_CONFIG1

7	6	5	4	3	2	1	0
VCC1_CFG		VEXT_CFG		VCC1_SINK	VEXT_V_CFG		
R/W-10b		R/W-00b		R/W-0b	R/W-000b		

Table 10-16. VREG_CONFIG1 Register Field Description

Bit	Field	Type	Reset	Description
7-6	VCC1_CFG	R/W	10b	VCC1 voltage regulator configuration 00b = Reserved 01b = On in all SBC modes except Fail-safe mode 10b = On in all SBC modes except Sleep and Fail-safe modes 11b = RSVD
5-4	VEXT_CFG	R/W	00b	VEXCC external PNP configuration 00b = Off in all SBC modes 01b = On in all SBC modes except Fail-safe mode 10b = On in all SBC modes except Sleep and Fail-safe modes 11b = RSVD
3	VCC1_SINK	R/W	0b	VCC1 sink current control. This sink is ON when VCC1 is enabled 0b = 10µA 1b = 100µA
2-0	VEXT_V_CFG	R/W	000b	External PNP voltage control 000b = 1.8V 001b = 2.5V 010b = 3.3V 011b = 5V 100b = Load sharing 101b - 111b = Reserved

10.1.8 SBC_CONFIG1 Register (Address = 0Eh) [reset = 01h]

SBC_CONFIG1 is shown in Table 10-17 and described in Table 10-18.

Return to Table 10-1.

Used to configure the SW. Bits 0, 3- 5 and 7 can be saved to EEPROM if used.

Table 10-17. SBC_CONFIG1 Register

7	6	5	4	3	2	1	0
RSVD	FSM_CYC_WK_EN	VCC1_SLP_ACT	UVCC1_SEL		SW_FSM_EN	SW_SLP_EN	SW_POL_SEL
R-0b	R/W-0b	R/W-0b	R/W-00b		R/W-0b	R/W-0b	R/W-1b

Table 10-18. SBC_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	RSVD
6	FSM_CYC_WK_EN	R/W	0b	Enables cyclic wake in fail-safe mode 0b = Disabled 1b = Enabled
5	VCC1_SLP_ACT	R/W	0b	Action to take when VCC1 is enabled on in sleep mode due to a wake event 0b = indicate wake event with nINT pin only 1b = Transition to restart mode
4-3	UVCC1_SEL	R/W	00b	VCC1 under-voltage threshold select 00b = Threshold 1 01b = Threshold 2 10b = Threshold 3 11b = Threshold 4
2	SW_FSM_EN	R/W	0b	Enables the SW pin to become a digital wake up pin when in fail-safe mode: 0b = Disabled 1b = Enabled
1	SW_SLP_EN	R/W	0b	Enables the SW pin to become a digital wake up pin when in sleep mode: 0b = Disabled 1b = Enabled
0	SW_POL_SEL	R/W	1b	Selects the input polarity of the SW pin 0b = Active low 1b = Active high

10.1.9 Scratch_Pad_SPI Register (Address = 0Fh) [reset = 00h]

Scratch_Pad_SPI is shown in Table 10-19 and described in Table 10-20.

Return to Table 10-1.

Read and Write Test Register SPI

Table 10-19. Scratch_Pad_SPI Register

7	6	5	4	3	2	1	0
Scratch_Pad							
R/W-00h							

Table 10-20. Scratch_Pad_SPI Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Scratch_Pad	R/W	00h	Read and Write Test Register SPI

10.1.10 CAN_CNTRL_1 Register (Address = 10h) [reset = 04h]

CAN_CNTRL_1 is shown in Table 10-21 and described in Table 10-22.

Return to Table 10-1.

Controls CAN1 modes and transceiver.

Table 10-21. CAN_CNTRL_1 Register

7	6	5	4	3	2	1	0
SW_EN	TXD_DTO_DIS	FD_EN	RSVD	CAN1_FSM_DIS	CAN1_TRX_SEL		
RH/W-0b	R/W-0b	R/W-0b	R-0b	R/W-0b	R/W-100b		

Table 10-22. CAN_CNTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SW_EN	R/W	0b	Selective wake enable 0b = Disabled 1b = Enabled
6	TXD_DTO_DIS	R/W	0b	CTXD Dominant time out disabled 0b = Enabled 1b = Disabled
5	FD_EN	R/W	0b	Bus fault diagnostic enable 0b = Disabled 1b = Enabled
4	RSVD	R	0b	Reserved
3	CAN1_FSM_DIS	R/W	0b	Sets the CAN transceiver operating state when device enters FSM 0b = Wake capable 1b = Disabled
2-0	CAN1_TRX_SEL	R/W	100b	CAN transceiver control 000b = Off 001b = Reserved 010b = SBC Mode Control WUP Disabled 011b = Reserved 100b = Wake capable 101b = Listen 110b = SBC Mode Control 111b = On

10.1.11 WAKE_PIN_CONFIG1 Register (Address = 11h) [reset = 00h]

WAKE_PIN_CONFIG1 is shown in Table 10-23 and described in Table 10-24.

Return to Table 10-1.

Device wake configuration register

Bits 0-4 are saved to EEPROM if used.

Table 10-23. WAKE_PIN_CONFIG1 Register

7	6	5	4	3	2	1	0
WAKE_CONFIG		WAKE1_STAT	WAKE_VBAT_MON	WAKE_WIDTH_INVALID		WAKE_WIDTH_MAX	
R/W-00b		R/H-0b	R/W-0b	R/W-00b		R/W-00b	

Table 10-24. WAKE_PIN_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	WAKE_CONFIG	R/W	00b	WAKE pin configuration: Note: Pulse requires more programming 00b = Bi-directional - either edge 01b = Rising edge 10b = Falling edge 11b = Pulse
5	WAKE1_STAT	R/H	0b	WAKE1 pin status when WAKE1 pin is configured on 0b = Low 1b = High
4	WAKE_VBAT_MON	R/W	0b	Closes the switch between WAKE1 and WAKE2 enabling VBAT monitoring capability. 0b = Off (default) 1b = On **Note** When WAKE_VBAT_MON is on, WAKE1 and WAKE2 cannot be used as local wake input pins.
3-2	WAKE_WIDTH_INVALID	R/W	00b	Pulses less than or equal to these pulses are considered invalid 0b = 5ms and sets $t_{WAKE\_WIDTH\_MIN}$ to 10ms 1b = 10ms and sets $t_{WAKE\_WIDTH\_MIN}$ to 20ms 10b = 20ms and sets $t_{WAKE\_WIDTH\_MIN}$ to 40ms 11b = 40ms and sets $t_{WAKE\_WIDTH\_MIN}$ to 80ms
1-0	WAKE_WIDTH_MAX	R/W	00b	Maximum WAKE pin input pulse width to be considered valid. 0b = 750ms 1b = 1000ms 10b = 1500ms 11b = 2000ms

10.1.12 WAKE_PIN_CONFIG2 Register (Address = 12h) [reset = 02h]

WAKE_PIN_CONFIG2 is shown in Table 10-25 and described in Table 10-26.

Return to Table 10-1.

Device wake configuration register

Bits 0-1, 5, and 6 are saved to EEPROM if used.

Table 10-25. WAKE_PIN_CONFIG2 Register

7	6	5	4	3	2	1	0
WAKE_PULSE_CONFIG	WAKE1_SENSE	TWK_CYC_SET	nINT_SEL		RXD_WK_CONFIG	WAKE1_LEVEL	
R/W-0b	R/W-0b	R/W-0b	R/W-00b		R/W-0b	R/W-10b	

Table 10-26. WAKE_PIN_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WAKE_PULSE_CONFIG	R/W	0b	Set WAKE pin expected pulse direction for all WAKE pins 0b = Low –> High –> Low 1b = High –> Low –> High
6	WAKE1_SENSE	R/W	0b	This bit is a dual function bit which is determined by how the WAKE_VBAT_MON bit is configured: When **WAKE_VBAT_MON = 0b** the bit is WAKE1_SENSE and configures the WAKE1 pin for static or cyclic wake 0b = Static 1b = Cyclic When **WAKE_VBAT_MON = 1b** the bit becomes OV_WAKE12SW_DIS, which is used to link the internal switch between WAKE1 and WAKE2 pins to OVHSS 0b = Enabled and if OVHSS is reached, the switch is turned off 1b = Disabled
5	TWK_CYC_SET	R/W	0b	Sets the t_{WK_CYC} time (µs) for determining WAKE pin status for cyclic sensing for all WAKE pins 0b = Shorter time window 1b = Longer Time window
4-3	nINT_SEL	R/W	00b	nINT configuration selection: active low 00b = Global interrupt 01b = Watchdog failure output 10b = Bus fault interrupt 11b = Wake request
2	RXD_WK_CONFIG	R/W	0b	Configures RXD pin behavior from a wake event 0b = Pulled low 1b = Toggle
1-0	WAKE1_LEVEL	R/W	10b	WAKE1 pin threshold level; Mid-point value in 2V window, except for 00b. 00b = VCC1 01b = 2.5V 10b = 4V 11b = 6V

10.1.13 WD_CONFIG_1 Register (Address = 13h) [reset = 82h]

WD_CONFIG_1 is shown in Table 10-27 and described in Table 10-28.

Return to Table 10-1.

Watchdog configuration register.

Bits 0-7 are saved to EEPROM if used.

Table 10-27. WD_CONFIG_1 Register

7	6	5	4	3	2	1	0
WD_CONFIG		WD_PRE		WD_SLP_EN	WD_STBY_TYPE	WD_LW_SEL	
R/W-10b		R/W-00b		R/W-0b	R/W-0b	R/W-10b	

Table 10-28. WD_CONFIG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	WD_CONFIG	R/W	10b	Watchdog configuration 00b = Disabled 01b = Timeout 10b = Window 11b = Q&A
5-4	WD_PRE	R/W	00b	Watchdog prescalar 00b = Factor 1 01b = Factor 2 10b = Factor 3 11b = Factor 4
3	WD_SLP_EN	R/W	0b	Enables a timeout WD in sleep mode 0b = Disabled (default) 1b =Enabled
2	WD_STBY_TYPE	R/W	0b	Watchdog type select in standby mode 0b = Timeout if enabled 1b = Based on WD_CONFIG 0x13[7:6]
1-0	WD_LW_SEL	R/W	10b	Selects the duration of the watchdog long window 00b = 150ms 01b = 300ms 10b = 600ms (default) 11b = 1000ms

10.1.14 WD_CONFIG_2 Register (Address = 14h) [reset = 60h]

WD_CONFIG_2 is shown in Table 10-29 and described in Table 10-30.

Return to Table 10-1.

Watchdog timer and error counter register.

Bits 0, 5-7 are saved to EEPROM if used.

Table 10-29. WD_CONFIG_2 Register

7	6	5	4	3	2	1	0
WD_TIMER			WD_ERR_CNT				WD_STBY_DIS
R/W-011b			RH-0000b				R/W-0b

Table 10-30. WD_CONFIG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	WD_TIMER	R/W	011b	Sets window or timeout times based upon the WD_PRE setting, See WD_TIMER table
4-1	WD_ERR_CNT	RH	0000b	Watchdog error counter Running count of errors up to 15 errors
0	WD_STBY_DIS	R/W	0b	Disables the watchdog in standby mode. 0b = Enabled 1b = Disabled

10.1.15 WD_INPUT_TRIG Register (Address = 15h) [reset = 00h]

WD_INPUT_TRIG is shown in Table 10-31 and described in Table 10-32.

Return to Table 10-1.

Writing FFh resets WD timer if accomplished at appropriate time

Table 10-31. WD_INPUT_TRIG Register

7	6	5	4	3	2	1	0
WD_INPUT							
R/W1C-00h							

Table 10-32. WD_INPUT_TRIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	WD_INPUT	R/W1C	00h	Write FFh to trigger WD

10.1.16 WD_RST_PULSE Register (Address = 16h) [reset = 00h]

WD_RST_PULSE is shown in Table 10-33 and described in Table 10-34.

Return to Table 10-1.

The register sets the WD counter which determines the number of WD error events before the device enters restart mode. Can be programmed up to 15. The restart counter which counts the number of times the device has entered restart mode and which causes the device to transition to sleep mode once programmed counter value has been exceeded. Counter must be reset often to avoid this transition.

Bits 4-7 are saved to EEPROM if used.

Table 10-33. WD_RST_PULSE Register

7	6	5	4	3	2	1	0
WD_ERR_CNT_SET				RSRT_CNTR			
R/W-0000b				R/W1C-0000b			

Table 10-34. WD_RST_PULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	WD_ERR_CNT_SET	R/W	0000b	Sets the number of watchdog error event threshold for the device to enter restart mode.
3-0	RSRT_CNTR	R/W1C	0000b	Provides the number of times the device has entered restart mode and must be cleared prior to reaching the RSRT_CNTR_SEL value

10.1.17 FSM_CONFIG Register (Address = 17h) [reset = 00h]

FSM_CONFIG is shown in Table 10-35 and described in Table 10-36.

Return to Table 10-1 .

Configures the fail-safe mode and provides status of what caused the device to enter fail-safe mode. When FSM is disabled 8'h17[3:1] provides the fault information that caused the device to enter sleep mode.

Table 10-35. FSM_CONFIG Register

7	6	5	4	3	2	1	0
FSM_CNTR_ACT				FSM_SLP_STAT			FSM_DIS
R/W-0000b				RH-000b			R/W-0b

Table 10-36. FSM_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	FSM_CNTR_ACT	R/W	0000b	Action if fail-safe counter exceeds programmed value 0000b = Disabled 0001b - 0010b = Reserved 0011b = Perform hard reset - POR 0100b = Stop responding to wake events and go to sleep until power cycle reset 1001b - 1111b - Reserved
3-1	FSM_SLP_STAT	RH	000b	Reason for entering fail-safe or sleep mode 000b = Status clear 001b = Thermal shut down event 010b = Reserved 011b = VCC1 fault 100b = Reserved 101b = SWE timer (Sleep mode) 110b = Reserved 111b = Restart counter exceeded These values are held until cleared by writing 0h to FSM_CNTR_STAT
0	FSM_DIS	R/W	0b	Fail-safe mode disable: 0b = Enabled 1b = Disabled

Note

FSM_SLP_STAT provides information on what fault caused the device to enter fail-safe mode or sleep mode. The interrupt registers provide more information, example: if VCC1 fault is the reason, the interrupt registers show the fault is over-voltage or short circuit. When FSM is enabled INT_3 register 8'h53[5] is set indicating that the device entered fail-safe mode. When VEXCC and VCC1 are load sharing, VCC1 represents the fault condition.

When fail-safe mode is disabled FSM_SLP_STAT indicates which fault caused the device to enter sleep mode. The behavior is similar to when the device enters fail-safe mode but with the following differences:

- INT_2 register 8'h52[7] is set indicating that the device entered sleep mode
- UVCC1 fault and watchdog failure events do not cause the device to enter sleep mode unless the event causes the restart counter to exceeds the limit which then is indicated by 111b restart counter exceeded. The under-voltage or watchdog interrupt is set.

10.1.18 FSM_CNTR Register (Address = 18h) [reset = 00h]

FSM_CNTR is shown in Table 10-37 and described in Table 10-38.

Return to Table 10-1.

Set fail safe counter and status.

Table 10-37. FSM_CNTR Register

7	6	5	4	3	2	1	0
FSM_CNTR_SET				FSM_CNTR_STAT			
R/W-0000b				RH-0000b			

Table 10-38. FSM_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	FSM_CNTR_SET	R/W	0000b	Sets the number of times FS mode enters before action taken. Value is one less than the number of times FS mode is entered. Range is 0-15, representing entering Failsafe mode 1-16 times
3-0	FSM_CNTR_STAT	RH	0000b	Reads back the number of time FSM has been entered in a row up to 15. Can be cleared by writing 0h.

10.1.19 DEVICE_CONFIG0 Register (Address = 19h) [reset = 10h]

DEVICE_CONFIG0 is shown in Table 10-39 and described in Table 10-40.

Return to Table 10-1.

Forces a soft or hard reset. Provides the internal NVM revision

Table 10-39. DEVICE_CONFIG0 Register

7	6	5	4	3	2	1	0
NVM_REV				RESERVED		SF_RST	HD_RST
R-0001b				R-00b		R/W1C-0b	R/W1C-0b

Table 10-40. DEVICE_CONFIG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	NVM_REV	R	0001b	Internal NVM revision
3-2	RESERVED	R	00b	Reserved
1	SF_RST	R/W1C	0b	Soft Reset: Writing a 1 causes a soft reset. Device registers are reloaded from EEPROM while keeping LDOs on.
0	HD_RST	R/W1C	0b	Hard Reset: Forces a power on reset when writing a 1. **Note** This sets the PWRON interrupt flag.

10.1.20 DEVICE_CONFIG1 (Address = 1Ah) [reset = 00h]

DEVICE_CONFIG1 is shown in Table 10-41 and described in Table 10-42.

Return to Table 10-1.

LIMP pin configuration.

Bits 0, 4, and 7 are saved to EEPROM if used.

Table 10-41. DEVICE_CONFIG1

7	6	5	4	3	2	1	0
LIMP_SLP_FLT_EN	LIMP_RD_EN	LIMP_STATE	LIMP_DIS	LIMP_SEL_RESET		LIMP_RESET	FSM_CYC_SEN_EN
R/W-0b	R/W-0b	R-0b	R/W - 0b	R/W - 00b		R/W1C - 0b	R/W - 0b

Table 10-42. DEVICE_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LIMP_SLP_FLT_EN	R/W	0b	Any fault that causes a FSM entrance causes LIMP pin to turn on until turned off 0b = Disabled (default) 1b = Enabled
6	LIMP_RD_EN	R/W	0b	Enables the LIMP pin read back buffer to provide the status of the LIMP pin and reflected at LIMP_STATE 0b = Disabled (default) 1b = Enabled
5	LIMP_STATE	R	0b	Reads back the state of the LIMP pin 0b = Inactive 1b = Active
4	LIMP_DIS	R/W	0b	LIMP pin disable 0b = Enabled 1b = Disabled
3-2	LIMP_SEL_RESET	R/W	00b	Selects the method to reset/turn off the LIMP pin 00b = On third successful input trigger the error counter receives 01b = First correct input trigger 10b = Reserved 11b = Reserved
1	LIMP_RESET	R/W1C	0b	LIMP reset Writing a one to this location resets the LIMP pin to off state and bit automatically clears
0	FSM_CYC_SEN_EN	R/W	0b	Enables cyclic sensing wake up for fail-safe mode 0b = Disabled 1b = Enabled

10.1.21 DEVICE_CONFIG2 (Address = 1Bh) [reset = 00h]

DEVICE_CONFIG2 is shown in Table 10-43 and described in Table 10-44.

Return to Table 10-1.

WAKE pin and channel expansion configuration and control.

Bit 0 is saved to EEPROM if used.

Table 10-43. DEVICE_CONFIG2

7	6	5	4	3	2	1	0
RSVD						WAKE_WIDTH_MAX_DIS	nINT_TOG_EN
R-000000b						R/W-0b	R/W-0b

Table 10-44. DEVICE_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RSVD	R	000000b	Reserved
1	WAKE_WIDTH_MAX_DIS	R/W	0b	Disables the Max limit, $t_{WK\_PULSE\_WIDTH\_MAX}$ detection when pulse is selected for WAKE pin wake up. 0b = Enabled 1b = Disabled
0	nINT_TOG_EN	R/W	0b	Enables the nINT pin to toggle instead of being latched low for an interrupt 0b = Disabled 1b = Enabled

10.1.22 SWE_TIMER (Address = 1Ch) [reset = 28h]

SWE_TIMER is shown in Table 10-45 and described in Table 10-46.

Return to Table 10-1.

Sleep wake error timer configuration. Power up always sets to default value

Bits 3-7 are saved to EEPROM if used.

Table 10-45. SWE_TIMER

7	6	5	4	3	2	1	0
SWE_EN	SWE_TIMER_SET				CANSLNT_SWE_DIS	LIN1_FSM_DIS	RSVD
R/W-0b	R/W-0101b				R/W-0b	R/W-0b	R-0b

Table 10-46. SWE_TIMER Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SWE_EN	R/W	0b	Sleep wake error enable: NOTE: If enabled, a SPI read or write must take place within this window or the device goes back to sleep. This does not disable the function for initial power on or in case of a power on reset. 0b = Disabled 1b = Enabled
6-3	SWE_TIMER_SET	R/W	0101b	Sets the timer used for $t_{INACTIVE}$ (minutes) 0000b = 2 0001b = 2.5 0010b = 3 0011b = 3.5 0100b = 4 0101b = 4.5 0110b = 5 0111b = 5.5 1000b = 6 1001b = 6.5 1010b = 8 1011b = 8.5 1100b = 10 1101b = Reserved 1110b = Reserved 1111b = Reserved
2	CANSLNT_SWE_DIS	R/W	0b	Disables the SWE timer connection with the CANSLNT flag. 0b = Enabled 1b = Disabled
1	LIN1_FSM_DIS	R/W	0b	Disables LIN transceiver when entering FSM 0b = Wake capable 1b = Off
0	RSVD	R	0b	Reserved

10.1.23 LIN_CNTL (Address = 1Dh) [reset = 20h]

LIN_CNTL is shown in Table 10-47 and described in Table 10-48.

Return to Table 10-1.

LIN1 transceiver state and dominant timeout control.

Table 10-47. LIN_CNTL

7	6	5	4	3	2	1	0
LIN1_TRX_CNTRL			LIN1_TXD_DTO_DIS	RSVD			
R/W/H-001b			R/W/H-0b	R-0000b			

Table 10-48. LIN_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	LIN1_TRX_CNTRL	R/W/H	001b	Channel 1 LIN transceiver control 000b = Off 001b = Wake Capable 010b = On 011b = Fast 100b = Listen 101b = SBC Mode Control 110b - 111b =Reserved
4	LIN1_TXD_DTO_DIS	R/W/H	0b	Port 1 LIN LTXD1 dominant state timeout disable 0b = Enabled 1b = Disabled
3-0	RSVD	R	0000b	Reserved

10.1.24 HSS_CNTL (Address = 1Eh) [reset = 00h]

HSS_CNTL is shown in Table 10-49 and described in Table 10-50.

Return to Table 10-1.

HSS1 and HSS2 high side switch control.

Table 10-49. HSS_CNTL

7	6	5	4	3	2	1	0
HSS1_CNTL				HSS2_CNTL			
R/W-0000b				R/W-0000b			

Table 10-50. HSS_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	HSS1_CNTL	R/W	0000b	Control for HSS1 0000b = Off 0001b = PWM1 0010b = PWM2 0011b = Timer1 0100b = Timer2 0101b = On 0110b = PWM3 0111b = PWM4 1000b = Direct Drive with slow slew rate setting 1001b = Direct Drive with faster slew rate setting All other values are reserved
3-0	HSS2_CNTL	R/W	0000b	Control for HSS2 0000b = Off 0001b = PWM1 0010b = PWM2 0011b = Timer1 0100b = Timer2 0101b = On 0110b = PWM3 0111b = PWM4 1000b = Direct Drive with slow slew rate setting 1001b = Direct Drive with faster slew rate setting All other values are reserved

10.1.25 PWM1_CNTL1 (Address = 1Fh) [reset = 00h]

PWM1_CNTL1 is shown in Table 10-51 and described in Table 10-52.

Return to Table 10-1.

Sets the pulse width modulation frequency, PWM1. When multiple high side switches are available more PWMs may be needed. PWM1 becomes PWM3 if a HSS3 is available, and these registers are used.

Table 10-51. PWM1_CNTL1

7	6	5	4	3	2	1	0
PWM1_FREQ	PWM1_FREQ_RSVD						
R/W-0b	R-0000000b						

Table 10-52. PWM1_CNTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PWM1_FREQ	R/W	0b	PWM frequency select (Hz) 0b = 200 1b = 400
6-0	PWM1_FREQ_RSVD	R	0000000b	Reserved

Note

When configuring HSS3, align PWM3 if PWM is to be used. PWM1 control changes to PWM3 when register 8'hC[5:4] = 01b.

10.1.26 PWM1_CNTL2 (Address = 20h) [reset = 00h]

PWM1_CNTL2 is shown in Table 10-53 and described in Table 10-54.

Return to Table 10-1.

Set the two most significant bit for the 10-bit PWM1. These work with register h'21

Table 10-53. PWM1_CNTL2

7	6	5	4	3	2	1	0
PWM1_RSVD						PWM1_DC_MSB	
R-000000b						R/W-00b	

Table 10-54. PWM1_CNTL2L Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	PWM1_RSVD	R	000000b	Reserved
1-0	PWM1_DC_MSB	R/W	00b	Most significant two bits for 10-bit PWM1 duty cycle select. Works with 'h21[7:0] 00b = 100% off when used with 'h21[7:0] and is 00h xxb = on time with an increase of ≅ 0.1% when used with 'h21[7:0] 11b = 100% of when used with 'h21[7:0] and is FFh

Note

When configuring HSS3, align PWM3 if PWM is to be used. PWM1 control changes to PWM3 when register 8'hC[5:4] = 01b.

10.1.27 PWM1_CNTL3 (Address = 21h) [reset = 00h]

PWM1_CNTL3 is shown in Table 10-55 and described in Table 10-56 .

Return to Table 10-1 .

Bits 0 - 7 of the 10-bit PWM1 and PWM3. Used with register h'20[1:0]. Rewrite these register bits (even if unchanged) if h'22 or h'23 are changed. New PWM settings take effect only after writing into the LSB bits.

Table 10-55. PWM1_CNTL3

7	6	5	4	3	2	1	0
PWM1_DC							
R/W-00h							

Table 10-56. PWM1_CNTL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PWM1_DC	R/W	00h	Bits 0 - 7 of the 10-bit PWM1 00h = 100% off when used with 'h20[1:0] = 00b xxh = On time with an increase of ≅ 0.1% when used with 'h20[1:0] FFh = 100% on when used with 'h20[1:0] = 11b

Note

When configuring HSS3, align PWM3 if PWM is to be used. PWM1 control changes to PWM3 when register 8'hC[5:4] = 01b.

10.1.28 PWM2_CNTL1 (Address = 22h) [reset = 00h]

PWM2_CNTL1 is shown in Table 10-57 and described in Table 10-58.

Return to Table 10-1.

Sets the pulse width modulation frequency, PWM2. When multiple high side switches are available more PWMs can be needed. PWM2 becomes PWM4 if a HSS4 is available, and these registers are used.

Table 10-57. PWM2_CNTL1

7	6	5	4	3	2	1	0
PWM2_FREQ	PWM2_FREQ_RSVD						
R/W-0b	R-0000000b						

Table 10-58. PWM2_CNTL1 Register Field Descriptions

Bit	Filed	Type	Reset	Description
7	PWM2_FREQ	R/W	0b	PWM frequency select (Hz) 0b = 200 1b = 400
6-0	PWM2_FREQ_RSVD	R	0000000b	Reserved

Note

When configuring HSS4, align PWM4 if PWM is to be used. PWM2 control changes to PWM4 when register 8'hC[5:4] = 01b.

10.1.29 PWM2_CNTL2 (Address = 23h) [reset = 00h]

PWM2_CNTL2 is shown in Table 10-59 and described in Table 10-60.

Return to Table 10-1.

Set the two most significant bit for the 10-bit PWM2. These work with register h'24

Table 10-59. PWM2_CNTL2

7	6	5	4	3	2	1	0
PWM2_RSVD						PWM2_DC_MSB	
R-000000b						R/W-00b	

Table 10-60. PWM2_CNTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	PWM2_RSVD	R	000000b	Reserved
1-0	PWM2_DC_MSB	R/W	00b	Most significant two bits for 10-bit PWM2 duty cycle select. Works with 'h24[7:0] 00b = 100% off when used with 'h24[7:0] and is 00h xxb = on time with an increase of ≅ 0.1% when used with 'h24[7:0] 11b = 100% of when used with 'h24[7:0] and is FFh

Note

When configuring HSS4, align PWM4 if PWM is to be used. PWM2 control changes to PWM4 when register 8'hC[5:4] = 01b.

10.1.30 PWM2_CNTL3 (Address = 24h) [reset = 00h]

PWM2_CNTL3 is shown in Table 10-61 and described in Table 10-62.

Return to Table 10-1.

Bits 0 - 7 of the 10-bit PWM2 and PWM4. Used with register h'23[1:0]. Rewrite these register bits (even if unchanged) if h'22 or h'23 are changed. New PWM settings take effect only after writing into the LSB bits.

Table 10-61. PWM2_CNTL3

7	6	5	4	3	2	1	0
PWM2_DC							
R/W-00h							

Table 10-62. PWM2_CNTL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PWM2_DC	R/W	00h	Bits 0 - 7 of the 10-bit PWM2 00h = 100% off when used with 'h23[1:0] = 00b xxh = On time with an increase of≅ 0.1% when used with 'h23[1:0] FFh = 100% on when used with 'h23[1:0] = 11b

Note

When configuring HSS4, align PWM4 if PWM is to be used. PWM2 control changes to PWM4 when register 8'hC[5:4] = 01b.

10.1.31 TIMER1_CONFIG (Address = 25h) [reset = 00h]

TIMER1_CONFIG is shown in Table 10-63 and described in Table 10-64.

Return to Table 10-1.

Sets timer 1 period and on time. Careful selection is important as selecting a 200ms on width and a 10ms period is not possible. Timer1 or Timer2 selections cannot be shared across cyclic wake, HSS, or cyclic sensing wake. These timers only support one of these three functions. Timer1 can be used for one function and TImer2 for another function.

Table 10-63. TIMER1_CONFIG

7	6	5	4	3	2	1	0
TIMER1_ON_WIDTH				TIMER1_CYC_WK_EN	TIMER1_PERIOD		
R/W-0000b				R/W-0b	R/W-000b		

Table 10-64. TIMER1_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	TIMER1_ON_WIDTH	R/W	0000b	Sets the high side switch on time (ms) for timer 1 0000b = Off (HSS is high impedance) 0001b = 0.1 0010b = 0.3 0011b = 0.5 0100b = 1 0101b = 10 0110b = 20 0111b = 30 1000b = 40 1001b = 50 1010b = 60 1011b = 80 1100b = 100 1101b = 150 1110b = 200 1111b = On (HSS is on 100%)
3	TIMER1_CYC_WK_EN	R/W	0b	Enables timer1 for cyclic wake 0b = Disabled 1b = Enabled
2-0	TIMER1_PERIOD	R/W	000b	Sets the timer period (ms) for timer 1 000b = 10 001b = 20 010b = 50 011b = 100 100b = 200 101b = 500 110b = 1000 111b = 2000

10.1.32 TIMER2_CONFIG (Address = 26h) [reset = 00h]

TIMER2_CONFIG is shown in Table 10-65 and described in Table 10-66.

Return to Table 10-1.

Sets timer 2 period and on time. Careful selection is important as selecting a 200ms on width and a 10ms period is not possible. Timer1 or Timer2 selections cannot be shared across cyclic wake, HSS, or cyclic sensing wake. These timers only support one of these three functions. Timer1 can be used for one function and TImer2 for another function.

Table 10-65. TIMER2_CONFIG

7	6	5	4	3	2	1	0
TIMER2_ON_WIDTH				TIMER2_CYC_WK_EN	TIMER2_PERIOD		
R/W-0000b				R/W-0b	R/W-000b		

Table 10-66. TIMER2_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	TIMER2_ON_WIDTH	R/W	0000b	Sets the high side switch on time (ms) for timer 2 0000b = Off (HSS is high impedance) 0001b = 0.1 0010b = 0.3 0011b = 0.5 0100b = 1 0101b = 10 0110b = 20 0111b = 30 1000b = 40 1001b = 50 1010b = 60 1011b = 80 1100b = 100 1101b = 150 1110b = 200 1111b = On (HSS is on 100%)
3	TIMER2_CYC_WK_EN	R/W	0b	Enables timer2 for cyclic wake 0b = Disabled 1b = Enabled
2-0	TIMER2_PERIOD	R/W	000b	Sets the timer period (ms) for timer 2 000b = 10 001b = 20 010b = 50 011b = 100 100b = 200 101b = 500 110b = 1000 111b = 2000

10.1.33 RSRT_CNTR (Address = 28h) [reset = 40h]

RSRT_CNTR is shown in Table 10-67 and described in Table 10-68.

Return to Table 10-1.

Restart mode counter set. Sets the number of times the device can enter restart mode which causes the device to transition to sleep mode once programmed counter value has been exceeded.

Table 10-67. RSRT_CNTR

7	6	5	4	3	2	1	0
RSRT_CNTR_SEL				RSVD			
R/W-0100b				R-0000b			

Table 10-68. RSRT_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RSRT_CNTR_SEL	R/W	0100b	Selects the number of times the device can enter restart mode prior to device entering sleep mode, 1 to 15 times. Writing 0h here disables the restart counter.
3-0	RSVD	R	0000b	Reserved

10.1.34 nRST_CNTL (Address = 29h) [reset = 2Ch]

nRST_CNTL is shown in Table 10-69 and described in Table 10-70.

Return to Table 10-1.

nRST and GFO pins control register.

Bit 5 is saved to EEPROM if used.

Table 10-69. nRST_CNTL

7	6	5	4	3	2	1	0
RSVD		nRST_PULSE_WIDTH	GFO_POL_SEL	GFO_SEL			RSVD
R-00b		R/W-1b	R/W-0b	R/W-110b			R-0b

Table 10-70. nRST_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RSVD	R	00b	Reserved
5	nRST_PULSE_WIDTH	R/W	1b	Sets the pulse width for toggling nRST from high-->low-->high when device enters restart mode due to watchdog failure (ms) 0b = 2 1b = 15
4	GFO_POL_SEL	R/W	0b	Selects the polarity for the GFO pin 0b = Active Low 1b = Active High **Note** Selects the output level when register 8'h29[3:1] = 110b making the pin a general-purpose output pin; 0 = Low and 1 = High
3-1	GFO_SEL	R/W	110b	Selects the information that causes this pin to be pulled to the state selected by 'h29[4] for t_{NRST_TOG} except for when general purpose output is selected 000b = VCC1, VCC2 and/or VEXCC Interrupt (overvoltage, undervoltage or short) 001b = WD interrupt event 010b = Reserved 011b = Local wake request (LWU) 100b = Bus wake request (WUP) 101b = Restart counter exceeded (indicated in standby mode) 110b = General purpose output (default) 111b = CAN Bus fault
0	RSVD	R	0b	RSVD

10.1.35 WAKE_PIN_CONFIG3 Register (Address = 2Ah) [reset = E0h]

WAKE_PIN_CONFIG3 is shown in Table 10-71 and described in Table 10-72.

Return to Table 10-1

Register to configure the number of inputs to the WAKE pin and which inputs caused the wake.

MULTI_WAKE_STAT provides which WAKE input state has changed based upon specific bits. Bits represent WAKE input so if multiple WAKE input bits are set, this indicates that those specific WAKE inputs cause the WAKE event. An example is if h'2A[4:0] = 00101b then WAKE 0 and WAKE 2 have changed states.

Table 10-71. WAKE_PIN_CONFIG3

7	6	5	4	3	2	1	0
WAKE_PIN_SET			MULTI_WAKE_STAT				
R/W = 111b			R/W0C/H = 00000b				

Table 10-72. WAKE_PIN_CONFIG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	WAKE_PIN_SET	R/W	111b	Sets which WAKE input are on 000b = None 001b = WAKE1 on 010b = WAKE2 on 011b = WAKE1, WAKE2 on 100b = WAKE3 on 101b = WAKE1, WAKE3 on 110b = WAKE2, WAKE3 on 111b = WAKE1, WAKE2, WAKE3 on
4-0	MULTI_WAKE_STAT	R/W0C/H	00000b	Provides information on which individual or combination of wake input signal took place. 00000b = None 00001b = Wake1 00010b = Wake 2 00100b = Wake 3 **Note** Note: The bit correspond to the WAKE pin sets to one allowing for multiple WAKE pins providing a local wake up input. An example is if WAKE 1 and WAKE3 happened, this shows up as 00101b.

10.1.36 WAKE_PIN_CONFIG4 Register (Address = 2Bh) [reset = 22h]

CONFIG_RSVD_y is shown in Table 10-73 and described in Table 10-74.

Return to Table 10-1.

Configures WAKE pins 2 and 3

Bits 0-1, 3, 4-5, and 7 are saved to EEPROM if used.

Table 10-73. WAKE_PIN_CONFIG4

7	6	5	4	3	2	1	0
WAKE2_SENSE	WAKE2_STAT	WAKE2_LEVEL		WAKE3_SENSE	WAKE3_STAT	WAKE3_LEVEL	
R/W-0b	R/H-0b	R/W-10b		R/W-0b	R/H-0b	R/W-10b	

Table 10-74. WAKE_PIN_CONFIG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WAKE2_SENSE	R/W	0b	WAKE pin 2 sense configuration 0b = Static 1b = Cyclic
6	WAKE2_STAT	R/H	0b	WAKE2 pin status when WAKE2 pin is configured on 0b = Low 1b = High
5-4	WAKE2_LEVEL	R/W	10b	WAKE2 pin threshold level; Mid-point value in 2V window, except for 00b. 00b = VCC1 01b = 2.5V 10b = 4V 11b = 6V
3	WAKE3_SENSE	R/W	0b	WAKE pin 3 sense configuration 0b = Static 1b = Cyclic
2	WAKE3_STAT	R/H	0b	WAKE3 pin status when WAKE3 pin is configured on 0b = Low 1b = High
1-0	WAKE3_LEVEL	R/W	10b	WAKE3 pin threshold level; Mid-point value in 2V window, except for 00b. 00b = VCC1 01b = 2.5V 10b = 4V 11b = 6V

10.1.37 WD_QA_CONFIG Register (Address = 2Dh) [reset = 0Ah]

WD_QA_CONFIG is shown in Table 10-75 and described in Table 10-76.

Return to Table 10-1.

Q&A watchdog configuration bits.

All bits are saved to EEPROM if used.

Table 10-75. WD_QA_CONFIG Register

7	6	5	4	3	2	1	0
WD_ANSW_GEN_CFG		WD_QA_POLY_CFG		WD_QA_POLY_SEED			
R/W-00b		R/W-00b		R/W-1010b			

Table 10-76. WD_QA_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	WD_ANSW_GEN_CFG	R/W	00b	WD answer generation configuration
5-4	WD_QA_POLY_CFG	R/W	00b	WD Q&A polynomial configuration
3-0	WD_QA_POLY_SEED	R/W	1010b	WD Q&A polynomial seed value loaded when device is in the RESET state

10.1.38 WD_QA_ANSWER Register (Address = 2Eh) [reset = 00h]

WD_QA_ANSWER is shown in Table 10-77 and described in Table 10-78.

Return to Table 10-1.

Q&A watchdog answer bits

Table 10-77. WD_QA_ANSWER Register

7	6	5	4	3	2	1	0
WD_QA_ANSWER							
R/W1C-00h							

Table 10-78. WD_QA_ANSWER Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	WD_QA_ANSWER	R/W1C	00h	MCU watchdog Q&A answer response byte

10.1.39 WD_QA_QUESTION Register (Address = 2Fh) [reset = 3Ch]

WD_QA_QUESTION is shown in Table 10-79 and described in Table 10-80.

Return to Table 10-1.

Q&A watchdog question bits

Table 10-79. WD_QA_QUESTION Register

7	6	5	4	3	2	1	0
WD_QA_RSVD	WD_QA_ERR	WD_ANSW_CNT		WD_QUESTION			
R-0b	W1C-0b	RH-11b		RH-1100b			

Table 10-80. WD_QA_QUESTION Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WD_QA_RSVD	R	0b	Reserved
6	WD_QA_ERR	W1C	0b	Watchdog Q&A answer error flag
5-4	WD_ANSW_CNT	RH	11b	Current state of received watchdog Q&A error counter
3-0	WD_QUESTION	RH	1100b	Current watchdog question value

10.1.40 SW_ID1 Register (Address = 30h) [reset = 00h]

SW_ID1 is shown in Table 10-81 and described in Table 10-82.

Return to Table 10-1.

Extended ID bits 17:10

Table 10-81. SW_ID1 Register

7	6	5	4	3	2	1	0
EXT_ID_17:10							
R/W-00h							

Table 10-82. SW_ID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EXT_ID_17:10	R/W	00h	Extended ID bits 17:10

10.1.41 SW_ID2 Register (Address = 31h) [reset = 00h]

SW_ID2 is shown in Table 10-83 and described in Table 10-84.

Return to Table 10-1.

Extended ID bits 9:2.

Table 10-83. SW_ID2 Register

7	6	5	4	3	2	1	0
EXT_ID_9:2							
R/W-00h							

Table 10-84. SW_ID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EXT_ID_9:2	R/W	00h	Extended ID bits 9:2

10.1.42 SW_ID3 Register (Address = 32h) [reset = 00h]

SW_ID3 is shown in Table 10-85 and described in Table 10-86.

Return to Table 10-1.

Extended ID bits 1:0, Extended ID Field, ID[10:6] and Extended ID[28:24]

Table 10-85. SW_ID3 Register

7	6	5	4	3	2	1	0
EXT_ID_1:0		IDE	ID_10:6__EXT_ID_28:24				
R/W-00b		R/W-0b	R/W-00000b				

Table 10-86. SW_ID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	EXT_ID_1:0	R/W	00b	Extended ID bits 1:0
5	IDE	R/W	0b	Extended ID field 0b = Standard ID (11-bits) 1b = Extended ID (29-bits)
4-0	ID_10:6__EXT_ID_28:24	R/W	00000b	ID[10:6] and Extended ID[28:24]

10.1.43 SW_ID4 Register (Address = 33h) [reset = 00h]

SW_ID4 is shown in Table 10-87 and described in Table 10-88.

Return to Table 10-1.

ID[5:0] and Extended ID[23:18]

Table 10-87. SW_ID4 Register

7	6	5	4	3	2	1	0
ID_5:0__EXT_ID_23:18						RESERVED	
R/W-000000b						R-00b	

Table 10-88. SW_ID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	ID_5:0__EXT_ID_23:18	R/W	000000b	ID[5:0] and Extended ID[23:18]
1-0	RESERVED	R	00b	Reserved

10.1.44 SW_ID_MASK1 Register (Address = 34h) [reset = 00h]

SW_ID_MASK1 is shown in Table 10-89 and described in Table 10-90.

Return to Table 10-1.

Extended ID Mask 17:16

Table 10-89. SW_ID_MASK1 Register

7	6	5	4	3	2	1	0
RESERVED						EXT_ID_MASK_17:16	
R-000000b						R/W-00b	

Table 10-90. SW_ID_MASK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000b	Reserved
1-0	EXT_ID_MASK_17:16	R/W	00b	Extended ID Mask 17:16

10.1.45 SW_ID_MASK2 Register (Address = 35h) [reset = 00h]

SW_ID_MASK2 is shown in Table 10-91 and described in Table 10-92.

Return to Table 10-1.

Extended ID Mask 15:8

Table 10-91. SW_ID_MASK2 Register

7	6	5	4	3	2	1	0
EXT_ID_MASK_15:8							
R/W-00h							

Table 10-92. SW_ID_MASK2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EXT_ID_MASK_15:8	R/W	00h	Extended ID Mask 15:8

10.1.46 SW_ID_MASK3 Register (Address = 36h) [reset = 00h]

SW_ID_MASK3 is shown in Table 10-93 and described in Table 10-94.

Return to Table 10-1.

Extended ID Mask 7:0

Table 10-93. SW_ID_MASK3

7	6	5	4	3	2	1	0
EXT_ID_MASK_7:0							
R/W-00h							

Table 10-94. SW_ID_MASK3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EXT_ID_MASK_7:0	R/W	00h	Extended ID Mask 7:0

10.1.47 SW_ID_MASK4 Register (Address = 37h) [reset = 00h]

SW_ID_MASK4 is shown in Table 10-95 and described in Table 10-96.

Return to Table 10-1.

ID Mask 10:3 and Extended ID Mask 28:21 (Base ID)

Table 10-95. SW_ID_MASK4 Register

7	6	5	4	3	2	1	0
ID_MASK_10:3__EXT_ID_MASK_28:21							
R/W-00h							

Table 10-96. SW_ID_MASK4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ID_MASK_10:3__EXT_ID_MASK_28:21	R/W	00h	ID Mask 10:3 and Extended ID Mask 28:21 (Base ID)

10.1.48 SW_ID_MASK_DLC Register (Address = 38h) [reset = 00h]

SW_ID_MASK_DLC is shown in Table 10-97 and described in Table 10-98.

Return to Table 10-1.

ID Mask 2:0 and Extended ID Mask 20:18 (Base ID), DLC[3:0] and data mask enable

Table 10-97. SW_ID_MASK_DLC Register

7	6	5	4	3	2	1	0
ID_MASK[2:0]_EXT_ID_MASK[20:18]			DLC				DATA_MASK_EN
R/W-000b			R/W-0000b				R/W-0b

Table 10-98. SW_ID_MASK_DLC Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	ID_MASK[2:0]_EXT_ID_MASK[20:18]	R/W	000b	ID Mask 2:0 and Extended ID Mask 20:18 (Base ID)
4-1	DLC	R/W	0000b	DLC[3:0]
0	DATA_MASK_EN	R/W	0b	Data mask enable 0b = DLC field and Data field are not compared and assumed valid. Remote frames are allowed. 1b = DLC field must match DLC[3:0] register and data field bytes are compared with DATAx registers for a matching 1. Remote frames are ignored

10.1.49 DATA_y Register (Address = 39h + formula) [reset = 00h]

DATA_y is shown in Table 10-99 and described in Table 10-100.

Return to Table 10-1.

Register address 39h through 40h

Offset = 39h + (y x 1h); where y = 0h to 7h

Table 10-99. DATA_y Register

7	6	5	4	3	2	1	0
DATAx							
R/W-00h							

Table 10-100. DATA_y Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DATAx	R/W	00h	CAN data byte x

10.1.50 SW_RSVD_y Register (Address = 41h + formula) [reset = 00h]

SW_RSVD_y is shown in Table 10-101 and described in Table 10-102.

Return to Table 10-1.

Register address 41h through 43F

Offset = 41h + (y x 1h); where y = 0h to 2h

Table 10-101. SW_RSVD_y Register

7	6	5	4	3	2	1	0
RESERVED							
R-00h							

Table 10-102. SW_RSVD_y Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	00h	Reserved

10.1.51 SW_CONFIG_1 Register (Address = 44h) [reset = 50h]

SW_CONFIG_1 is shown in Table 10-103 and described in Table 10-104.

Return to Table 10-1.

CAN and CAN FD DR

Table 10-103. SW_CONFIG_1 Register

7	6	5	4	3	2	1	0
SW_FD_PASSIVE	CAN_DR			FD_DR		RESERVED	
R/W-0b	R/W-101b			R/W-00b		R-00b	

Table 10-104. SW_CONFIG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SW_FD_PASSIVE	R/W	0b	Selective Wake FD Passive: this bit modifies the behavior of the error counter when CAN with flexible data rate frames are seen. 0b = CAN with flexible data rate frame is counted as an error frame 1b = CAN with flexible data rate frame are ignored (passive)
6-4	CAN_DR	R/W	101b	CAN bus data rate 000b = 50Kbps 001b = 100Kbps 010b = 125Kbps 011b = 250Kbps 100b = Reserved 101b = 500Kbps 110b = Reserved 111b = 1Mbps
3-2	FD_DR	R/W	00b	CAN bus FD data rate ratio verses CAN data rate 00b = CAN FD <= 4x CAN data rate 01b = CAN FD => 5x and <= 10x CAN data rate 10b = CAN FD 8Mbps versus 500k CAN data rate 11b = Reserved
1-0	RESERVED	R	00b	Reserved

10.1.52 SW_CONFIG_2 Register (Address = 45h) [reset = 00h]

SW_CONFIG_2 is shown in Table 10-105 and described in Table 10-106.

Return to Table 10-1

Frame Error Counter: this error counter is incremented by 1 for every received frame error detected (stuff bit, CRC or CRC delimiter form error). The counter is decremented by 1 for every correctly received CAN frame assuming the counter is not zero. In case the device is set for passive on CAN with flexible data rate frames, any frame detected as a CAN FD frame has no impact on the frame error counter (no increment or decrement). If the frame counter reaches FRAME_CNT_THRESHOLD[7:0] value the next increment overflows the counter, set FRAME_OVF flag. The counter is reset by the following: enabling the frame detection or $t_{SILENCE}$ detection.

Table 10-105. SW_CONFIG_2 Register

7	6	5	4	3	2	1	0
FRAME_CNTx							
RH-00h							

Table 10-106. SW_CONFIG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FRAME_CNTx	RH	00h	Frame Error Counter: this error counter is incremented by 1 for every received frame error detected (stuff bit, CRC or CRC delimiter form error). The counter is decremented by 1 for every correctly received CAN frame assuming the counter is not zero. In case the device is set for passive on CAN with flexible data rate frames, any frame detected as a CAN FD frame has no impact on the frame error counter (no increment or decrement). If the frame counter reaches FRAME_CNT_THRESHOLD[7:0] value the next increment overflows the counter, set FRAME_OVF flag. The counter is reset by the following: enabling the frame detection or $t_{SILENCE}$ detection.

10.1.53 SW_CONFIG_3 Register (Address = 46h) [reset = 1Fh]

SW_CONFIG_3 is shown in Table 10-107 and described in Table 10-108.

Return to Table 10-1.

Frame Error Counter Threshold: these bits set the point at which the error counter reaches the maximum and on the next error frame overflows and set the FRAME_OVF flag. Default is 31 so the 32nd error sets the overflow flag.

Table 10-107. SW_CONFIG_3 Register

7	6	5	4	3	2	1	0
FRAME_CNT_THRESHOLD							
R/W-1Fh							

Table 10-108. SW_CONFIG_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FRAME_CNT_THRESHOLD	R/W	1Fh	Frame Error Counter Threshold: these bits set the point at which the error counter reaches the maximum and on the next error frame overflows and set the FRAME_OVF flag. Default is 31 so the 32nd error sets the overflow flag.

10.1.54 SW_CONFIG_4 Register (Address = 47h) [reset = 00h]

SW_CONFIG_4 is shown in Table 10-109 and described in Table 10-110.

Return to Table 10-1.

Table 10-109. SW_CONFIG_4 Register

7	6	5	4	3	2	1	0
SWCFG	CAN_SYNC_FD	CAN_SYNC	RESERVED				
RH/W-0b	RH-0b	RH-0b	R-00000b				

Table 10-110. SW_CONFIG_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SWCFG	RH/W	0b	Selective wake configuration complete 0b = SW registers not configured 1b = SW registers configured Note: Make this the last step in configuring and turning on selective wake. **Note** Writing to any of these wake configuration registers (8'h30-8'h44, 8'h46) clears the SWCFG bit.
6	CAN_SYNC_FD	RH	0b	device is properly decoding CAN FD frames if frame detection is enabled. This flag is updated after every received frame. By polling this flag, the system can determine if the device is properly decoding CAN FD frames, up to but not including the Data Field. This flag is self-clearing.
5	CAN_SYNC	RH	0b	Synchronized to CAN data: this flag indicates the device is properly decoding CAN frames if frame detection is enabled. This flag is updated after every received frame. By polling this flag, the system can determine if the device is properly decoding CAN frames. This flag is self-clearing.
4-0	RESERVED	R	00000b	Reserved

10.1.55 SW_CONFIG_RSVD_y Register (Address = 48h + formula) [reset = 00h]

SW_CONFIG_RSVD_y is shown in Table 10-111 and described in Table 10-112.

Return to Table 10-1.

Register address 48h through 4Dh

Offset = 48h + (y x 1h); where y = 0h to 5h

Table 10-111. SW_CONFIG_RSVD_y Register

7	6	5	4	3	2	1	0
RESERVED							
R-00h							

Table 10-112. SW_CONFIG_RSVD_y Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	00h	Reserved

10.1.56 HSS_CNTL2 (Address = 4Dh) [reset = 00h]

HSS_CNTL2 is shown in Table 10-113 and described in Table 10-114.

Return to Table 10-1.

HSS3 and HSS4 high side switch control.

Table 10-113. HSS_CNTL2

7	6	5	4	3	2	1	0
HSS3_CNTL				HSS4_CNTL			
R/W-0000b				R/W-0000b			

Table 10-114. HSS_CNTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	HSS3_CNTL	R/W	0000b	Control for HSS3 000b = Off 0001b = PWM1 0010b = PWM2 0011b = Timer1 0100b = Timer2 0101b = On 0110b = PWM3 0111b = PWM4 1000b = Direct Drive with slow slew rate setting 1001b = Direct Drive with faster slew rate setting All other values are reserved
3-0	HSS4_CNTL	R/W	0000b	Control for HSS4 000b = Off 0001b = PWM1 0010b = PWM2 0011b = Timer1 0100b = Timer2 0101b = On 0110b = PWM3 0111b = PWM4 1000b = Direct Drive with slow slew rate setting 1001b = Direct Drive with faster slew rate setting All other values are reserved

Note

- When configuring HSS3 and HSS4 and HSS3 and HSS4 need to align PWM3 and PWM4, if PWM, PWM1, and PWM2 control changes to PWM3 and PWM4 when setting register 8'hC[5:4] = 01b
- When Cyclic Sensing Wake is enabled, HSS4 needs to be either Timer1 or Timer2

10.1.57 EEPROM_CONFIG (Address = 4Eh) [reset = 00h]

EEPROM_CONFIG is shown in Table 10-115 and described in Table 10-116.

Return to Table 10-1.

The register controls the access to the EEPROM.

Table 10-115. EEPROM_CONFIG

7	6	5	4	3	2	1	0
EEPROM_SAVE	EEPROM_CRC_CHK	EEPROM_RELOAD	RSVD	EEPROM_CODE			
R/W-0b	R/W-0b	R/W-0b	R-0b	R/W-0000b			

Table 10-116. EEPROM_CONFIG Register Field Description

Bit	Field	Type	Reset	Description
7	EEPROM_SAVE	R/W	0b	Write a 1b & correct code to register 8'h4E[3:0] to save configuration bits to EEPROM. Self clears after EEPROM is written to.
6	EEPROM_CRC_CHK	R/W	0b	Write a 1b to force a EEPROM read and CRC check. Automatically clears upon completion
5	EEPROM_RELOAD	R/W	0b	Write a 1b to reload memory from the EEPROM
4	RSVD	R	0b	Reserved
3-0	EEPROM_CODE	W	0000b	Required code to update EEPROM. 0Ah is used and reads back 0h.

10.1.58 HSS_CNTL3 (Address = 4Fh) [reset = 00h]

HSS_CNTL3 is shown in Figure 10-1 and described in Table 10-117.

Return to Table 10-1.

Used to determine HSS behavior during VHSS over/under-voltage and Register 8'h0E[7:5] provides the status of VEXCC, VCC2 and VCAN.

Bit 0 and 4 are saved to EEPROM if used.

Figure 10-1. HSS_CNTL3

7	6	5	4	3	2	1	0
HSS_OV_SD_DIS	HSS_UV_SD_DIS	HSS_OV_UV_REC	SLP_CYC_WK_EN	VEXCC_STATUS	VCC2_STATUS	VCAN_STATUS	RSTRT_TMR_SEL
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/H-0b	R/H-0b	R/H-0b	R/W-0b

Table 10-117. HSS_CNTL3 Register Field Description

Bit	Field	Type	Reset	Description
7	HSS_OV_SD_DIS	R/W	0b	Disables high-side switches from shutting down due to an OVHSS event 0b = HSS are turned off due to OVHSS Enabled 1b = HSS remain as configured under OVHSS condition
6	HSS_UV_SD_DIS	R/W	0b	Disables high-side switches from shutting down due to an UVHSS event 0b = HSS are turned off due to UVHSS 1b = HSS remain as configured under UVHSS condition
5	HSS_OV_UV_REC	R/W	0b	Disables high-side switches from automatically recovering to previous state due to an OVHSS or UVHSS event 0b = Enabled 1b = Disabled
4	SLP_CYC_WK_EN	R/W	0b	Enables Cyclic Wake in sleep mode based upon timer 1, timer 2, or SWE timer 0b = Disabled 1b = Enabled
3	VEXCC_STATUS	R/H	0b	VEXCC status 0b = UVEXCC or off 1b = In regulation
2	VCC2_STATUS	R/H	0b	VCC2 status 0b = UVCC2 or off 1b = In regulation
1	VCAN_STATUS	R/H	0b	VCAN status 0b = UVCAN or off 1b = Good
0	RSTRT_TMR_SEL	R/W	0b	Selects the restart timer used to exit restart mode if VCC1 does not exceed UVCC1R 0b = t_{RSTTO} 1b = $t_{INACTIVE}$; which must be enabled

10.1.59 INT_GLOBAL Register (Address = 50h) [reset = 00h]

INT_GLOBAL is shown in Table 10-118 and described in Table 10-119.

Return to Table 10-1.

Logical OR of all to certain interrupts

Table 10-118. INT_GLOBAL Register

7	6	5	4	3	2	1	0
INT_7	INT_1	INT_2	INT_3	INT_CANBUS	INT_4	RSVD	INT_6
RH-0b	RH-0b	RH-0b	RH-0b	RH-0b	RH-0b	R-0b	RH-0b

Table 10-119. INT_GLOBAL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_7	RH	0b	Logical OR of INT_7 register
6	INT_1	RH	0b	Logical OR of INT_1 register
5	INT_2	RH	0b	Logical OR of INT_2 register
4	INT_3	RH	0b	Logical OR of INT_3 register
3	INT_CANBUS	RH	0b	Logical OR of INT_CANBUS register
2	INT_4	RH	0b	Logical OR of INT_4 register
1	RSVD	R	0b	Reserved
0	INT_6	RH	0b	Logical OR of INT_6 register

10.1.60 INT_1 Register (Address = 51h) [reset = 00h]

INT_1 is shown in Table 10-120 and described in Table 10-121.

Return to Table 10-1.

Table 10-120. INT_1 Register

7	6	5	4	3	2	1	0
WD	CANINT1	LWU	WKERR	FRAME_OVF_1	CANSLNT_1	SWPIN	CANDOM_1
R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b

Table 10-121. INT_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WD	R/W1C	0b	Watchdog event interrupt. **Note** This interrupt bit is set for every watchdog error event and does not rely upon the Watchdog error counter
6	CANINT1	R/W1C	0b	CAN bus wake up interrupt
5	LWU	R/W1C	0b	Local wake up
4	WKERR	R/W1C	0b	Wake error bit is set when the SWE timer has expired and the state machine has returned to Sleep mode
3	FRAME_OVF_1	R/W1C	0b	Frame error counter overflow
2	CANSLNT_1	R/W1C	0b	CAN bus inactive for $t_{SILENCE}$
1	SWPIN	R/W1C	0b	SW pin is used to wake the device
0	CANDOM_1	R/W1C	0b	CAN TXD stuck dominant

10.1.61 INT_2 Register (Address = 52h) [reset = 40h]

INT_2 is shown in Table 10-122 and described in Table 10-123.

Return to Table 10-1.

Table 10-122. INT_2 Register

7	6	5	4	3	2	1	0
SMS	PWRON	OVCC1	UVSUP5	UVSUP3	UVCC1	TSD_VCC1_VEXCC	SME
R/W1C-0b	R/W1C-1b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b

Table 10-123. INT_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SMS	R/W1C	0b	Sleep mode status flag. Sets whenever Sleep mode is entered from a WKERR or an SBC fault.
6	PWRON	R/W1C	1b	Power on
5	OVCC1	R/W1C	0b	VCC1 overvoltage
4	UVSUP5	R/W1C	0b	VSUP undervoltage for 5V
3	UVSUP3	R/W1C	0b	VSUP undervoltage for 3.3V
2	UVCC1	R/W1C	0b	VCC1 undervoltage
1	TSD_VCC1_VEXCC	R/W1C	0b	Thermal Shutdown due to VCC1 or VEXCC
0	SME	R/W1C	0b	Sleep Mode Exit interrupt when device is in sleep mode, VCC1 is on and exited to restart or fail-safe mode due to a VCC1 fault or watchdog fault if enabled

10.1.62 INT_3 Register (Address 53h) [reset = 00h]

INT_3 is shown in Table 10-124 and described in Table 10-125.

Return to Table 10-1.

Interrupt set when the internal EEPROM used for trimming has a CRC error. Upon power up, the device loads an internal register from the EEPROM and performs a CRC check. If an error is present after eight attempts of loading valid data the CRC_EEPROM interrupt is set. This indicates an error that can impact device performance. This is repeated when the device leaves sleep mode or fail-safe mode due to a wake event.

Table 10-124. INT_3 Register

7	6	5	4	3	2	1	0
SPIERR	SWERR	FSM	CRCERR	VCC1SC	RSTR_CNT	TSD_CAN_LIN	CRC_EEPROM
R/W1C-0b	RH-0b	R/W1C-0b	R/W1C/H-0b	R/W1C/H-0b	R/W1C/H-0b	R/W1C-0b	R/W1C-0b

Table 10-125. INT_3 Register Field Descriptions

Bit	Field	Type	Reset	Description0b
7	SPIERR	R/W1C	0b	Sets when SPI status bit sets
6	SWERR	RH	0b	Logical OR of (SW_EN=1 and NOT(SWCFG)) and FRAME_OVF. Selective Wake is not always enabled while SWERR is set
5	FSM	R/W1C	0b	Entered fail-safe mode.
4	CRCERR	R/W1C/H	0b	SPI CRC error detected
3	VCC1SC	R/W1C/H	0b	VCC1 short detected
2	RSTR_CNT	R/W1C/H	0b	Restart counter exceeded programmed count
1	TSD_CAN_LIN	R/W1C	0b	Thermal Shutdown due to VCC2, CAN or LIN transceiver
0	CRC_EEPROM	R/W1C	0b	EEPROM CRC error

10.1.63 INT_CANBUS_1 Register (Address = 54h) [reset = 00h]

INT_CANBUS is shown in Table 10-126 and described in Table 10-127.

Return to Table 10-1.

CAN bus faults that include shorts and opens CAN port 1

Table 10-126. INT_CANBUS_1 Register

7	6	5	4	3	2	1	0
UVCAN	RSVD	CANHCANL	CANHBAT	CANLGND	CANBUSOPEN	CANBUSGND	CANBUSBAT
R/W1C-0b	R-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b

Table 10-127. INT_CANBUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	UVCAN	R/W1C	0b	VCAN undervoltage
6	RSVD	R	0b	Reserved
5	CANHCANL	R/W1C	0b	CANH and CANL shorted together
4	CANHBAT	R/W1C	0b	CANH shorted to Vbat
3	CANLGND	R/W1C	0b	CANL shorted to GND
2	CANBUSOPEN	R/W1C	0b	CAN bus open
1	CANBUSGND	R/W1C	0b	CAN bus shorted to GND or CANH shorted to GND
0	CANBUSBAT	R/W1C	0b	CAN bus shorted to Vbat or CANL shorted to Vbat

10.1.64 INT_7 (Address = 55h) [reset = 00h]

INT_7 is shown in Table 10-128 and described in Table 10-129.

Return to Table 10-1.

High side switch interrupts.

Table 10-128. INT_7

7	6	5	4	3	2	1	0
HSSOC1	HSSOL1	HSSOC2	HSSOL2	HSSOC3	HSSOL3	HSSOC4	HSSOL4
R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b

Table 10-129. INT_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	HSSOC1	R/W1C	0b	High side switch 1 over current
6	HSSOL1	R/W1C	0b	High side switch 1 open load
5	HSSOC2	R/W1C	0b	High side switch 2 over current
4	HSSOL2	R/W1C	0b	High side switch 2 open load
3	HSSOC3	R/W1C	0b	High side switch 3 over current
2	HSSOL3	R/W1C	0b	High side switch 3 open load
1	HSSOC4	R/W1C	0b	High side switch 4 over current
0	HSSOL4	R/W1C	0b	High side switch 4 open load

10.1.65 INT_EN_1 Register (Address = 56h) [reset = FFh]

INT_EN_1 is shown in Table 10-130 and described in Table 10-131.

Return to Table 10-1.

Interrupt mask for INT_1. CAN errors are for CAN port 1.

Table 10-130. INT_EN_1 Register

7	6	5	4	3	2	1	0
WD_EN	CANINT_EN_1	LWU_EN	WKERR_EN	FRAME_OVF_EN_1	CANSLNT_EN_1	SWPIN_EN	CANDOM_EN_1
R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b

Table 10-131. INT_EN_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WD_EN	R/W	1b	Watchdog event interrupt mask
6	CANINT_EN_1	R/W	1b	CAN bus wake up interrupt mask
5	LWU_EN	R/W	1b	Local wake up mask
4	WKERR_EN	R/W	1b	Wake error mask
3	FRAME_OVF_EN_1	R/W	1b	Frame error counter overflow mask
2	CANSLNT_EN_1	R/W	1b	CAN silent mask
1	SWPIN_EN	R/W	1b	SWPIN wake mask
0	CANDOM_EN_1	R/W	1b	CAN TXD stuck dominant mask

10.1.66 INT_EN_2 Register (Address = 57h) [reset = 7Eh]

INT_EN_2 is shown in Table 10-132 and described in Table 10-133.

Return to Table 10-1.

Interrupt mask for INT_2

Table 10-132. INT_EN_2 Register

7	6	5	4	3	2	1	0
SMS_EN	PWRON_EN	OVCC1_EN	UVSUP5_EN	UVSUP3_EN	UVCC1_EN	TSD_VCC1_VEXCC_EN	SME_EN
R-0b	R-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R-0b

Table 10-133. INT_EN_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SMS_EN	R	0b	SMS read only
6	PWRON_EN	R	1b	Power on read only
5	OVCC1_EN	R/W	1b	VCC1 over-voltage mask
4	UVSUP5_EN	R/W	1b	VSUP5 undervoltage mask
3	UVSUP3_EN	R/W	1b	VSUP3 undervoltage mask
2	UVCC1_EN	R/W	1b	VCC1 undervoltage mask
1	TSD_VCC1_VEXCC_EN	R/W	1b	VCC1 and VEXCC thermal shutdown mask
0	SME_EN	R	0b	SME read only

10.1.67 INT_EN_3 Register (Address = 58h) [reset = FEh]

INT_EN_3 is shown in Table 10-134 and described in Table 10-135.

Return to Table 10-1.

Interrupt mask for INT_3

Table 10-134. INT_EN_3 Register

7	6	5	4	3	2	1	0
SPIERR_EN	SWERR_EN	FSM_EN	CRCERR_EN	VCC1SC_EN	RSRT_CNT_EN	TSD_CAN_LIN_EN	RSVD
R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R-1b	R-0b

Table 10-135. INT_EN_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SPIERR_ENABLE	R/W	1b	SPI error interrupt mask
6	SWERR_ENABLE	R/W	1b	Selective wake error interrupt mask
5	FSM_ENABLE	R/W	1b	Fail-safe mode interrupt mask
4	CRCERR_EN	R/W	1b	SPI CRC error interrupt mask
3	VCC1SC_EN	R/W	1b	VCC1 short circuit interrupt mask
2	RSRT_CNT_EN	R/W	1b	Restart counter exceeded programmed count mask
1	TSD_CAN_LIN_EN	R/W	1b	VCC2, CAN and LIN transceiver thermal shutdown mask
0	RSVD	R	0b	Reserved

10.1.68 INT_EN_CANBUS_1 Register (Address = 59h) [reset = BFh]

INT_EN_CANBUS is shown in Table 10-136 and described in Table 10-137.

Return to Table 10-1.

Interrupt mask for CAN port 1 bus faults

Table 10-136. INT_EN_CANBUS_1 Register

7	6	5	4	3	2	1	0
UVCAN_EN	RSVD	CANHCANL_EN	CANHBAT_EN	CANLGND_EN	CANBUSOPEN_EN	CANBUSGND_EN	CANBUSBAT_EN
R/W-1b	R-0b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b

Table 10-137. INT_EN_CANBUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	UVCAN_EN	R/W	1b	VCAN undervoltage mask
6	RSVD	R	0b	Reserved
5	CANHCANL_EN	R/W	1b	CANH and CANL shorted together mask
4	CANHBAT_EN	R/W	1b	CANH shorted to Vbat mask
3	CANLGND_EN	R/W	1b	CANL shorted to GND mask
2	CANBUSOPEN_EN	R/W	1b	CAN bus open mask
1	CANBUSGND_EN	R/W	1b	CAN bus shorted to GND mask
0	CANBUSBAT_EN	R/W	1b	CAN bus shorted to Vbat mask

10.1.69 INT_4 Register (Address = 5Ah) [reset = 00h]

INT_4 is shown in Table 10-138 and described in Table 10-139.

Return to Table 10-1.

Interrupt for LIN and high side switches

Table 10-138. INT_4 Register

7	6	5	4	3	2	1	0
LIN1_WUP	LIN1_DTO	RSVD	CYC_WUP	MODE_ERR	OVHSS	EEPROM_CRC_INT	UVHSS
R/W1C-0b	R/W1C-0b	R-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b

Table 10-139. INT_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LIN1_WUP	R/W1C	0b	LIN 1 bus wake
6	LIN1_DTO	R/W1C	0b	LIN 1 dominant state timeout, LTXD_DTO
5	RSVD	R	0b	Reserved
4	CYC_WUP	R/W1C	0b	Cyclic wake-up using the timer
3	MODE_ERR	R/W1C	0b	Illegal transceiver state for mode change request
2	OVHSS	R/W1C	0b	Over-voltage on VHSS pin for high-side switches
1	EEPROM_CRC_INT	R/W1C	0b	EEPROM saved configuration CRC error
0	UVHSS	R/W1C	0b	Under-voltage on VHSS pin for high-side switches

10.1.70 INT_6 Register (Address 5Ch) [reset = 00h]

INT_6 is shown in Table 10-140 and described in Table 10-141.

Return to Table 10-1.

Table 10-140. INT_6 Register

7	6	5	4	3	2	1	0
TSDW	UVCC1PW	UVEXCC	OVEXCC	VEXCCSC	UVCC2	OVCC2	VCC2SC
R/W1C -0b	R/W1C -0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b

Table 10-141. INT_6 Register Field Descriptions

Bit	Field	Type	Reset	Description0b
7	TSDW	R/W1C	0b	Thermal shutdown warning
6	UVCC1PW	R/W1C	0b	VCC1 under-voltage pre-warning
5	UVEXCC	R/W1C	0b	VEXCC undervoltage
4	OVEXCC	R/W1C	0b	VEXCC over-voltage
3	VEXCCSC	R/W1C	0b	VEXCC short circuit
2	UVCC2	R/W1C	0b	VCC2 under-voltage
1	OVCC2	R/W1C	0b	VCC2 over-voltage
0	VCC2SC	R/W1C	0b	VCC2 short circuit

10.1.71 INT_EN_4 Register (Address = 5Eh) [reset = DFh]

INT_EN_4 is shown in Table 10-142 and described in Table 10-143.

Return to Table 10-1.

Interrupt mask for INT_4.

Table 10-142. INT_EN_4 Register

7	6	5	4	3	2	1	0
LIN1_WUP_EN	LIN1_DTO_EN	RSVD	CYC_WUP_EN	MODE_ERR_EN	OVHSS_EN	EEPROM_CRC_INT_EN	UVHSS_EN
R/W-1b	R/W-1b	R -0b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b

Table 10-143. INT_EN_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LIN1_WUP_EN	R/W	1b	LIN 1 bus wake interrupt mask
6	LIN1_DTO_EN	R/W	1b	LIN 1 dominant state timeout interrupt mask
5	RSVD	R	0b	Reserved
4	CYC_WUP_EN	R/W	1b	Cyclic wake-up interrupt mask
3	MODE_ERR_EN	R/W	1b	Illegal transceiver state for mode change request mask
2	OVHSS_EN	R/W	1b	VHSS over-voltage mask for high-side switches
1	EEPROM_CRC_INT_EN	R/W	1b	Mask for the saved configuration data to EERPOM error
0	UVHSS	R/W	1b	VHSS under-voltage mask for high-side switches

10.1.72 INT_EN_6 Register (Address = 60h) [reset = FFh]

INT_EN_6 is shown in Table 10-144 and described in Table 10-145.

Return to Table 10-1.

Interrupt mask for INT_6.

Table 10-144. INT_EN_6 Register

7	6	5	4	3	2	1	0
TSDW_EN	UVCC1PW_EN	UVEXCC_EN	OVEXCC_EN	VEXCCSC_EN	UVCC2_EN	OVCC2_EN	VCC2SC_EN
R/W -1b	R/W -1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b

Table 10-145. INT_EN_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TSDW_EN	R/W	1b	Thermal shutdown warning mask
6	UVCC1PW_EN	R/W	1b	VCC1 under-voltage pre-warning mask
5	UVEXCC_EN	R/W	1b	VEXCC under-voltage mask
4	OVEXCC_EN	R/W	1b	VEXCC over-voltage mask
3	VEXCCSC_EN	R/W	1b	VEXCC short circuit mask
2	UVCC2_EN	R/W	1b	VCC2 pin under-voltage mask
1	OVCC2_EN	R/W	1b	VCC2 pin over-voltage mask
0	VCC2SC_EN	R/W	1b	VCC2 short circuit mask

10.1.73 INT_EN_7 Register (Address = 62) [reset = FFh]

INT_EN_7 is shown in Table 10-146 and described in Table 10-147.

Return to Table 10-1.

Interrupt mask high side switch interrupts, INT_7.

Table 10-146. INT_EN_7 Register

7	6	5	4	3	2	1	0
HSSOC1_EN	HSSOL1_EN	HSSOC2_EN	HSSOL2_EN	HSSOC3_EN	HSSOL3_EN	HSSOC4_EN	HSSOL4_EN
R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b

Table 10-147. INT_EN_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	HSSOC1_EN	R/W	1b	High side switch 1 over current interrupt mask
6	HSSOL1_EN	R/W	1b	High side switch 1 open load interrupt mask
5	HSSOC2_EN	R/W	1b	High side switch 2 over current interrupt mask
4	HSSOL2_EN	R/W	1b	High side switch 2 open load interrupt mask
3	HSSOC3_EN	R/W	1b	High side switch 3 over current interrupt mask
2	HSSOL3_EN	R/W	1b	High side switch 3 open load interrupt mask
1	HSSOC4_EN	R/W	1b	High side switch 4 over current interrupt mask
0	HSSOL4_EN	R/W	1b	High side switch 4 open load interrupt mask

11 Device and Documentation Support

This device conforms to the following CAN standards. The core of what is needed is covered within this system spec, however reference should be made to these standards and any discrepancies pointed out and discussed. This document should provide all the basics of what is needed. However, for a full understanding of CAN including the protocol these additional sources are helpful as the scope of CAN protocol in detail is outside the scope of this physical layer (transceiver) specification.

11.1 Documentation Support

11.1.1 CAN Transceiver Physical Layer Standards:

- ISO 11898-2:2024: High speed medium access unit with low power mode (super sets -2 standard electrically in several specs and adds the original wake up capability via the bus in low power mode)
- ISO 8802-3: CSMA/CD – referenced for collision detection from ISO11898-2
- SAE J2284-2: High Speed CAN (HSC) for Vehicle Applications at 250kbps
- SAE J2284-3: High Speed CAN (HSC) for Vehicle Applications at 500kbps

11.1.2 LIN Transceiver Physical Layer Standards

- ISO/DIS 17987-1: Road vehicles -- Local Interconnect Network (LIN) -- Part 1: General information and use case definition
- ISO/DIS 17987-4: 2023 Road vehicles -- Local Interconnect Network (LIN) -- Part 4: Electrical Physical Layer (EPL) specification 12V
- SAEJ2602-1: LIN Network for Vehicle Applications
- LIN2.0, LIN2.1, LIN2.2 and LIN2.2A specification

11.1.3 EMC Requirements:

- SAEJ2962-2: US3 requirements for CAN Transceivers (-2, -5, GM proposes updates to address -6 + FD, but this is the best place for a working start)
- HW Requirements for CAN, LIN, FR V1.3: German OEM requirements for CAN and LIN
- ISO 10605: Road vehicles - Test methods for electrical disturbances from electrostatic discharge
- ISO 11452-4:2011: Road vehicles - Component test methods for electrical disturbances from narrowband radiated electromagnetic energy - Part 4: Harness excitation methods
- ISO 7637-1:2015: Road vehicles - Electrical disturbances from conduction and coupling - Part 1: Definitions and general considerations
- ISO 7637-3: Road vehicles - Electrical disturbances from conduction and coupling - Part 3: Electrical transient transmission by capacitive and inductive coupling via lines other than supply lines
- IEC 62132-4:2006: Integrated circuits - Measurement of electromagnetic immunity 150kHz to 1GHz - Part 4: Direct RF power injection method
- IEC 61000-4-2
- IEC 61967-4
- CISPR25

11.1.4 Conformance Test Requirements:

- HS_TRX_Test_Spec_V_1_0: GIFT / ICT CAN test requirements for High Speed Physical Layer
- ISO/DIS 17987-7: Road vehicles -- Local Interconnect Network (LIN) -- Part 7: Electrical Physical Layer (EPL) conformance test specification
- SAEJ2602-2: LIN Network for Vehicle Applications Conformance Test

11.1.5 Related Documentation

- “A Comprehensible Guide to Controller Area Network”, Wilfried Voss, Copperhill Media Corporation
- “CAN System Engineering: From Theory to Practical Applications”, 2nd Edition, 2013; Dr. Wolfhard Lawrenz, Springer.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

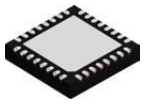
Changes from Revision * (November 2024) to Revision A (October 2025)	Page
• Updated the document from *Advanced Information* to *Production Data*	1
• Added TCAN2855-Q1 and TCAN2857-Q1 Diagram images	1

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

13.1 Mechanical Data

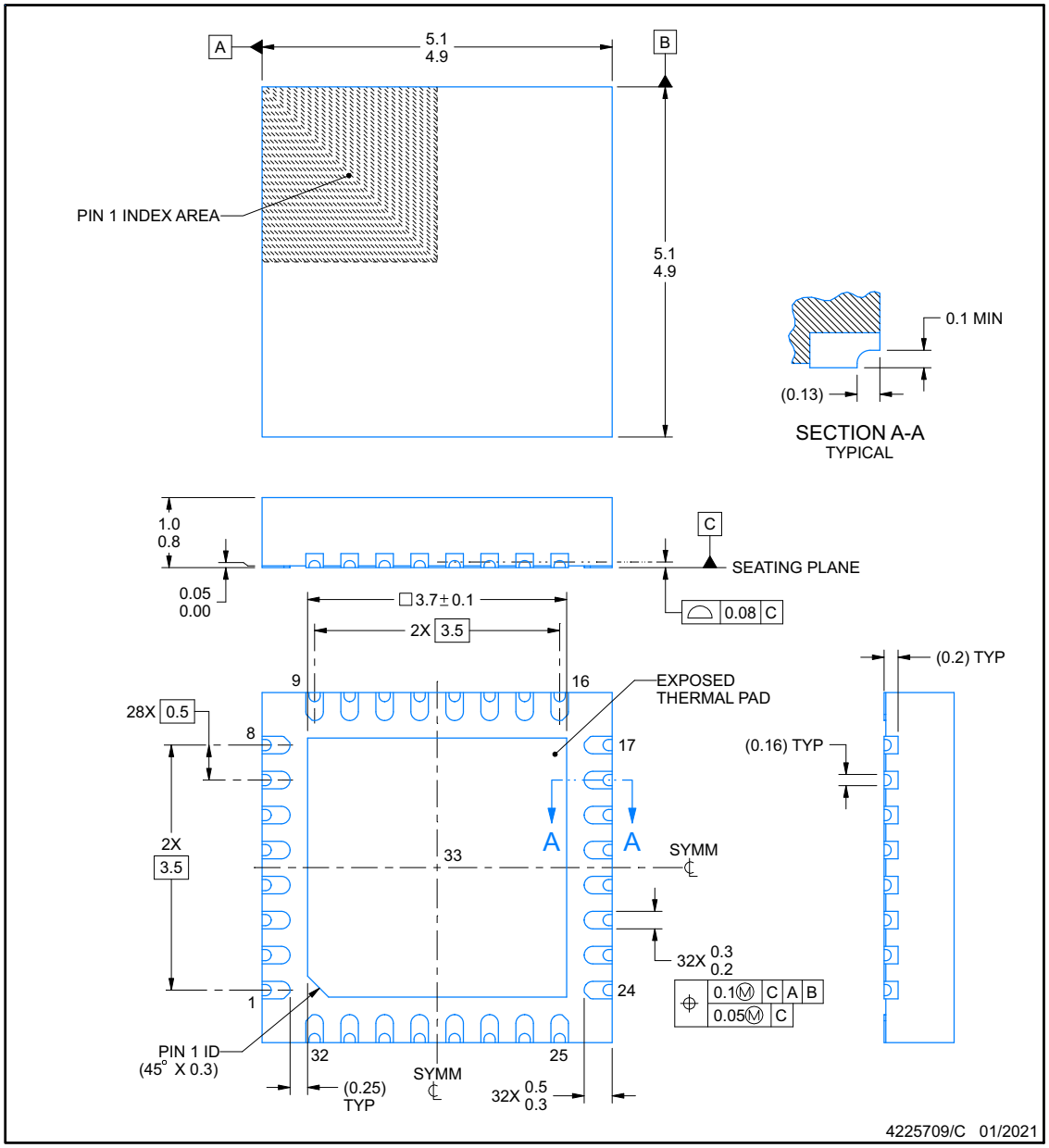
RHB0032U



PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

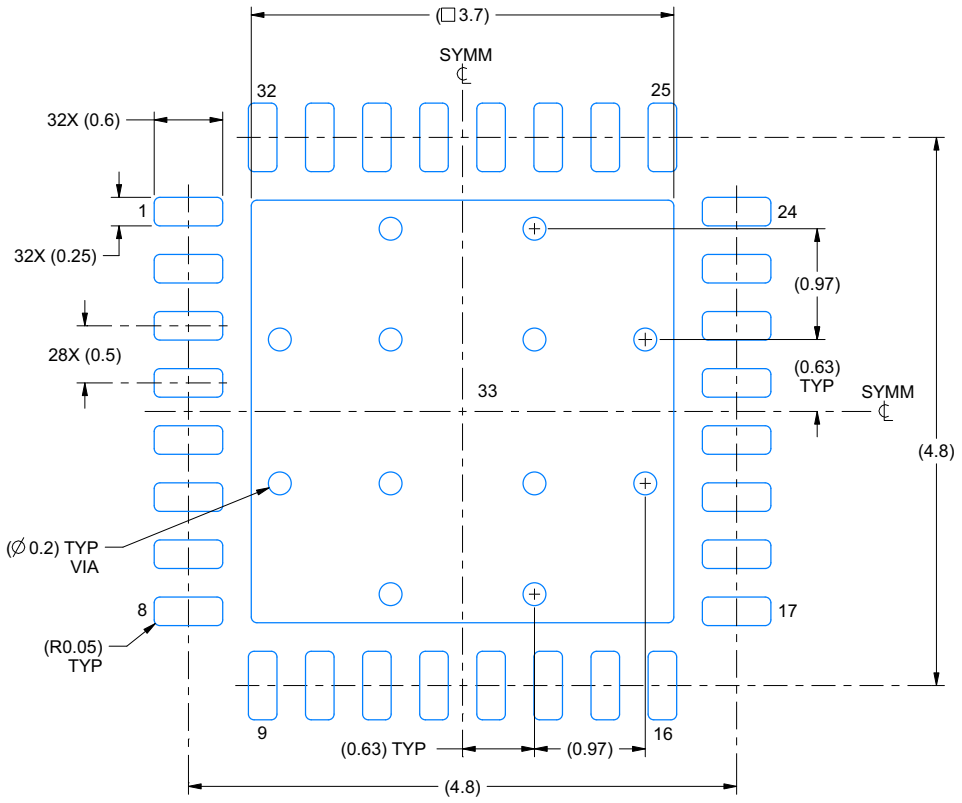
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

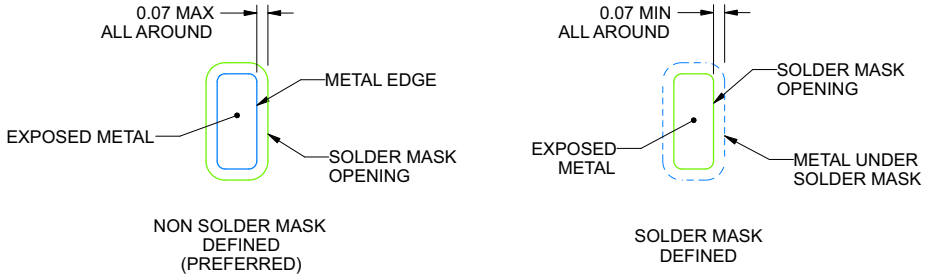
RHB0032U

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4225709/C 01/2021

NOTES: (continued)

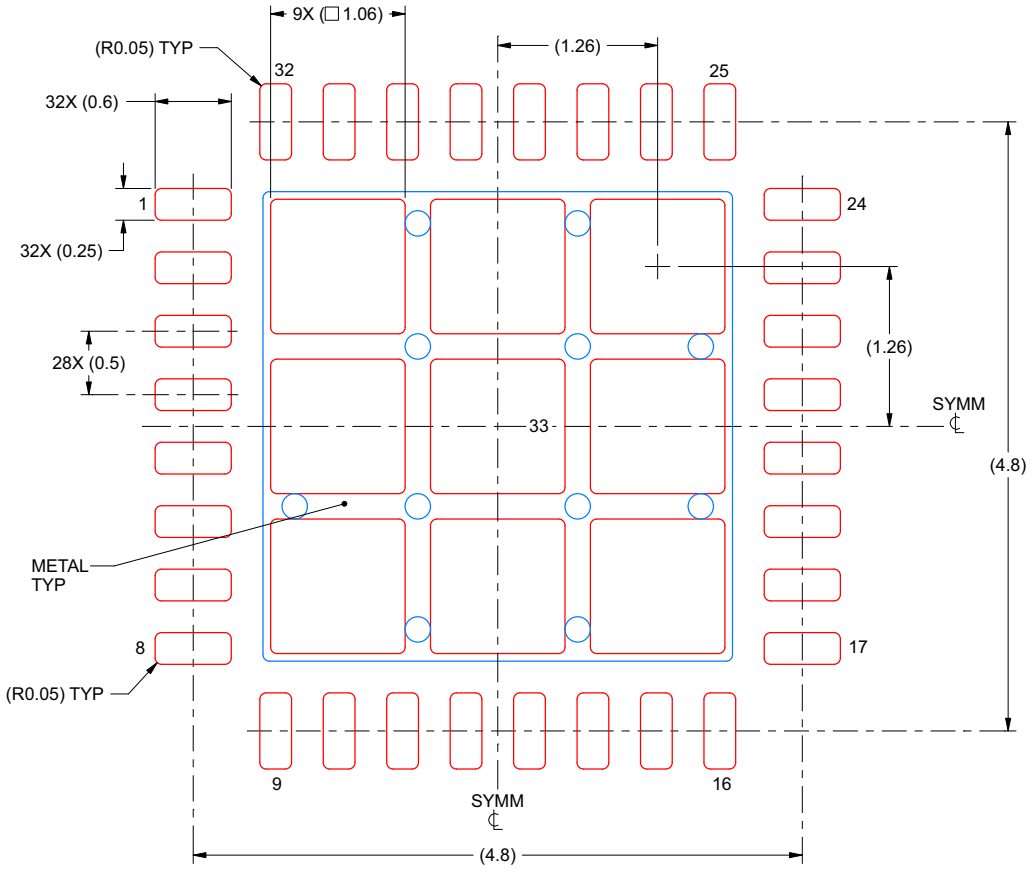
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHB0032U

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
74% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4225709/C 01/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTCAN28553RHBRQ1.A	Active	Preproduction	VQFN (RHB) | 32	5000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTCAN28555RHBRQ1.A	Active	Preproduction	VQFN (RHB) | 32	5000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTCAN28573RHBRQ1.A	Active	Preproduction	VQFN (RHB) | 32	5000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTCAN28575RHBRQ1.A	Active	Preproduction	VQFN (RHB) | 32	5000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TCAN28553RHBRQ1	Active	Production	VQFN (RHB) | 32	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TCAN 28553
TCAN28555RHBRQ1	Active	Production	VQFN (RHB) | 32	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TCAN 28555
TCAN28573RHBRQ1	Active	Production	VQFN (RHB) | 32	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TCAN 28573
TCAN28575RHBRQ1	Active	Production	VQFN (RHB) | 32	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TCAN 28575

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

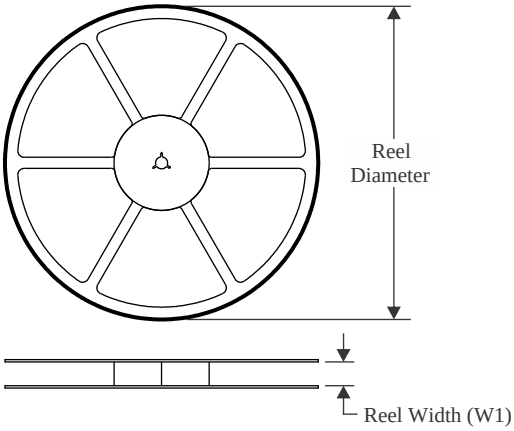
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

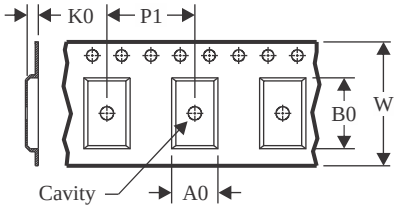
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

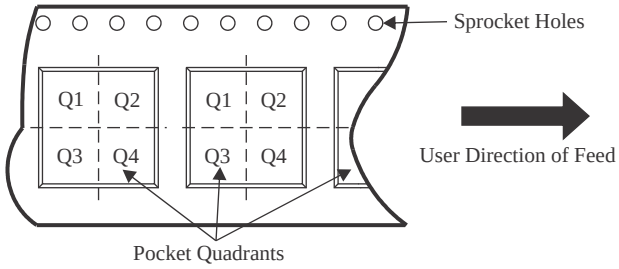


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

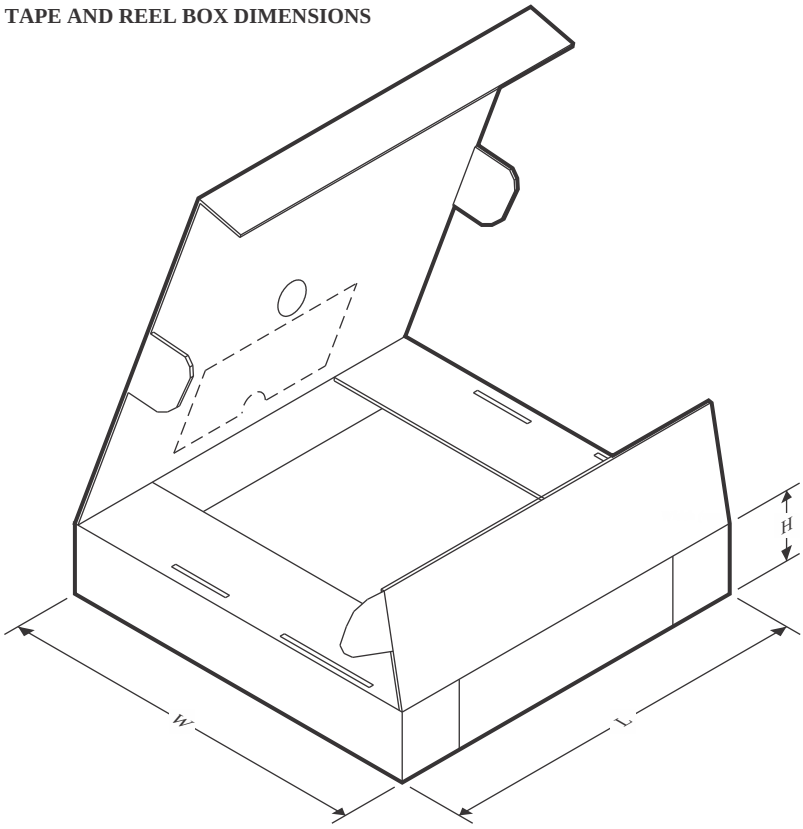
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCAN28553RHBRQ1	VQFN	RHB	32	5000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TCAN28555RHBRQ1	VQFN	RHB	32	5000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TCAN28573RHBRQ1	VQFN	RHB	32	5000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TCAN28575RHBRQ1	VQFN	RHB	32	5000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCAN28553RHBRQ1	VQFN	RHB	32	5000	360.0	360.0	36.0
TCAN28555RHBRQ1	VQFN	RHB	32	5000	360.0	360.0	36.0
TCAN28573RHBRQ1	VQFN	RHB	32	5000	360.0	360.0	36.0
TCAN28575RHBRQ1	VQFN	RHB	32	5000	360.0	360.0	36.0

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Last updated 10/2025