TCAN4572-Q1 Automotive Controller Area Network Flexible Data Rate (CAN FD) Controller with Integrated Transceiver

1 Features

- AEC-Q100: Qualified for automotive applications
  - Temperature: –40°C to 125°C T_A
- Functional Safety-Capable
- CAN FD controller with integrated CAN SIC transceiver
- CAN FD and FD Light controller supports ISO 11898-1:2024
- Transceiver meets the requirements of ISO 11898-2:2024 Annex A up to 5 Mbps
- Supports CAN FD data rates up to 5Mbps with up to 40MHz SPI clock speed
- Classic CAN backwards compatible
- Operating modes: normal, standby, sleep, and failsafe
- Wide operating ranges on CAN bus
  - ±58V bus fault protection
  - ±12V common mode
- Optimized behavior when unpowered
  - Bus and logic terminals are high impedance (No load to operating bus or application)
  - Power up and down glitch free operation

2 Applications

- Body electronics and lighting
- Infotainment and cluster
- Industrial transportation

3 Description

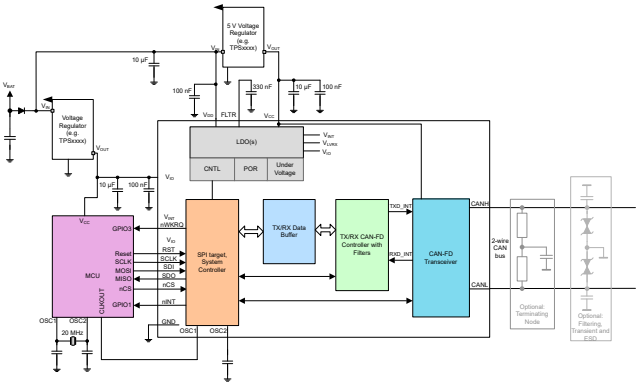
The TCAN4572-Q1 is a CAN FD controller with an integrated CAN Signal Improvement Capable (SIC) transceiver. The CAN FD controller meets the specifications of ISO11898-1:2015 and the physical layer requirements of ISO11898–2:2016. In addition, the CAN controller supports CAN FD Light protocol. The TCAN4572-Q1 provides an interface between the CAN bus and the system processor through serial peripheral interface (SPI), allowing port expansion or CAN FD support to processors. The TCAN4572-Q1 supports bus wake using the CAN bus implementing the ISO11898-2:2016 Wake Up Pattern (WUP).

The device includes many protection features providing device and CAN bus robustness. These features include failsafe mode, internal dominant state timeout, and a wide bus operating range.

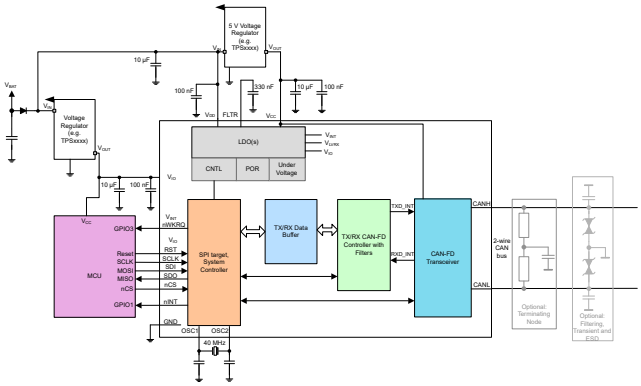
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TCAN4572	SOT-23 (16)	4.2mm × 2mm

(1) For more information, see Section 12.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematics, CLKIN from MCU



Simplified Schematics, Crystal

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4 Pin Configuration and Functions

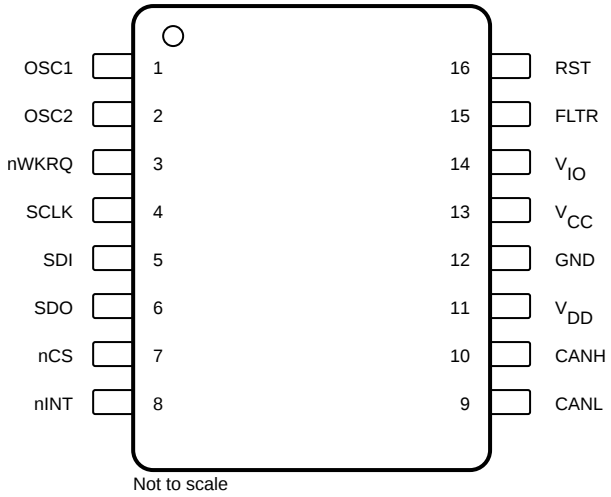

Figure 4-1. DYY Package, 16 Pin (SOT)
(Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	OSC1	I	External crystal oscillator or clock input
2	OSC2	O	External crystal oscillator output. When using single input clock to OSC1, this pin must be connected to ground
3	nWKRQ	DO	Wake request (active low). This pin is an open drain output and requires a pull-up resistor.
4	SCLK	DI	SPI clock input
5	SDI	DI	SPI responder data input from controller output
6	SDO	DO	SPI responder data output to controller input
7	nCS	DI	SPI chip select (active low)
8	nINT	DO	Interrupt pin to MCU (active low). This pin is an open drain output and requires a pull-up resistor.
9	CANL	HV Bus I/O	Low level CAN bus line
10	CANH	HV Bus I/O	High level CAN bus line
11	V_{DD}	Supply	Wide range supply input. Can be connected to battery
12	GND	GND	Ground connection
13	V_{CC}	Supply In	5V CAN bus supply voltage
14	V_{IO}	Supply In	Digital I/O voltage supply
15	FLTR	—	Internal regulator filter. Requires an external capacitor to ground
16	RST	DI	Device reset input

(1) Note: DI = Digital Input; DO = Digital Output; HV = High Voltage

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5 Specification

5.1 Absolute Maximum Ratings

over operating virtual junction temperature range for – 40 °C ≤ T_{VJ} ≤ 150 °C (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}	Device supply voltage	–0.3	42	V
V_{IO}	Supply voltage I/O level shifter	–0.3	6	V
V_{CC}	5V CAN transceiver supply voltage	–0.3	6	V
V_{FLTR}	FLTR internal digital supply pin	–0.3	1.8	V
V_{BUS_CAN}	CAN bus I/O voltage (CANH, CANL)	–42	42	V
V_I	Digital logic input terminal voltage	–0.3	6	V
V_{DO}	Digital output terminal voltage	–0.5	6	V
$I_{O(DO)}$	Digital output current		8	mA
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM) classification level H2, per AEC Q100-002 (1)	All terminal except for CANH and CANL	±4000	V
		Human body model (HBM) classification level 3A, per AEC Q100-002(2)	CANH and CANL	±12000	
		Charged device model (CDM) classification level C5, per AEC Q100-011	All terminals	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) Terminals stressed with respect to GND

5.3 ESD Ratings, IEC ESD and ISO Transient Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge according to IBEE CAN EMC (1)	Contact discharge	±8 000	V
$V_{(ESD)}$	Electrostatic discharge according to SAEJ2962-2 (2)	Contact discharge	±8 000	V
		Air discharge	±15 000	V
V_{TRAN}	ISO-7637-2 Transients according to IBEE CAN EMC test spec CAN bus terminals (CANH and CANL), and V_{DD} to GND(3)	Pulse 1	-100	V
		Pulse 2	75	V
		Pulse 3a	-150	V
		Pulse 3b	100	V
	ISO-7637-3 Transients according to IBEE CAN EMC test spec CAN terminals (CANH and CANL) to GND(3)	Direct coupling capacitor "slow transient pulse" with 100 nF coupling capacitor - powered	±30	V

(1) Results given here are specific to the IBEE CAN EMC Test specification conditions. Different system-level configurations may lead to different results. Testing performed at 3 rd party IBEE Zwickau test house, test report available upon request.
(2) SAEJ2962-2 Testing performed at 3rd party US3 approved EMC test facility, test report available upon request.

(3) ISO7637 is a system-level transient test. Results given here are specific to the IBEE CAN EMC Test specification conditions. Different system-level configurations may lead to different results.

5.4 Recommended Operating Conditions

over operating virtual junction temperature range for – 40 °C ≤ T_{VJ} ≤ 150 °C (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{DD}	Device supply voltage	4.5		36	V
V_{CC}	CAN transceiver supply voltage	4.75		5.25	V
V_{IO}	Logic pin supply voltage	1.71		5.5	V
$V_{I/O}$	Digital logic input and output terminal voltage	0		5.5	V
$I_{OH(DO)}$	Digital terminal high-level output current	–2			mA
$I_{OL(DO)}$	Digital terminal low-level output current			2	mA
C_{FLTR}	FLTR pin capacitance recommended	230	330	600	nF
		230	470	600	
C_{VDD}	V_{DD} pin capacitance recommended		100		nF
C_{VCC}	V_{CC} pin capacitance recommended		100		nF
C_{VIO}	V_{IO} pin capacitance recommended		100		nF
T_{VJ}	Virtual junction temperature	–40		150	°C

5.5 Thermal Information

THERMAL METRIC[1]		PKG DYY 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	80.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	28.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	27.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.6 Supply Characteristics

over operating virtual junction temperature range for – 40 °C ≤ T_{VJ} ≤ 150 °C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}							
I_{DD}	Device supply current	Normal	40MHz Crystal or Clock		3	4	mA
I_{DD}	Device supply current	Normal	20Mhz Crystal, Clock, or Internal		1.5	2.3	mA
I_{DD}	Device supply current	Standby	4.5V ≤ V_{DD} ≤ 36; Bus idle		1	1.5	mA
I_{DD}	Device supply current	Standby	4.5V ≤ V_{DD} ≤ 36; Bus idle		600	900	µA
I_{DD}	Device supply current	Sleep	4.5V ≤ V_{DD} ≤ 36, nCS = high; Bus idle T_J ≤ 125 °C		20	85	µA
			4.5V ≤ V_{DD} ≤ 36, nCS = high; Bus idle T_J > 125 °C		100	150	

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5.6 Supply Characteristics (continued)

over operating virtual junction temperature range for – 40 ℃ ≤ T_{VJ} ≤ 150 ℃ (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
UV_{DD}	Under voltage detection on V_{DD} rising ramp for undervotlage protection mode	Rising		3.3	3.7	4.1	V
	Under voltage detection on V_{DD} falling ramp for undervoltage protection mode	Falling		3.2	3.6	4	V
V_{DD_POR}	Power on reset for V_{DD} rising ramp	Rising		2.2	2.8	3.6	V
	Power on reset for V_{DD} falling ramp	Falling		2	2.7	3.4	V
V_{CC}							
I_{CC}	CAN Supply current, normal mode	Dominant	R_L = 60Ω, C_L = open. typical bus load			60	mA
I_{CC}	CAN Supply current, normal mode	Dominant	R_L = 50Ω, C_L = open, high bus load.			65	mA
I_{CC}	CAN Supply current, normal mode	Dominant with bus fault	CANH = - 25V, R_L = open, C_L = open			90	mA
I_{CC}	CAN Supply current, normal mode	Recessive	R_L = 60Ω, C_L = open, R_{CM} = open		2.5	4	mA
I_{CC}	CAN Supply current, standby mode	Standby mode	R_L = 60Ω, C_L = open, CANH/L terminated to 2.5V		1	5	µA
I_{CC}	CAN Supply current, sleep mode	Sleep mode	R_L = 60Ω, C_L = open, CANH/L terminated to 2.5V		1	4	µA
UV_{CCR}	Under voltage detection on V_{CC} rising ramp for protected mode				4.2	4.4	V
UV_{CCF}	Under voltage detection on V_{CC} falling ramp for protected mode			3.5	4		V
V_{IO}							
I_{IO}	I/O supply current	Normal/Standby mode	CLKIN = 40MHz,V_{IO} = 5.5V		200	2500	µA
I_{IO}	I/O supply current		Crystal = 40MHz, V_{IO} = 5.5V			3	mA
I_{IO}	I/O supply current	Normal/Standby mode	V_{IO} = 5.5V, OSC1 = OSC2 = GND			5	µA
I_{IO}	I/O supply current	Sleep mode	V_{IO} = 5.5V, OSC1 = CLKIN = 0V and OSC2 = GND			5	µA
UV_{IOR}	Under voltage detection on V_{IO} rising ramp for protected mode				1.4	1.65	V
UV_{IOF}	Under voltage detection on V_{IO} falling ramp for protected mode			1	1.25		V

5.7 Electrical Characteristics

over operating virtual junction temperature range for – 40 ℃ ≤ T_{VJ} ≤ 150 ℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS [1]	MIN	TYP	MAX	UNIT
CAN Driver Electrical Characteristics						
$V_{O(D)}$	Bus output voltage (dominant) on CANH	45Ω ≤ R_L ≤ 65Ω, C_L = open, R_{CM} = open	3		4.26	V
	Bus output voltage (dominant) on CANL		0.75		2.01	V
$V_{O(R)}$	Bus output voltage (recessive) for CANH and CANL	R_L = 45Ω ≤ R_L ≤ 65Ω, Split terminantion capacitance 4.7nF	2.256	2.5	2.756	V
$V_{O(R)}$	Bus output voltage (recessive) for CANH and CANL	R_L = open (no load), R_{CM} = open	2	2.5	3	V

5.7 Electrical Characteristics (continued)

over operating virtual junction temperature range for – 40 °C ≤ T_{VJ} ≤ 150 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS (1)	MIN	TYP	MAX	UNIT
$V_{O(INACT)}$	Bus output voltage on CANH while bus biasing inactive (Standby Mode)	R_L = open (no load), R_{CM} = open	-0.1		0.1	V
	Bus output voltage on CANL while bus biasing inactive (Standby Mode)		-0.1		0.1	V
	Bus output voltage while bus biasing inactive (Standby Mode) CANH - CANL		-0.2		0.2	V
$V_{OD(D)}$	Differential output voltage (dominant)	45Ω ≤ R_L ≤ 65Ω, C_L = open, R_{CM} = open	1.5		3	V
		45Ω ≤ R_L ≤ 70Ω, C_L = open, R_{CM} = open	1.5		3.3	V
		R_L = 2.24kΩ, C_L = open, R_{CM} = open	1.5		5	V
$V_{OD(R)}$	Differential output voltage (recessive)	R_L = 60Ω, C_L = open, R_{CM} = open	-120		12	mV
		R_L = open (no load), C_L = open, R_{CM} = open	-50		50	mV
V_{SYM}	Output symmetry (dominant or recessive) (VO(CANH) + VO(CANL)) / V_{REC}	R_L = 45Ω ≤ R_L ≤ 65Ω, C_L = open, R_{CM} = open, C1= 4.7nF, TXD_INT = 250kHz, 1MHz, 2.5MHz	0.95		1.05	V/V
V_{SYM_DC}	Output symmetry (dominant or recessive) (VCC – VO(CANH) – VO(CANL))	R_L = 45Ω ≤ R_L ≤ 65Ω, C_L = open, R_{CM} = open, C1= 4.7nF	-300		300	mV
I_{OS_DOM}	Short-circuit steady-state output current, dominant	-3.0V ≤ V_{CANH} ≤ 18.0V, CANL = open	-115			mA
		-3.0V ≤ V_{CANL} ≤+18.0V, CANH = open			115	mA
I_{OS_REC}	Short-circuit steady-state output current, recessive	– 27V ≤ V_{BUS} ≤ 42V, V_{BUS} = CANH = CANL	-5		5	mA
$R_{SE\_ACT\_REC}$	Single ended SIC impedance (CANH to common mode bias and CANL to common mode bias) during active recessive drive phase	TXD= 0V, 2V ≤ $V_{O(D)}$ ≤ VCC - 2V if –12V ≤ $V_{O(D)}$ ≤ 12V Use Delta V/ Delta I method(same as used for $R_{SE\_PAS\_REC}$/$R_{DIFF\_PAS\_REC}$ in RX section), no load on bus	37.5		66.5	Ω
$R_{DIFF\_ACT\_REC}$	Differential input resistance in active recessive drive phase (CANH to CANL)	2V ≤ $V_{O(D)}$ ≤ VCC - 2V Duration from TXD= From low-to-high edge to elapse of active recessive drive period (t_{REC_START}), Use Delta V/ Delta I method(same as used for $R_{SE\_PAS\_REC}$/ $R_{DIFF\_PAS\_REC}$ in RX section), no load on bus	75		133	Ω
CAN Receiver Electrical Characteristics						
V_{ITDOM}	Receiver dominant state differential input voltage range, bus biasing active	-12.0V ≤ V_{CANL} ≤ +12.0V -12.0V ≤ V_{CANH} ≤ +12.0V	0.9		8	V
V_{ITREC}	Receiver recessive state differential input voltage range bus biasing active		-3		0.5	V
V_{HYS}	Hysteresis voltage for input-threshold, normal modes			135		mV
V_{DIFF_DOM}	Receiver dominant state differential input voltage range, bus biasing inactive	-12.0V ≤ V_{CANL} ≤ +12.0V -12.0V ≤ V_{CANH} ≤ +12.0V	1.15		8	V
V_{DIFF_REC}	Receiver recessive state differential input voltage range, bus biasing inactive	-12.0V ≤ V_{CANL} ≤ +12.0V -12.0V ≤ V_{CANH} ≤ +12.0V	-3		0.4	V
V_{CM}	Common mode range: normal and standby mode		-12		12	V
$I_{IOFF(LKG)}$	Power-off (unpowered) bus input leakage current	V_{CANH} = V_{CANL} = 5V, V_{sup} to GND via 0Ω and 47kΩ resistor	-5		5	µA
C_I	Input capacitance to ground (CANH or CANL)				20	pF

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5.7 Electrical Characteristics (continued)

over operating virtual junction temperature range for – 40 ℃ ≤ T_{VJ} ≤ 150 ℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS (1)	MIN	TYP	MAX	UNIT
C_{ID}	Differential input capacitance				10	pF
$R_{DIFF\_PAS\_REC}$	Differential input resistance during passive recessive phase	V_{TXD} = V_{IO}, normal mode: –2V ≤ V_{CANH} ≤ +7V; –2V ≤ V_{CANL} ≤ +7V	12		100	kΩ
$R_{SE\_CANH/L}$	Single ended Input resistance during passive recessive phase (CANH or CANL)	–2V ≤ V_{CANH} ≤ +7V –2V ≤ V_{CANL} ≤ +7V	6		50	kΩ
$R_{IN(M)}$	Input resistance matching: [1– ($R_{IN(CANH)}$) / ($R_{IN(CANL)}$)] × 100%	V_{CANH} = V_{CANL} = 5.0V	–1		1	%
Thermal Shutdown						
T_{SDR}	Thermal shutdown rising		155	170	185	℃
T_{SDF}	Thermal shutdown falling		150	165	180	℃
$T_{SD(HYS)}$	Thermal shutdown hysteresis			5		℃
T_{CSD}	Thermal critical shutdown			185	200	℃
$T_{SDR\_TO\_CSD}$	Delta between thermal shutdown rising and critical themal shutdown		10	16		℃
FLTR Terminal						
V_{FLTR}	Voltage measured at FLTR pin			1.5		V
SDI, SCLK Input Terminals						
V_{IH}	High-level input voltage		0.70			V_{IO}
V_{IL}	Low-level input voltage				0.3	V_{IO}
I_{IL}	Low-level input leakage current	Inputs = 0V	-1		1	µA
I_{IH}	High-level input leakage current	Inputs = V_{IO} = 5.5V	5		30	µA
$I_{LKG(OFF)}$	Unpowered leakage current (SDI and SCK only)	Inputs = 5.5V, V_{IO} = V_{DD} = 0V	-1		1	µA
R_{PD}	Internal pull-down resistance		250	350	450	kΩ
C_{IN}	Input capacitance	20MHz		15	20	pF
SDO Output Terminal						
V_{OH}	High-level output voltage	I_{OH} = 2mA	0.8			V_{IO}
V_{OL}	Low-level output voltage	I_{OL} = 2mA			0.2	V_{IO}
$I_{LKG(OFF)}$	Unpowered leakage current	Inputs = 5.5V, V_{IO} = V_{DD} = 0V	-1		1	µA
nCS Input Terminal						
V_{IH}	High-level input voltage		0.70			V_{IO}
V_{IL}	Low-level input voltage				0.3	V_{IO}
I_{IH}	High-level input leakage current	nCS = V_{IO} = 5.5V	-1		1	µA
I_{IL}	Low-level input leakage current	nCS = 0V, V_{IO} = 5.5V	-50		-5	µA
$I_{LKG(OFF)}$	Unpowered leakage current	nCS = 5.5V, V_{IO} = V_{DD} = 0V	-1		1	µA
R_{PU}	Internal pull-up resistor		250	350	450	kΩ
C_{IN}	Input capacitance	20MHz		15	20	pF
RST Input Terminal						
V_{IH}	High-level input voltage		0.7			V_{IO}
V_{IL}	Low-level input voltage				0.3	V_{IO}
I_{IH}	High-level input leakage current	RST = V_{IO} = 5.5V	1		10	µA
I_{IL}	Low-level input leakage current	RST = 0V, V_{IO} = 5.5V	-1		1	µA
$I_{LKG(OFF)}$	Unpowered leakage current	RST = V_{IO}, V_{DD} = 0V	-1		1	µA
R_{PD}	Internal pull-down resistor		0.65	1.3	1.95	MΩ

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5.7 Electrical Characteristics (continued)

over operating virtual junction temperature range for – 40 °C ≤ T_{VJ} ≤ 150 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS (1)	MIN	TYP	MAX	UNIT
$\overline{INT}$ Output Terminal						
V_{OL}	Low-level output voltage	I_{OL} = 6mA			0.7	V
nWKRQ Output Terminal						
V_{OL}	Low-level output voltage	I_{OL} = 6mA			0.7	V
OSC1/OSC2 Terminal and Crystal Specification						
V_{IH}	High-level input voltage	Single Ended Clock Input. OSC2 = GND, OSC1 is tested	0.85			V_{IO}
V_{IL}	Low-level input voltage	Single Ended Clock Input. OSC2 = GND, OSC1 is tested			0.3	V_{IO}
F_{OSC1}	Clock-In frequency tolerance	20MHz	-0.5		0.5	%
F_{OSC1}	Clock-In frequency tolerance	40MHz	-0.5		0.5	%
C_{OSC1}	Pin capacitance of OSC1		6	8	10	pF
C_{OSC2}	Pin capacitance of OSC2		3	5	7	pF
t_{OSC}	Clock-in period		12		50	ns
t_{DC}	Input duty cycle		45		55	%
ESR	Crystal ESR for load capacitance				60	Ω

(1) All TXD_INT, RXD_INT and EN_INT references are for internal nodes that represent the same functions for a physical layer transceiver.

5.8 Timing Requirements

over operating virtual junction temperature range for – 40 °C ≤ T_{VJ} ≤ 150 °C (unless otherwise noted)

Parameter		Test Conditions	MIN	TYP	MAX	UNIT
Supply						
t_{TSD}	Thermal shutdown timer	Upon a thermal shutdown event this timer starts and provides time for junction temperature to return. See Thermal Shutdown for description of thermal shut down.	250		550	ms
$t_{UVIO\_RE\text{-}ENABLE}$	Re-enable time after UV event clears	Time for device to be ready for SPI transactions once the UV_{IO} under voltage event is cleared			300	µs
t_{UV}	Under voltage filter time	If a UV_{CC} or UV_{IO} event expires this timer, the device can go to sleep if failsafe feature is enabled.	250		550	ms
t_{UVIO}	Under voltage filter time	Upon a UV_{IO} event this timer starts and provides time for the supply input to return. When it expires, it will disable the output drivers.	20	30	40	µs
t_{UVCC}	Under voltage filter time	Upon a UV_{CC} event this timer starts. When it expires, it disables the CAN driver.	7	10	20	µs
Mode Change Timing						
$t_{MODE\_POR\_STBY}$	Time from device powering VDD and VIO to first nINT assertion (internal clock)	VDD powered up, power VIO, OSC1 = OSC2 = GND			1	ms
$t_{MODE\_STBY\_NOM}$	Standby to normal mode change time based upon SPI write			3	5	µs
$t_{MODE\_NOM\_SLP}$	SPI write to go to Sleep from Normal: WKRQ turned off			5	10	µs

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5.8 Timing Requirements (continued)

over operating virtual junction temperature range for – 40 °C ≤ T_{VJ} ≤ 150 °C (unless otherwise noted)

Parameter		Test Conditions	MIN	TYP	MAX	UNIT
$t_{MODE\_SLP\_STBY}$	Time from WUP event until nWKRQ goes low. Clocks begin power up at nWKRQ going low			1.2	5	µs
$t_{MODE\_NOM\_STBY}$	SPI write to go to standby from normal mode.			3	5	µs
Reset						
t_{RST}	RST pin pulse width to reset device. Shorter pulses than minimum might be ignored		50			µs
t_{RESET_TIME}	The time after a reset event before the device is ready.	CLKIN/Crystal = 20MHz			700	µs
Clock Switching						
$t_{CLKIN\_STARTUP}$ (1)	If clock input is toggling before nINT/nWKRQ (from sleep) goes low, the minimum wait time from nINT going low to when ready for a SPI transaction	20MHz or 40MHz Clock Input After POR or coming out of sleep mode.	300			µs
$t_{CLKIN\_STARTUP}$ (1)	The minimum wait time from the input clock starting to toggle to when ready for a SPI transaction when input clock begins to toggle after nINT/nWKRQ going low	20MHz or 40MHz Clock Input After POR or coming out of sleep mode.	300			µs
t_{CLOCK_SWITCH}	The required time it takes for the system to switch to the requested clock. This is the time the MCU must wait after a clock switch event before the device is ready to use the clock. When switching to a crystal, the time can be longer since each crystal start up time is different	Switching to internal HS clock or external clock in. Switch time with a crystal is dependent upon crystal and capacitance used.	100			µs

(1) This specification is guaranteed by design and is not tested in production

5.9 Switching Characteristics

over operating virtual junction temperature range for – 40 °C ≤ T_{VJ} ≤ 150 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Internal Oscillator						
OSC1 and OSC2 Pins						
t_{OSC_READY}	High-speed oscillator stabilization period from UVIO to oscillator stable	40MHz Crystal Note: This value is application and crystal dependent		3		ms
Device Switching Characteristics						
t_{WK_FILTER}	Bus time to meet filtered bus requirements for wake-up request	Standby mode	500		950	ns
$t_{WK\_TIMEOUT}$	Bus wake-up timeout: time that a WUP must take place within to be considered valid		0.8		2	ms
$t_{SILENCE}$	Timeout for bus inactivity	Timer is reset and restarted when bus changes from dominant to recessive or vice versa.	0.6		1.2	s

ADVANCE INFORMATION

5.9 Switching Characteristics (continued)

over operating virtual junction temperature range for – 40 °C ≤ T_{VJ} ≤ 150 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{INACTIVE}$	Time required for the processor to clear wake flag or put the device into normal mode upon power up, power on reset or after wake event otherwise the device will enter sleep mode		2	4	6	min
t_{BIAS}	Time from the start of a dominant-recessive-dominant sequence	Each phase 6µs until V_{sym} ≥ 0.1			250	µs
$t_{TXD\_INT\_DTO}$	Dominant time out(2) (CAN transceiver only)(1)		1		5	ms
Transmitter and Receiver Switching Characteristics						
$t_{BIT(BUS)-2M}$	Transmitted recessive bit width at 2Mbps	RST = 0V, 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF	490		510	ns
$t_{BIT(BUS)-5M}$	Transmitted recessive bit width at 5Mbps	RST = 0V, 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF	190		210	ns
$t_{BIT(RXD)-2M}$	Received recessive bit width at 2Mbps	RST = 0V, 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF	470		520	ns
$t_{BIT(RXD)-5M}$	Received recessive bit width at 5Mbps	RST = 0V, 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF	170		220	ns
Δt_{REC} (3)	Receiver Timing symmetry at 2Mbps	RST = 0V, 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF	-20		15	ns
Δt_{REC} (3)	Receiver Timing symmetry at 5Mbps	RST = 0V, 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF	-20		15	ns
$t_{PAS\_REC\_START}$	Signal improvement start time of passive recessive phase	Measured from rising TXD edge with < 5ns slope at 50% threshold, to the end of the signal improvement phase; $R_{DIFF\_PAS\_REC}$ ≥ MIN $R_{DIFF\_ACT\_REC}$; $R_{SE\_CANH/L}$ ≥ MIN $R_{SE\_SIC\_REC}$			530	ns
$t_{ACT\_REC\_START}$	Start time of active signal improvement phase	Measured from rising TXD edge with < 5ns slope at 50% threshold,			120	ns
$t_{ACT\_REC\_END}$	End time of active signal improvement phase	Measured from rising TXD edge with < 5ns slope at 50% threshold,	355			ns
$t_{prop(TXD\_BUSREC)}$	Propagation delay time, low-to-high TXD edge to driver recessive (dominant to recessive)	Typical conditions: 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF, R_{CM} = open		55	80	ns
$t_{prop(TXD\_BUSDOM)}$	Propagation delay time, high-to-low TXD edge to driver dominant (recessive to dominant)	Typical conditions: 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF, R_{CM} = open		55	80	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHR} - t_{PLD} \rvert$)	Typical conditions: 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF, R_{CM} = open		15	25	ns
t_R	Differential output signal rise time:	Typical conditions: 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF, R_{CM} = open		30	60	ns
t_F	Differential output signal fall time:	Typical conditions: 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF, R_{CM} = open		30	55	ns
$t_{prop(BUSREC\_RXD)}$	Propagation delay time, bus recessive input to RXD high output (dominant to recessive)	C_{RXD} = 15pF; CANL = 1.5V, CANH = 3.5V		65	110	ns
$t_{prop(BUSDOM\_RXD)}$	Propagation delay time, bus dominant input to RXD low output (recessive to dominant)	C_{RXD} = 15pF; CANL = 1.5V, CANH = 3.5V		60	110	ns
t_{LOOP}	Loop Delay(1)	Typical conditions: 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF, C_{RXD} = 15pF, 4.5V ≤ VCC ≤ 5.5V, VCC1 ± 2%			190	ns
SPI Switching Characteristics						

ADVANCE INFORMATION

5.9 Switching Characteristics (continued)

over operating virtual junction temperature range for – 40 °C ≤ T_{VJ} ≤ 150 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCK}	SCLK, SPI clock frequency	f_{OSC} = 20 (CRC Off), 40Mhz V_{IO} ≥ 3.0V Standby or Normal Mode			40	MHz
		f_{OSC} = 20 (CRC Off), 40Mhz V_{IO} < 3.0V Standby or Normal Mode			20	
		f_{OSC} = 20MHz (CRC On) Standby or Normal Mode			20	
		Sleep Mode			20	
t_{SCK}	SCLK, SPI clock period		25			ns
t_{RSCK}	SCLK rise time	f_{SCLK} = 40MHz			6	ns
t_{FSCK}	SCLK fall time	f_{SCLK} = 40MHz			6	ns
t_{SCKH}	SCLK, SPI clock high		11			ns
t_{SCKL}	SCLK, SPI clock low		11			ns
t_{CSS}	Chip select setup time		10			ns
t_{CSH}	Chip select hold time		10			ns
t_{CSD}	Chip select disable time		50			ns
t_{SISU}	Data in setup time		5			ns
t_{SIH}	Data in hold time		5			ns
t_{SOV}	Data out valid				10	ns
t_{RSO}	SDO rise time	C_L = 10pF			10	ns
t_{FSO}	SDO fall time	C_L = 10pF			10	ns

(1) All TXD_INT, RXD_INT, EN_INT and CAN transceiver only references are for internal nodes that represent the same functions for a stand-alone transceiver.

(2) The TXD_INT dominant time out ($t_{TXD\_INT\_DTO}$) disables the driver of the transceiver once the TXD_INT has been dominant longer than $t_{TXD\_INT\_DTO}$, which releases the bus lines to recessive, preventing a local failure from locking the bus dominant. The driver can only transmit dominant again after TXD_INT has been returned HIGH (recessive). While this protects the bus from local faults, locking the bus dominant, it limits the minimum data rate possible. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD_INT) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the $t_{TXD\_INT\_DTO}$ minimum, limits the minimum bit rate. The minimum bit rate can be calculated by: Minimum Bit Rate = 11/ $t_{TXD\_INT\_DTO}$ = 11 bits / 1.2ms = 9.2kbps.

(3) $\Delta t_{Rec} = t_{BIT(RXD)} - t_{BIT(BUS)}$

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6 Parameter Measurement Information

Note

All TXD_INT, RXD_INT and EN_INT references are for internal nodes that represent the same functions for a physical layer transceiver. In test mode these can be brought out to pins to test the transceiver or CAN FD controller.

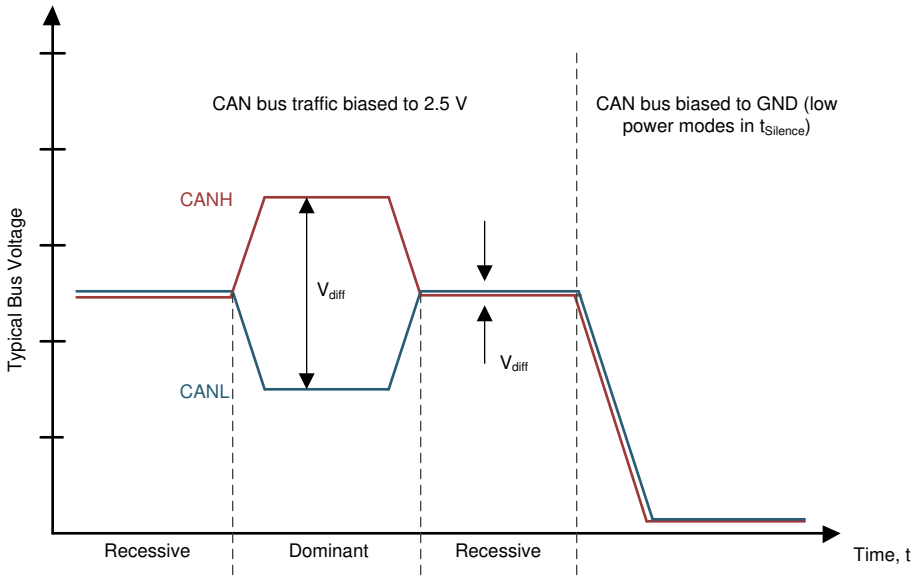
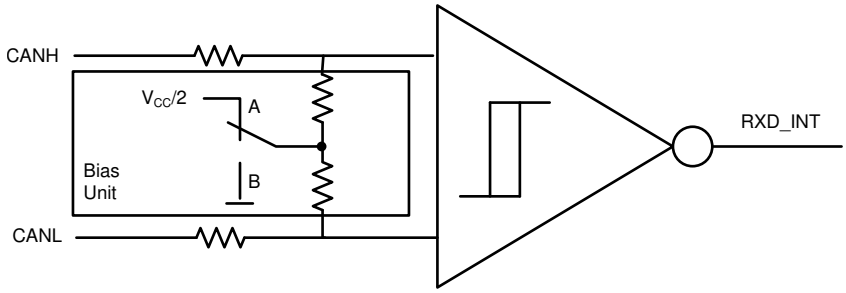


Figure 6-1. Bus States (Physical Bit Representation)



A. A: Selective Wake
B. B: Standby and Sleep Modes (Low Power)

Figure 6-2. Simplified Recessive Common Mode Bias Unit and Receiver

ADVANCE INFORMATION

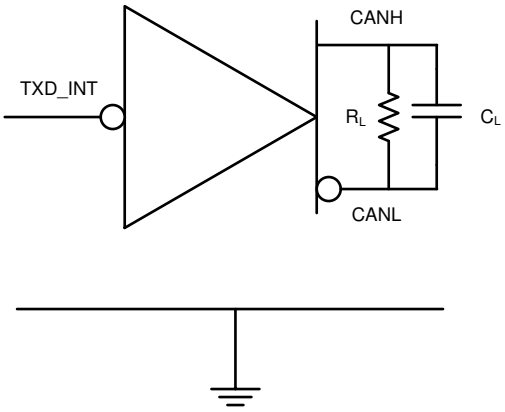


Figure 6-3. Supply Test Circuit

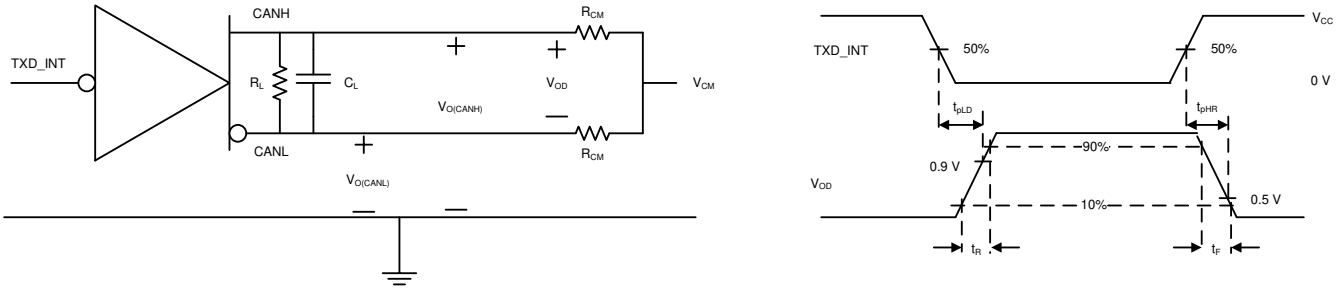


Figure 6-4. Driver Test Circuit and Measurement

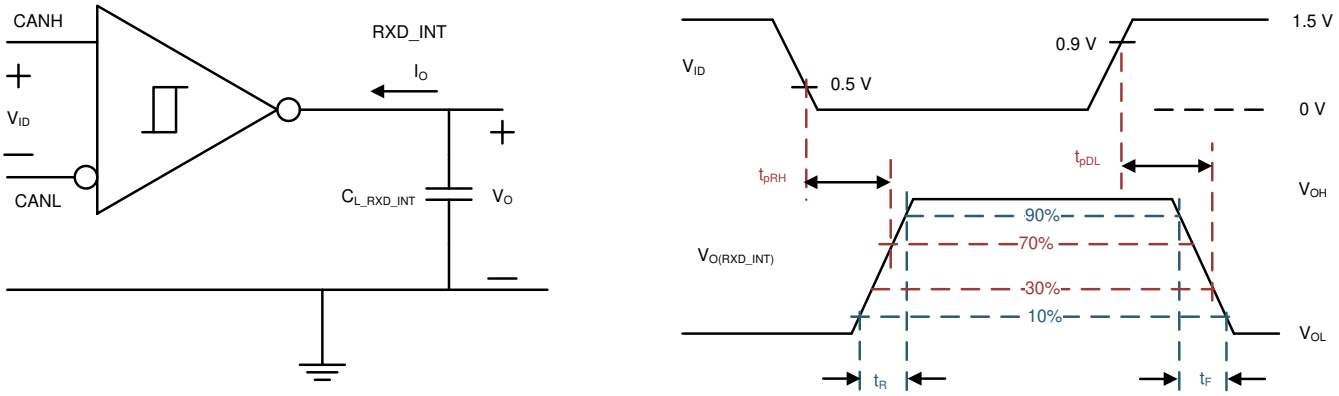


Figure 6-5. Receiver Test Circuit and Measurement

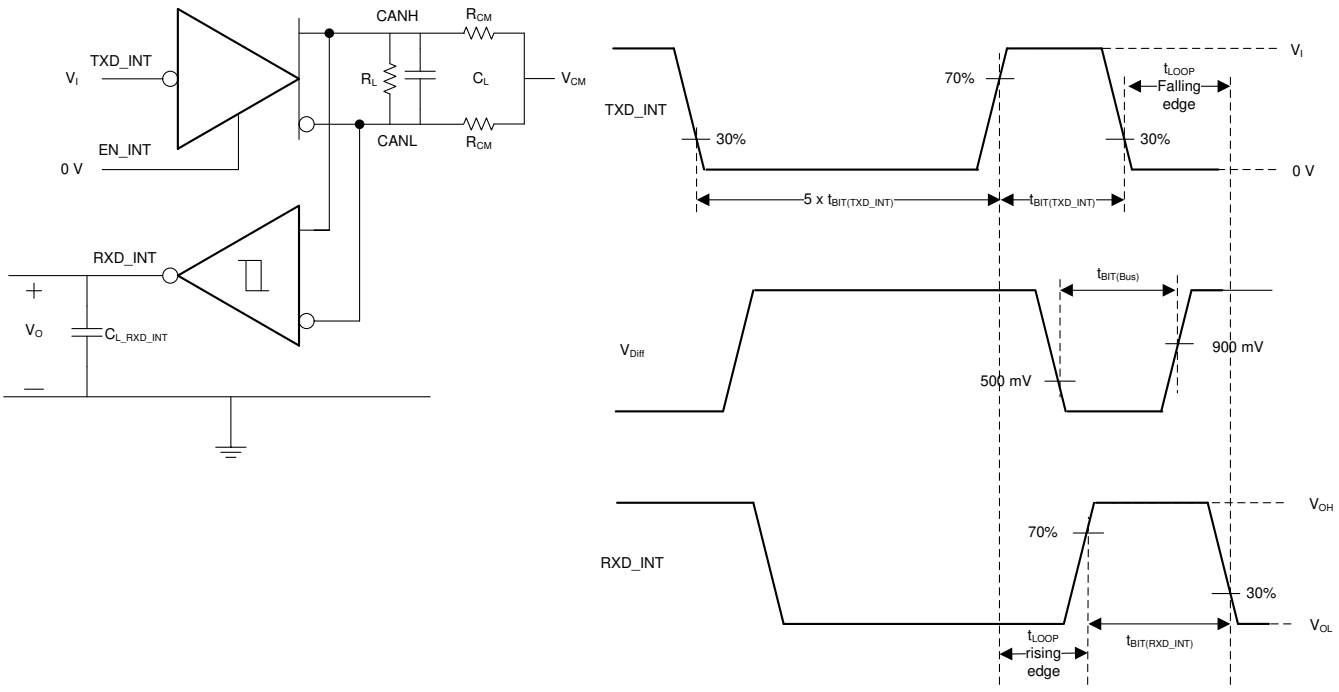


Figure 6-6. Transmitter and Receiver Timing Behavior Test Circuit and Measurement

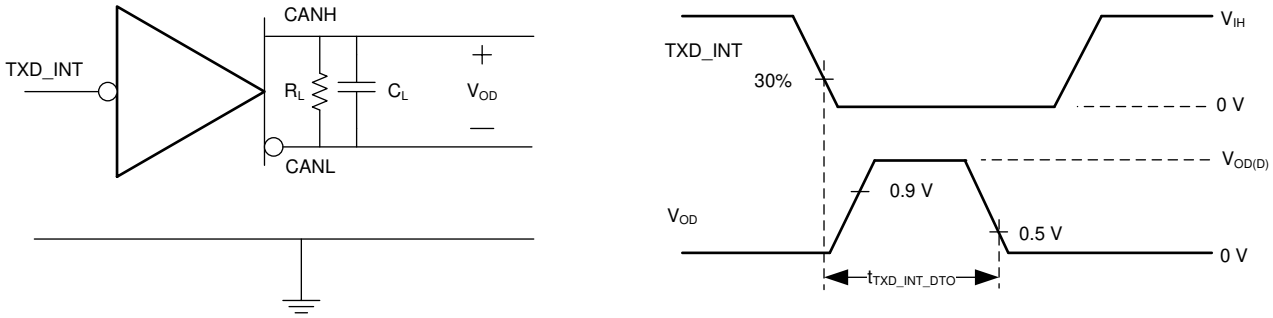


Figure 6-7. TXD_INT Dominant Timeout Test Circuit and Measurement

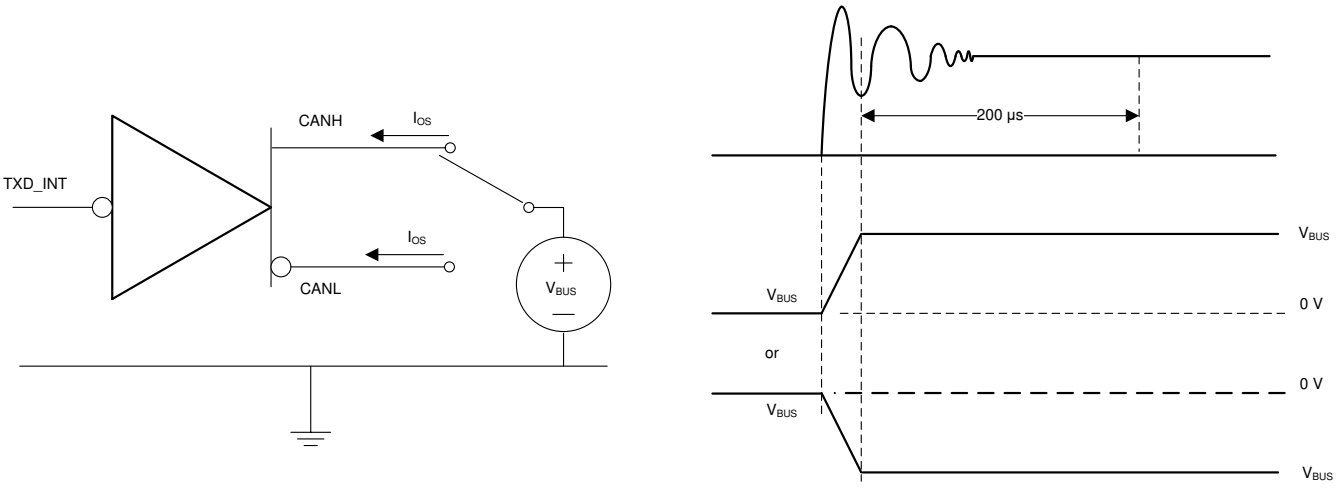


Figure 6-8. Driver Short-Circuit Current Test and Measurement

ADVANCE INFORMATION

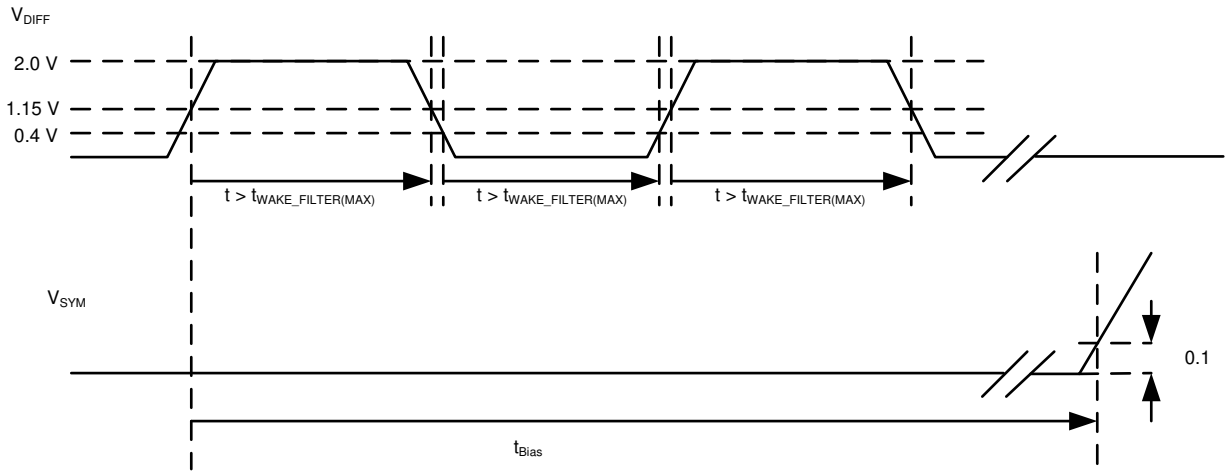


Figure 6-9. Test Signal Definition for Bias Reaction Time Measurement

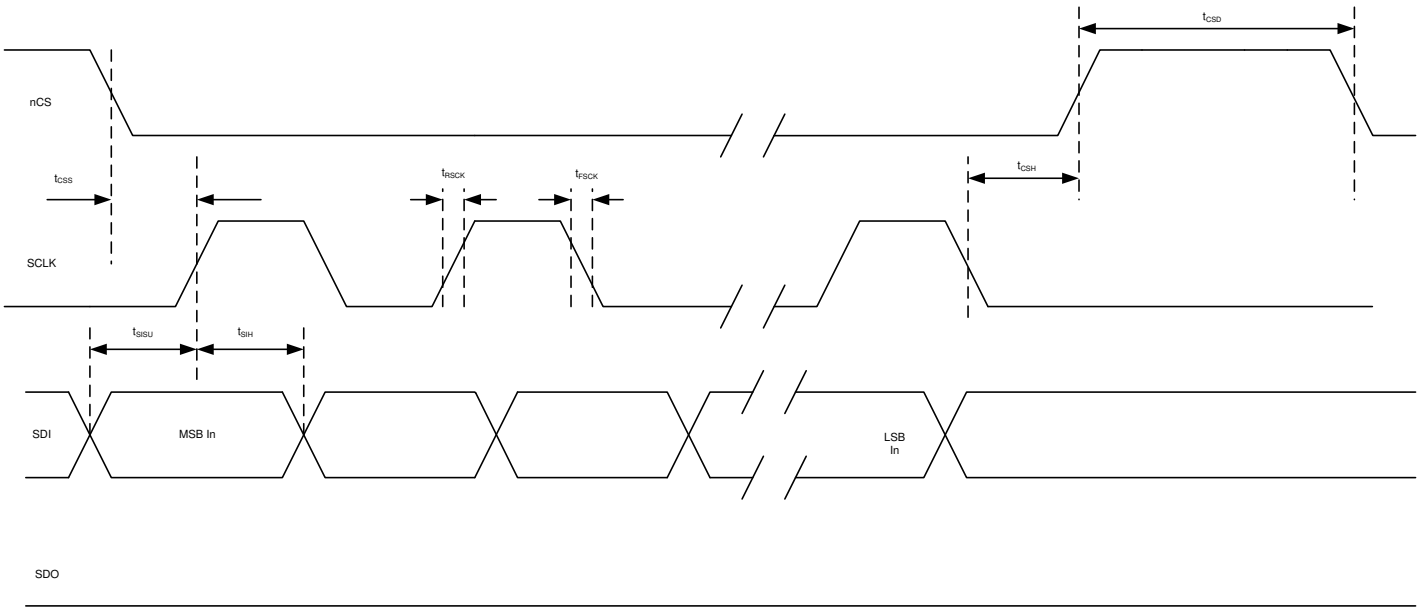


Figure 6-10. SPI AC Characteristic Write

ADVANCE INFORMATION

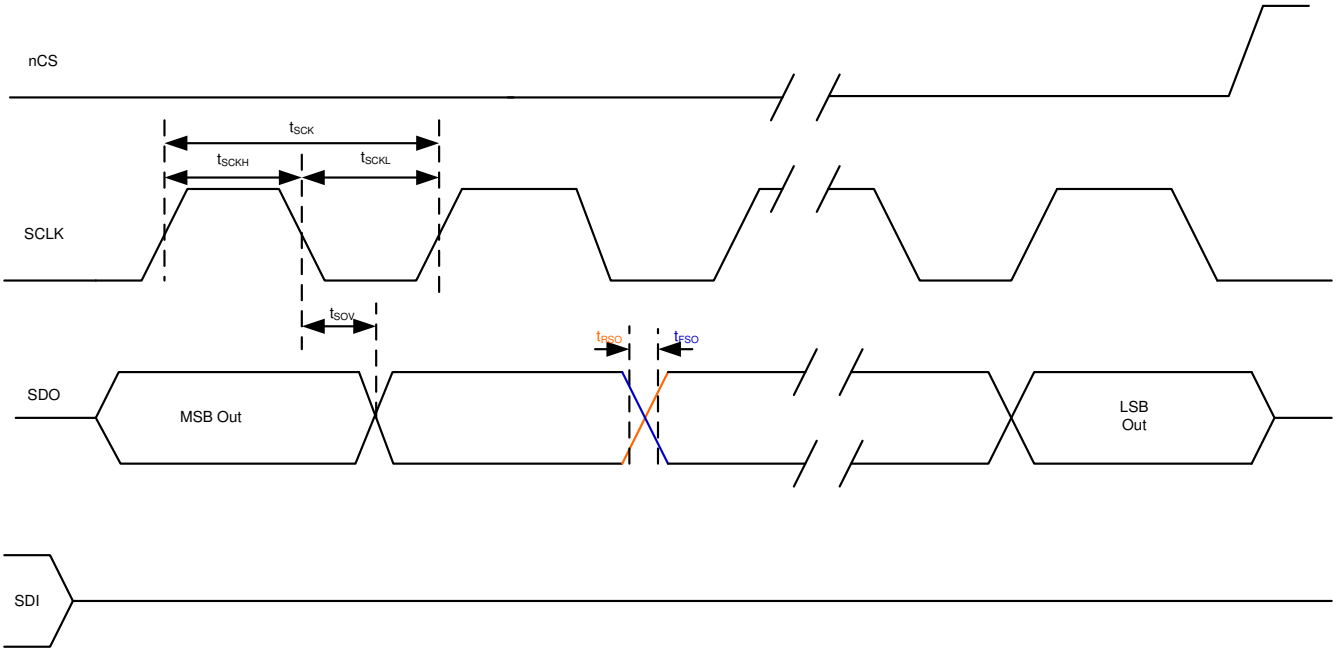


Figure 6-11. SPI AC Characteristic Read

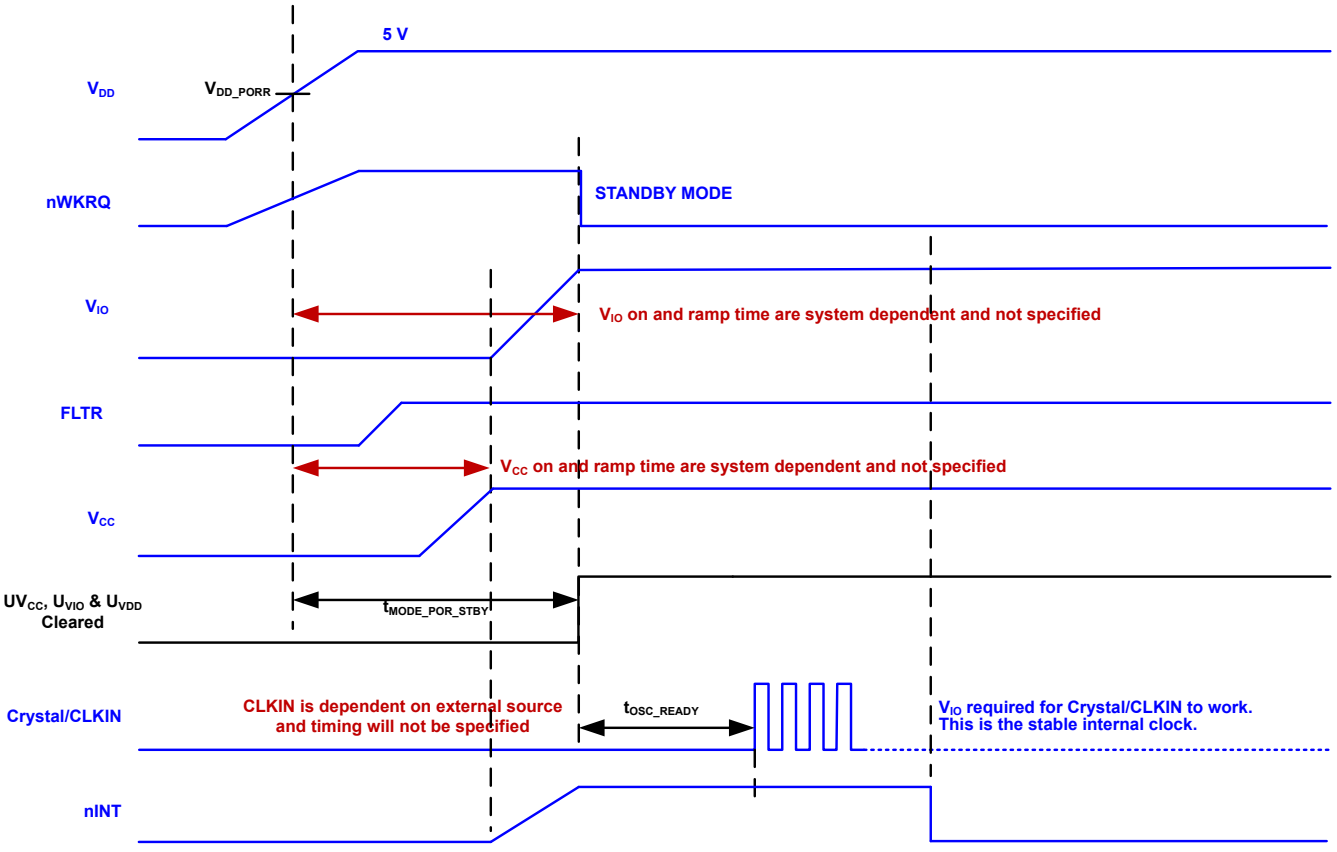


Figure 6-12. Power Up Timing

ADVANCE INFORMATION

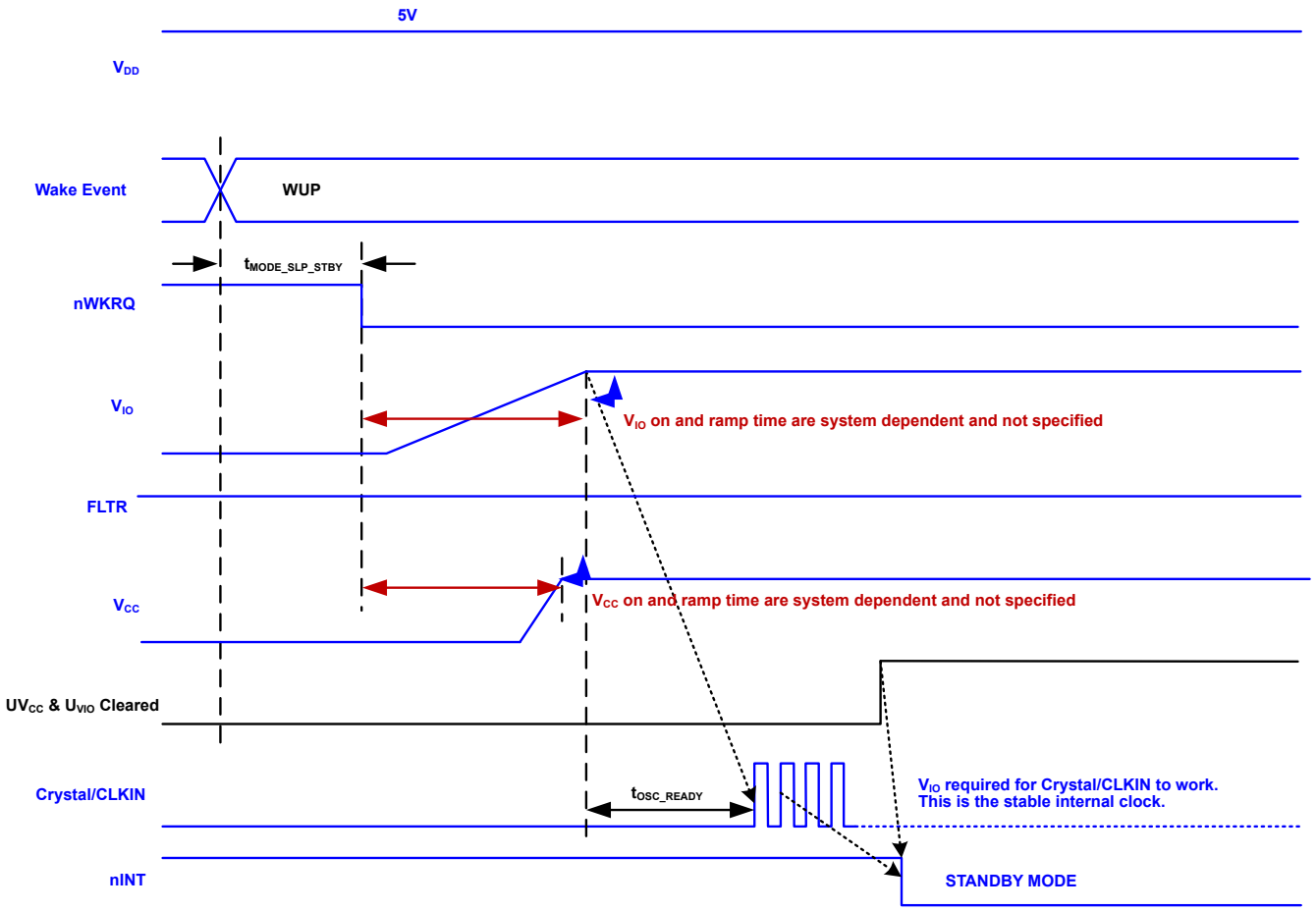


Figure 6-13. Sleep to Standby Timing (via bus or SPI)

Note

When using single ended clock input, the nINT pin can assert prior to receiving the single ended input clock due to using an internal clock while waiting for the single ended input.

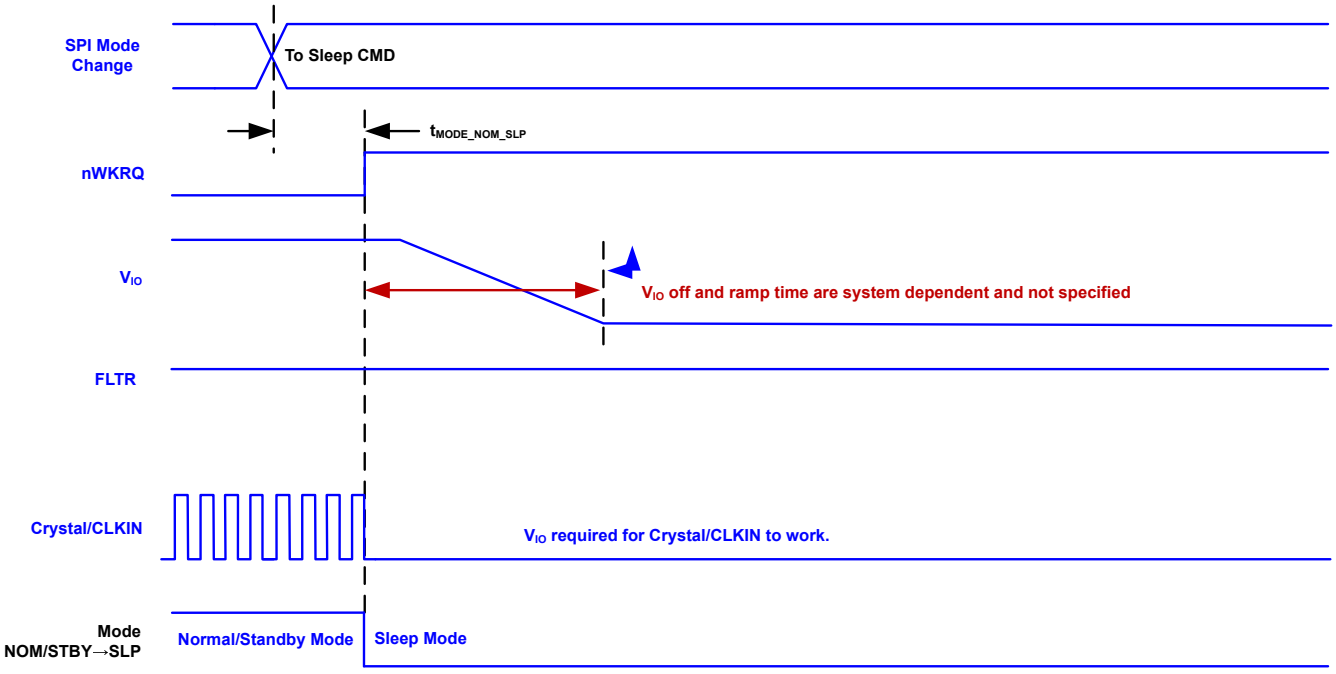


Figure 6-14. Normal or Standby to Sleep Timing

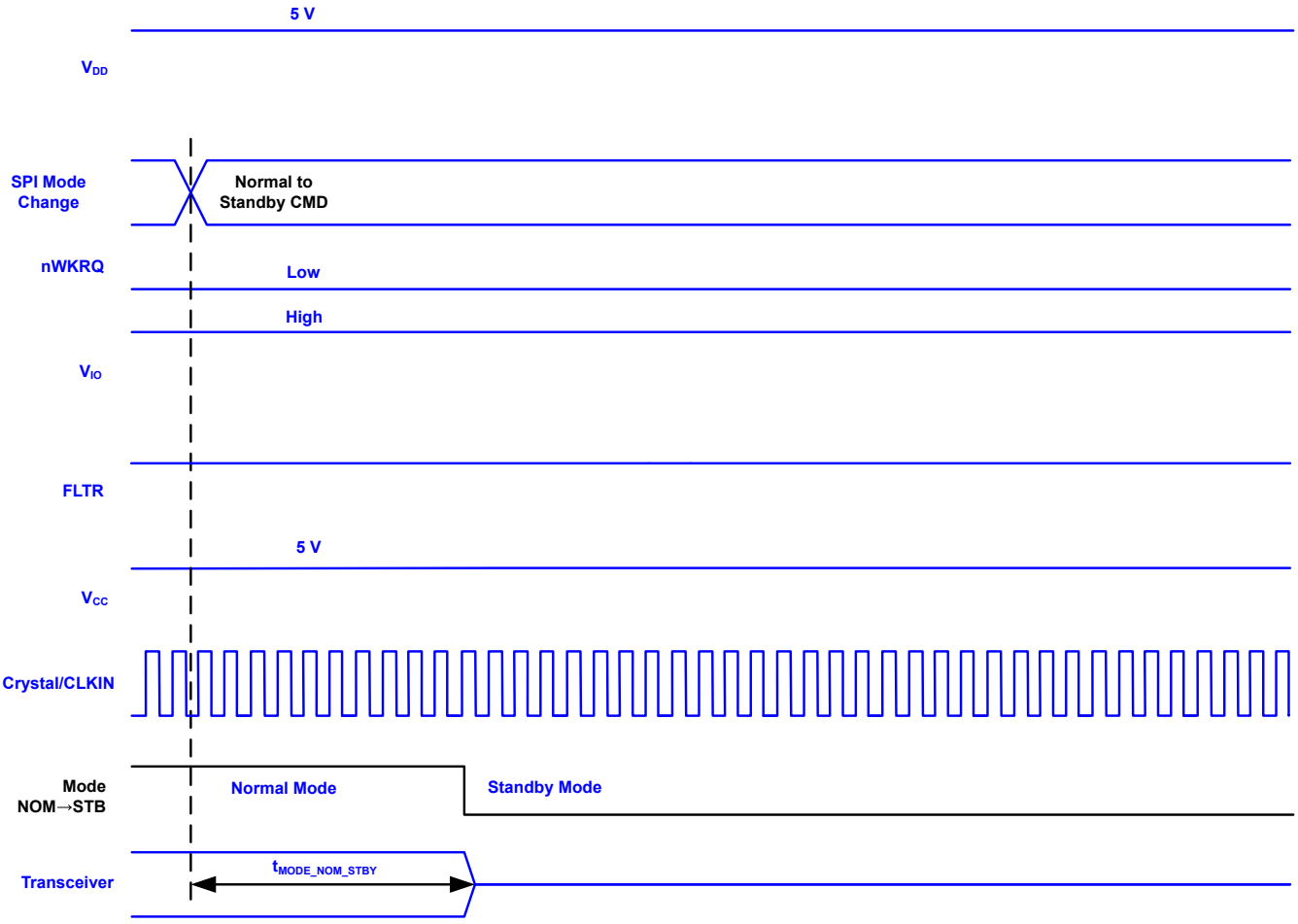


Figure 6-15. Normal to Standby Timing

ADVANCE INFORMATION

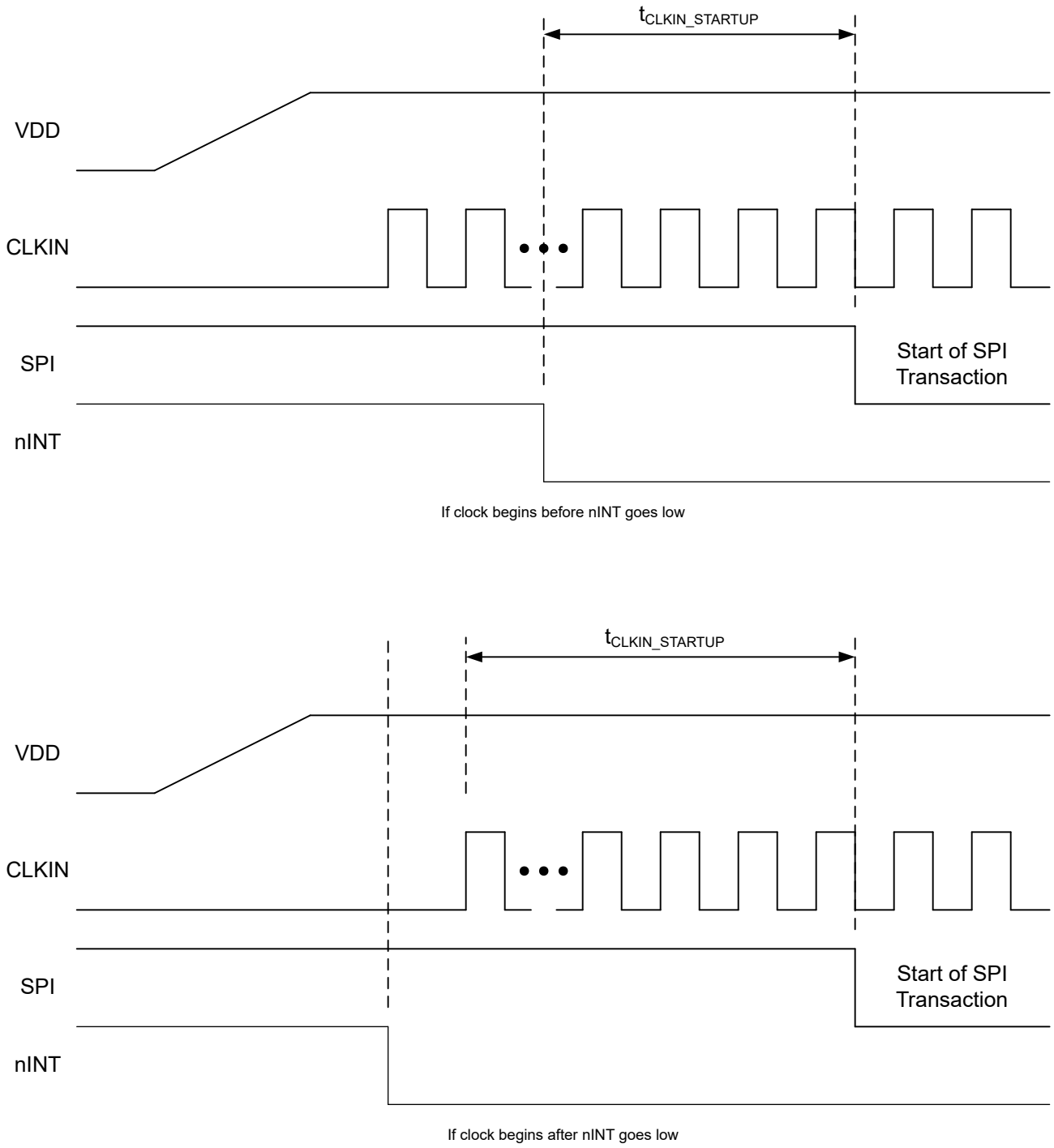


Figure 6-16. Single Ended Clock Input Timing

7 Detailed Description

7.1 Overview

The TCAN4572-Q1 is a CAN FD controller with an integrated CAN FD transceiver supporting data rates up to 5Mbps. The CAN FD controller meets the specifications of the ISO 11898-1:2015 high speed Controller Area Network (CAN) data link layer and meets the physical layer requirements of the ISO 11898-2:2016 High Speed Controller Area Network (CAN) specification providing an interface between the CAN bus and the CAN protocol controller supporting both classical CAN and CAN FD up to 5 megabits per second (Mbps). The TCAN4572-Q1 provides CAN FD transceiver functionality: differential transmit capability to the bus and differential receive capability from the bus. The device includes many protection features providing device and CAN bus robustness. The device can also wake up via remote wake up using CAN bus implementing the ISO 11898-2:2016 Wake Up Pattern (WUP). The TCAN4572-Q1 has a Serial Peripheral Interface (SPI) that connects to a local microprocessor for the device's configuration; transmission and reception of CAN frames.

The CAN bus has two logical states during operation: recessive and dominant.

In the recessive bus state, the bus is biased to a common mode of 2.5V via the high resistance internal input resistors of the receiver of each node. Recessive is equivalent to logic high. The recessive state is also the idle state.

In the dominant bus state, the bus is driven differentially by one or more drivers. Current flows through the termination resistors and generates a differential voltage on the bus. Dominant is equivalent to logic low. A dominant state overwrites the recessive state.

During arbitration, multiple CAN nodes can transmit a dominant bit at the same time. In this case, the differential voltage of the bus is greater than the differential voltage of a single driver.

Transceivers with low power Standby Mode have a third bus state where the bus terminals are weakly biased to ground via the high resistance internal resistors of the receiver. The TCAN4572-Q1 supports auto biasing, see Section 8.1.3.2

ADVANCE INFORMATION

7.2 Functional Block Diagram

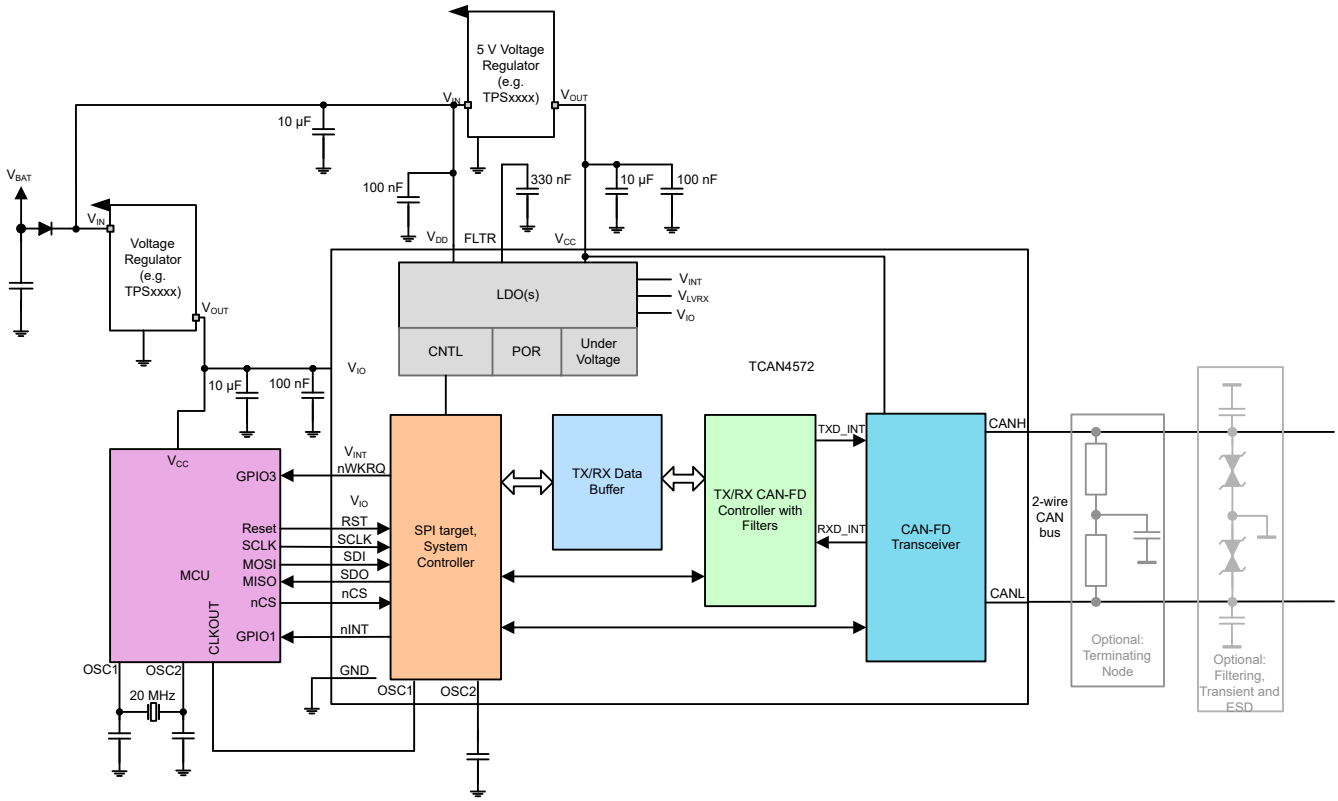


Figure 7-1.

ADVANCE INFORMATION

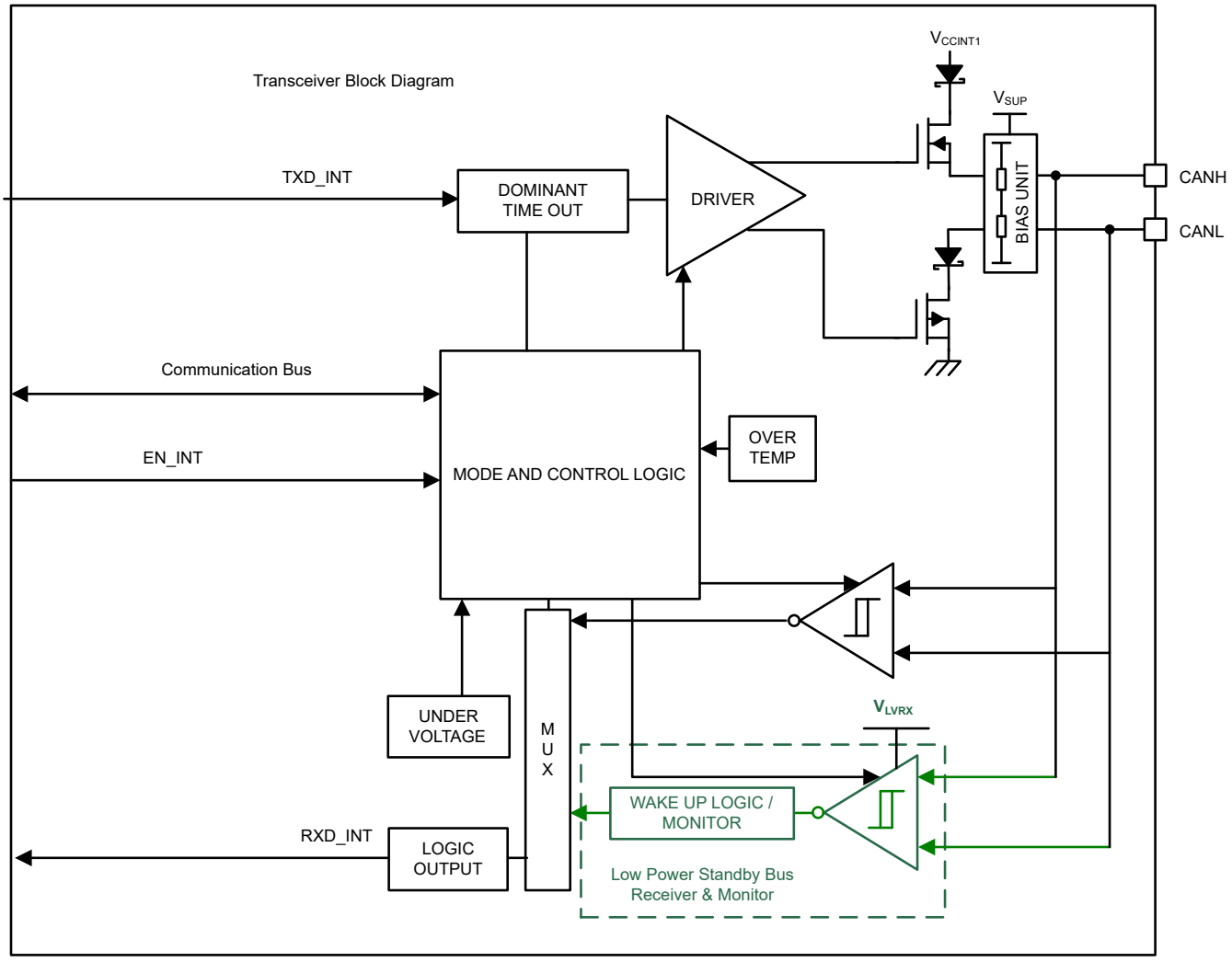


Figure 7-2. CAN Transceiver Block Diagram

ADVANCE INFORMATION

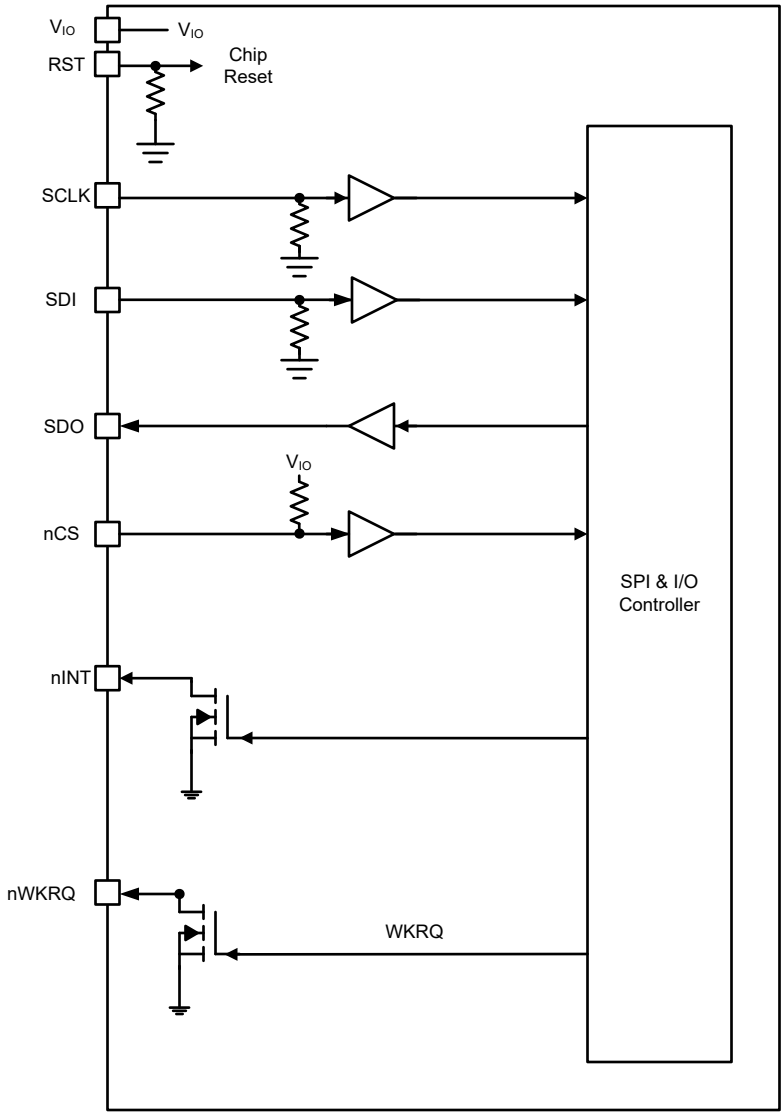


Figure 7-3. SPI and Digital IO Block Diagram

7.3 Feature Description

7.3.1 V_{DD} Pin

This pin connects to the main supply, and can be connected to the battery. The pin provides the supply to the internal regulators that support the digital core. This pin requires a 100nF capacitor at the pin. See Section 8.3 for more information. Upon power up, V_{DD} needs to rise above UV_{DD} rising threshold.

When the VDD pin voltage drops below UV_{DD}, the device is placed into a protected state, which will set all VIO-controlled IOs to high impedance. This means that SPI is inaccessible when VDD is below UV_{DD}. Once the device exits the UV_{DD} condition, a UV_{DD} interrupt will be set, to let the processor know that the device was placed into a protected mode due to a UV_{DD} condition.

7.3.2 V_{CC} Pin

This pin provides the 5V supply to the internal CAN transceiver. See Section 8.3 for more information. Upon power up, V_{CC} needs to rise above UV_{CC} rising threshold.

7.3.3 V_{IO} Pin

The V_{IO} pin provides the digital IO voltage to match the microprocessor IO voltage thus avoiding the requirements for a level shifter. V_{IO} supports IO pins SPI IO voltage levels. **The pin also provides power to the oscillator block supporting the crystal or CLKIN pins.** It supports a range of 1.71Vto 5.5V providing the widest range of controller support. This pin requires a 100nF capacitor at the pin. See Section 8.3 for more information.

7.3.4 GND

This pin is a ground pin as is the thermal pad. Both need to connect to a ground plane to support heat dissipation.

7.3.5 RST Pin

The RST pin is a device reset pin. It has a weak internal pull down resistor for normal operation. If communication has stopped with the TCAN4572-Q1, the RST pin can be pulsed high and then back low for greater than t_{PULSE_WIDTH} to perform a power on reset to the device. This resets the device to the default settings and puts the device into standby mode. If the device was in normal or standby mode, the INH and nWKRQ pins remain active (on) and do not toggle; see Figure 7-4. If the device is in sleep mode and reset is toggled, the device enters standby mode and at that time nWKRQ will assert (go low); see Figure 7-5.

After a RST has taken place, a wait time of ≥ 700µs must be used before reading or writing to the TCAN4572-Q1.

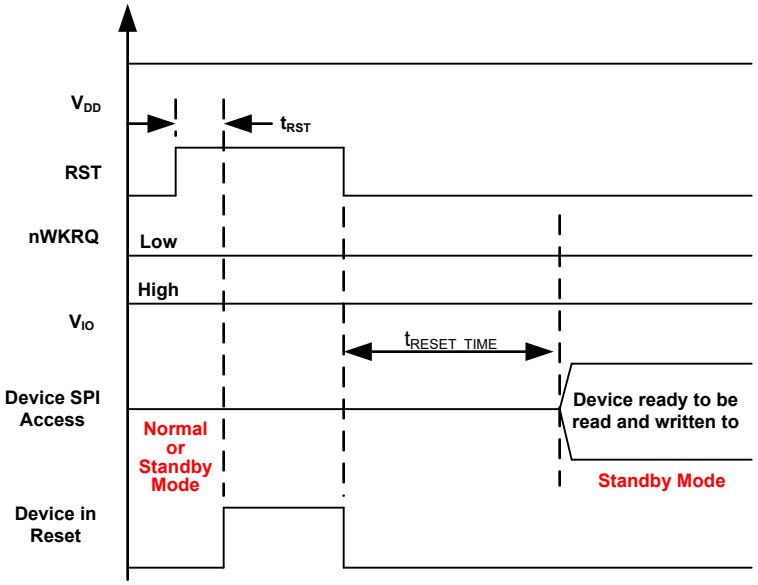


Figure 7-4. Timing for RST Pin in Normal and Standby Modes

ADVANCE INFORMATION

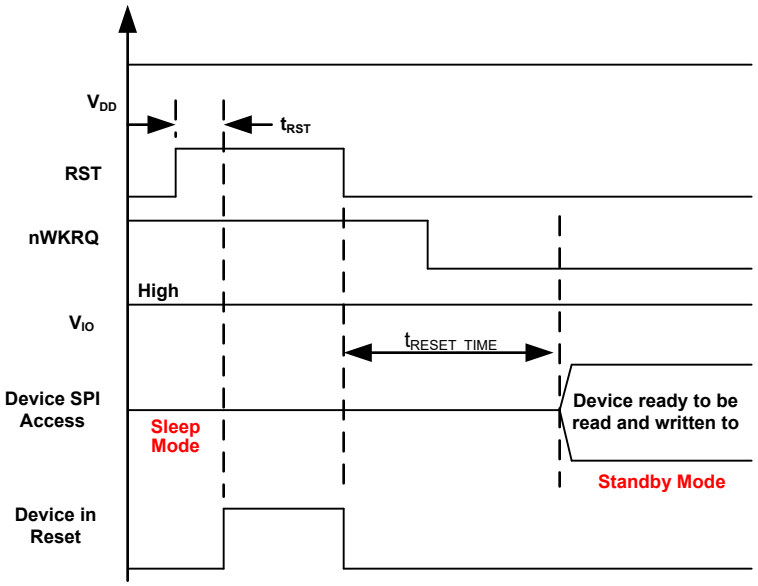


Figure 7-5. Timing for RST Pin in Sleep Mode

7.3.6 SPI CRC Feature

The TCAN4572-Q1 supports 16-bit SPI CRC support. This feature prevents writes with invalid CRCs from occurring by blocking a write with an invalid CRC, and making sure the communication between the CPU and device is correct. For more information, see Section 7.5.1.6.

7.3.7 OSC1, OSC2 Pins and Automatic Clock Detection

These pins are used for a crystal oscillator. The OSC1 pin can also be used as a single-ended clock input from the microprocessor or some other clock source. See Section 8.1 section for further information on the functions of these pins. Note that the crystal drive circuit is powered from the VIO supply.

To use the internal oscillator automatically at power up, both OSC1 and OSC2 must be shorted to ground. When both pins are shorted to ground, the internal 20MHz oscillator is used.

The OSC1 and OSC2 pins have multiple functions depending on how the device needs to be clocked. If using an external crystal oscillator, OSC1 and OSC2 connects to the crystal. If using a single ended input, then OSC2 is grounded and OSC1 receives the single ended clock input from an external source.

The detection logic for the clock block is that upon power up, the OSC2 pin is checked to see if it is connected to ground or to a crystal oscillator. This detection happens quickly and tells the device which drive mode to use. Once this initial detection is done, the clock mode does not change until a power on reset event to reduce the chance of noise switching clock modes.If the internal oscillator is used, once OSC2 is detected as being grounded, the internal oscillator is always used at the start. The internal clock is used until the OSC1 pin begins to toggle from an external source. Once OSC1 is seen as toggling, the device switches to that external single ended input, and stays 'locked' to the clock until a power reset and the detection process begins again. A SPI transaction in standby mode also 'locks' the clock to the internal oscillator if an external clock input has not been seen by the time a valid SPI transaction occurs. Once the SPI frame finishes the SPI header (to determine if it is valid), the device locks to the internal clock if no external clock has been seen yet.

Note

For early revision of silicon, please use the device with an external crystal to ensure functionality of the device. To determine if you have early silicon, please read register DEVICE_REV at address 0x8 and if REV_MINOR (bit 7-0) reads 0x0 then please migrate to the latest silicon.

7.3.8 Manual Clock Selection

The clock can be manually selected between external and internal clock "on the fly" as a way to reduce power consumption if the application calls for it. There are some notes about this functionality. Please see Section 7.3.7 about how the automatic clock detection scheme functions, as resets to the device triggers a partial or full clock detection action as outlined below. Note that only a VDD toggle that goes below the POR threshold re-triggers a crystal detection.

Note

When switching between clocks manually, the processor must wait t_{CLOCK_SWITCH} time before any further SPI writes to give the device sufficient time to switch between clocks. If switching to an external crystal, the time needed to wait is dependent upon the crystal start up time. This time varies per crystal used and needs to be evaluated for each application.

Table 7-1. Clock Behavior when Reset After Manual Selection

Clock Detected at Power Up	After Reset (Forced to Internal)	After Reset (Forced to External)
Crystal	Crystal	Crystal
Single Ended Clock Input	Redetection of single ended input or internal clock	Redetection of single ended input or internal clock
Internal Clock	Redetection of single ended input or internal clock	Redetection of single ended input or internal clock

When switching between clocks, there is an important note that affects the case where the power-up detected clock is an external singled ended clock input. If the clock is forced to internal clock and then clock force is cleared, the clock source remains on internal clock. If the user wants to go back to external single ended clock, then the user needs to select it and force it, or perform a reset event which re-detects the clock source. The same is true if switching from internal clock source to external clock single-ended input

Table 7-2. High Speed Clock Source Selection

Power-Up Detected Clock	CLK_SEL	CLK_FORCE Write Value	
		1	0 (Previous value is 1)
INT (Internal 20 MHz)	0	INT	INT
	1	ECI	ECI
XTAL (External Crystal)	0	INT	XTAL
	1	XTAL	XTAL
ECI (External Clock Single Ended Input)	0	INT	INT
	1	ECI	ECI

7.3.9 nWKRQ, nINT1 Pin

This pin by default is an open-drain wake-up request pin from a bus wake (WUP) request, and power on (PWRON). The nWKRQ pin is defaulted to a wake enable based upon a wake event (similar to an INH output). In this configuration, the output is pulled low and latched to serve as an enable for a regulator. The nWKRQ pin can be configured by setting 16'h0800[8] = 1 as an interrupt pin for wake interrupts that pulls the output low, but once the wake interrupt flag is cleared it releases the output back to a high. In this configuration, if a wake event takes place, the nWKRQ pin switches from high to low. This pin is an open drain output and requires an external pull-up resistor to V_{IO} rail. Some external regulators or power management chips can need a digital logic pin for a wake-up request, this pin can be used.

An alternative function of this pin is to be used as an active-low interrupt output for M_CAN INT1. This allows users to configure some interrupts (such as a new message interrupt for transmission complete interrupt) for an alternative pin to help with device throughput by saving some SPI reads and optimizing certain interrupt service routines (ISR). To use the pin as an INT1 output, MCAN must also be configured to enable INT1 and select which interrupts are used by configuring the MCAN ILE and ILS registers.

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This pin driver is driven off of the main digital supply, and is not dependent upon V_{IO} to pull low.

Table 7-3. nWKRQ Pin Configuration

Function	nWKRQ_CONFIG(0x0800[8])	nWKRQ_MCAN_INT1(0x0800[10])
MCAN INT1 Interrupt (Active Low)	x	1
Wake Interrupt (Active Low)	1	0
INH Functionality (Active Low)	0	0

Note

- This pin is active low and is logical OR of CANINT, and WKERR from register 16'h0820 that are not masked when configured as a wake interrupt functionality

7.3.10 nINT Interrupt Pin

The nINT is a dedicated open drain global interrupt output pin. This pin needs an external pull-up resistor to V_{IO} to function properly. All interrupt requests are reflected by this pin when pulled low.

There is a de-glitch feature to provide for a minimum time the pin is de-asserted (logic high). This value varies depending on the input clock frequency used, and is specified in the switching characteristics section. If an interrupt occurs immediately after clearing the interrupts, the feature provides a small delay before the next assertion (logic low). Making sure the processor sees a falling edge transition.

Note

This pin is an active low and is the logical OR of all faults in registers 16'h0820 and 16'h0824 that are not masked.

7.3.11 CANH and CANL Bus Pins

These are the CAN high and CAN low differential bus pins. These pins are connected to the CAN transceiver and the low voltage WUP CAN receiver. The functionality of these is explained throughout the document. See Section 8.1.3.2 for CAN bus biasing.

7.4 Device Functional Modes

The TCAN4572-Q1 has several operating modes: normal, standby, sleep and a protected mode. The first three mode selections are made by the SPI register. The protected mode is a modified standby mode used to protect the device or bus. The TCAN4572-Q1 automatically goes from sleep to standby mode when receiving a wake up event. See Table 7-4 for the various modes and what parts of the device are active during each mode.

The TCAN4572-Q1 state diagram figure shows the biasing of the CAN bus in each of the modes of operation.

Table 7-4. Mode Overview

Mode	RST Pin	nINT	nWKRQ	Low Power CAN RX	SPI	CAN TX/ RX	Memory & Configuration
Normal	L	On	On	Off	On	On	Saved
Standby	L	On	On	On	On	Off	Saved
TSD Protected	L	On	On	On	On	Off	Saved
Sleep	L	Off	Off	On	On(1)	Off	Partial Saved

(1) Reduced subset of registers is accessible while in sleep mode. Requires V_{IO} to be powered up.

Table 7-5. Clock States

Clock	Sleep Mode	Standby Mode	Normal Mode	TSD Protected
External HS Oscillator	Inactive	Active	Active	Inactive
Internal HS Oscillator	Inactive(1)	Inactive(1)	Inactive(1)	Inactive

Table 7-5. Clock States (continued)

Clock	Sleep Mode	Standby Mode	Normal Mode	TSD Protected
Internal LS Oscillator	Inactive(2)	Active	Active	Active

(1) Active if CAN bus bias is active and selective wake is enabled
(2) Active if CAN bus bias is active

Note

- SPI is active as long as V_{IO} is above U_{VIO}, since the buffers are referenced to V_{IO}

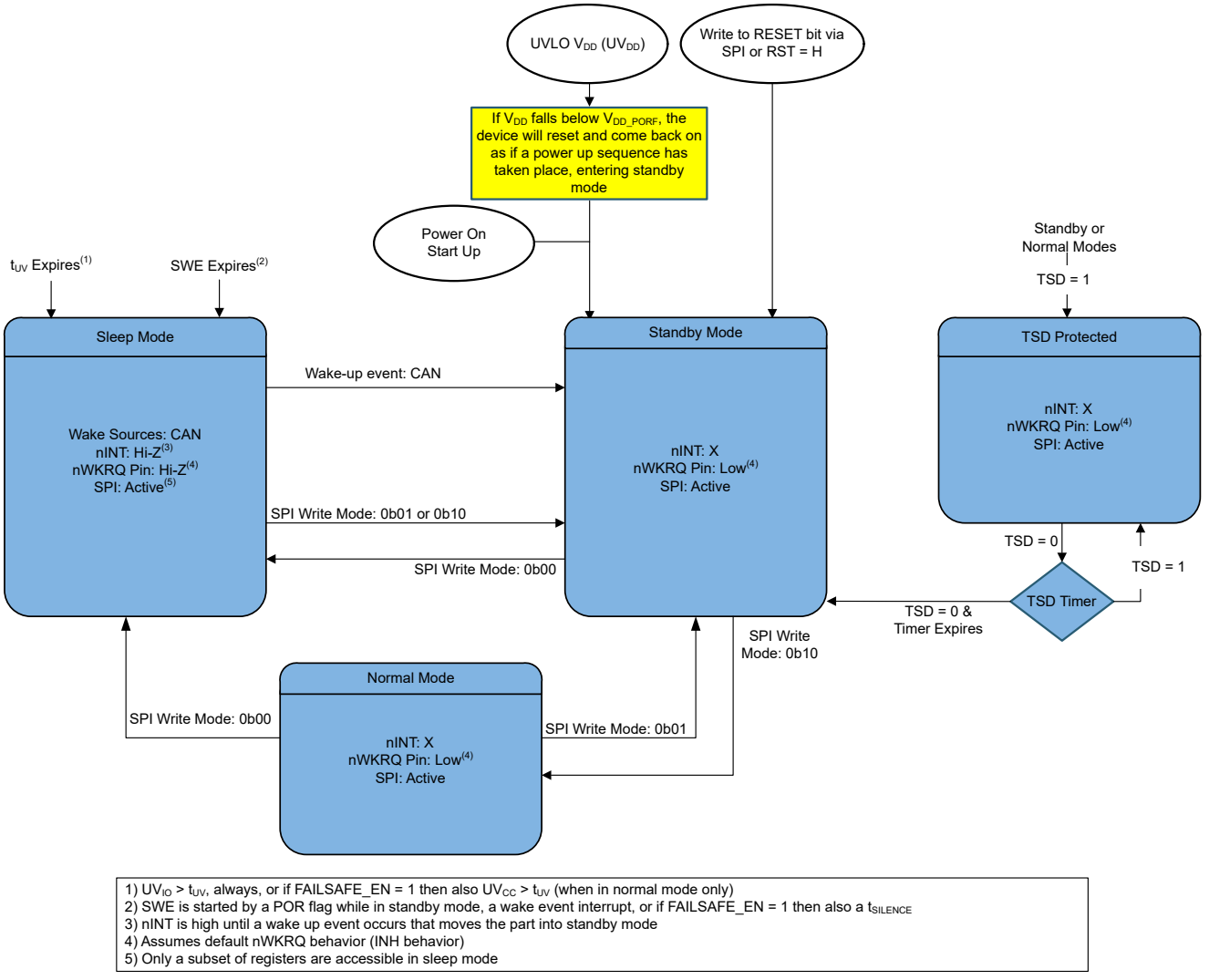

Figure 7-6. Device State Diagram

7.4.1 Normal Mode

This is the normal operating mode of the device. The CAN driver and receiver are enabled. The driver translates a digital input on the internal TXD_INT signal from the CAN FD controller to a differential output on CANH and CANL. The receiver translates the differential signal from CANH and CANL to a digital output on the internal RXD_INT signal to the CAN FD controller. Normal mode is enabled or disabled via the SPI interface.

If the device is in normal mode, the PWRON flag does not cause the SWE to run. However, other faults can make the SWE timer run (for example, if $t_{SILENCE}$ is set, and FAILSAFE_EN = 1, then the SWE timer runs).

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7.4.2 Standby Mode

In standby mode, the bus transmitter does not send data nor does the normal mode receiver accept data. There are several blocks that are active in this mode. The low power CAN receiver is active, monitoring for a CAN wake-up pattern (WUP). The SPI interface is active so that the microprocessor can read and write registers in the memory for status and configuration. The nWKRQ pin is low in this mode in the default configuration and can also be used as a digital enable pin to an external regulator or power management integrated circuit (PMIC). All other blocks are put into the lowest power state possible. This is the only mode that the TCAN4572-Q1 automatically switches to without a SPI transaction. The device goes from sleep mode to standby mode automatically upon a bus WUP event. Upon entry to Standby Mode, only one wake interrupt is given (CANINT). New wake interrupts are not given in standby mode unless the device changes to normal or sleep mode and then back to standby. This prevents bus traffic from spamming the processor with interrupts while in standby, and it gives the processor the first wake interrupt that was issued.

A power on reset or wake event from sleep mode causes the TCAN4572-Q1 to enter standby mode. This starts a four minute timer, $t_{INACTIVE}$ (also referred to as the sleep wake error SWE timer), that requires the processor to either clear the wake event or power on reset flags, or configure the device to normal mode prior to expiration of the timer. If the timer expires, the device is placed into sleep mode. This feature makes sure the node is in the lowest power mode if the processor does not come up properly. This automatic mode change also takes place when the device has been put into sleep mode and receives a wake event (from the bus). To disable this feature for sleep events, register 16'h0800[1] (SWE_DIS) must be set to one. This does not disable the feature when powering up or when a power on reset takes place.

The standby mode sets the CCCR.INIT bit to 1 making sure no communication occurs while in standby mode or during configuration. This bit is automatically cleared while transitioning from standby to normal mode.

7.4.3 Sleep Mode

Sleep mode is similar to the standby mode except the SPI interface can be disabled if V_{IO} is pulled low. As the low power CAN receiver is powered off of V_{DD} the implementer can turn off V_{IO}. The nWKRQ pin is powered off the V_{DD} supply internal logic level regulator. This allows the TCAN4572-Q1 to provide an interrupt to the MCU when a wake event takes place without requiring V_{IO} to be up. When the device goes into sleep mode the high speed oscillators are is shut down to conserve power. Data in the registers is NOT lost unless V_{DD} falls below the POR threshold. SPI is active as long as V_{IO} is above UV_{IO}. A sleep mode status flag is provided to determine if the device entered sleep mode through normal operation or if a fault caused the mode change. Register 16'h0820[23] provides the status. If a fault causes the device to enter sleep mode, this flag is set to a one.

Note

To wake the device up via SPI, write 2'b01 or 2'b10 to the device mode field (7:6) in 0x0800 wakes the device up and places it in standby mode. Only a single word write is allowed while in sleep mode. A multi-word write is ignored.

Note

The maximum allowed SPI frequency is lower when the device is in sleep mode. See device switching characteristics section for more information.

Note

Difference between sleep and standby mode

- Sleep mode reduces whole node power by deasserting nWKRQ, which can be connected to an external VREG to shut off external supplies to further save power. In addition, the device oscillators are disabled if there is no bus activity.
- Standby mode reduces TCAN4572-Q1 power by disabling the CAN transceiver. The device oscillators are still enabled, and device configuration can occur in standby mode. Sleep mode uses less current than standby mode.

7.4.3.1 Sleep Mode: Register Data and Access

In sleep mode, the state of all device registers is retained. Only during a POR event (or if V_{DD} drops below the POR threshold) are the registers reset.

While in sleep mode, only a subset of registers are still accessible. The list of accessible registers and their access is listed below.

Note

While in sleep mode, the maximum SPI frequency is limited. See device switching characteristics for more information.

Table 7-6. Sleep Accessible Registers

Register	Access	Description
0x0800	R/W	Only bits 0x0800[7:6] are accessible and all other bits are ignored while writing. Writing a normal or standby mode request to bits [7:6] will place the part into standby mode.
0x0820	R	Reading device interrupts
0x0824	R	Reading MCAN interrupts

Note

Only the summary interrupt registers are available in sleep mode (0x0820 to 0x0824), not the source register that they come from (such as 0x1050)

7.4.3.2 Bus Wake via RXD_INT Request (BWRR) in Sleep Mode

As the TCAN4572-Q1 supports low power sleep mode and uses a wake-up from the CAN bus mechanism called bus wake via RXD_INT Request (BWRR). Once this pattern is received, the TCAN4572-Q1 automatically switches to standby mode and inserts an interrupt onto the nINT and nWKRQ pins to indicate to a host microprocessor that the bus is active, and it must wake-up and service the TCAN4572-Q1. The low power receiver and bus monitor are enabled in sleep mode to allow for RXD_INT Wake Requests via the CAN bus. A wake-up request is output to the internal RXD_INT (driven low) as shown in Figure 7-8. The wake logic monitors RXD_INT for transitions (high to low) and reactivate the device to standby mode based on the RXD_INT Wake Request. The CAN bus terminals are weakly pulled to GND during this mode.

These devices use the wake-up pattern (WUP) from ISO 11898-2:2016 to qualify bus traffic into a request to wake the host microprocessor. The bus wake request is signaled to the integrated CAN FD controller by a falling edge and low corresponding to a “filtered” bus dominant on the RXD_INT terminal (BWRR).

The wake-up pattern (WUP) consists of :

- A filtered dominant bus of at least t_{WK_FILTER} followed by
- A filtered recessive bus time of at least t_{WK_FILTER} followed by
- A second filtered dominant bus time of at least t_{WK_FILTER}

Once the WUP is detected, the device starts issuing wake-up requests (BWRR) on the RXD_INT signal every time a filtered dominant time is received from the bus. The first filtered dominant initiates the WUP and the bus monitor is now waiting on a filtered recessive, other bus traffic does not reset the bus monitor. Once a filtered recessive is received, the bus monitor is now waiting on a filtered dominant and again, other bus traffic does not reset the bus monitor. Immediately upon receiving of the second filtered dominant the bus monitor recognizes the WUP and transition to BWRR output. Immediately upon verification receiving a WUP the device transitions the bus monitor into BWRR mode, and indicates all filtered dominant bus times on the RXD_INT internal signal by driving it low for the dominant bus time that is in excess of t_{WK_FILTER}, thus the RXD_INT output during BWRR matches the classical 8 pin CAN devices that used the single filtered dominant on the bus as the wake-up request mechanism from ISO 11898-2:2016.

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For a dominant or recessive to be considered “filtered”, the bus must be in that state for more than t_{WK_FILTER} time. Due to variability in the t_{WK_FILTER} the following scenarios are applicable.

- Bus state times less than $t_{WK\_FILTER(MIN)}$ are never detected as part of a WUP, and thus no BWRR is generated.
- Bus state times between $t_{WK\_FILTER(MIN)}$ and $t_{WK\_FILTER(MAX)}$ can be detected as part of a WUP and a BWRR can be generated.
- Bus state times more than $t_{WK\_FILTER(MAX)}$ is always detected as part of a WUP, and thus, a BWRR is always be generated.

See Figure 7-7 for the timing diagram of the WUP.

The pattern and t_{WK_FILTER} time used for the WUP and BWRR prevents noise and bus stuck dominant faults from causing false wake requests while allowing any CAN or CAN FD message to initiate a BWRR. If the device is switched to normal mode or an under-voltage event occurs on V_{CC} the BWRR is lost. The WUP pattern must take place within the $t_{WK\_TIMEOUT}$ time otherwise the device is in a state waiting for the next recessive and then a valid WUP pattern.

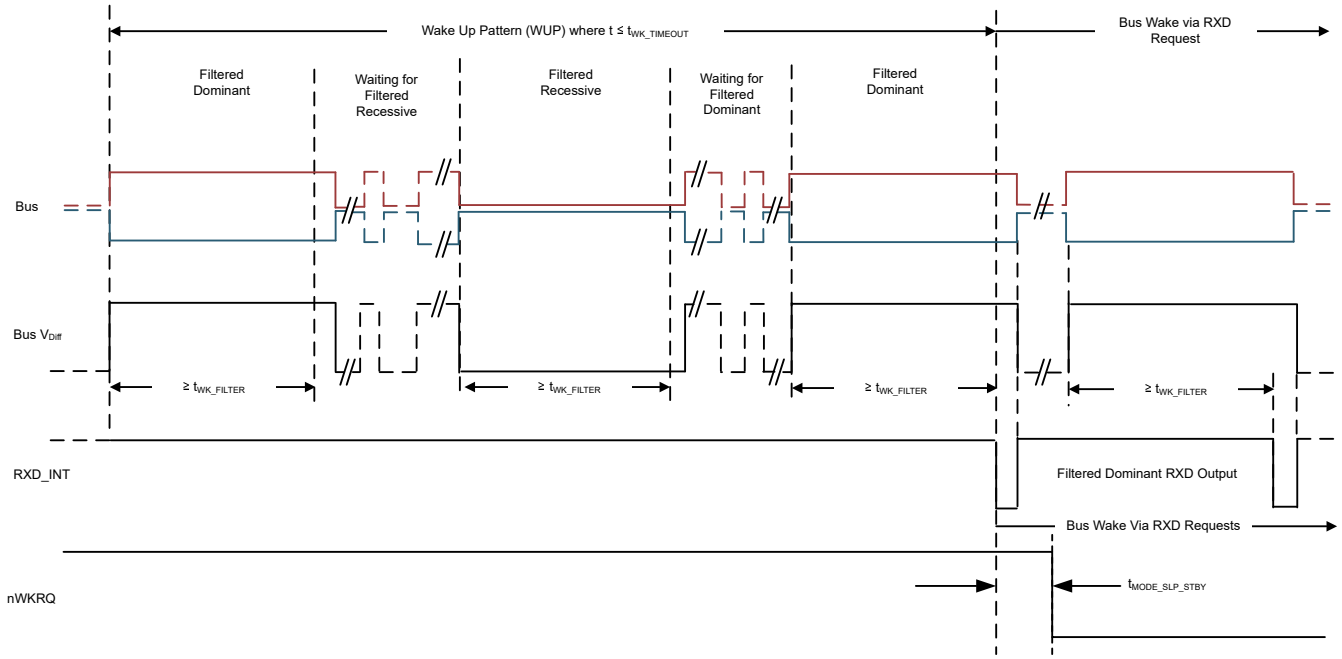

Figure 7-7. Wake-up Pattern (WUP) and Bus Wake via RXD_INT Request (BWRR)

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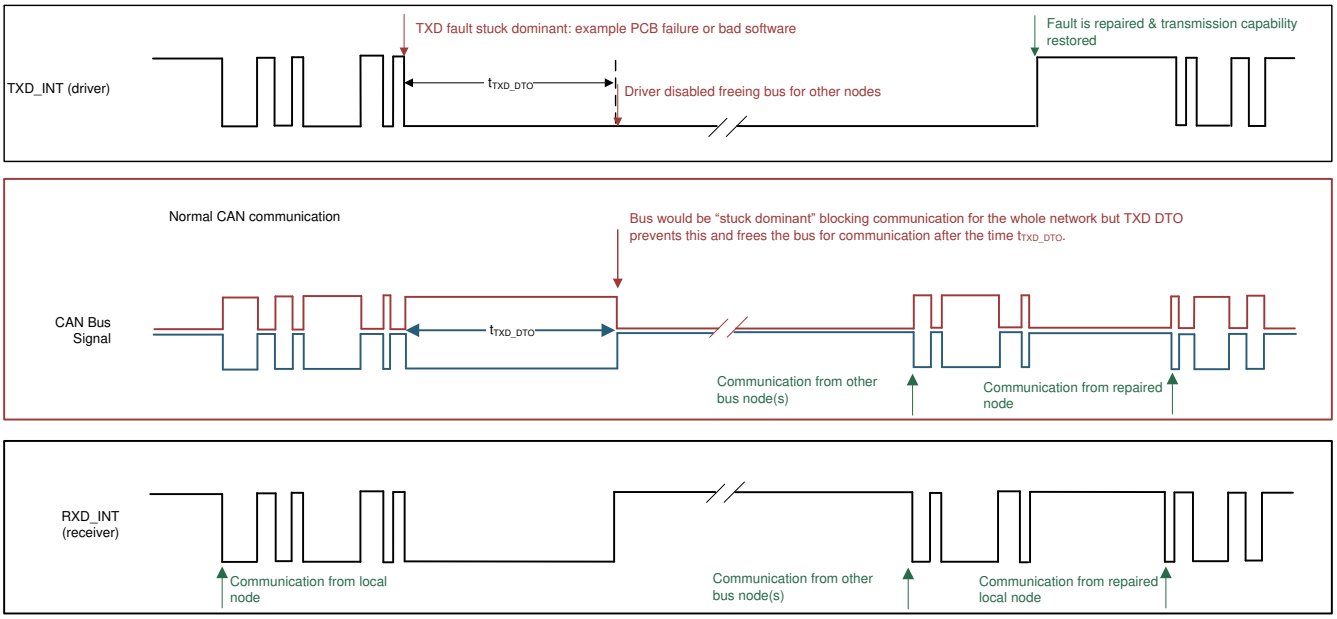

Figure 7-8. Example Timing Diagram with TXD_INT DTO

The device turns on the low speed clock when the first dominant is seen from an idle bus. Once a valid WUP has been detected, the high speed clock is requested to turn on.

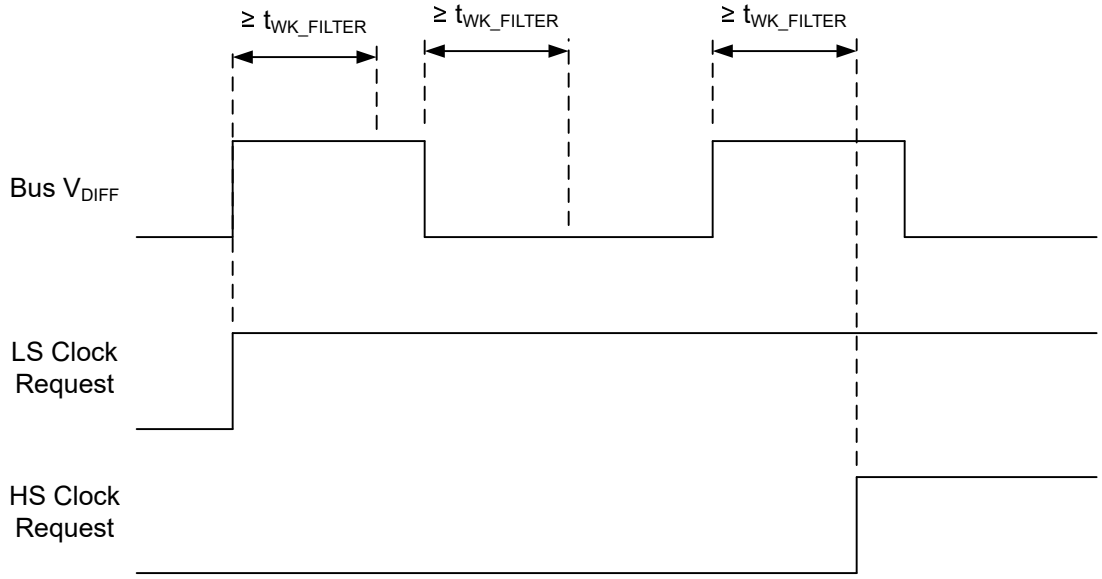

Figure 7-9. CAN WUP Clock Requests

7.4.4 Test Modes

The TCAN4572-Q1 includes a test mode that has three configurations. One is enabled by the SPI interface using the configuration register by setting register bit 16'h0800[21] = 1. In this mode the transceiver TXD_INT_PHY is mapped to the SDI pin and RXD_INT_PHY is mapped to the SDO pin. EN_INT pin is mapped to the SCLK pin, see Figure 7-10. This mode is entered immediately after nCS is deasserted following the write to enable the transceiver test mode in 16'h0800. SPI communication is NOT possible while in this test mode, because the SPI pins are muxed to the transceiver. The test mode remains enabled as long as nCS remains high. Once nCS goes low (or a POR event occurs), the test mode is immediately disabled and SPI communication resumes normally.

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There are two M_CAN core specific test modes entered using SPI but written to the M_CAN core registers directly, see Figure 7-11 and Figure 7-12.

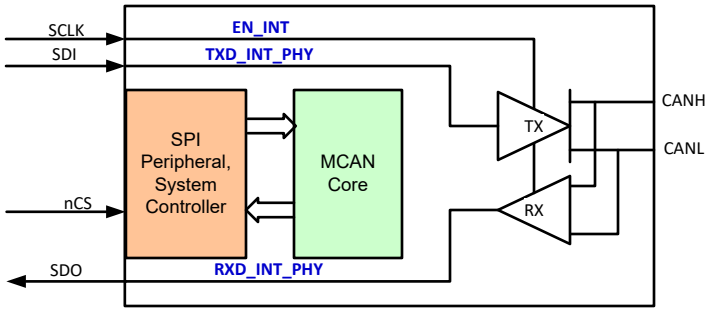

Figure 7-10. Transceiver Test Mode

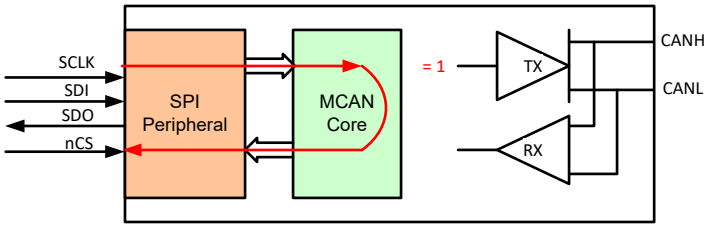

Figure 7-11. M_CAN Internal Loop Back Test Mode

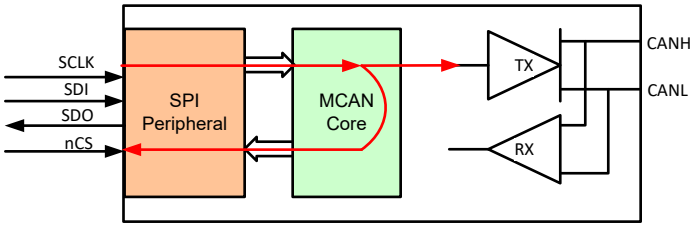

Figure 7-12. M_CAN External Loop Back Test Mode

Table 7-7. CAN Test Mode Register Configurations

Test Mode	TEST_MODE_EN (0x0800[21])	CCCR.TEST(0x1018[7])	CCCR.MON(0x1018[5])	TEST.LBCK(0x1010[4])
Transceiver Test Mode	1	0	0	0
M_CAN Internal Loop Back	0	1	1	1
M_CAN External Loop Back	0	1	0	1

7.4.5 Failsafe Feature

The failsafe feature refers to various methods that the TCAN4572-Q1 can reduce node power consumption in the event of a system issue. Some of these features can be enabled or disabled via the FAILSAFE_EN bit in 0x0800 (Mode and Pin Configuration Register) and others rely on the Sleep Wake Error (SWE) timer, which can be disabled via the SWE_DIS bit in 0x0800 (Mode and Pin Configuration Register). The SWE_DIS bit is only used for disabling the SWE timer for wake timers. The table below shows the required values of the FAILSAFE_EN and SWE_DIS to enable specific additional failsafe features. The failsafe feature and SWE timer are used to put the device into a low-power state when a failure occurs for a specified amount of time.

Table 7-8. Failsafe Features

Feature	Description	Required FAILSAFE_EN Value	Required SWE_DIS Value
PWRON Inactivity	After a POR, the SWE timer starts once the state machine moves to standby mode, and the MCU has about 4 minutes to clear the PWRON flag, or switch to normal mode to stop the timer. If the timer expires, the device enters sleep mode. This feature CANNOT be disabled.	N/A	N/A
Wake Inactivity	When the TCAN4572-Q1 receives a wake event that causes the device to wake up into standby mode, the SWE ($t_{INACTIVE}$) timer starts. If the wake interrupts (CANINT) are not cleared or device is not put into normal mode before $t_{INACTIVE}$ expires, the device goes back to sleep.	N/A	0
Normal Mode Bus Silence	While in normal mode, if the bus goes silent long enough for the $t_{SILENCE}$ timer to expire, a CANSLNT interrupt is set. This starts a SWE timer that expires after $t_{INACTIVE}$. If the silent bus interrupt is not cleared before the SWE timer expires, the device goes to sleep. If the device is in standby mode, the SWE timer does not place the device into sleep mode when it expires.	1	N/A
VCC Under Voltage Event	While in normal mode, if a UV event occurs that sets a UVCC interrupt (which requires a UV event that lasts longer than t_{UVCC}), the t_{UV} timer will start. If VCC has not risen above the UVCC threshold before the t_{UV} timer expires, the device will transition to sleep mode. While in standby mode, the UVCC flag cannot be set. For more information about the undervoltage lockout features, see Section 7.4.6.6.	1	N/A
UVIO Under Voltage Event	While in normal or standby mode, if a UV event occurs that sets a UVIO interrupt, the t_{UV} timer starts. If VIO has not risen above the UVIO threshold before the t_{UV} timer expires, the device transitions to sleep mode. This feature cannot be disabled because VIO is used for the SPI interface. For more information about the undervoltage lockout features, see Section 7.4.6.6.	N/A	N/A

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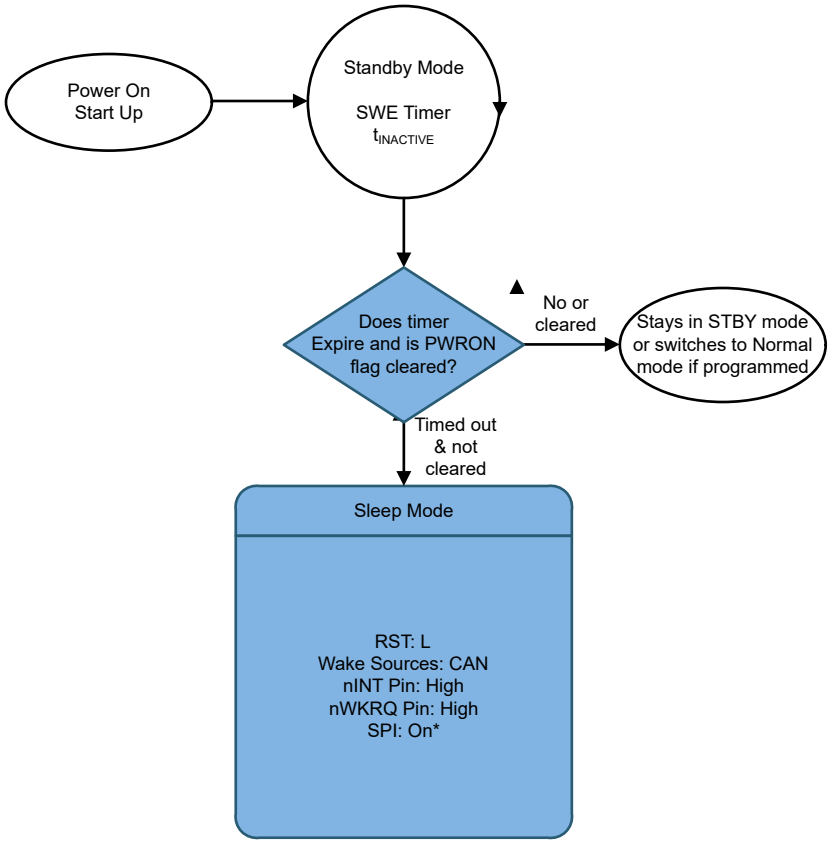
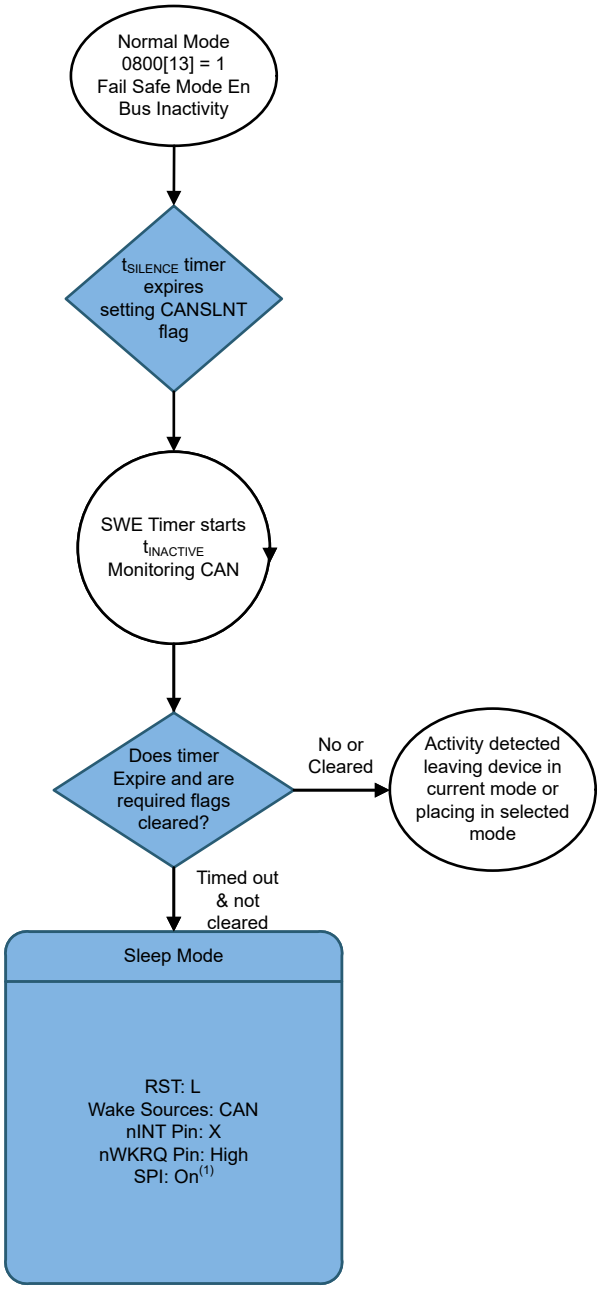


*Only register 0x0800 (Device mode and pin control) is accessible in sleep mode

Figure 7-13. Power On Failsafe Feature



1) Only a subset of registers are accessible in sleep mode, see sleep mode section for more information.

Figure 7-14. Normal and Standby Failsafe Feature

7.4.6 Protection Features

The TCAN4572-Q1 has several protection features that are described as follows.

7.4.6.1 Driver and Receiver Function

The TXD_INT and RXD_INT are internal signal paths that behave like the TXD and RXD pins for a physical layer transceiver. During normal operation they are not accessible to external pins. The TCAN4572-Q1 provides a test mode that maps these signals to external pins see Section 7.4.4. The digital logic input and output levels for these devices are CMOS levels with respect to V_{IO} for compatibility with protocol controllers having 1.8V to 5V logic or I/O. Table 7-9 and Table 7-10 provides the states of the CAN driver and CAN receiver in each mode.

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Table 7-9. Driver Function Table

DEVICE MODE	TXD_INT INPUT	BUS OUTPUTS		DRIVEN BUS STATE
		CANH	CANL	
Normal	L	H	L	Dominant
	H or Open	Z	Z	Biased Recessive
Standby	X	Z	Z	Weak Pull to GND
Sleep	X	Z	Z	Weak Pull to GND

Table 7-10. Receiver Function Table Normal and Standby Modes

DEVICE MODE	CAN DIFFERENTIAL INPUTS $V_{ID} = V_{CANH} – V_{CANL}$	BUS STATE	RXD_INT TERMINAL
Normal	$V_{ID} \geq 0.9$ V	Dominant	L
	$0.5V < V_{ID} < 0.9$ V	Undefined	Undefined
	$V_{ID} \leq 0.5V$	Recessive	H
Standby/Sleep	$V_{ID} \geq 1.15V$	Dominant	See Figure 7-7
	0.4 V $< V_{ID} < 1.15V$	Undefined	
	$V_{ID} \leq 0.4$ V	Recessive	
Any	Open ($V_{ID} \approx 0$ V)	Open	H

7.4.6.2 Floating Terminals

There are internal pull ups and pull downs on critical terminals to place the device into known states if the terminal floats. See Table 7-11 for details on terminal bias conditions.

Table 7-11. Terminal Bias

TERMINAL	PULL UP or PULL DOWN	COMMENT
SCLK	Pull down	Weakly biases input to ground
SDI	Pull down	Weakly biases input to ground
nCS	Pull up	Weakly biases input to V_{IO} so the device is not selected
nWKRQ	None	Since this pin is an open drain buffer, an external pull up is needed.
RST	Pull down	Weakly biases RST terminal towards normal operation mode

Note

The internal bias must not be relied upon as only termination, especially in noisy environments but must be considered a failsafe protection. Special care needs to be taken when the device is used with MCUs using open drain outputs.

7.4.6.3 CAN TXD_INT Dominant Timeout (DTO)

The TCAN4572-Q1 supports dominant state timeout. This is an internal function based upon the TXD_INT path. The TXD_INT DTO circuit prevents the local node from blocking network communication in the event of a hardware or software failure where TXD_INT is held dominant (low) longer than the timeout period $t_{TXD\_INT\_DTO}$. The TXD_INT DTO circuit is triggered by a falling edge on TXD_INT. If no rising edge is seen before the timeout constant of the circuit, $t_{TXD\_INT\_DTO}$, the CAN driver is disabled. This frees the bus for communication between other nodes on the network. The CAN driver is re-activated when a recessive signal (high) is seen on TXD_INT terminal, thus clearing the dominant timeout. The receiver remains active and the RXD_INT terminal reflects the activity on the CAN bus and the bus terminals is biased to recessive level during a TXD_INT DTO fault.

Note

The minimum dominant TXD_INT time allowed by the TXD_INT DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD_INT) for the worst case, where five successive dominant bits are followed immediately by an error frame.

7.4.6.4 CAN Bus Short Circuit Current Limiting

This device has several protection features that limit the short circuit current when a CAN bus line is shorted. These include CAN driver current limiting. The device has TXD_INT dominant timeout which prevents permanently having the higher short circuit current of dominant state in case of a system fault. During CAN communication the bus switches between dominant and recessive states, thus the short circuit current may be viewed either as the current during each bus state or as a DC average current. For system current and power considerations in the termination resistors and common mode choke ratings the average short circuit current must be used. The percentage dominant is limited by the TXD_INT dominant timeout and CAN protocol which has forced state changes and recessive bits such as bit stuffing, control fields, and inter frame space. These provides for a minimum recessive amount of time on the bus even if the data field contains a high percentage of dominant bits.

Note

The short circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short circuit currents. The average short circuit current may be calculated using Equation 1.

$$I_{OS(AVG)} = \%Transmit \times [(\%REC\_Bits \times IOS(SS)\_REC) + (\%DOM\_Bits \times IOS(SS)\_DOM)] + [\%Receive \times IOS(SS)\_REC] \quad (1)$$

Where

- $I_{OS(AVG)}$ is the average short circuit current.
- %Transmit is the percentage the node is transmitting CAN messages.
- %Receive is the percentage the node is receiving CAN messages.
- %REC_Bits is the percentage of recessive bits in the transmitted CAN messages.
- %DOM_Bits is the percentage of dominant bits in the transmitted CAN messages.
- IOS(SS)_REC is the recessive steady state short circuit current and IOS(SS)_DOM is the dominant steady state short circuit current.

Note

The short circuit current and possible fault cases of the network must be taken into consideration when sizing the power ratings of the termination resistance, other network components, and the power supply used to generate V_{SUP}.

7.4.6.5 Thermal Shutdown

This is a device preservation event. If the junction temperature of the device exceeds the thermal shut down threshold, the device turns off the CAN transceiver thus blocking the signal to bus transmission path. A thermal shut down interrupt flag is set so that the microprocessor is informed. If this event happens, other interrupt flags may be set as an example a bus fault where the CAN bus is shorted to V_{BAT} (V_{DD}). When this happens the digital core and SPI interface are still active. Once the thermal shutdown event is cleared, a ≈ 300ms timer starts and once expired (after checking if the TSD fault is still cleared), the device exits to standby mode. While in thermal shut down protected mode a SPI write to change the device to either Normal or Standby mode is ignored while writes to change to sleep mode is accepted.

There is an additional critical thermal shut down (t_{CSD}), which turns off the digital supply if the regular thermal shut down is unable to keep the temperature from rising. This thermal shut down kills the power supply to digital,

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which means that the device will behave as if it is unpowered until it cools off. This is to provide additional protection to the device.

Note

A UV_{IO} event does not put the device to sleep while in TSD. Once the device exits TSD, if the UV_{IO} event still persists and expires the t_{UV} timer, then the device goes to sleep.

7.4.6.6 Under Voltage Lockout (UVLO) and Unpowered Device

The TCAN4572-Q1 monitors the V_{DD}, V_{IO} and V_{CC} pin for undervoltage events. These voltage rails have under voltage detection circuitry which places the device into a protected state if an under voltage fault occurs for V_{DD} and V_{IO} . This protects the bus during an under voltage event on these terminals. If V_{DD} is in under voltage, the device loses the source needed to keep the internal regulators active. This causes the device to go into a state where communication between the microprocessor and the TCAN4572-Q1 is disabled. The TCAN4572-Q1 is not able to receive information from the bus, and thus does not pass any signals from the bus, including any Bus Wake via BWRR signals to the microprocessor.

A UV_{CC} event is monitored only after UV_{CC} is exited (after power up or sleep) or when the device is requested to move to normal mode. For example, since this device supports flexible power supply orders, an interrupt for UV_{CC} is not set immediately at power up, because the device waits to see VCC come up. Once VCC is above UV_{CC}, if it crosses below UV_{CC}, an interrupt is set. Another scenario is if the processor requests a move to normal mode but VCC is still below UV_{CC}, a fault interrupt is set.

A UV_{DD} event will set an interrupt flag and move the device to standby mode, to alert the CPU, regardless of the state of the FAILSAFE_EN feature.

Note

Regardless of the state of the FAILSAFE_EN feature, a UV_{IO} event moves the device into standby mode and set an interrupt flag to alert the MCU. If a UV_{IO} event occurs long enough for t_{UV} to expire, the device goes to sleep mode.

Note

The POR threshold voltage is checked against the FLTR pin voltage, rather than VDD directly. Depending on how quickly VDD is ramping up or down, there could be a delayed effect on the FLTR pin. This provides additional robustness against supply noise since a POR event resets the entire device.

The UVLO circuit monitors both rising and falling edge of a power rail when ramping and declining.

Table 7-12. Under Voltage Lockout and IO Level Shifting Devices

V_{DD}	V_{IO}	DEVICE STATE	CAN BUS	RXD_INT	GPIOs/SPI
> UV_{DD}	> UV_{VIO}	Normal	Per TXD_INT	Mirrors Bus	Normal
< UV_{DD}	> UV_{VIO}	Protected	High Impedance	High (Recessive)	High Impedance
> UV_{DD}	< UV_{VIO}	Protected	Recessive	High Impedance	High Impedance
< UV_{DD}	< UV_{VIO}	Protected	High Impedance	High Impedance	High Impedance

Note

Once an under voltage condition and interrupt flags are cleared and the V_{DD} supply has returned to valid level, the device typically need t_{MODE_CHANGE} to transition to normal operation. The host processor must not attempt to send or receive messages until this transition time has expired.

7.4.6.6.1 UV_{CC}

A UV_{CC} interrupt can be set when the device is in normal mode and VCC falls below the UVCC threshold longer than t_{UVCC}. This will turn off the CAN transceiver, and hold MCAN in reset. The device does not leave

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normal mode. An interrupt is set and the MCAN/CAN is held in a pseudo reset state (MCAN INIT bit is set and transceiver is turned off). Note that a UVCC event in sleep mode does not do anything, since the device expects power can be removed from VCC, and uses the internal power rail to bias the CAN bus if needed, allowing for decoding of incoming CAN frames while in sleep without VCC.

7.4.6.6.2 UV_{IO}

If V_{IO} drops below UV_{IO} under the voltage detection threshold, several functions are disabled. The transceiver switches off until V_{IO} has recovered. The input clock or crystal circuits are disabled and the IO between the TCAN4572-Q1 and microprocessor is not active. When UV_{IO} triggers the t_{UV} timer starts. If the timer times out and the UV_{IO} is still there, the device enters sleep mode. The device does not automatically wake up if V_{IO} returns. Once in sleep mode, a wake event is required to place the TCAN4572-Q1 into standby mode, or a write to SPI if V_{IO} returns to place the device back into standby mode. Since registers are not cleared in sleep mode, the UV_{IO} interrupt flag is retained when V_{IO} returns above the UV_{IO} threshold. If the UV_{IO} event is still in place, the cycle repeats. If during a thermal shut down event a UV_{IO} event happens, the device automatically enters sleep mode.

The device is designed to be a "passive" or “no load” to the CAN bus if the device is unpowered. The bus terminals (CANH, CANL) have low leakage currents when the device is unpowered so it does not load the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains operational. Logic terminals also have low leakage currents when the device is unpowered, so they do not load other circuits which may remain powered.

7.4.6.6.3 Fault and M_CAN Core Behavior:

During a UV_{IO} or TSD fault the TCAN4572-Q1 automatically does the following to keep the M_CAN core in a known state. A write of 1 to CCCR.INIT is issued anytime there is a transition from Normal → Standby. Any currently pending TX or RX processing is halted. Once the device re-enters normal mode, a write of 0 to CCCR.INIT is issued, and any pending messages (TXBRP active bits) is automatically transmitted.

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7.5 Programming

The TCAN4572-Q1 uses 32 bit accesses. The TCAN4572-Q1 provides 2K bytes of device memory RAM (called MRAM) that is fully configurable for TX/RX buffer/FIFO as needed based upon the system needs. To prevent an ECC error from happening on reads to portions of memory that have not yet been written to, after a POR, the MRAM is automatically 0-filled. This process generates valid ECC values for the MRAM, and puts it into a known state.

7.5.1 SPI Communication

The SPI communication uses a standard SPI interface. Physically the digital interface pins are nCS (Chip Select Not), SDI (SPI Data In), SDO (SPI Data Out) and SCLK (SPI Clock). Each SPI transaction is a 32 bit word containing a command byte followed by two address bytes and length bytes. The data shifted out on the SDO pin for the transaction always starts with the Global Status Register (byte). This register provides the high level status information about the device status. The two data bytes which are the ‘response’ to the command byte are shifted out next. Data bytes shifted out during a write command is content of the registers prior to the new data being written and updating the registers. Data bytes shifted out during a read command are the current content of the registers and the registers is not updated.

The SPI input data on SDI is sampled on the low to high edge of the SCLK. The SPI output data on SDO is changed on the high to low edge of the SCLK.

7.5.1.1 Chip Select Not (nCS):

This input pin is used to select the device for a SPI transaction. The pin is active low, so while nCS is high the SDO pin of the device is high impedance allowing a SPI bus to be designed. When nCS is low the SDO driver is activated and communication may be started. The nCS pin is held low for a SPI transaction. A special feature on this device allows the SDO pin to immediately show the Global Fault Flag on a falling edge of nCS.

Note

To protect the state of the nCS pin in the event that the pin floats, there is an internal pull-up resistor.

7.5.1.2 SPI Clock Input (SCLK):

This input pin is used to input the clock for the SPI to synchronize the input and output serial data bit streams. The SPI Data Input is sampled on the rising edge of SCLK and the SPI Data Output is changed on the falling edge of the SCLK.

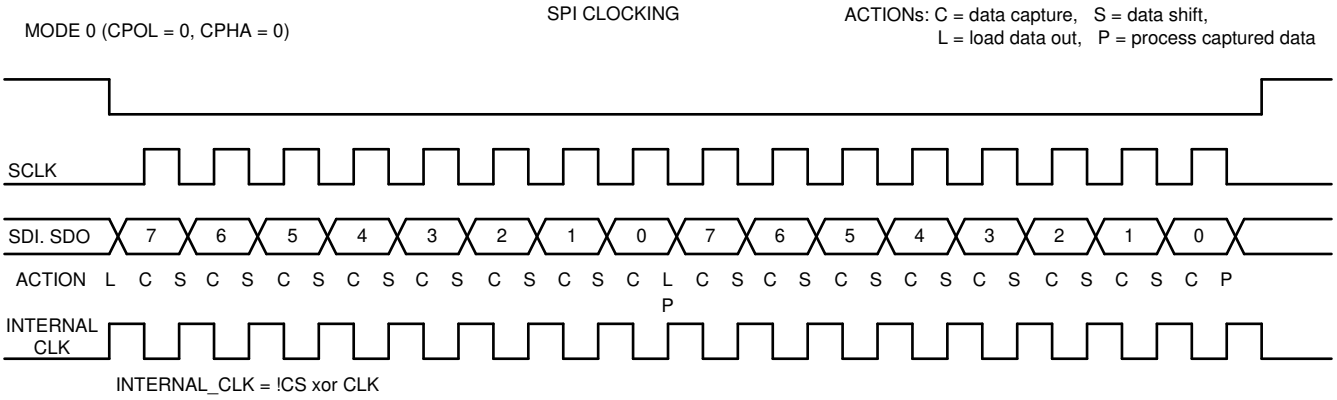

Figure 7-15. SPI Clocking

Note

To protect the state of the nCS pin in the event that the pin floats, there is an internal pull-up resistor.

7.5.1.3 SPI Data Input (SDI):

This input pin is used to shift data into the device. Once the SPI is enabled by a low on nCS the SDI samples the input shifted data on each rising edge of the SCLK. The data is shifted into a 32 bit shift register. If the command code was a write, the new data is written into the addressed register only after exactly 32 bits have been shifted in by SCLK and the nCS has a rising edge to deselect the device. If there are not exactly a multiple of 32 bits shifted in to the device, the during one SPI transaction (nCS low) the last word of the transfer is ignored, the SPIERR flag is set.

Note

Due to needing multiples of 32 bits on each SPI transaction, the device must be wired for parallel operation of the SPI as a bus with control to the device via nCS and not as a daisy chain of shift registers.

Note

To protect the state of the SDI pin in the event that the pin floats, there is an internal pull-up resistor.

7.5.1.4 SPI Data Output (SDO)

This pin is high impedance until the SPI output is enabled via nCS. Once the SPI is enabled by a low on nCS, the SDO is immediately driven high or low showing the Global Fault Flag status which is also the first bit (bit 32) to be shifted out if the SPI is clocked. Once SCLK begins, on the first low to high edge of the clock the SDO retains the Global Fault Flag which is bit 31 of the shift. On the first falling edge of SCLK, the shifting out of the data continues with each falling edge on SCLK until all 32 bits have been shifted out the shift register.

7.5.1.5 SPI Header Format and Byte Order

Each SPI frame starts with a 1-word SPI header. This header contains information that tells the device several key pieces of information about the SPI frame to be transferred. It contains:

1. The operation code (Op code), which defines whether the frame is a read or a write (as well as byte order)
2. The start address of the register that is being accessed
3. The number of words (4 bytes per word) to be transferred

If SPI CRC is enabled, then every SPI frame will end with a CRC word. See Section 7.5.1.6 for more information.

The start address must be word aligned (32-bit). Any time the registers are accessed, bits [1:0] of the address are ignored as the addresses are always word (32-bit/4-byte) aligned. As an example for accessing the M_CAN registers, for the register 0x1004, give the SPI address 1004, 1005, 1006 or 1007, and access register 1004. The registers are 32 bit and only 1004 is valid in this example.

When entering the MRAM start address, the 0x8000 prefix is not necessary. For example, if the desired start address is 0x8634, then bits SA[15:0] is 0x0634.

Table 7-13 provides programming op codes.

Table 7-13. Access Commands

NAME	OP CODE	DESCRIPTION	USAGE (IN HEADER)
WRITE_B_H (burst: one fixed length SPI write, high data byte first)	8'h61	Write one or more addresses with high data byte first	< WRITE_B_FL > <2 address bytes> <1 length bytes> <data payload to device>
READ_B_H (burst: one fixed length SPI read, high data byte first)	8'h41	Read one or more addresses with high data byte first	< READ_B_FL > <2 address bytes> <1 length bytes> <data payload from device>
WRITE_B_L (burst: one fixed length SPI write, low data byte first)	8'h60	Write one or more addresses with low data byte first	< WRITE_B_FL > <2 address bytes> <1 length bytes> <data payload to device>
READ_B_L (burst: one fixed length SPI read, high data byte first)	8'h40	Read one or more addresses with low data byte first	< READ_B_FL > <2 address bytes> <1 length bytes> <data payload from device>

Note

The length field does NOT include the header word, ONLY the bytes of data transferred after the header. If CRC is used, then the CRC word is NOT included as well.

Note

- The two low order address bits is ignored
- A length of 8'h00 indicates 256 words to be transferred

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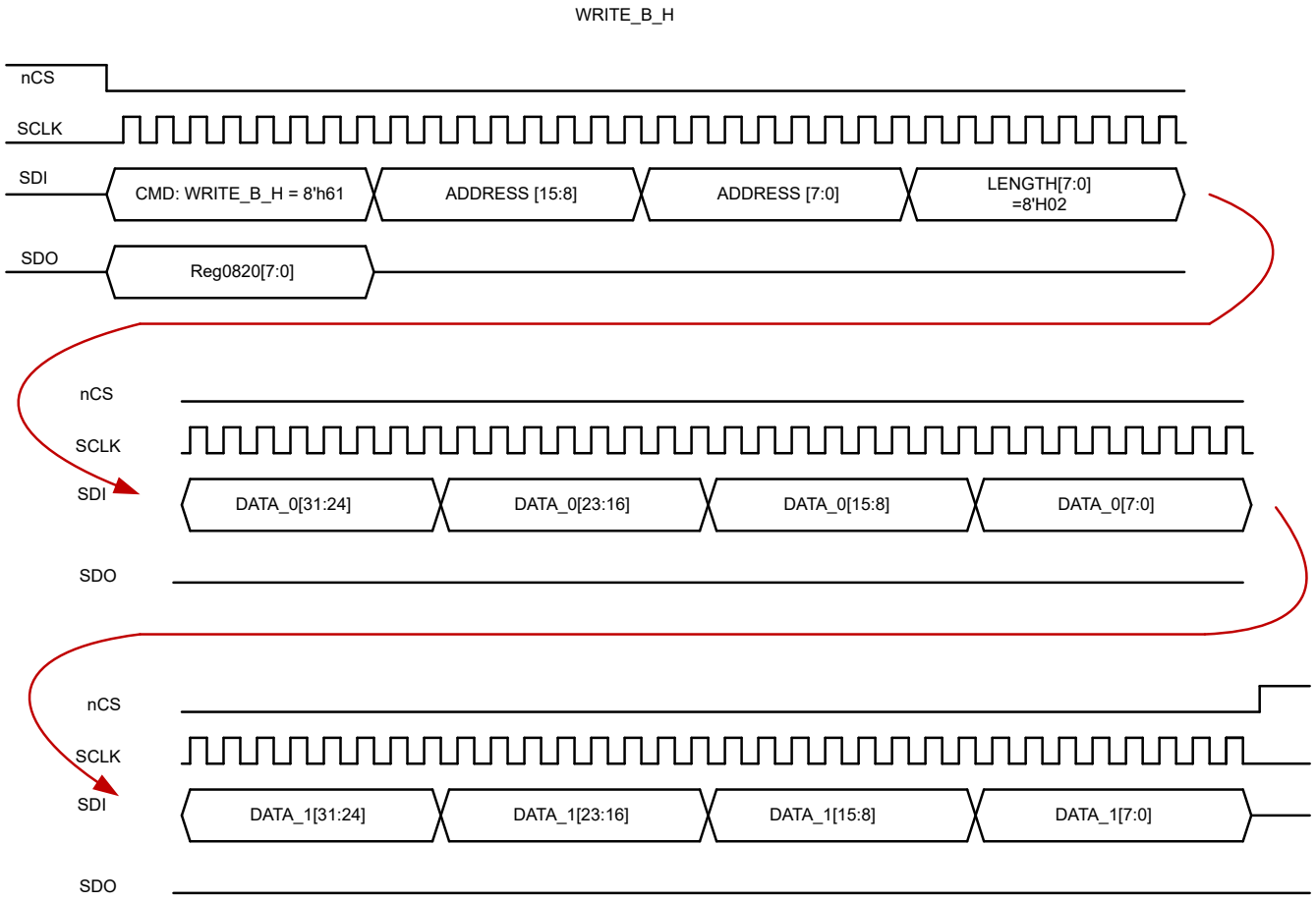

Figure 7-16. Write, High byte first (Command Op Code 8'h61)

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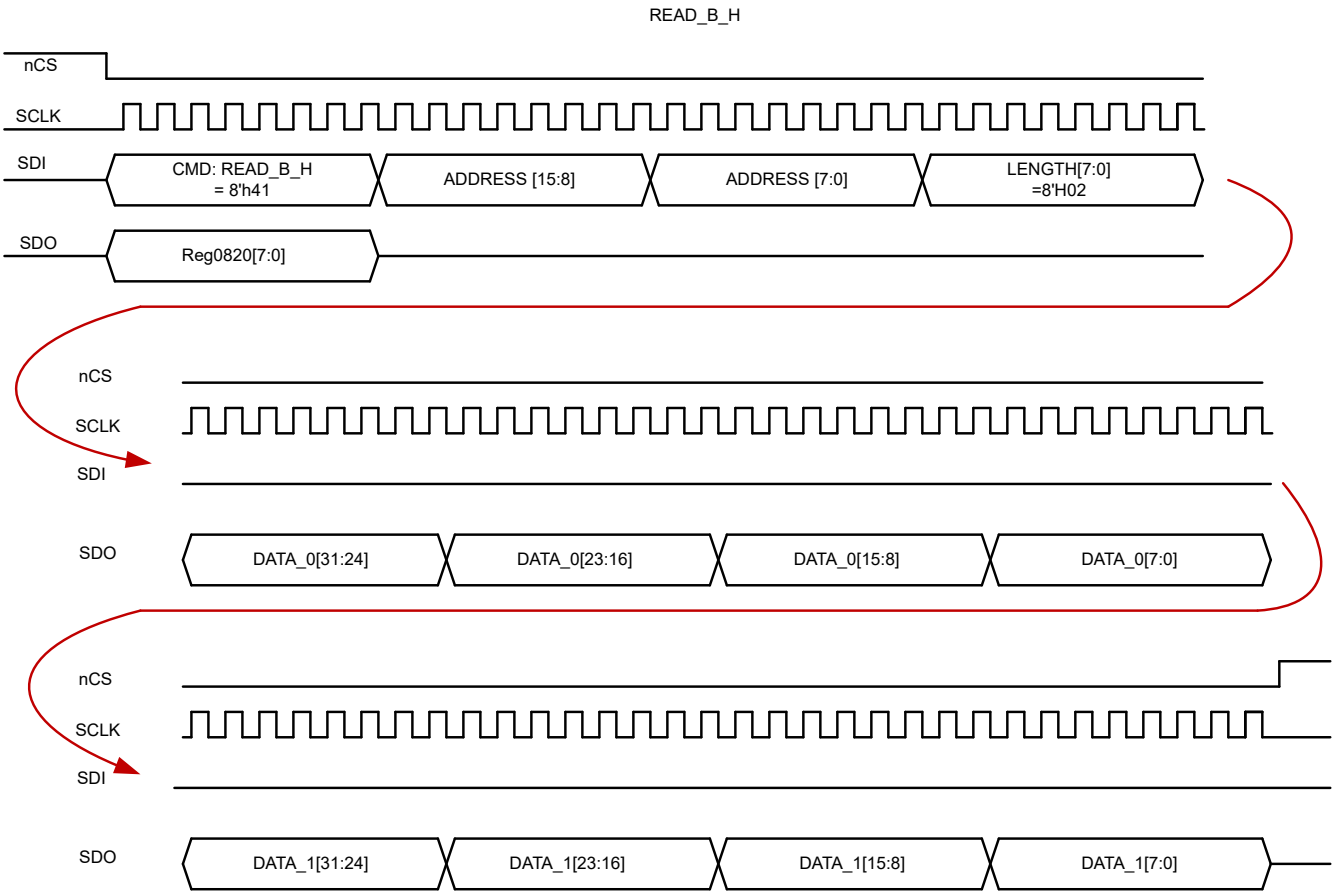

Figure 7-17. Read, High byte first (Command Op Code 8'h41)

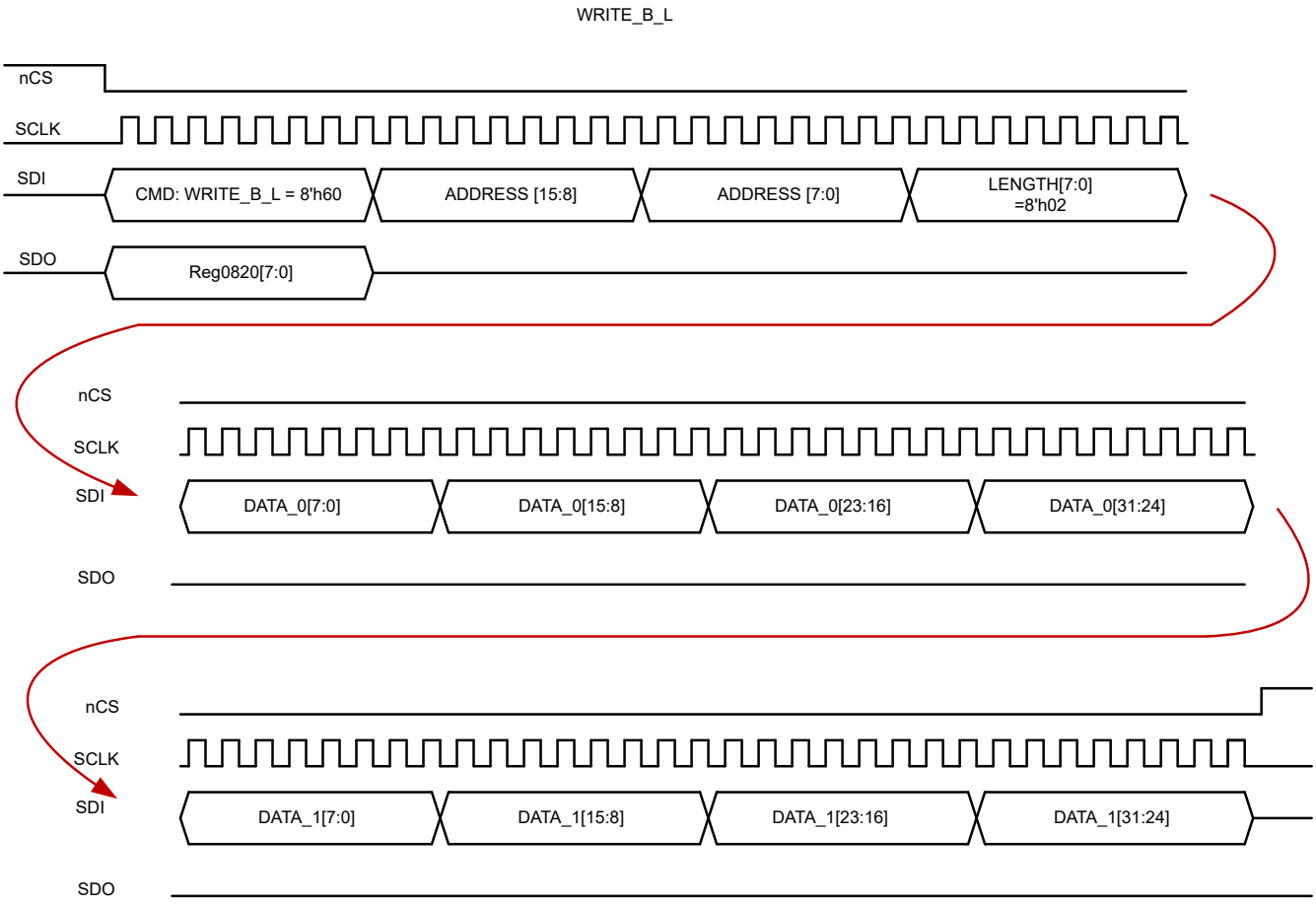

Figure 7-18. Write, Low byte first (Command Op Code 8'h60)

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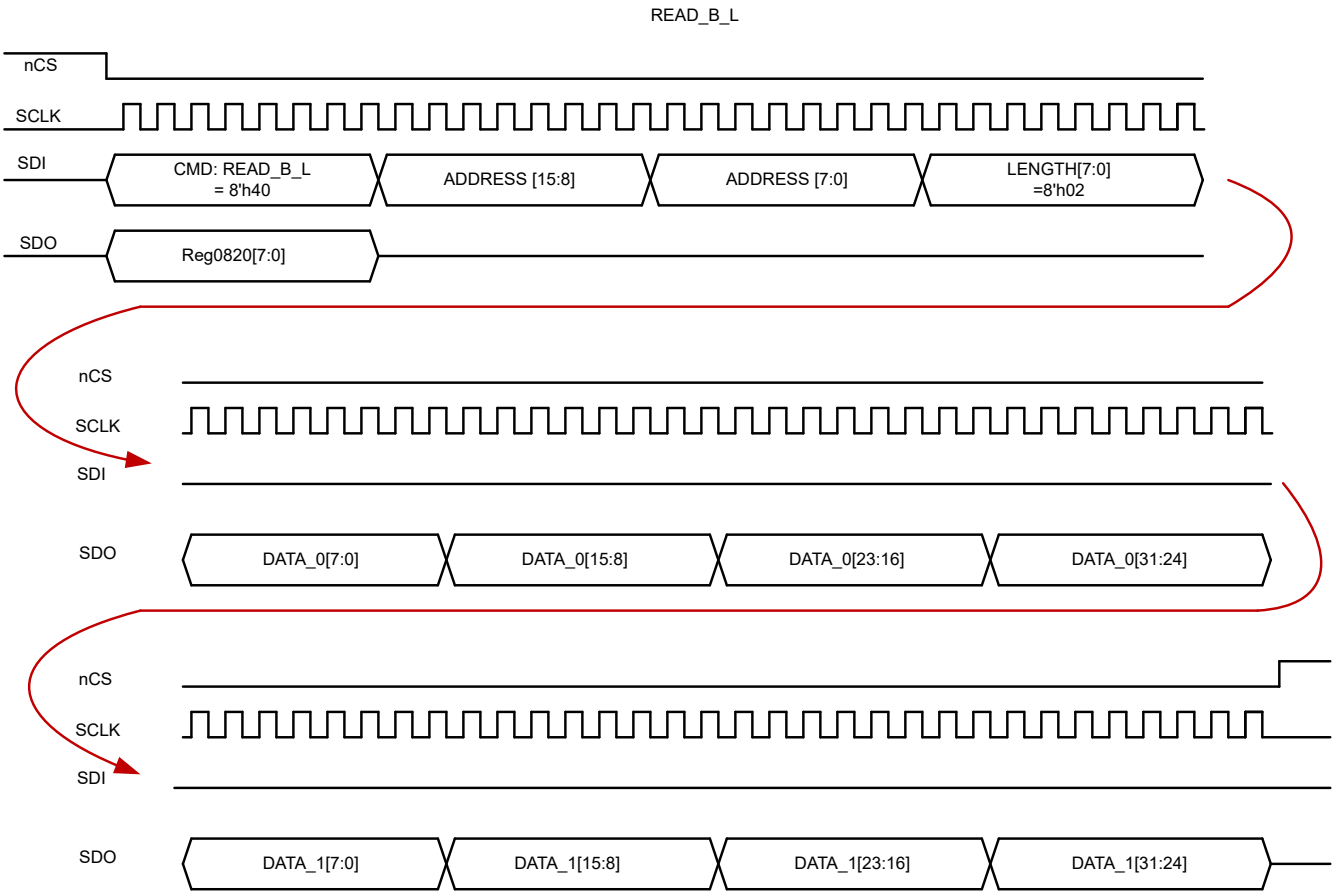

Figure 7-19. Read, Low byte first (Command Op Code 8'h40)

7.5.1.6 SPI Cyclic Redundancy Check (CRC)

The SPI interface supports the use of a SPI frame 16-bit CRC. A 16-bit CRC is used for the data to allow for a status flag to be transmitted at the end of the 32-bit word used for CRC.

By default, CRC is NOT enabled. To enable CRC, the appropriate bit must be enabled in the SPI configuration register. When it is enabled, the SPI module does a store-and-forward type of behavior, waiting until the end of the SPI transaction to verify the calculated CRC matches before writing the data to the desired register. If a CRC does not match, then the CRC_STATUS byte reflects a negative response and the data is NOT written to the register. This makes sure no data corruption occurs due to flipped bits.

The CRC configuration supports flipping (byte order flipping for CRC calculation), and programmable 32 bit seed, which is used as the starting seed for each SPI transaction.

Note

When SPI CRC is enabled, the maximum word length per SPI transaction for non-SPI domain registers (registers 0x1000 and above) is 18 words (72 bytes). Any longer transaction is needed to be split into multiple shorter messages. If a word length greater than 18 is requested with CRC enabled, the write is ignored. For reads, the 18 word limit does not apply, and the maximum of 256 words (represented as 0) is still allowed. For SPI domain registers (0x0000 to 0x0FFF), maximum size is less.

As shown in Figure 7-20, the CRC word is always the last word of a transaction, for both reads and writes. The first 16 bits of the SPI word is always the 16 bit CRC value. Placing it at the beginning of the word gives the device enough time to compute the CRC and return the status.

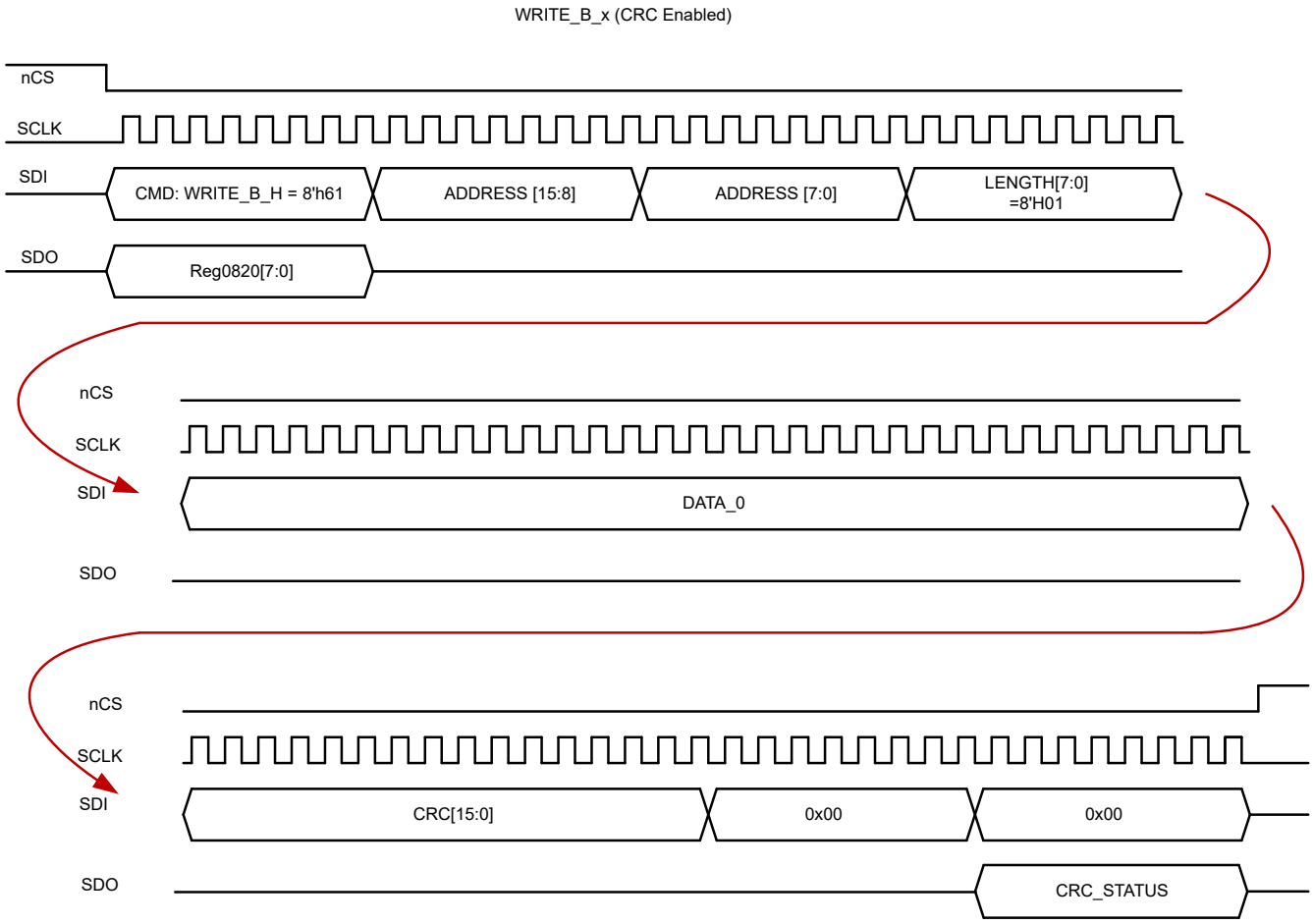

Figure 7-20. Example CRC SPI Transaction

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7.5.2 MCAN CAN FD Controller and MRAM Programming

The TCAN4572-Q1 has an integrated Bosch MCAN CAN FD controller, that is used to send and receive CAN messages. For information and examples on how to send and receive CAN frames, please refer to CAN / CAN FD section inside of the TCAN45xx Software User's Guide. This user guide provides examples on how to configure the MRAM and send/receive CAN frames.

7.5.3 MRAM Allocation

The TCAN4572-Q1 provides 2048 bytes of device memory RAM (called MRAM) that is fully configurable for TX/RX buffer/FIFO as needed based upon the system needs. To prevent an ECC error from happening on reads to portions of memory that have not yet been written to, upon a POR, the MRAM is automatically 0-filled. This process generates valid ECC values for the MRAM, and puts it into a known state.

This memory is shared by all MCAN features (Message Filters, TX FIFOs, RX FIFOs, RX Buffers, and so on).

It is important that care is taken to prevent overlap of these sections: otherwise, unexpected behavior can occur.

7.5.4 MCAN DMA Improvements

The TCAN4572-Q1 has additional features to improve throughput. This feature allows for DMA-like functionality by reading and writing to known addresses to shift CAN messages into or out of the internal TCAN4572-Q1 MRAM. The nWKRQ pin can also be re-purposed to be a dedicated "new message" interrupt output, which clears and sets based on if new messages exist in the FIFO.

The result is several SPI register reads being eliminated. As an example of the typical process to read a message out of MRAM for RX FIFO 0:

1. Read IR register, see MCAN bit is set.
2. Read MCAN IR register, see RX0N is set (new message in RX FIFO 0).
3. Read RXF0S to see how many messages are in the FIFO, and what the start address is.
4. If the base address in MRAM is not stored, read RXF0C to determine the base address
5. Do the math to determine the FIFO address. Read the contents of the FIFO from MRAM.
6. Acknowledge the FIFO message by writing to RXF0A.

An example process to read from the RX DMA is

1. nWKRQ (in new message interrupt mode) is pulled low.
2. MCU reads a full FIFO element word of data from the RX DMA address (16'h5100).
3. Check if nWKRQ is still low. If so, repeat step 2 until nWKRQ goes high.

This results in a single SPI read instead of 6+ reads being needed for every incoming message.

The addresses for each of the DMA sections are as follows:

- Registers 16'h5000 through 16'h5044 is the TX DMA
- Registers 16'h5100 through 16'h5144 is the RX0 DMA
- Registers 16'h5200 through 16'h5244 is the RX1 DMA

Note

The MRAM must still be configured as normal. The device must be set up for FIFO mode and the user must not manually access this register space in the 0x8000 register space, or unexpected results may happen.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Design Consideration

8.1.1 Crystal and Clock Input Requirements

Selecting the crystal or clock input depends upon system implementation. To support 2 and 5 Mbps CAN FD the clock in or crystal needs to have 0.5% frequency accuracy. The minimum value of 20 MHz is needed to support CAN FD with a rate of 2 Mbps. The recommended value for CLKIN or crystal is 40 MHz to meet CAN FD rates up to 5 Mbps data rates to support higher data throughout. If a crystal is used see the manufacturers documentation on proper biasing.

Crystal layout important, and it is also recommended that a power dissipation resistor is placed between the OSC1 pin and the crystal terminal. 0 Ω can be used initially, but placing the foot print gives the user the ability to adjust the power delivered to the crystal if required.

Note

The TCAN4572-Q1 was evaluated with the NX2016SA 20 MHz, and 40 MHz crystals

8.1.2 Bus Loading, Length and Number of Nodes

A typical CAN application can have a maximum bus length of 40m and maximum stub length of 0.3m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A high number of nodes require a transceiver with high input impedance such as this transceiver family.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2:2016 standard. They made system level trade off decisions for data rate, cable length, and parasitic loading of the bus. Examples of these CAN systems level specifications are ARINC825, CANopen, DeviceNet, SAE J2284, SAE J1939, and NMEA200.

A CAN system design is a series of tradeoffs. In ISO 11898-2:2016 the driver differential output is specified with a bus load that can range from 50Ω to 65Ω where the differential output must be greater than 1.5V. The TCAN4572-Q1 is specified to meet the 1.5V requirement with a across this load range and is specified to meet 1.4V differential output at 45Ω bus load. The differential input resistance of this family of transceiver is a minimum of 30kΩ. If 167 of these transceivers are in parallel on a bus, this is equivalent to an 180Ω differential load in parallel with the 60Ω from termination gives a total bus load of 45Ω. Therefore, this family theoretically supports over 167 transceivers on a single bus segment with margin to the 1.2V minimum differential input voltage requirement at each receiving node. However for CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is much lower. Bus length may also be extended beyond the original ISO 11898-2:2016 standard of 40m by careful system design and data rate tradeoffs. For example CANopen network design guidelines allow the network to be up to 1km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of its key strengths allowing for these system level network extensions and additional standards to build on the original ISO 11898-2 CAN standard. However, when using this flexibility the CAN network system designer must take the responsibility of good network design for robust network operation.

8.1.3 CAN Termination

The standard CAN bus interconnection to be a single twisted pair cable (shielded or unshielded) with 120Ω characteristic impedance (Z_O).

8.1.3.1 Termination

Resistors equal to the characteristic impedance of the line ares used to terminate both ends of the cable to prevent signal reflections. Unterminated drop-lines (stubs) connecting nodes to the bus must be kept as short as possible to minimize signal reflections. The termination may be in a node but is generally not recommended, especially if the node may be removed from the bus. Termination must be carefully placed, so that it is not removed from the bus. System level CAN implementations such as CANopen allow for different termination and cabling concepts for example to add cable length.

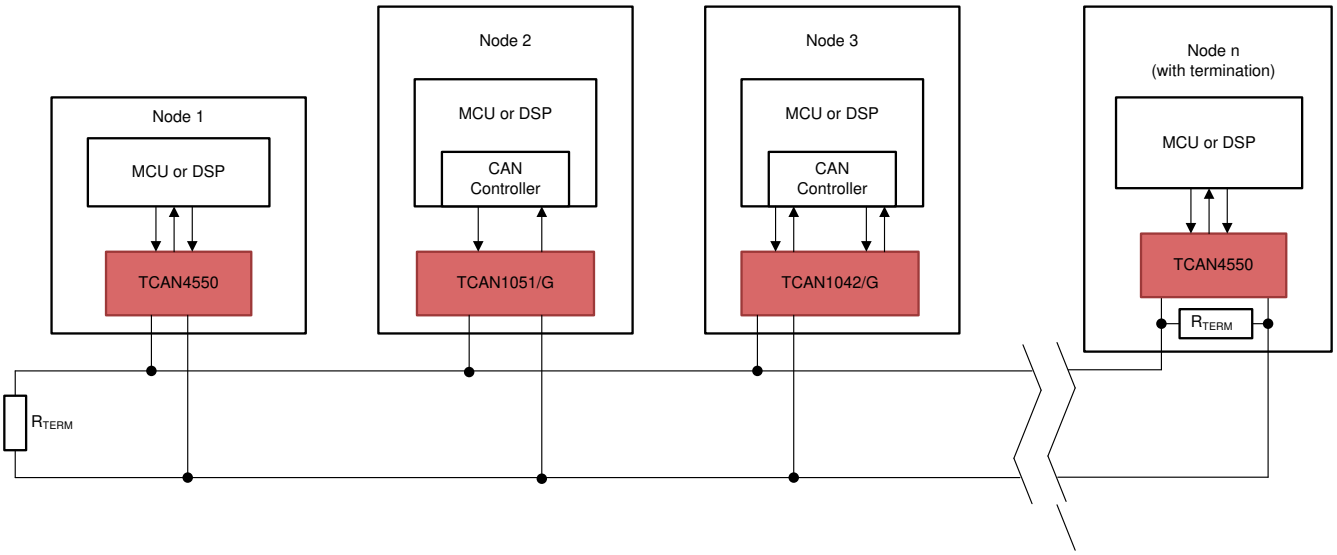

Figure 8-1. Typical CAN Bus

Termination may be a single 120Ω resistor at each end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common mode voltage of the bus is desired then “split termination” may be used, see Figure 8-2. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common mode voltage levels at the start and end of message transmissions.

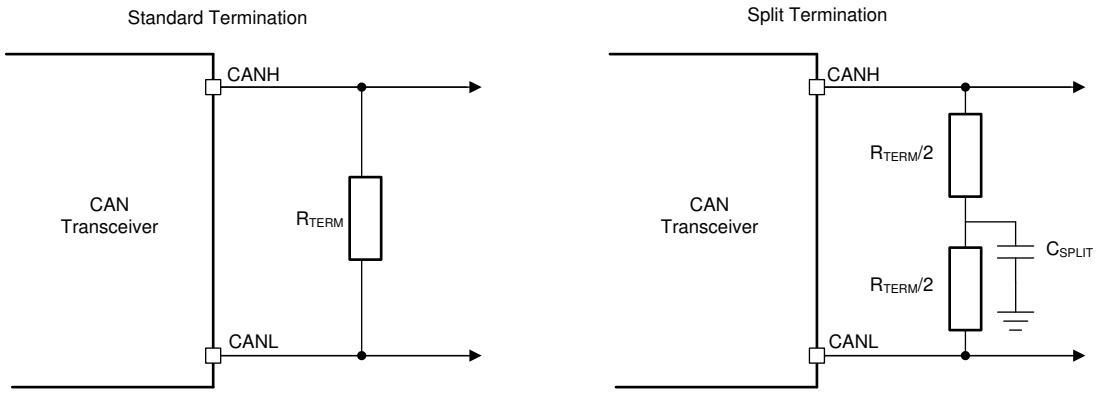

Figure 8-2. CAN Bus Termination Concepts

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8.1.3.2 CAN Bus Biasing

Bus biasing can be normal biasing, active in normal mode and inactive in low-power mode. Automatic voltage biasing is where the bus is active in normal mode but is controlled by the voltage between CANH and CANL in lower power modes. See Figure 8-3 for the state diagram on how the TCAN4572-Q1 performs automatic biasing. Figure 8-4 provides the bus biasing based upon the mode of operation.

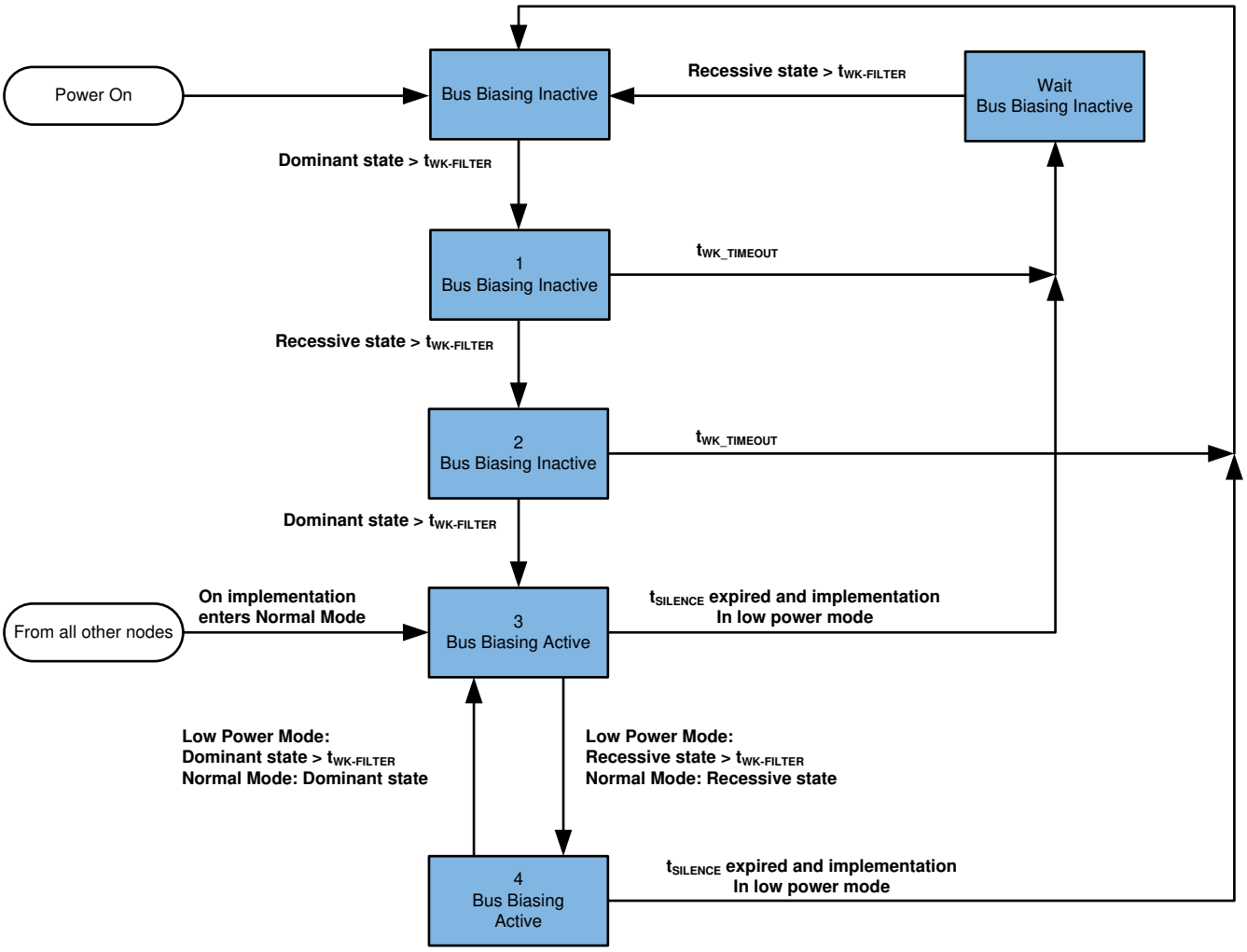

Figure 8-3. Automatic bus biasing state diagram

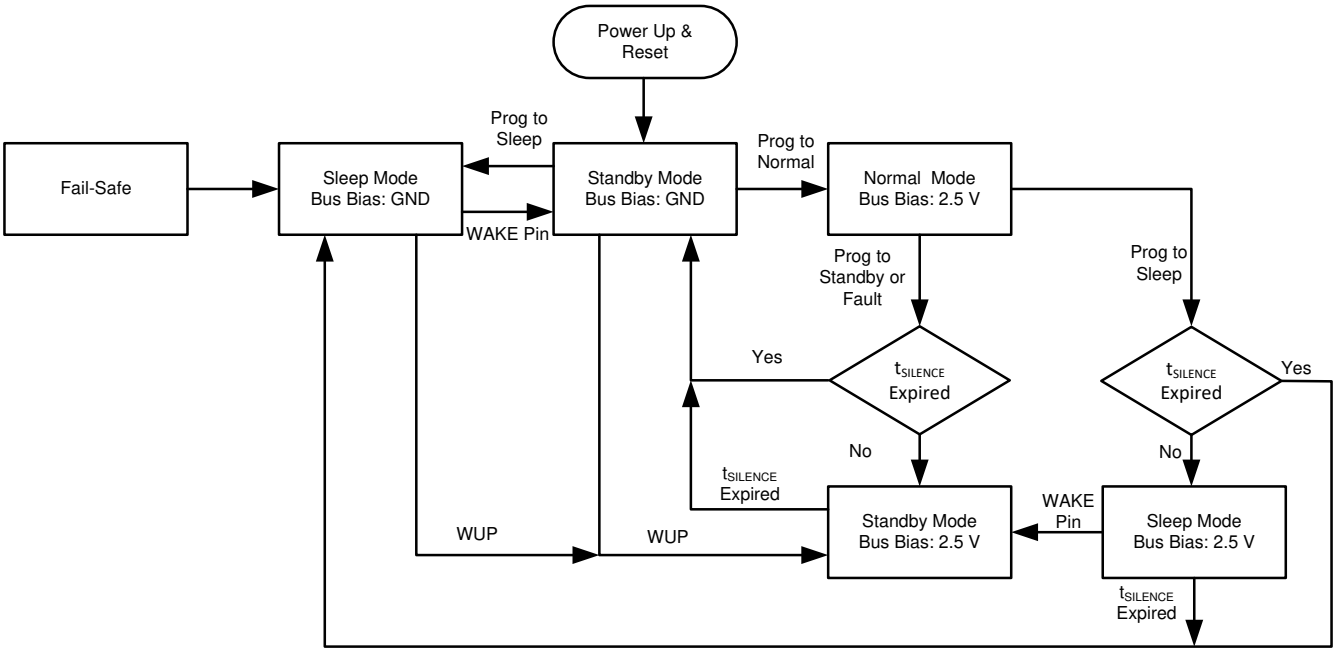

Figure 8-4. Bus Biasing Based on Modes of Operation

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8.2 Typical Application

The TCAN4572-Q1 is typically used in applications with a host microprocessor or FPGA that does not include the link layer portion of the CAN protocol. Figure 8-5 is a typical application configuration for 3.3V microprocessor applications.

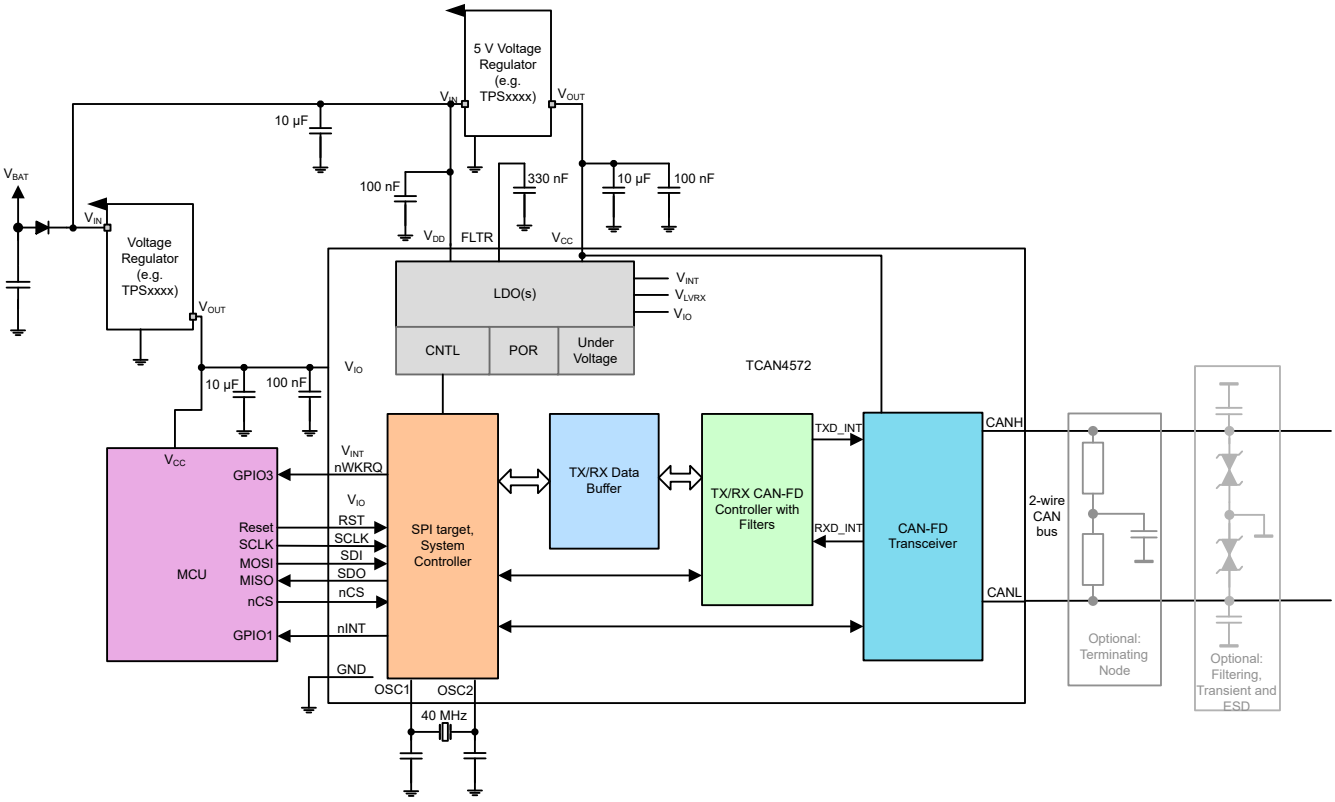

Figure 8-5. Typical CAN Applications for TCAN4572-Q1 for 3.3V µC and Crystal

8.2.1 Detailed Requirements

The TCAN4572-Q1 works with 3.3V and 5V microprocessors when using the V_{IO} pin from the microprocessor voltage regulator. The bus termination is shown for illustrative purposes.

8.2.2 Detailed Design Procedures

The TCAN4572-Q1 is designed to work in application using the ISO 11898 standard supporting bus loads from 45Ω to 65Ω. As the TCAN4572-Q1 supports CAN FD data rates up to 5Mbps, the recommendation is to use a 40MHz crystal and keep trace lengths matched and short as feasible between the processor and device. As the CAN stub length are defined in the standard, the recommendation is to design the system according to the standards. With the high temperature and input voltage range, the recommendation is to use a high-k board using proper thermal dissipation methods for the highest performance.

8.2.3 Application Curves

The internal oscillator value changes with temperature, and generally slows down at each extreme edge of temperature (cold and hot corners). It is also important to note that extremely low VDD voltages can also slow the oscillator down.

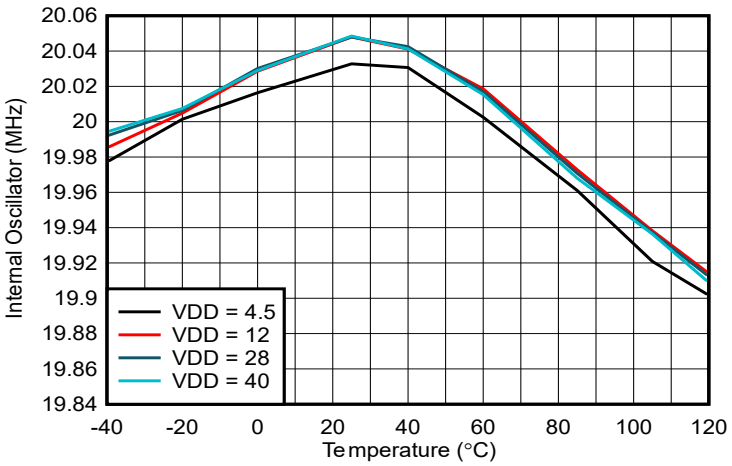

Figure 8-6. Oscillator Value Across Temperature and Voltage

8.3 Power Supply Recommendations

The TCAN4572-Q1 is designed to operate off of a wide range of voltages on the V_{DD} pin. The CAN transceiver is supported by the V_{CC} input. To support a wide range of microprocessors the SPI interface is powered off of the V_{IO} pin which supports levels from 1.8V to 5V nominal rails. Bulk capacitance, must be placed on the V_{DD}, the V_{IO}, and the V_{CC} voltage rails where system requirements are met. It is recommended that a capacitance of a 100nF is placed near the V_{DD}, the V_{IO}, and the V_{CC} supply terminals to aid decoupling noise.

Note

- The capacitance values selected must take into consideration the degradation over time such that the values do not fall below the minimum values shown.
- Above is a minimum amount of capacitance but due to system considerations more may be needed.

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8.4 Layout

Robust and reliable bus node design often requires the use of external transient protection device to protect against EFT and surge transients that may occur in industrial environments. Because ESD and transients have a wide frequency bandwidth from approximately 3MHz to 3GHz, high-frequency layout techniques must be applied during PCB design. The family comes with high on-chip IEC ESD protection, but if higher levels of system level immunity are desired external TVS diodes can be used. TVS diodes and bus filtering capacitors must be placed as close to the on-board connectors as possible to prevent noisy transient events from propagating further into the PCB and system.

8.4.1 Layout Guidelines

Place the protection and filtering circuitry as close to the bus connector, J1, to prevent transients, ESD and noise from propagating onto the board. The layout example provides information on components around the device. Transient voltage suppression (TVS) device can be added for extra protection, shown as D1. The production solution can be either a bi-directional TVS diode or a varistor with ratings matching the application requirements. This example also shows optional bus filter capacitors C10 and C11. A series common mode choke (CMC) is placed on the CANH and CANL lines between TCAN4572-Q1 and connector J1.

Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device. Use supply and ground planes to provide low inductance.

Note

High-frequency currents follows the path of least impedance and not the path of least resistance.

There are special considerations for the crystal oscillator and users are recommended to read the TCAN455x Clock Optimization and Design Guidelines application note *TCAN455x Clock Optimization and Design Guidelines (SLLA549)*. Some of these recommendations are listed below

- Place a power dissipation resistor between OSC1 and the crystal. This resistor can be used to reduce power to the crystal if the crystal is over-driven. This is shown in the example with R1

Use at least two vias for supply and ground connections of bypass capacitors and protection devices, if needed, to minimize trace and via inductance.

- Bypass and bulk capacitors must be placed as close as possible to the supply terminals of transceiver, examples are C3, C4 and C5 on the FLTR, V_{IO}, V_{CC}, pins and C6 and C7 on the V_{DD} supply.
- Bus termination: this layout example shows split termination. This is where the termination is split into two resistors, R5 and R6, with the center or split tap of the termination connected to ground via capacitor C9. Split termination provides common mode filtering for the bus. When bus termination is placed on the board instead of directly on the bus, additional care must be taken to make sure the terminating node is not removed from the bus thus also removing the termination.
- As nINT and nWKRQ are open drain, an external resistor to a supply (typically V_{IO}) is required. These can have a value between 1kΩ and 10kΩ.

8.4.2 Layout Example

Note

The choke and more advanced balancing network on CANH and CANL is not a requirement, but will provide improved emissions performance.

9 Register Maps

The TCAN4572-Q1 has a comprehensive register set with 32 bit addressing. The register is broken down into several sections:

- Device ID and Interrupt/Diagnostic Flag Registers: 16'h0000 to 16'h002F
- Device Configuration Registers: 16'h0800 to 16'h08FF
- CAN FD Registers: 16'h1000 to 16'h10FF
- CAN TX DMA Registers: 16'h5000 to 16'h5044
- CAN RX0 DMA Registers: 16'h5100 to 16'h5144
- CAN RX1 DMA Registers: 16'h5200 to 16'h5244

9.1 DEVICE_INFO_AND_SPI Registers

Section 9.1 lists the memory-mapped registers for the Device_Info_and_SPI registers. All register offset addresses not listed in Section 9.1 must be considered as reserved locations and the register contents must not be modified.

DEVICE INFO AND SPI REGISTERS

Table 9-1. DEVICE_INFO_AND_SPI Registers

Address	Acronym	Register Name	Section
0x0	DEVICE_ID0	Device ID 0	Section 9.1.1
0x4	DEVICE_ID1	Device ID 1	Section 9.1.2
0x8	DEVICE_REV	Device Revision	Section 9.1.3
0xC	SPI_IR_STATUS	SPI Status and Interrupts	Section 9.1.4
0x10	SPI_IE	SPI Interrupt Enable	Section 9.1.5
0x14	SPI_CRC_CONF	SPI CRC Configuration	Section 9.1.6
0x18	SPI_CRC_SEED	SPI CRC Seed Value	Section 9.1.7
0x1C	SCRATCHPAD	Scratchpad	Section 9.1.8

Complex bit access types are encoded to fit into small table cells. Section 9.1 shows the codes that are used for access types in this section.

Table 9-2. Device_Info_and_SPI Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RH	R H	Read Set or cleared by hardware
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
Reset or Default Value		
-n		Value after reset or the default value

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9.1.1 DEVICE_ID0 Register (Address = 0x0) [Reset = 0x4E414354]

DEVICE_ID0 is shown in Figure 9-1 and described in Table 9-3.

Return to the Summary Table.

Figure 9-1. DEVICE_ID0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEVICE_ID0[31:0]																															
R-0x4E414354																															

Table 9-3. DEVICE_ID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DEVICE_ID0[31:0]	R	0x4E414354	ASCII for "TCAN"

ADVANCE INFORMATION

9.1.2 DEVICE_ID1 Register (Address = 0x4) [Reset = 0x32373534]

DEVICE_ID1 is shown in Figure 9-2 and described in Table 9-4.

Return to the Summary Table.

Figure 9-2. DEVICE_ID1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEVICE_ID1[31:0]																															
R-0x32373534																															

Table 9-4. DEVICE_ID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DEVICE_ID1[31:0]	R	0x32373534	ASCII for "4572"

ADVANCE INFORMATION

9.1.3 DEVICE_REV Register (Address = 0x8) [Reset = 0x04000300]

DEVICE_REV is shown in Figure 9-3 and described in Table 9-5.

Return to the Summary Table.

Figure 9-3. DEVICE_REV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SPI_REVISION								RESERVED							
R-0x4								R-0x0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REV_MAJOR								REV_MINOR							
R-0x3								R-0x0							

Table 9-5. DEVICE_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	SPI_REVISION	R	0x4	Revision version of the SPI module
23-16	RESERVED	R	0x0	Reserved
15-8	REV_MAJOR	R	0x3	Device revision ID major
7-0	REV_MINOR	R	0x0	Device revision ID minor

9.1.4 SPI_IR_STATUS Register (Address = 0xC) [Reset = 0x00000000]

SPI_IR_STATUS is shown in Figure 9-4 and described in Table 9-6.

Return to the Summary Table.

Figure 9-4. SPI_IR_STATUS Register

31	30	29	28	27	26	25	24
RESERVED	SLP_IA	INT_R_ERR	INT_W_ERR	ERR_LOG_NE	R_FIFO_UF	R_FIFO_EMPTY	W_FIFO_OF
R-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0
23	22	21	20	19	18	17	16
RESERVED	CRC_ERR	SPI_END_ERR	IC	SPI_W_OF	SPI_W_UF	SPI_R_OF	SPI_R_UF
R-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0
15	14	13	12	11	10	9	8
RESERVED							
R-0x0							
7	6	5	4	3	2	1	0
RESERVED		W_FIFO_A	R_FIFO_A	INT_ACT	INT_ERR	SPI_ERR	INTERRUPT
R-0x0		R-0x0	R-0x0	RH-0x0	R-0x0	R-0x0	R-0x0

Table 9-6. SPI_IR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0x0	Reserved
30	SLP_IA	R/W1C	0x0	Attempt to read to invalid address while in sleep mode. Most registers are not accessible in sleep mode
29	INT_R_ERR	R/W1C	0x0	Internal read error
28	INT_W_ERR	R/W1C	0x0	Internal write error
27	ERR_LOG_NE	R/W1C	0x0	Entry has been written to internal error log
26	R_FIFO_UF	R/W1C	0x0	Read fifo underflow after 1 or more read data words returned. This typically indicates an issue with the high speed clock
25	R_FIFO_EMPTY	R/W1C	0x0	Read FIFO empty for first read data word to return via SPI. This typically indicates an issue with the high speed clock
24	W_FIFO_OF	R/W1C	0x0	Write/command FIFO overflow. This typically indicates an issue with the high speed clock
23	RESERVED	R	0x0	Reserved
22	CRC_ERR	R/W1C	0x0	SPI CRC error has occurred. A received CRC did not match the expected value, and if the data was a write request, it was ignored.
21	SPI_END_ERR	R/W1C	0x0	SPI transfer did not end on a byte boundary. Typically indicates glitching/noise on the SPI lines
20	IC	R/W1C	0x0	Invalid command was received in the SPI request
19	SPI_W_OF	R/W1C	0x0	SPI write overflow, the write sequence continued after the specified number of words were transferred. This is caused by writing more words of data than specified in the SPI header
18	SPI_W_UF	R/W1C	0x0	SPI write underflow, the write sequence ended before the specified number of words were transferred. This is caused by writing fewer words of data than specified in the SPI header
17	SPI_R_OF	R/W1C	0x0	SPI read overflow, the read sequence continued after the specified number of words were transferred. This is caused by reading more words of data than specified in the SPI header

Table 9-6. SPI_IR_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	SPI_R_UF	R/W1C	0x0	SPI read underflow, the read sequence ended before the specified number of words were transferred. This is caused by reading fewer words of data than specified in the SPI header
15-6	RESERVED	R	0x0	Reserved
5	W_FIFO_A	R	0x0	Write FIFO has available space. This is a status flag and not an interrupt
4	R_FIFO_A	R	0x0	Read FIFO has available space. This is a status flag and not an interrupt
3	INT_ACT	RH	0x0	Internal transfer mode access is currently in progress. This is a status flag and not an interrupt
2	INT_ERR	R	0x0	Unmasked internal error flag. Is set if any internal transfer error interrupts are set
1	SPI_ERR	R	0x0	Unmasked SPI error flag. Is set if any SPI transfer error interrupts are set
0	INTERRUPT	R	0x0	Interrupt output. Is set if any masked interrupts are set

9.1.5 SPI_IE Register (Address = 0x10) [Reset = 0x00000000]

SPI_IE is shown in Figure 9-5 and described in Table 9-7.

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Figure 9-5. SPI_IE Register

31	30	29	28	27	26	25	24
RESERVED	SLP_IA	INT_R_ERR	INT_W_ERR	ERR_LOG_NE	R_FIFO_UF	R_FIFO_EMPTY	W_FIFO_OF
R-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0
23	22	21	20	19	18	17	16
RESERVED		SPI_END_ERR	IC	SPI_W_OF	SPI_W_UF	SPI_R_OF	SPI_R_UF
R-0x0		R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0
15	14	13	12	11	10	9	8
RESERVED							
R-0x0							
7	6	5	4	3	2	1	0
RESERVED							
R-0x0							

Table 9-7. SPI_IE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0x0	Reserved
30	SLP_IA	R/W	0x0	Attempt to read to invalid address while in sleep mode. Most registers are not accessible in sleep mode 0x0 = Interrupt disabled 0x1 = Interrupt enabled
29	INT_R_ERR	R/W	0x0	Internal read error 0x0 = Interrupt disabled 0x1 = Interrupt enabled
28	INT_W_ERR	R/W	0x0	Internal write error 0x0 = Interrupt disabled 0x1 = Interrupt enabled
27	ERR_LOG_NE	R/W	0x0	Entry has been written to internal error log 0x0 = Interrupt disabled 0x1 = Interrupt enabled
26	R_FIFO_UF	R/W	0x0	Read fifo underflow after 1 or more read data words returned. This typically indicates an issue with the high speed clock 0x0 = Interrupt disabled 0x1 = Interrupt enabled
25	R_FIFO_EMPTY	R/W	0x0	Read FIFO empty for first read data word to return via SPI. This typically indicates an issue with the high speed clock 0x0 = Interrupt disabled 0x1 = Interrupt enabled
24	W_FIFO_OF	R/W	0x0	Write/command FIFO overflow. This typically indicates an issue with the high speed clock 0x0 = Interrupt disabled 0x1 = Interrupt enabled
23-22	RESERVED	R	0x0	Reserved
21	SPI_END_ERR	R/W	0x0	SPI transfer did not end on a byte boundary. Typically indicates glitching/noise on the SPI lines 0x0 = Interrupt disabled 0x1 = Interrupt enabled
20	IC	R/W	0x0	Invalid command was received in the SPI request 0x0 = Interrupt disabled 0x1 = Interrupt enabled

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Table 9-7. SPI_IE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	SPI_W_OF	R/W	0x0	SPI write overflow, the write sequence continued after the specified number of words were transferred. This is caused by writing more words of data than specified in the SPI header 0x0 = Interrupt disabled 0x1 = Interrupt enabled
18	SPI_W_UF	R/W	0x0	SPI write underflow, the write sequence ended before the specified number of words were transferred. This is caused by writing fewer words of data than specified in the SPI header 0x0 = Interrupt disabled 0x1 = Interrupt enabled
17	SPI_R_OF	R/W	0x0	SPI read overflow, the read sequence continued after the specified number of words were transferred. This is caused by reading more words of data than specified in the SPI header 0x0 = Interrupt disabled 0x1 = Interrupt enabled
16	SPI_R_UF	R/W	0x0	SPI read underflow, the read sequence ended before the specified number of words were transferred. This is caused by reading fewer words of data than specified in the SPI header 0x0 = Interrupt disabled 0x1 = Interrupt enabled
15-0	RESERVED	R	0x0	Reserved

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9.1.6 SPI_CRC_CONF Register (Address = 0x14) [Reset = 0x00000000]

SPI_CRC_CONF is shown in Figure 9-6 and described in Table 9-8.

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Figure 9-6. SPI_CRC_CONF Register

31	30	29	28	27	26	25	24
RESERVED							
R-0x0							
23	22	21	20	19	18	17	16
RESERVED							
R-0x0							
15	14	13	12	11	10	9	8
RESERVED							
R-0x0							
7	6	5	4	3	2	1	0
RESERVED		CRC_BYTE_ORDER	CRC_POLY		CRC_SEED_CFG		CRC_EN
R-0x0		R/W-0x0	R/W-0x0		R/W-0x0		R/W-0x0

Table 9-8. SPI_CRC_CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0x0	Reserved
5	CRC_BYTE_ORDER	R/W	0x0	CRC byte order 0x0 = MSB first 0x1 = LSB first
4-3	CRC_POLY	R/W	0x0	CRC polynomial used for CRC calculations 0x0 = 0x8005 (CRC-16-IBM) 0x1 = 0x1021 (CRC-16-CCITT) 0x2 = 0xC867 (CRC-16-CDMA2000) 0x3 = 0x0589 (CRC-16-DECT)
2-1	CRC_SEED_CFG	R/W	0x0	CRC seed value used for each SPI frame 0x0 = 0x0000 0x1 = 0xFFFF 0x2 = Use value in CRC_SEED 0x3 = Reserved
0	CRC_EN	R/W	0x0	CRC enable 0x0 = SPI CRC is disabled 0x1 = SPI CRC is enabled

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9.1.7 SPI_CRC_SEED Register (Address = 0x18) [Reset = 0x00000000]

SPI_CRC_SEED is shown in Figure 9-7 and described in Table 9-9.

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Figure 9-7. SPI_CRC_SEED Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																SPI_CRC_SEED															
R-0x0																R/W-0x0															

Table 9-9. SPI_CRC_SEED Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0x0	Reserved
15-0	SPI_CRC_SEED	R/W	0x0	The initial seed value used for CRC calculations for each SPI frame. Only used if SPI_CRC_CONF.SPI_SEED_CFG = 2

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9.1.8 SCRATCHPAD Register (Address = 0x1C) [Reset = 0x00000000]

SCRATCHPAD is shown in Figure 9-8 and described in Table 9-10.

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Figure 9-8. SCRATCHPAD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCRATCHPAD																															
R/W-0x0																															

Table 9-10. SCRATCHPAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SCRATCHPAD	R/W	0x0	Scratchpad register used for testing. It is not preserved through resets

9.2 DEVICE_CONFIG Registers

Section 9.2 lists the memory-mapped registers for the DEVICE_CONFIG registers. All register offset addresses not listed in Section 9.2 must be considered as reserved locations and the register contents must not be modified.

DEVICE INFO AND SPI REGISTERS

Table 9-11. DEVICE_CONFIG Registers

Address	Acronym	Register Name	Section
0x800	DEV_MODE_PINS	Device Modes of Operation and Pin Configurations	Section 9.2.1
0x804	TIMESTAMP_PRESCALER	Timestamp Prescaler	Section 9.2.2
0x808	SCRATCHPAD	Device Timestamp	Section 9.2.3
0x80C	ECC_CONFIG	ECC Configuration	Section 9.2.4
0x814	IP_EN_CNTRL	IP Enable and Control	Section 9.2.5
0x820	INT_DEVICE	Device Interrupt Flags	Section 9.2.6
0x824	INT_MCAN	MCAN Interrupt Flags	Section 9.2.7
0x830	INT_DEVICE_EN	Device Interrupts Enable	Section 9.2.8
0x830	INT_DEVICE_EN	Device Interrupts Enable	Section 9.2.9

Complex bit access types are encoded to fit into small table cells. Section 9.2 shows the codes that are used for access types in this section.

Table 9-12. DEVICE_CONFIG Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
RH	R H	Read Set or cleared by hardware
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
W1S	W 1S	Write 1 to set
WP	W P	Write Requires privileged access
Reset or Default Value		

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Table 9-12. DEVICE_CONFIG Access Type Codes (continued)

Access Type	Code	Description
-n		Value after reset or the default value

9.2.1 DEV_MODE_PINS Register (Address = 0x800) [Reset = 0x00000040]

DEV_MODE_PINS is shown in Figure 9-9 and described in Table 9-13.

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Note

The MODE_SEL field changes the mode, but a read back will read back the mode that the device is currently in.

Figure 9-9. DEV_MODE_PINS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0x0							
23	22	21	20	19	18	17	16
RESERVED		TEST_MODE_EN	RESERVED				
R-0x0		R/W-0x0	R-0x0				
15	14	13	12	11	10	9	8
RESERVED		FAILSAFE_EN	RESERVED		nWKRQ_MCAN_INT1	RESERVED	nWKRQ_CONFIG
R-0x0		R/W-0x0	R-0x0		R/W-0x0	R-0x0	R/W-0x0
7	6	5	4	3	2	1	0
MODE_SEL		RESERVED	RESERVED	RESERVED	DEV_RESET	SWE_DIS	RESERVED
R/W-0x1		R-0x0	R-0x0	R-0x0	R-0x0	R/W-0x0	R-0x0

Table 9-13. DEV_MODE_PINS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R	0x0	Reserved
21	TEST_MODE_EN	R/W	0x0	Transceiver test mode enable **Note** This bit always reads 0, because even if it is set to 1, the act of trying to read the register will exit test mode, making it a 0 0x0 = Disabled 0x1 = Enabled. CAN transceiver TXD is mapped to SDI, RXD is connected to SDO, and EN is connected to SCLK. Test mode becomes active immediately after nCS is deasserted. Test mode is exited immediately when nCS is re-asserted.
20-14	RESERVED	R	0x0	Reserved
13	FAILSAFE_EN	R/W	0x0	Failsafe mode enable **Note** Excludes power up failsafe. See failsafe section for more information 0x0 = Disabled 0x1 = Enabled
12-11	RESERVED	R	0x0	Reserved

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Table 9-13. DEV_MODE_PINS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	nWKRQ_MCAN_INT1	R/W	0x0	nWKRQ to MCAN INT1 override. Set the functionality of the nWKRQ to be connected to MCAN's INT1 output line. **Note** To utilize INT1 in MCAN, the MCAN_ILE register must enable INT1 and MCAN_ILS is used to select which INT line is used for various MCAN interrupts 0x0 = nWKRQ is configured according nWKRQ_CONFIG 0x1 = nWKRQ is MCAN_INT1 (active low)
9	RESERVED	R	0x0	Reserved
8	nWKRQ_CONFIG	R/W	0x0	nWKRQ pin function 0x0 = nWKRQ mirrors INH function 0x1 = nWKRQ is a wake request interrupt pin (active low)
7-6	MODE_SEL	R/W	0x1	Device mode selection **Note** When changing the device to normal mode, a write of 0 to the CCCR.INIT bit is automatically issued. When changing from normal to standby or sleep modes, a write of 1 to CCCR.INIT is automatically issued. 0x0 = Sleep 0x1 = Standby 0x2 = Normal 0x3 = TSD Protected (read only)
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	DEV_RESET	R	0x0	Device reset **Note** The device must be in standby, normal or TSD protected modes for this bit to function. If asleep, the device must first be woken up by going to standby mode 0x0 = nWKRQ mirrors INH function 0x1 = nWKRQ is a wake request interrupt pin (active low)
1	SWE_DIS	R/W	0x0	Sleep wake error disable. **Note** This disables the device from starting the four minute timer when coming out of sleep mode on a wake event. If the sleep wake error is enabled (= 0), then a SPI read or write must take place within this four minute window or the device will go back to sleep. This does not disable the functionality on initial power on reset
0	RESERVED	R	0x0	Reserved

9.2.2 TIMESTAMP_PRESCALER Register (Address = 0x804) [Reset = 0x00000002]

TIMESTAMP_PRESCALER is shown in Figure 9-10 and described in Table 9-14.

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Figure 9-10. TIMESTAMP_PRESCALER Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0x0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PRESCALER							
R-0x0								R/W-0x2							

Table 9-14. TIMESTAMP_PRESCALER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0x0	Reserved
7-0	PRESCALER	R/W	0x2	Writing to this register resets the internal timestamp counter to 0 and will set the internal CAN clock divider used for MCAN timestamp generation to (timestamp prescaler x 8)

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9.2.3 SCRATCHPAD Register (Address = 0x808) [Reset = 0x00000000]

SCRATCHPAD is shown in Figure 9-11 and described in Table 9-15.

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Figure 9-11. SCRATCHPAD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCRATCHPAD																															
R/W-0x0																															

Table 9-15. SCRATCHPAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SCRATCHPAD	R/W	0x0	Test read and write scratchpad register

9.2.4 ECC_CONFIG Register (Address = 0x80C) [Reset = 0x00000000]

ECC_CONFIG is shown in Figure 9-12 and described in Table 9-16.

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Figure 9-12. ECC_CONFIG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0x0							
23	22	21	20	19	18	17	16
RESERVED			ECC_ERR_FORCE_BIT_SEL				
R-0x0			R/W-0x0				
15	14	13	12	11	10	9	8
RESERVED			ECC_ERR_FORCE	ECC_ERR_CHECK	RESERVED		
R-0x0			R/W-0x0	R/W1C-0x0	R-0x0		
7	6	5	4	3	2	1	0
RESERVED							
R-0x0							

Table 9-16. ECC_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R	0x0	Reserved
21-16	ECC_ERR_FORCE_BIT_SEL	R/W	0x0	Sets a specific bit in the bit to be flipped from correct value. 6b 000000 = Bit 0 6b 000001 = Bit 1 6b 000010 = Bit 2 and 6b 100110 = Bit 38
15-13	RESERVED	R	0x0	Reserved
12	ECC_ERR_FORCE	R/W	0x0	Force a single bit ECC error 0x0 = No error is forced 0x1 = Force a single bit ECC error for MRAM
11	ECC_ERR_CHECK	R/W1C	0x0	Status bit if an ECC error is detected. 0x0 = No single bit ECC error detected 0x1 = Single bit ECC error detected
10-0	RESERVED	R	0x0	Reserved

9.2.5 IP_EN_CNTRL Register (Address = 0x814) [Reset = 0x000000X0]

Figure 9-13. IP_EN_CNTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0x0							
23	22	21	20	19	18	17	16
RESERVED							
R-0x0							
15	14	13	12	11	10	9	8
RESERVED		CLK_SEL	CLK_FORCE	RESERVED			
R-0x0		R/WP-0x0	R/WP-0x0	R-0x0			
7	6	5	4	3	2	1	0
CLK_EXT	CLK_XTAL	FDL_ACK_DIS	FDL_CMDR_EN	RESERVED			CCE
R-0xX	R-0xX	R/WP-0x0	R/WP-0x0	R-0x0			R/W-0x0

Table 9-17. IP_EN_CNTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R	0x0	Reserved
13	CLK_SEL	R/WP	0x0	Clock source selection This bit selects which clock source is used if CLK_FORCE is enabled 0x0 = Internal 20 MHz clock 0x1 = External clock source
12	CLK_FORCE	R/WP	0x0	Clock source override This bit will override the automatic clock selection logic and will force the device to use the clock source specified in CLK_SEL. **Note** When changing the clock source, it's important to wait t_{CLOCK_SWITCH} time to let the system switch clocks. If switching to an external crystal, the wait time is dependent upon the crystal start up time. 0x0 = Use automatic clock detection source 0x1 = Override clock source
11-8	RESERVED	R	0x0	Reserved
7	CLK_EXT	R	X	Clock status: External Reflects the currently selected clock source 0x0 = Internal clock source 0x1 = External clock source
6	CLK_XTAL	R	X	Crystal Detected Reflects if the device detected a crystal oscillator at power up. 0x0 = No crystal detected (external clock in or internal clock in) 0x1 = Crystal detected
5	FDL_ACK_DIS	R/WP	0x0	Acknowledge Disable Bit If in CAN FD Light Commander mode (bit 4 = 1), this bit is used to disable the ACK bit. At speeds greater than 1 Mbps, it is recommended to disable the ACK bit by setting this bit to 1 0x0 = Acknowledge bit is enabled (like normal CAN behavior) 0x1 = Acknowledge bit is disabled
4	FDL_CMDR_EN	R/WP	0x0	CAN FD Light Commander Mode Enable Used to enable CAN FD Light Commander functionality 0x0 = CAN FD Functionality 0x1 = CAN FD Light Commander Functionality
3-1	RESERVED	R	0x0	Reserved

Table 9-17. IP_EN_CNTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CCE	R/W	0x0	Configuration change enable **Note** The CCE bit allows access to protected bits in this IP enable register only (0x0814). This bit can only be set while in standby mode. Attempts to set it in normal mode will be ignored. Also note that a transition from standby to normal mode will automatically clear the CCE bit. 0x0 = No write access to the protected configuration registers 0x1 = Write access to the protected configuration registers is enabled (requires device to be in standby mode)

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9.2.6 INT_DEVICE Register (Address = 0x820) [Reset = 0x00100000]

INT_DEVICE is shown in Figure 9-14 and described in Table 9-18.

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Figure 9-14. INT_DEVICE Register

31	30	29	28	27	26	25	24
RESERVED	MODE_SLEEP	RESERVED					
R-0x0	R-0x0	R-0x0					
23	22	21	20	19	18	17	16
SMS	UV_{DD}	UV_{IO}	PWRON	TSD	RESERVED	UVCC	ECCERR
R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x1	R/W1C-0x0	R-0x0	R/W1C-0x0	R/W1C-0x0
15	14	13	12	11	10	9	8
	RESERVED	WKERR		CRCERR_INT	CANSLNT	RESERVED	CANDOM
	R-0x0	R-0x0		R/W1C-0x0	R/W1C-0x0	R-0x0	R/W1C-0x0
7	6	5	4	3	2	1	0
GLOBALERR	WKRQ	CANERR	CBF	SPIERR	RESERVED	MCAN_INT	VT
R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0

Table 9-18. INT_DEVICE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0x0	Reserved
30	MODE_SLEEP	R	0x0	A bit to indicate to the MCU that the device is currently in sleep mode. If the device is asleep, only a subset of registers are accessible. If this flag is set, the device must first be woken to clear any interrupts. See the sleep mode section for more information.
29-24	RESERVED	R	0x0	Reserved
23	SMS	R/W1C	0x0	Sleep mode status (Flag and not an interrupt). Only sets when sleep mode is entered by a WKERR, UV_{IO} timeout or a UVCC timeout (if failsafe is enabled)
22	UV_{DD}	R/W1C	0x0	Undervoltage for VDD. This is just a flag to alert the user before a POR happens
21	UV_{IO}	R/W1C	0x0	Undervoltage for V_{IO}.
20	PWRON	R/W1C	0x1	Power on resist interrupt. This is set any time a power reset event occurs. This flag can also be cleared by going to sleep mode or normal mode.
19	TSD	R/W1C	0x0	Thermal shutdown
18	RESERVED	R	0x0	Reserved
17	UVCC	R/W1C	0x0	Under voltage on VCC. This flag cannot be cleared until the fault is gone.
16	ECCERR	R/W1C	0x0	Uncorrectable ECC error detected
14	RESERVED	R	0x0	Reserved
13	WKERR	R	0x0	Wake error If the device receives a wake up request (WUP) and does not transition to normal mode or clear the PWRON or wake flag before $t_{INACTIVE}$, the device will transition to sleep mode. After the wake event, a wake error (WKERR) will be reported and the SMS flag will be set to 1.
12	RESERVED	R	0x0	Reserved
11	CRCERR_INT	R/W1C	0x0	Internal EEPROM CRC error detected
10	CANSLNT	R/W1C	0x0	CAN silent ($t_{SILENCE}$) timer has expired due to CAN bus silence
9	RESERVED	R	0x0	Reserved

Table 9-18. INT_DEVICE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	CANDOM	R/W1C	0x0	CAN bus stuck dominant
7	GLOBALERR	R	0x0	Global error (any fault) Logical OR of all faults/interrupts. Some status flags are not included (sleep mode flag)
6	WKRQ	R	0x0	Wake request Logical OR of CANINT, and WKERR
5	CANERR	R	0x0	CAN error Logical OR of CANSLNT and CANDOM faults
4	CBF	R	0x0	CAN bus faults Logical OR of CANHCANL, CANHVDD, CANLGND, CANBUSOPEN, CANBUSGND, and CANBUSVDD faults
3	SPIERR	R	0x0	SPI error Will be set if any of the interrupts in 0x000C[30:16] is set. To clear these interrupts, the bits in 0x000C must be cleared.
2	SWERR	R	0x0	Selective wake error
2	RESERVED	R	0x0	Reserved
1	MCAN_INT	R	0x0	A logical OR of the MCAN global INT
0	VT	R	0x0	Global voltage, temperature or ECC errors Logical OR of UVCC, UVDD, UV_{IO}, TSD, and ECCERR.

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9.2.7 INT_MCAN Register (Address = 0x824) [Reset = 0x00000000]

INT_MCAN is shown in Figure 9-15 and described in Table 9-19.

Return to the Summary Table.

Figure 9-15. INT_MCAN Register

31	30	29	28	27	26	25	24
RESERVED		ARA	PED	PEA	WDI	BO	EW
R-0x0		R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0
23	22	21	20	19	18	17	16
EP	ELO	BEU	BEC	DRX	TOO	MRAF	TSW
R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0
15	14	13	12	11	10	9	8
TEFL	TEFF	TEFW	TEFN	TFE	TCF	TC	HPM
R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0
7	6	5	4	3	2	1	0
RF1L	RF1F	RF1W	RF1N	RF0L	RF0F	RF0W	RF0N
R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0

Table 9-19. INT_MCAN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0x0	Reserved
29	ARA	R	0x0	Access to reserved address
28	PED	R	0x0	Protocol error in data phase (data bit time is used)
27	PEA	R	0x0	Protocol error in arbitration phase (nominal bit time is used)
26	WDI	R	0x0	MRAM watchdog interrupt
25	BO	R	0x0	Bus off interrupt
24	EW	R	0x0	Warning status
23	EP	R	0x0	Error passive
22	ELO	R	0x0	Error logging overflow
21	BEU	R	0x0	Bit error uncorrected
20	BEC	R	0x0	Bit error corrected
19	DRX	R	0x0	Message stored to dedicated RX buffer
18	TOO	R	0x0	Timeout occurred
17	MRAF	R	0x0	Message RAM access failure
16	TSW	R	0x0	Timestamp wraparound
15	TEFL	R	0x0	TX event FIFO element lost
14	TEFF	R	0x0	TX event FIFO full
13	TEFW	R	0x0	TX event FIFO watermark reached
12	TEFN	R	0x0	TX Event FIFO new entry
11	TFE	R	0x0	TX FIFO empty
10	TCF	R	0x0	Transmission cancellation finished
9	TC	R	0x0	Transmission Completed
8	HPM	R	0x0	High priority message
7	RF1L	R	0x0	RX FIFO 1 message lost
6	RF1F	R	0x0	RX FIFO 1 full
5	RF1W	R	0x0	RX FIFO 1 watermark reached
4	RF1N	R	0x0	RX FIFO 1 new message
3	RF0L	R	0x0	RX FIFO 0 message lost

Table 9-19. INT_MCAN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RF0F	R	0x0	RX FIFO 0 full
1	RF0W	R	0x0	RX FIFO 0 watermark reached
0	RF0N	R	0x0	RX FIFO 0 new message

9.2.8 INT_DEVICE_EN Register (Address = 0x830) [Reset = 0xFFFFFF01]

INT_DEVICE_EN is shown in Figure 9-16 and described in Table 9-20.

Return to the Summary Table.

Figure 9-16. INT_DEVICE_EN Register

31	30	29	28	27	26	25	24
RESERVED		CANHCANL	CANHVDD	CANLGND	CANBUSOPEN	CANBUSGND	CANBUSVDD
R-0x0		R/W-0x1	R/W-0x1	R/W-0x1	R/W-0x1	R/W-0x1	R/W-0x1
23	22	21	20	19	18	17	16
RESERVED		UV_{IO}	RESERVED	TSD	RESERVED	UVCC	ECCERR
R-0x0		R/W-0x1	R-0x0	R/W-0x1	R-0x0	R/W-0x1	R/W-0x1
15	14	13	12	11	10	9	8
CANINT		RESERVED			CANSLNT	RESERVED	CANDOM
R/W-0x1		R-0x0			R/W-0x1	R-0x0	R/W-0x1
7	6	5	4	3	2	1	0
RESERVED							
R-0x0							

Table 9-20. INT_DEVICE_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0x0	Reserved
29	CANHCANL	R/W	0x1	CANH and CANL are shorted together
28	CANHVDD	R/W	0x1	CANH shorted to VDD
27	CANLGND	R/W	0x1	CANL shorted to GND
26	CANBUSOPEN	R/W	0x1	CAN bus open (one of 3 possible locations)
25	CANBUSGND	R/W	0x1	CANH shorted to GND or both CANH and CANL are shorted to GND
24	CANBUSVDD	R/W	0x1	CANH shorted to VDD or both CANH and CANL are shorted to VDD
23	RESERVED	R	0x0	Reserved
21	UV_{IO}	R/W	0x1	Undervoltage for V_{IO}.
20	RESERVED	R	0x0	Reserved
19	TSD	R/W	0x1	Thermal shutdown
18	RESERVED	R	0x0	Reserved
17	UVCC	R/W	0x1	Under voltage on VCC. This flag cannot be cleared until the fault is gone.
16	ECCERR	R/W	0x1	Uncorrectable ECC error detected
15	CANINT	R/W	0x1	CAN bus wake up interrupt. Indicates a wake up event occurred from a CAN wake up event. Flag can also be cleared by moving to normal or sleep modes
13-11	RESERVED	R	0x0	Reserved
10	CANSLNT	R/W	0x1	CAN silent ($t_{SILENCE}$) timer has expired due to CAN bus silence
9	RESERVED	R	0x0	Reserved
8	CANDOM	R/W	0x1	CAN bus stuck dominant
7-0	RESERVED	R	0x0	Reserved

9.2.9 INT_DEVICE_EN Register (Address = 0x830) [Reset = 0xFFFFFF01]

INT_DEVICE_EN is shown in Figure 9-17 and described in Table 9-21.

Return to the Summary Table.

Figure 9-17. INT_DEVICE_EN Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED	CANHCANL	CANHVDD	CANLGND	CANBUSOPEN	CANBUSGND	CANBUSVDD
R-0x0	R-0x0	R/W-0x1	R/W-0x1	R/W-0x1	R/W-0x1	R/W-0x1	R/W-0x1
23	22	21	20	19	18	17	16
RESERVED	RESERVED	UV_{IO}	RESERVED	TSD	RESERVED	UVCC	ECCERR
R-0x0	R-0x0	R/W-0x1	R-0x0	R/W-0x1	R-0x0	R/W-0x1	R/W-0x1
15	14	13	12	11	10	9	8
CANINT	RESERVED	RESERVED			CANSLNT	RESERVED	CANDOM
R/W-0x1	R-0x0	R-0x0			R/W-0x1	R-0x0	R/W-0x1
7	6	5	4	3	2	1	0
RESERVED							
R-0x0							

Table 9-21. INT_DEVICE_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0x0	Reserved
30	RESERVED	R	0x0	Reserved
29	CANHCANL	R/W	0x1	CANH and CANL are shorted together
28	CANHVDD	R/W	0x1	CANH shorted to VDD
27	CANLGND	R/W	0x1	CANL shorted to GND
26	CANBUSOPEN	R/W	0x1	CAN bus open (one of 3 possible locations)
25	CANBUSGND	R/W	0x1	CANH shorted to GND or both CANH and CANL are shorted to GND
24	CANBUSVDD	R/W	0x1	CANH shorted to VDD or both CANH and CANL are shorted to VDD
23	RESERVED	R	0x0	Reserved
22	RESERVED	R	0x0	Reserved
21	UV_{IO}	R/W	0x1	Undervoltage for V_{IO}.
20	RESERVED	R	0x0	Reserved
19	TSD	R/W	0x1	Thermal shutdown
18	RESERVED	R	0x0	Reserved
17	UVCC	R/W	0x1	Under voltage on VCC. This flag cannot be cleared until the fault is gone.
16	ECCERR	R/W	0x1	Uncorrectable ECC error detected
15	CANINT	R/W	0x1	CAN bus wake up interrupt. Indicates a wake up event occurred from a CAN wake up event. Flag can also be cleared by moving to normal or sleep modes
14	RESERVED	R	0x0	Reserved
13-11	RESERVED	R	0x0	Reserved
10	CANSLNT	R/W	0x1	CAN silent ($t_{SILENCE}$) timer has expired due to CAN bus silence
9	RESERVED	R	0x0	Reserved
8	CANDOM	R/W	0x1	CAN bus stuck dominant
7-0	RESERVED	R	0x0	Reserved

ADVANCE INFORMATION

9.3 Interrupt/Diagnostic Flag and Enable Flag Registers: 16'h0820 to 16'h0830

This register block provides all the interrupt flags for the device. As the M-CAN interrupt flags 16'h0824 are described in 16'h1050 MCAN register description section and will be shown here but need to go to 16'h1050 for description. 16h'0830 is Interrupt enable to trigger an interrupt for 16'h0820.

9.3.1 Interrupts (address = h0820) [reset = h00100000]

Figure 9-18. Interrupts

31	30	29	28	27	26	25	24
RSVD	MODE_SLEEP	CANHCANL	CANHVDD	CANLGND	CANBUSOPEN	CANBUSGND	CANBUSVDD
R	R	R	R	R	R	R	R
23	22	21	20	19	18	17	16
SMS		UVIO	PWRON	TSD	RSVD	UVCC	ECCERR
R	R	R/WC	R/WC/U	R/WC	R	R/WC	R/WC
15	14	13	12	11	10	9	8
CANINT	RSVD	WKERR	RSVD	CRCERR_INT	CANSLNT	RSVD	CANDOM
R/WC	R	R/WC	R	R/WC	R/WC	R	R/WC
7	6	5	4	3	2	1	0
GLOBALERR	WKRQ	CANERR	RSVD	SPIERR	RSVD	M_CAN_INT	VT
R	R	R	R	R	R	R	R

Table 9-22. Interrupts Field Descriptions

Bit	Field	Type	Reset	Description
31	RSVD	R	1'b0	Reserved
30	MODE_SLEEP	R	1'b0	A bit to indicate to the MCU that the device is currently asleep. If the device is asleep, only a subset of registers are accessible. This lets the CPU know that it must wake the device to clear interrupts.
29	CANHCANL	R/WC	1'b0	CANH and CANL are shorted together
28	CANHVDD	R/WC	1'b0	CANH shorted to V_{DD}
27	CANLGND	R/WC	1'b0	CANL shorted to GND
26	CANBUSOPEN	R/WC	1'b0	CAN bus open (one of 3 possible places)
25	CANBUSGND	R/WC	1'b0	CANH shorted to GND or both CANH & CANL shorted to GND
24	CANBUSVDD	R/WC	1'b0	CANH shorted to V_{DD} or both CANH and CANL shorted to V_{DD}
23	SMS	R/WC	1'b0	Sleep Mode Status (Flag & Not an interrupt) Only sets when sleep mode is entered by a WKERR, UVIO timeout, or UVCC timeout (if failsafe is enabled)
22	UVDD	R/WC	1'b0	Under Voltage on V_{DD}. This flag cannot be cleared until the fault is gone.
21	UVIO	R/WC	1'b0	Under Voltage for V_{IO}
20	PWRON	R/WC/U	1'b1	Power On Reset interrupt
19	TSD	R/WC	1'b0	Thermal Shutdown
18	RSVD	R	1'b0	Reserved
17	UVCC	R/WC	1'b0	Under Voltage on V_{CC}. This flag cannot be cleared until the fault is gone.
16	ECCERR	R/WC	1'b0	Uncorrectable ECC error detected
15	CANINT	R/WC	1'b0	Can Bus Wake Up Interrupt
14	RSVD	R	1'b0	Reserved
13	WKERR	R/WC	1'b0	Wake Error
12	RSVD	R	1'b0	Reserved

Table 9-22. Interrupts Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CRCERR_INT	R/WC	1'b0	Internal EEPROM CRC error detected
10	CANSLNT	R/WC	1'b0	CAN Silent
9	RSVD	R	1'b0	Reserved
8	CANDOM	R/WC	1'b0	CAN Stuck Dominant
7	GLOBALERR	R	1'b0	Global Error (Any Fault)
6	WKRQ	R	1'b0	Wake Request
5	CANERR	R	1'b0	CAN Error
4	CBF	R	1'b0	CAN Bus Fault
3	SPIERR	R	1'b0	SPI Error
2	RSVD	R	1'b0	Reserved
1	M_CAN_INT	R	1'b0	M_CAN global INT
0	VT	R	1'b0	Global Voltage, Temp or ECC errors

GLOBALERR: Logical OR of all faults/interrupts in registers 0x0820-0824.

WKRQ: Logical OR of CANINT, and WKERR.

CANBUSNOM is not an interrupt but a flag. In normal mode after the first dominant-recessive transition it sets. It resets to 0 when entering Standby or Sleep modes or when a bus fault condition takes place in normal mode.

CANERR: Logical OR of CANSLNT and CANDOM faults.

CBF: Logical OR of CANBUSTERMOPEN, CANHCANL, CANHVDD, CANLGND, CANBUSOPEN, CANBUSGND, and CANBUSVDD faults.

SPIERR: Will be set if any of the SPI status register 16'h000C[30:16] is set.

- In the event of a SPI underflow, the error is not detected/alerted until the start of the next SPI transaction.
- 16'h0010[30:16] are the mask for these errors

VT: Logical or of UV_{CC}, UV_{DD}, UV_{IO}, TSD, and ECCERR.

CANINT: Indicates a WUP has occurred; Flag can be cleared by changing to Normal or Sleep modes.

WKERR: If the device receives a wake up request WUP and does not transition to Normal mode or clear the PWRON or Wake flag before $t_{INACTIVE}$, the device transitions to Sleep Mode. After the wake event, a Wake Error (WKERR) will be reported and the SMS flag will be set to 1.

Note

PWRON Flag is cleared by either writing a 1 or by going to sleep mode or normal mode from standby mode.

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9.3.2 MCAN Interrupts (address = h0824) [reset = h00000000]

Note

Bits in the interrupt register will be set, even if the corresponding interrupt enable (IE) register bits are not enabled. However, if the IE bits are not set, the interrupt bit does not cause nINT to get deasserted.

Figure 9-19. MCAN Interrupts

31	30	29	28	27	26	25	24
RSVD		ARA	PED	PEA	WDI	BO	EW
R		R	R	R	R	R	R
23	22	21	20	19	18	17	16
EP	ELO	BEU	BEC	DRX	TOO	MRAF	TSW
R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
TEFL	TEFF	TEFW	TEFN	TFE	TCF	TC	HPM
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
RF1L	RF1F	RF1W	RF1N	RF0L	RF0F	RF0W	RF0N
R	R	R	R	R	R	R	R

Table 9-23. MCAN Interrupts Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RSVD	R	1'b0	Reserved
29	ARA	R	1'b0	ARA: Access to Reserved Address
28	PED	R	1'b0	PED: Protocol Error in Data Phase (Data Bit Time is used)
27	PEA	R	1'b0	PEA: Protocol Error in Arbitration Phase (Nominal Bit Time is used)
26	WDI	R	1'b0	WDI: Watchdog Interrupt
25	BO	R	1'b0	BO: Bus_Off Status
24	EW	R	1'b0	EW: Warning Status
23	EP	R	1'b0	EP: Error Passive
22	ELO	R	1'b0	ELO: Error Logging Overflow
21	BEU	R	1'b0	BEU: Bit Error Uncorrected
20	BEC	R	1'b0	BEC: Bit Error Corrected
19	DRX	R	1'b0	DRX: Message stored to Dedicated Rx Buffer
18	TOO	R	1'b0	TOO: Timeout Occurred
17	MRAF	R	1'b0	MRAF: Message RAM Access Failure
16	TSW	R	1'b0	TSW: Timestamp Wraparound
15	TEFL	R	1'b0	TEFL: Tx Event FIFO Element Lost
14	TEFF	R	1'b0	TEFF: Tx Event FIFO Full
13	TEFW	R	1'b0	TEFW: Tx Event FIFO Watermark Reached
12	TEFN	R	1'b0	TEFN: Tx Event FIFO New Entry
11	TFE	R	1'b0	TFE: Tx FIFO Empty
10	TCF	R	1'b0	TCF: Transmission Cancellation Finished
9	TC	R	1'b0	TC: Transmission Completed
8	HPM	R	1'b0	HPM: High Priority Message
7	RF1L	R	1'b0	RF1L: Rx FIFO 1 Message Lost
6	RF1F	R	1'b0	RF1F: Rx FIFO 1 Full

Table 9-23. MCAN Interrupts Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	RF1W	R	1'b0	RF1W: Rx FIFO 1 Watermark Reached
4	RF1N	R	1'b0	RF1N: Rx FIFO 1 New Message
3	RF0L	R	1'b0	RF0L: Rx FIFO 0 Message Lost
2	RF0F	R	1'b0	RF0F: Rx FIFO 0 Full
1	RF0W	R	1'b0	RF0W: Rx FIFO 0 Watermark Reached
0	RF0N	R	1'b0	RF0N: Rx FIFO 0 New Message

9.3.3 Interrupt Enables (address = h0830) [reset = hFFFFFFFF]

Figure 9-20. 32-bit, 4 Rows

31	30	29	28	27	26	25	24
RSVD	CANBUSTERMOPEN	CANHCANL	CANHVDD	CANLGND	CANBUSOPEN	CANBUSGND	CANBUSVDD
R	R	R	R	R	R	R	R
23	22	21	20	19	18	17	16
RSVD	UVDD	UVIO	RSVD	TSD	RSVD	UVCC	ECCERR
R	R/W	R/W	R	R/W	R	R	R/W
15	14	13	12	11	10	9	8
CANINT	RSVD				CANSLNT	RSVD	CANDOM
R/W	R				R/W	R	R
7	6	5	4	3	2	1	0
RSVD							
R							

Table 9-24. Interrupt Enables Field Descriptions

Bit	Field	Type	Reset	Description
31	RSVD	R	1'b1	Reserved
30	CANBUSTERMOPEN	R/W	1'b1	CAN Bus has one termination point open detection enable
29	CANHCANL	R/W	1'b1	CANH and CANL short detection enable
28	CANHVDD	R/W	1'b1	CANH short to V_{DD} detection enable
27	CANLGND	R/W	1'b1	CANL short to GND detection enable
26	CANBUSOPEN	R/W	1'b1	CAN bus open detection enable
25	CANBUSGND	R/W	1'b1	CANH short to GND or both CANH & CANL short to GND detection enable
24	CANBUSVDD	R/W	1'b1	CANH short to V_{DD} or both CANH and CANL short to V_{DD} detection enable
23	RSVD	R	1'b1	Reserved
22	UVDD	R/W	1'b1	Under Voltage V_{DD}
21	UVIO	R/W	1'b1	Under Voltage V_{IO}
20	RSVD	R	1'b1	Reserved
19	TSD	R/W	1'b1	Thermal Shutdown
18	RSVD	R	1'b1	Reserved
17	UVCC	R/W	1'b1	Under Voltage V_{CC}
16	ECCERR	R/W	1'b1	Uncorrectable ECC error detected
15	CANINT	R/W	1'b1	Can Bus Wake Up Interrupt
14:11	RSVD	R	4'b1111	Reserved
10	CANSLNT	R/W	1'b1	CAN Silent
9	RSVD	R	1'b1	Reserved
8	CANDOM	R/W	1'b1	CAN Stuck Dominant
7:0	RSVD	R	8'hFF	Reserved

9.4 CAN_CONTROLLER Registers

Section 9.4 lists the memory-mapped registers for the CAN_Controller registers. All register offset addresses not listed in Section 9.4 must be considered as reserved locations and the register contents must not be modified.

CAN Controller

Table 9-25. CAN_CONTROLLER Registers

Address	Acronym	Register Name	Section
0x1000	CREL	Core Release Register	Section 9.4.1
0x1004	ENDN	Endian Register	Section 9.4.2
0x100C	DBTP	Data Bit Timing and Prescaler Register	Section 9.4.3
0x1010	TEST	Test Register	Section 9.4.4
0x1014	RWD	RAM Watchdog	Section 9.4.5
0x1018	CCCR	CC Control Register	Section 9.4.6
0x101C	NBTP	Nominal Bit Timing and Prescaler Register	Section 9.4.7
0x1020	TSCC	Timestamp Counter Configuration	Section 9.4.8
0x1024	TSCV	Timestamp Counter Value	Section 9.4.9
0x1028	TOCC	Timeout Counter Configuration	Section 9.4.10
0x102C	TOCV	Timeout Counter Value	Section 9.4.11
0x1040	ECR	Error Counter Register	Section 9.4.12
0x1044	PSR	Protocol Status Register	Section 9.4.13
0x1048	TDCR	Transmitter Delay Compensation Register	Section 9.4.14
0x1050	IR	Interrupt Register	Section 9.4.15
0x1054	IE	Interrupt Enable	Section 9.4.16
0x1058	ILS	Interrupt Line Select	Section 9.4.17
0x105C	ILE	Interrupt Line Enable	Section 9.4.18
0x1080	GFC	Global Filter Configuration	Section 9.4.19
0x1084	SIDFC	Standard ID Filter Configuration	Section 9.4.20
0x1088	XIDFC	Extended ID Filter Configuration	Section 9.4.21
0x1090	XIDAM	Extended ID and Mask	Section 9.4.22
0x1094	HPMS	High Priority Message Status	Section 9.4.23
0x1098	NDAT1	New Data 1	Section 9.4.24
0x109C	NDAT2	New Data 2	Section 9.4.25
0x10A0	RXF0C	Rx FIFO 0 Configuration	Section 9.4.26
0x10A4	RXF0S	Rx FIFO 0 Status	Section 9.4.27
0x10A8	RXF0A	Rx FIFO 0 Acknowledge	Section 9.4.28
0x10AC	RXBC	RX Buffer Configuration	Section 9.4.29
0x10B0	RXF1C	Rx FIFO 1 Configuration	Section 9.4.30
0x10B4	RXF1S	Rx FIFO 1 Status	Section 9.4.31
0x10B8	RXF1A	Rx FIFO 1 Acknowledge	Section 9.4.32
0x10BC	RXESC	Rx Buffer/FIFO Element Size Configuration	Section 9.4.33
0x10C0	TXBC	Tx Buffer Configuration	Section 9.4.34
0x10C4	TXFQS	Tx FIFO/Queue Status	Section 9.4.35
0x10C8	TXESC	Tx Buffer Element Size Configuration	Section 9.4.36
0x10CC	TXBRP	Tx Buffer Request Pending	Section 9.4.37
0x10D0	TXBAR	Tx Buffer Add Request	Section 9.4.38
0x10D4	TXBCR	Tx Buffer Cancellation Request	Section 9.4.39
0x10D8	TXBTO	Tx Buffer Transmission Occurred	Section 9.4.40
0x10DC	TXBCF	Tx Buffer Cancellation Finished	Section 9.4.41
0x10E0	TXBTIE	Tx Buffer Transmission Interupt Enable	Section 9.4.42
0x10E4	TXBCIE	Tx Buffer Cancellation Finished Interrupt Enable	Section 9.4.43
0x10F0	TXEFC	Tx Event FIFO Configuration	Section 9.4.44
0x10F4	TXEFS	Tx Event FIFO Status	Section 9.4.45
0x10F8	TXEFA	Tx Event FIFO Acknowledge	Section 9.4.46

Complex bit access types are encoded to fit into small table cells. Section 9.4 shows the codes that are used for access types in this section.

Table 9-26. CAN_Controller Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read

Table 9-26. CAN_Controller Access Type Codes (continued)

Access Type	Code	Description
R0	R	Read
RC	R C	Read to Clear
RH	R H	Read Set or cleared by hardware
RS	R S	Read to Set
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
W1S	W 1S	Write 1 to set
WP	W P	Write Requires privileged access
Reset or Default Value		
-n		Value after reset or the default value

9.4.1 CREL Register (Address = 0x1000) [Reset = 0x32380608]

CREL is shown in Figure 9-21 and described in Table 9-27.

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Figure 9-21. CREL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
REL				STEP				SUBSTEP				YEAR			
R-0x3				R-0x2				R-0x3				R-0x8			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MONTH								DAY							
R-0x6								R-0x8							

Table 9-27. CREL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	REL	R	0x3	One digit, BCD-coded
27-24	STEP	R	0x2	One digit, BCD-coded
23-20	SUBSTEP	R	0x3	One digit, BCD-coded
19-16	YEAR	R	0x8	One digit, BCD-coded
15-8	MONTH	R	0x6	Two Digits, BCD-coded
7-0	DAY	R	0x8	Two Digits, BCD-coded

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9.4.2 ENDN Register (Address = 0x1004) [Reset = 0x87654321]

ENDN is shown in Figure 9-22 and described in Table 9-28.

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Figure 9-22. ENDN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ETV_31:24								ETV_23:16							
R-0x87								R-0x65							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ETV_15:8								ETV_7:0							
R-0x43								R-0x21							

Table 9-28. ENDN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	ETV_31:24	R	0x87	Endianness Test Value
23-16	ETV_23:16	R	0x65	Endianness Test Value
15-8	ETV_15:8	R	0x43	Endianness Test Value
7-0	ETV_7:0	R	0x21	Endianness Test Value

9.4.3 DBTP Register (Address = 0x100C) [Reset = 0x00000A33]

DBTP is shown in Figure 9-23 and described in Table 9-29.

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Data phase bit timing configuration

Note

The bit rate configured for the CAN FD data phase via DBTP must be higher or equal to the bit rate configured for the arbitration phase via NBTP.

Figure 9-23. DBTP Register

31	30	29	28	27	26	25	24
RESERVED							
R-0x0							
23	22	21	20	19	18	17	16
TDC	RESERVED		DBRP				
R/WP-0x0	R-0x0		R/WP-0x0				
15	14	13	12	11	10	9	8
RESERVED			DTSEG1				
R-0x0			R/WP-0xA				
7	6	5	4	3	2	1	0
DTSEG2				DSJW			
R/WP-0x3				R/WP-0x3			

Table 9-29. DBTP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0x0	Reserved
23	TDC	R/WP	0x0	Transmitter Delay Compensation 0x0 = TDC Disabled 0x1 = TDC Enabled
22-21	RESERVED	R	0x0	Reserved
20-16	DBRP	R/WP	0x0	Data Bit Rate Prescaler: The value by which the oscillator frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid values for the Bit Rate Prescaler are 0 to 31. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.
15-13	RESERVED	R	0x0	Reserved
12-8	DTSEG1	R/WP	0xA	Data time segment before sample point: Valid values are 0 to 31. The actual interpretation by the hardware of this value is such that one more than the programmed value is used.
7-4	DTSEG2	R/WP	0x3	Data time segment after sample point: Valid values are 0 to 15. The actual interpretation by the hardware of this value is such that one more than the programmed value is used.
3-0	DSJW	R/WP	0x3	Data (Re)synchronization Jump Width: Valid values are 0 to 15. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.

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9.4.4 TEST Register (Address = 0x1010) [Reset = 0x00000000]

TEST is shown in Figure 9-24 and described in Table 9-30.

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Write access to the Test Register has to be enabled by setting bit CCCR.TEST to '1'. All test register functions are set to their reset values when bit CCCR.TEST is reset.

Figure 9-24. TEST Register

31	30	29	28	27	26	25	24
RESERVED							
R-0x0							
23	22	21	20	19	18	17	16
RESERVED							
R-0x0							
15	14	13	12	11	10	9	8
RESERVED							
R-0x0							
7	6	5	4	3	2	1	0
RX	RESERVED		LBCK	RESERVED			
RH-0x0	R-0x0		R/WP-0x0	R-0x0			

Table 9-30. TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0x0	Reserved
7	RX	RH	0x0	Receive Pin: Monitors the actual value of the MCAN RX pin
6-5	RESERVED	R	0x0	
4	LBCK	R/WP	0x0	Loop Back Mode: See CAN lookback mode section for more information 0x0 = Reset value, loop back mode is disabled 0x1 = Loop back mode is enabled
3-0	RESERVED	R	0x0	Reserved

9.4.5 RWD Register (Address = 0x1014) [Reset = 0x00000000]

RWD is shown in Figure 9-25 and described in Table 9-31.

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The RAM Watchdog monitors the READY output of the Message RAM. A Message RAM access via the M_CAN's generic Master Interface starts the Message RAM Watchdog Counter with the value configured by RWD.WDC. The counter is reloaded with RWD.WDC when the Message RAM signals successful completion by activating its READY output. In case there is no resposne from the Message RAM until the counter has counted down to zero, the counter stops and interrupt flag IR.WDI is set. The RAM Watchdog Counter is clocked by the host clock.

Figure 9-25. RWD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																WDV								WDC							
R-0x0																R-0x0								R/WP-0x0							

Table 9-31. RWD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0x0	Reserved
15-8	WDV	R	0x0	Actual Message RAM Counter value
7-0	WDC	R/WP	0x0	Start value of the Message RAM Watchdog Counter. With the reset value of "0", the counter is disabled.

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9.4.6 CCCR Register (Address = 0x1018) [Reset = 0x00000001]

CCCR is shown in Figure 9-26 and described in Table 9-32.

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Figure 9-26. CCCR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0x0							
23	22	21	20	19	18	17	16
RESERVED							
R-0x0							
15	14	13	12	11	10	9	8
NISO	TXP	EFBI	PXHD	RESERVED		BRSE	FDOE
R/WP-0x0	R/WP-0x0	R/WP-0x0	R/WP-0x0	R-0x0		R/WP-0x0	R/WP-0x0
7	6	5	4	3	2	1	0
TEST	DAR	MON	CSR	CSA	ASM	CCE	INIT
R/WP-0x0	R/WP-0x0	R/WP-0x0	R/WP-0x0	R-0x0	R/WP-0x0	R/WP-0x0	R/W-0x1

Table 9-32. CCCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0x0	Reserved
15	NISO	R/WP	0x0	Non-ISO Operation 0x0 = CAN FD Frame format according to ISO 11898-1:2015 0b1 = CAN FD Frame format according to Bosch CAN FD Specification V1.0
14	TXP	R/WP	0x0	Transmitter Pause: If this bit is set, the M_CAN pauses for two CAN bit times before starting the next transmission after itself has successfully transmitted a frame. 0x0 = Transmit pause disabled 0x1 = Transmit pause enabled
13	EFBI	R/WP	0x0	Edge Filtering during Bus Integration 0x0 = Edge filtering disabled 0x1 = Two consecutive dominant time quanta required to detect an edge for hard synchronization.
12	PXHD	R/WP	0x0	Protocol Exception Handling Disable. **Note** When protocol exception handling is disabled, the M_CAN will transmit an error frame when it detects a protocol exception condtiion (unless CAN FD Light mode is enabled) 0x0 = Protocol excepetion handling enabled 0x1 = Protocol exception handling disabled
11-10	RESERVED	R	0x0	Reserved

9	BRSE	R/WP	0x0	Bit Rate Switch Enable #NOTE#When CAN FD Operation is disabled (FDOE = 0)#/NOTE#
				0x0 = Bit rate switching for transmissions disabled
				0x1 = Bit rate switching for transmissions are enabled

8	FDOE	R/WP	0x0	FD Operation Enable 0x0 = FD operation disabled 0x1 = FD operation enabled
7	TEST	R/WP	0x0	Test Mode Enable 0x0 = Normal operation, TEST register holds reset values 0x1 = Test mode, write access to TEST register is enabled

Table 9-32. CCCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DAR	R/WP	0x0	Disable Automatic Retransmission 0x0 = Automatic retransmission of messages not transmitted successfully enabled 0x1 = Automatic retransmission disabled
5	MON	R/WP	0x0	Bus Monitoring Enable 0x0 = Bus monitoring mode is disabled 0x1 = Bus monitoring is enabled
4	CSR	R/WP	0x0	Clock Stop Request #NOTE#The device handles stop request through hardware. In standby mode, the clock stop request is set automatically. The user must make sure to write 0 to this bit if they do not want the clock stop request while doing a read-modify-write#/NOTE# 0x0 = No clock stop is requested 0x1 = Clock stop requested. When clock stop is requeested, first INIT and then CSA will be set after all pending transfer requests have been completed and the CAN bus reached idle.
3	CSA	R	0x0	Clock Stop Ackowledge 0x0 = No clock stop is requested 0x1 = M_CAN clock request is acknowledged and can clocks can be stopped (internally handled)
2	ASM	R/WP	0x0	Restricted Operation Mode: This bit can only be set by the host when both CCE and INIT are set to 1. This bet can reset by the host at any time. 0x0 = Normal CAN operation 0x1 = Restricted operation mode active

1	CCE	R/WP	0x0	Configuration Change Enable #NOTE#The CCE bit allows access to protected bits in the MCAN register space (0x1000-0x10F8)#/NOTE#
				0x0 = Host has no write access to the protected configuration registers
				0x1 = Host has write access to the protected configuration registers (Requires CCCR.INIT to be set to 1 to set this to 1)

0	INIT	R/W	0x1	Initialization: MCAN is held in a "reset" state#NOTE#When the device is placed in standby mode, the INIT bit is set by hardware#/NOTE# 0x0 = Normal Operation 0x1 = Initialization mode (needed to set CCCR.CCE to 1)

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9.4.7 NBTP Register (Address = 0x101C) [Reset = 0x06000A03]

NBTP is shown in Figure 9-27 and described in Table 9-33.

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Figure 9-27. NBTP Register

31	30	29	28	27	26	25	24
NSJW							NBRP
R/WP-0x3							R/WP-0x0
23	22	21	20	19	18	17	16
NBRP							
R/WP-0x0							
15	14	13	12	11	10	9	8
NTSEG1							
R/WP-0xA							
7	6	5	4	3	2	1	0
RESERVED	NTSEG2						
R-0x0	-0						

Table 9-33. NBTP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	NSJW	R/WP	0x3	Nominal (Re)synchronization jump width. Valid values are 0 to 127. The actual interpretation by the hardware is 1 more than the value programmed here
24-16	NBRP	R/WP	0x0	Nominal Bit Rate Prescaler: The value by which the oscillator frequency is divided for generating the bit time quanta. Valid values are 0 to 511. The actual interpretation by the hardware is 1 more than the value programmed here
15-8	NTSEG1	R/WP	0xA	Nominal Time Segment Before Sample Point. Valid values are 1 to 255. The actual interpretation by the hardware is 1 more than the value programmed here
7	RESERVED	R	0x0	Reserved
6-0	NTSEG2	0x0	Nominal Time Segment After Sample Point. Valid values are 1 to 127. The actual interpretation by the hardware is 1 more than the value programmed here	

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9.4.8 TSCC Register (Address = 0x1020) [Reset = 0x00000000]

TSCC is shown in Figure 9-28 and described in Table 9-34.

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Figure 9-28. TSCC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												TCP			
R-0x0												R/WP-0x0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														TSS	
R-0x0														R/WP-0x0	

Table 9-34. TSCC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0x0	Reserved
19-16	TCP	R/WP	0x0	Timestamp Counter Prescaler Valid values: 0x0 - 0xF: Configures the timestamp and timeout counters time unit in multiples of CAN bit times [1 &16]
15-2	RESERVED	R	0x0	Reserved
1-0	TSS	R/WP	0x0	Timestamp Select 0x0 = Timestamp counter value is always 0x0000 0x1 = Timestamp counter value is incremented according to TCP bit prescaler 0x2 = External timestamp counter value is used (same as device) 0x3 = Same as 0b00 configuration

9.4.9 TSCV Register (Address = 0x1024) [Reset = 0x00000000]

TSCV is shown in Figure 9-29 and described in Table 9-35.

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Figure 9-29. TSCV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TSC															
R-0x0																R/W1C-0x0															

Table 9-35. TSCV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0x0	Reserved
15-0	TSC	R/W1C	0x0	Timestamp Counter Value The internal/external timestamp counter value is captured on the start of frame (both RX and TX). When TSCC.TSS = 0b01, th etimestamp counter is incremented in multiples of CAN bit times [1 &16] depending on the configuration of TSCC.TCP. A wrap around sets interrupt flag IR.TSW. Write access resets the counter to zero. When TSCC.TSS = '0b10', TSC reflects the external timestamp counter value, and write access has no impact.

9.4.10 TOCC Register (Address = 0x1028) [Reset = 0xFFFF0000]

TOCC is shown in Figure 9-30 and described in Table 9-36.

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Figure 9-30. TOCC Register

31	30	29	28	27	26	25	24
TOP							
R/WP-0xFFFF							
23	22	21	20	19	18	17	16
TOP							
R/WP-0xFFFF							
15	14	13	12	11	10	9	8
RESERVED							
R-0x0							
7	6	5	4	3	2	1	0
RESERVED					TOS		ETOC
R-0x0					R/WP-0x0		R/WP-0x0

Table 9-36. TOCC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TOP	R/WP	0xFFFF	Timeout Period The start value of the timeout counter (down-counter). Configured the timeout period
15-3	RESERVED	R	0x0	Reserved
2-1	TOS	R/WP	0x0	Timeout Select When operating in Continuous mode, a write to TOCV presets the counter to the value configuration by TOCC.TOP and continues down-counting. When the Timeout Counter is controlled by one of the FIFOs, an empty FIFO presets the counter to the value configured by TOCC.TOP. Down-counting is started when the first FIFO element is stored. 0x0 = Continuous Operation 0b01 Timeout controlled by TX Event FIFO 0x2 = Timeout controlled by RX FIFO 0 0x3 = Timeout controlled by RX FIFO 1
0	ETOC	R/WP	0x0	Enable Timeout Counter 0x0 = Timeout counter disabled 0x1 = Timeout counter enabled

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9.4.11 TOCV Register (Address = 0x102C) [Reset = 0x0000FFFF]

TOCV is shown in Figure 9-31 and described in Table 9-37.

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Figure 9-31. TOCV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TOC															
R-0x0																R/W1C-0xFFFF															

Table 9-37. TOCV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0x0	Reserved
15-0	TOC	R/W1C	0xFFFF	Timeout Counter The timeout counter is decremented in multiples of CAN bit times [1 &16]

9.4.12 ECR Register (Address = 0x1040) [Reset = 0x00000000]

ECR is shown in Figure 9-32 and described in Table 9-38.

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Figure 9-32. ECR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								CEL							
R-0x0								RC-0x0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RP	REC							TEC							
R-0x0	R-0x0							R-0x0							

Table 9-38. ECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0x0	Reserved
23-16	CEL	RC	0x0	CAN Error Logging The counter is cremented each time when a CAN protocol error causes the Transmit Error Counter or the Receive Error Counter to be incremented. It is reset by the read access to CEL. The Counter stops at 0xFF, and the next increment of TEC or REC sets the interrupt flag IR.ELO
15	RP	R	0x0	Receive Error Passive 0x0 = The Receive Error Counter is below the error passive level of 128 0x1 = The Receive Error Counter has reached the error passive level of 128
14-8	REC	R	0x0	Actual State of Receive Error Counter, values between 0 and 127
7-0	TEC	R	0x0	Actual State of Transmit Error Counter, values between 0 and 255

9.4.13 PSR Register (Address = 0x1044) [Reset = 0x00000707]

PSR is shown in Figure 9-33 and described in Table 9-39.

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Note

When a frame in CAN FD format has reached the data phase with BRS flag set, the next CAN event (error or valid frame) will be shown in DLEC instead of LEC. An error in a fixed stuff bit of a CAN FD CRC sequence will be shown as a Form Error, not Stuff Error. The Bus_Off recovery sequence (see ISO 11898-1:2015) cannot be shortened by setting or resetting CCCR.INIT. If the device goes Bus_Off, it will set CCCR.INIT of its own accord, stopping all bus activities. Once CCCR.INIT has been cleared by the CPU, the device will then wait for 129 occurrences of Bus Idle (129 * 11 consecutive recessive bits) before resuming normal operation. At the end of the Bus_Off recovery sequence, the Error Management Counters will be reset. During the waiting time after the resetting of CCCR.INIT, each time a sequence of 11 recessive bits has been monitored, a Bit0Error code is written to PSR.LEC, enabling the CPU to readily checkup whether the CAN bus is stuck at dominant or continuously disturbed and to monitor the Bus_Off recovery sequence. ECR.REC is used to count these sequences.

Figure 9-33. PSR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0x0							
23	22	21	20	19	18	17	16
RESERVED	TDCV						
R-0x0	R-0x0						
15	14	13	12	11	10	9	8
RESERVED	PXE	RFDF	RBRS	RESI	DLEC		
R-0x0	RC-0x0	RC-0x0	RC-0x0	RC-0x0	RS-0x7		
7	6	5	4	3	2	1	0
BO	EW	EP	ACT		LEC		
R-0x0	R-0x0	R-0x0	R-0x0		RS-0x7		

Table 9-39. PSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R	0x0	Reserved
22-16	TDCV	R	0x0	Transmitter Delay Compensation Value 0x00-0x7F - Position of the secondary sample point, defined by the sum of the measured delay from m_can_tx to m_can_rx and TDCR.TDCO. The SSP position is, in the data phase, the number of tq between the start of the transmitted bit and the secondary sample point. Valid values are 0 to 127
15	RESERVED	R	0x0	Reserved
14	PXE	RC	0x0	Protocol Exception Event 0x0 = No protocol exception event occurred since last read access 0x1 = Protocol exception event occurred
13	RFDF	RC	0x0	Received a CAN FD Message This bit is set regardless of acceptance filtering 0x0 = Since this bit was reset by the CPU, no CAN FD message has been received 0x1 = Message in CAN FD format with FDF flag set has been received
12	RBRS	RC	0x0	BRS flag of last received CAN FD Message This bit is set together with RFDF, independent of acceptance filtering 0x0 = Last received CAN FD message did not have its BRS flag set 0x1 = Last received CAN FD message had its BRS flag set

Table 9-39. PSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	RESI	RC	0x0	ESI Flag of last received CAN FD Message This bit is set together with RFDF, independent of acceptance filtering 0x0 = Last received CAN FD message did not have its ESI flag set 0x1 = Last received CAN FD message had its ESI flag set
10-8	DLEC	RS	0x7	Type of last error that occurred in the data phase of a CAN FD format frame with its BRS flag set. This field will be cleared to zero when a CAN FD format frame with its BRS flag set has been received or transmitted without error. This field has the same values as the LEC field.
7	BO	R	0x0	Bus Off 0x0 = The M_CAN is not Bus_Off 0x1 = The M_CAN is in Bus_Off state
6	EW	R	0x0	Error Warning 0x0 = Both error counters are below the Error_Warning limit of 96 0x1 = At least one of the error counters has reached the Error_Warning limit of 96
5	EP	R	0x0	Error Passive 0x0 = The M_CAN is in the Error_Active State. It normally takes part in bus communication and sends an active error flag when an error has been detected 0x1 = The M_CAN is in the Error_Passive state
4-3	ACT	R	0x0	Activity Monitors the module's CAN communication state 0x0 = Synchronizing - Node is synchronizing on CAN communication 0x1 = Idle - node is neither receiver nor transmitter 0x2 = Receiver - node is operating as a receiver 0b11 - Transmitter - node is operating as a transmitter

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Table 9-39. PSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	LEC	RS	0x7	Type of last error that occurred on the CAN bus. This field will be cleared to zero when a message has been received or transmitted without error **Note** When a frame in CAN FD format has reached the data phase with the BRS flag set, the next CAN event (error or valid frame) will be shown in the DLEC instead of LEC. An error in a fixed stuff bit of a CAN FD CRC sequence will be shown as a Form Error, not Stuff Error. **Note** The Bus_Off recovery sequence (see ISO 11898-1:2015) cannot be shortned by setting or resetting CCCR.INIT. If the device goes Bus_Off, it will set the CCCR.INIT of its own accord, stopping all bus activities. Once CCCR.INIT has been cleared by the CPU, the device will then wait for 129 occurrences of Bus Idle (129 * 11 consecutive recessive bits) before resuming normal operation. At the end of the Bus_Off recovery sequence, the Error Management Counters will be reset. During the waiting time after the resetting of CCCR.INIT, each time a sequence of 11 recessive bits has been monitored, a Bit0Error code is written to PSR.LEC, enabling the CPU to readily check up whether the CAN bus is stuck at dominant or continuously disturbed and to monitor the Bus_Off recovery sequence. ECR.REC is used to count these sequences. 0x0 = No Error - No error occurred since DLEC has been reset by a successful reception or transmission 0x1 = Stuff Error - More than 5 equal bits in a sequence have occurred in a part of a received message where this is not allowed 0x2 = Form Error - A fixed format part of a received frame has the wrong format 0x3 = AckError - The message transmitted by the M_CAN was not acknowledged by another node 0x4 = Bit1Error - During the transmission of a message (with the exception of the arbitration field), the device wanted to send a recessive level (bit of logical value '1'), but the monitored bus value was dominant 0x5 = Bit0Error - During the transmission of a message (or acknowledge bit, or active error flag, or overload flat), the device wanted to send a dominant level (data or identifier bit logical value '0'), but the monitored bus value was recessive. During Bus_Off recovery this status is set each time a sequence of 11 recessive bits has been monitored. This enables the CPU to monitor the proceeding of the Bus_Off recovery sequence (indicating the bus is not stuck at dominant or continuously disturbed).

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9.4.14 TDCR Register (Address = 0x1048) [Reset = 0x00000000]

TDCR is shown in Figure 9-34 and described in Table 9-40.

Return to the Summary Table.

Figure 9-34. TDCR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0x0							
23	22	21	20	19	18	17	16
RESERVED							
R-0x0							
15	14	13	12	11	10	9	8
RESERVED	TDCO						
R-0x0	R/WP-0x0						
7	6	5	4	3	2	1	0
RESERVED	TDCF						
R-0x0	R/WP-0x0						

Table 9-40. TDCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0x0	Reserved
14-8	TDCO	R/WP	0x0	Transmitter Delay Compensation Offset Offset value defining the distance between the measured delay from m_can_tx to m_can_rx and the secondary sample point. Vlaid values are 0 to 127 tq
7	RESERVED	R	0x0	Reserved
6-0	TDCF	R/WP	0x0	Transmitter Delay Compensation Filter Window Length Defines the minimum value for the SSP position, dominant edges on m_can_rx that would result in an earlier SSP position are ignored for transmitter delay measurement. The feature is enabled when TDCF is configured to a value greater than TDCO. Valid values are 0 to 127 mtq

9.4.15 IR Register (Address = 0x1050) [Reset = 0x00000000]

IR is shown in Figure 9-35 and described in Table 9-41.

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Figure 9-35. IR Register

31	30	29	28	27	26	25	24
RESERVED		ARA	PED	PEA	WDI	BO	EW
R-0x0		R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0
23	22	21	20	19	18	17	16
EP	ELO	BEU	BEC	DRX	TOO	MRAF	TSW
R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0
15	14	13	12	11	10	9	8
TEFL	TEFF	TEFW	TEFN	TCE	TCF	TC	HPM
R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0
7	6	5	4	3	2	1	0
RF1L	RF1F	RF1W	RF1N	RF0L	RF0F	RF0W	RF0N
R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0

Table 9-41. IR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0x0	Reserved
29	ARA	R/W1C	0x0	Access to Reserved Address 0x0 = No access to reserved address occurred 0x1 = Access to reserved address occurred
28	PED	R/W1C	0x0	Protocol Error in Data Phase (Data Bit Time is Used) 0x0 = No protocol error in data phase
27	PEA	R/W1C	0x0	Protocol Error in Arbitration Phase (Nominal Bit Time is used) 0x0 = No protocol error in arbitration phase
26	WDI	R/W1C	0x0	Watchdog Interrupt 0x0 = No message RAM watchdog event occurred 0x1 = Message RAM watchdog event due to missing READY
25	BO	R/W1C	0x0	Bus_Off Status 0x0 = Bus_Off status unchanged 0x1 = Bus_Off status changed
24	EW	R/W1C	0x0	Warning Status 0x0 = Error_Warning status unchanged 0x1 = Error_Warning status changed
23	EP	R/W1C	0x0	Error Passive 0x0 = Error_Passive status unchanged 0x1 = Error_Passive status changed
22	ELO	R/W1C	0x0	Error Logging Overflow 0x0 = CAN Error Logging Counter did not overflow 0x1 = Overflow of CAN Error Logging Counter occurred
21	BEU	R/W1C	0x0	Bit Error Uncorrected Message RAM bit error detected, uncorrected. Controlled by the ECC logic attached to the message RAM. An uncorrected Message RAM bit error sets CCCR.INIT to '1'. This is done to avoid transmission of corrupted data. 0x0 = No bit error detected when reading from Message RAM 0x1 = Bit error detected, uncorrected
20	BEC	R/W1C	0x0	Message RAM bit error detected and corrected. Controlled by external ECC logic attached to the Message RAM 0x0 = No bit error detected when reading from Message RAM 0x1 = Bit error detected, corrected

Table 9-41. IR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	DRX	R/W1C	0x0	Message Stored to Dedicated Rx Buffer The flag is set whenever a received message has been stored into a dedicated Rx Buffer 0x0 = No Rx Buffer updated 0x1 = At least one received message stored into an Rx Buffer
18	TOO	R/W1C	0x0	Timeout Occurred 0x0 = No timeout 0x1 = Timeout reached
17	MRAF	R/W1C	0x0	Message RAM Access Failure The flag is set when the Rx Handler has not completed acceptance filtering or storage of an accepted message until the arbitration field of the following message has been received. In this case, acceptance filtering or message storage is aborted and the Rx Handler starts processing of the following message. It is also set if the Rx Handler was not able to write to a message to the Message RAM. In this case, message storage is aborted. In both cases, the FIFO put index is not updated. The flag is also set when the Tx Handler was not able to read a message from the Message RAM in time. In this case, message transmission is aborted. In case of a Tx Handler access failure, the M_CAN is switched into restricted operation mode. TO leave restricted operation mode, the host CPU has to reset CCCR.ASM. 0x0 = No Message RAM access failure occurred 0x1 = Message RAM access failure occurred
16	TSW	R/W1C	0x0	Timestamp Wraparound 0x0 = No timestamp counter wrap-around 0x1 = Timestamp counter wrapped around
15	TEFL	R/W1C	0x0	Tx Event FIFO Element Lost 0x0 = No Tx Event FIFO element lost 0x1 = Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero
14	TEFF	R/W1C	0x0	Tx Event FIFO Full 0x0 = Tx Event FIFO not full 0x1 = Tx Event FIFO is full
13	TEFW	R/W1C	0x0	Tx Event FIFO Watermark Reached 0x0 = Tx Event FIFO fill level below watermark 0x1 = Tx Event FIFO fill level has reached watermark
12	TEFN	R/W1C	0x0	Tx Event FIFO New Entry 0x0 = Tx Event FIFO unchanged 0x1 = Tx Event FIFO new element
11	TCE	R/W1C	0x0	Tx FIFO Empty 0x0 = Tx FIFO non-empty 0x1 = Tx FIFO empty
10	TCF	R/W1C	0x0	Transmission Cancellation Finished 0x0 = No transmission cancellation finished 0x1 = Transmission cancellation finished
9	TC	R/W1C	0x0	Transmission Completed 0x0 = No transmission completed 0x1 = Transmission completed
8	HPM	R/W1C	0x0	High Priority Message 0x0 = No high priority message received 0x1 = High priority message received
7	RF1L	R/W1C	0x0	Rx FIFO 1 Message Lost 0x0 = No Rx FIFO 1 message Lost 0x1 = Rx FIFO 1 message lost, also set after write attempt to Rx FIFO 1 of size zero

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Table 9-41. IR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	RF1F	R/W1C	0x0	Rx FIFO 1 Full 0x0 = Rx FIFO 1 not full 0x1 = Rx FIFO 1 full
5	RF1W	R/W1C	0x0	Rx FIFO 1 Watermark Reached 0x0 = Rx FIFO 1 fill level below watermark 0x1 = Rx FIFO 1 fill level has reached watermark
4	RF1N	R/W1C	0x0	Rx FIFO 1 New Message 0x0 = No Rx FIFO 1 new message 0x1 = Rx FIFO 1 new message
3	RF0L	R/W1C	0x0	Rx FIFO 0 Message Lost 0x0 = No Rx FIFO 0 message Lost 0x1 = Rx FIFO 0 message lost, also set after write attempt to Rx FIFO 0 of size zero
2	RF0F	R/W1C	0x0	Rx FIFO 0 Full 0x0 = Rx FIFO 0 not full 0x1 = Rx FIFO 0 full
1	RF0W	R/W1C	0x0	Rx FIFO 0 Watermark Reached 0x0 = Rx FIFO 0 fill level below watermark 0x1 = Rx FIFO 0 fill level has reached watermark
0	RF0N	R/W1C	0x0	Rx FIFO 0 New Message 0x0 = No Rx FIFO 0 new message 0x1 = Rx FIFO 0 new message

9.4.16 IE Register (Address = 0x1054) [Reset = 0x00000000]

IE is shown in Figure 9-36 and described in Table 9-42.

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Figure 9-36. IE Register

31	30	29	28	27	26	25	24
RESERVED		ARAE	PEDE	PEAE	WDIE	BOE	EWE
R-0x0		R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0
23	22	21	20	19	18	17	16
EPE	ELOE	BEUE	BECE	DRXE	TOOE	MRAFE	TSWE
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0
15	14	13	12	11	10	9	8
TEFLE	TEFFE	TEFWE	TEFNE	TCEE	TCFE	TCE	HPME
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0
7	6	5	4	3	2	1	0
RF1LE	RF1FE	RF1WE	RF1NE	RF0LE	RF0FE	RF0WE	RF0NE
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0

Table 9-42. IE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0x0	Reserved
29	ARAE	R/W	0x0	Access to Reserved Address Interrupt Enable 0x0 = Interrupt is disabled 0x1 = Interrupt is enabled
28	PEDE	R/W	0x0	Protocol Error in Data Phase Interrupt Enable 0x0 = Interrupt is disabled 0x1 = Interrupt is enabled
27	PEAE	R/W	0x0	Protocol Error in Arbitration Phase Interrupt Enable 0x0 = Interrupt is disabled 0x1 = Interrupt is enabled
26	WDIE	R/W	0x0	Watchdog Interrupt Enable 0x0 = Interrupt is disabled 0x1 = Interrupt is enabled
25	BOE	R/W	0x0	Bus_Off Status Interrupt Enable 0x0 = Interrupt is disabled 0x1 = Interrupt is enabled
24	EWE	R/W	0x0	Warning Status Interrupt Enable 0x0 = Interrupt is disabled 0x1 = Interrupt is enabled
23	EPE	R/W	0x0	Error Passive Interrupt Enable 0x0 = Interrupt is disabled 0x1 = Interrupt is enabled
22	ELOE	R/W	0x0	Error Logging Overflow Interrupt Enable 0x0 = Interrupt is disabled 0x1 = Interrupt is enabled
21	BEUE	R/W	0x0	Bit Error Uncorrected Interrupt Enable 0x0 = Interrupt is disabled 0x1 = Interrupt is enabled
20	BECE	R/W	0x0	Message RAM bit error Interrupt Enable 0x0 = Interrupt is disabled 0x1 = Interrupt is enabled
19	DRXE	R/W	0x0	Message Stored to Dedicated Rx Buffer Interrupt Enable 0x0 = Interrupt is disabled 0x1 = Interrupt is enabled

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Table 9-42. IE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	TOOE	R/W	0x0	Timeout Occurred Interrupt Enable 0x0 = Interrupt is disabled 0x1 = Interrupt is enabled
17	MRAFE	R/W	0x0	Message RAM Access Failure Interrupt Enable 0x0 = Interrupt is disabled 0x1 = Interrupt is enabled
16	TSWE	R/W	0x0	Timestamp Wraparound Interrupt Enable 0x0 = Interrupt is disabled 0x1 = Interrupt is enabled
15	TEFLE	R/W	0x0	Tx Event FIFO Element Lost Interrupt Enable 0x0 = Interrupt is disabled 0x1 = Interrupt is enabled
14	TEFFE	R/W	0x0	Tx Event FIFO Full Interrupt Enable 0x0 = Interrupt is disabled 0x1 = Interrupt is enabled
13	TEFWE	R/W	0x0	Tx Event FIFO Watermark Reached Interrupt Enable 0x0 = Interrupt is disabled 0x1 = Interrupt is enabled
12	TEFNE	R/W	0x0	Tx Event FIFO New Entry Interrupt Enable 0x0 = Interrupt is disabled 0x1 = Interrupt is enabled
11	TCEE	R/W	0x0	Tx FIFO Empty Interrupt Enable 0x0 = Interrupt is disabled 0x1 = Interrupt is enabled
10	TCFE	R/W	0x0	Transmission Cancellation Finished Interrupt Enable 0x0 = Interrupt is disabled 0x1 = Interrupt is enabled
9	TCE	R/W	0x0	Transmission Completed Interrupt Enable 0x0 = Interrupt is disabled 0x1 = Interrupt is enabled
8	HPME	R/W	0x0	High Priority Message Interrupt Enable 0x0 = Interrupt is disabled 0x1 = Interrupt is enabled
7	RF1LE	R/W	0x0	Rx FIFO 1 Message Lost Interrupt Enable 0x0 = Interrupt is disabled 0x1 = Interrupt is enabled
6	RF1FE	R/W	0x0	Rx FIFO 1 Full Interrupt Enable 0x0 = Interrupt is disabled 0x1 = Interrupt is enabled
5	RF1WE	R/W	0x0	Rx FIFO 1 Watermark Reached Interrupt Enable 0x0 = Interrupt is disabled 0x1 = Interrupt is enabled
4	RF1NE	R/W	0x0	Rx FIFO 1 New Message Interrupt Enable 0x0 = Interrupt is disabled 0x1 = Interrupt is enabled
3	RF0LE	R/W	0x0	Rx FIFO 0 Message Lost Interrupt Enable 0x0 = Interrupt is disabled 0x1 = Interrupt is enabled
2	RF0FE	R/W	0x0	Rx FIFO 0 Full Interrupt Enable 0x0 = Interrupt is disabled 0x1 = Interrupt is enabled
1	RF0WE	R/W	0x0	Rx FIFO 0 Watermark Reached Interrupt Enable 0x0 = Interrupt is disabled 0x1 = Interrupt is enabled

Table 9-42. IE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RF0NE	R/W	0x0	Rx FIFO 0 New Message Interrupt Enable 0x0 = Interrupt is disabled 0x1 = Interrupt is enabled

9.4.17 ILS Register (Address = 0x1058) [Reset = 0x00000000]

ILS is shown in Figure 9-37 and described in Table 9-43.

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Figure 9-37. ILS Register

31	30	29	28	27	26	25	24
RESERVED		ARAL	PEDL	PEAL	WDIL	BOL	EWL
R-0x0		R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0
23	22	21	20	19	18	17	16
EPL	ELOL	BEUL	BECL	DRXL	TOOL	MRAFL	TSWL
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0
15	14	13	12	11	10	9	8
TEFLL	TEFFL	TEFWL	TEFNL	TCEL	TCFL	TCL	HPML
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0
7	6	5	4	3	2	1	0
RF1LL	RF1FL	RF1WL	RF1NL	RF0LL	RF0FL	RF0WL	RF0NL
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0

Table 9-43. ILS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0x0	Reserved
29	ARAL	R/W	0x0	Access to Reserved Address Line 0x0 = Interrupt line 0 selected for this interrupt (if enabled) 0x1 = Interrupt line 1 selected for this interrupt (if enabled)
28	PEDL	R/W	0x0	Protocol Error in Data Phase Line 0x0 = Interrupt line 0 selected for this interrupt (if enabled) 0x1 = Interrupt line 1 selected for this interrupt (if enabled)
27	PEAL	R/W	0x0	Protocol Error in Arbitration Phase Line 0x0 = Interrupt line 0 selected for this interrupt (if enabled) 0x1 = Interrupt line 1 selected for this interrupt (if enabled)
26	WDIL	R/W	0x0	Watchdog Interrupt Line 0x0 = Interrupt line 0 selected for this interrupt (if enabled) 0x1 = Interrupt line 1 selected for this interrupt (if enabled)
25	BOL	R/W	0x0	Bus_Off Status Line 0x0 = Interrupt line 0 selected for this interrupt (if enabled) 0x1 = Interrupt line 1 selected for this interrupt (if enabled)
24	EWL	R/W	0x0	Warning Status Line 0x0 = Interrupt line 0 selected for this interrupt (if enabled) 0x1 = Interrupt line 1 selected for this interrupt (if enabled)
23	EPL	R/W	0x0	Error Passive Line 0x0 = Interrupt line 0 selected for this interrupt (if enabled) 0x1 = Interrupt line 1 selected for this interrupt (if enabled)
22	ELOL	R/W	0x0	Error Logging Overflow Line 0x0 = Interrupt line 0 selected for this interrupt (if enabled) 0x1 = Interrupt line 1 selected for this interrupt (if enabled)
21	BEUL	R/W	0x0	Bit Error Uncorrected Message RAM bit error detected, uncorrected Line 0x0 = Interrupt line 0 selected for this interrupt (if enabled) 0x1 = Interrupt line 1 selected for this interrupt (if enabled)
20	BECL	R/W	0x0	Message RAM bit error detected and corrected Line 0x0 = Interrupt line 0 selected for this interrupt (if enabled) 0x1 = Interrupt line 1 selected for this interrupt (if enabled)
19	DRXL	R/W	0x0	Message Stored to Dedicated Rx Buffer Line 0x0 = Interrupt line 0 selected for this interrupt (if enabled) 0x1 = Interrupt line 1 selected for this interrupt (if enabled)

Table 9-43. ILS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	TOOL	R/W	0x0	Timeout Occurred Line 0x0 = Interrupt line 0 selected for this interrupt (if enabled) 0x1 = Interrupt line 1 selected for this interrupt (if enabled)
17	MRAFL	R/W	0x0	Message RAM Access Failure Line 0x0 = Interrupt line 0 selected for this interrupt (if enabled) 0x1 = Interrupt line 1 selected for this interrupt (if enabled)
16	TSWL	R/W	0x0	Timestamp Wraparound Line 0x0 = Interrupt line 0 selected for this interrupt (if enabled) 0x1 = Interrupt line 1 selected for this interrupt (if enabled)
15	TEFLL	R/W	0x0	Tx Event FIFO Element Lost Line 0x0 = Interrupt line 0 selected for this interrupt (if enabled) 0x1 = Interrupt line 1 selected for this interrupt (if enabled)
14	TEFFL	R/W	0x0	Tx Event FIFO Full Line 0x0 = Interrupt line 0 selected for this interrupt (if enabled) 0x1 = Interrupt line 1 selected for this interrupt (if enabled)
13	TEFWL	R/W	0x0	Tx Event FIFO Watermark Reached Line 0x0 = Interrupt line 0 selected for this interrupt (if enabled) 0x1 = Interrupt line 1 selected for this interrupt (if enabled)
12	TEFNL	R/W	0x0	Tx Event FIFO New Entry Line 0x0 = Interrupt line 0 selected for this interrupt (if enabled) 0x1 = Interrupt line 1 selected for this interrupt (if enabled)
11	TCEL	R/W	0x0	Tx FIFO Empty Line 0x0 = Interrupt line 0 selected for this interrupt (if enabled) 0x1 = Interrupt line 1 selected for this interrupt (if enabled)
10	TCFL	R/W	0x0	Transmission Cancellation Finished Line 0x0 = Interrupt line 0 selected for this interrupt (if enabled) 0x1 = Interrupt line 1 selected for this interrupt (if enabled)
9	TCL	R/W	0x0	Transmission Completed Line 0x0 = Interrupt line 0 selected for this interrupt (if enabled) 0x1 = Interrupt line 1 selected for this interrupt (if enabled)
8	HPML	R/W	0x0	High Priority Message Line 0x0 = Interrupt line 0 selected for this interrupt (if enabled) 0x1 = Interrupt line 1 selected for this interrupt (if enabled)
7	RF1LL	R/W	0x0	Rx FIFO 1 Message Lost Line 0x0 = Interrupt line 0 selected for this interrupt (if enabled) 0x1 = Interrupt line 1 selected for this interrupt (if enabled)
6	RF1FL	R/W	0x0	Rx FIFO 1 Full Line 0x0 = Interrupt line 0 selected for this interrupt (if enabled) 0x1 = Interrupt line 1 selected for this interrupt (if enabled)
5	RF1WL	R/W	0x0	Rx FIFO 1 Watermark Reached Line 0x0 = Interrupt line 0 selected for this interrupt (if enabled) 0x1 = Interrupt line 1 selected for this interrupt (if enabled)
4	RF1NL	R/W	0x0	Rx FIFO 1 New Message Line 0x0 = Interrupt line 0 selected for this interrupt (if enabled) 0x1 = Interrupt line 1 selected for this interrupt (if enabled)
3	RF0LL	R/W	0x0	Rx FIFO 0 Message Lost Line 0x0 = Interrupt line 0 selected for this interrupt (if enabled) 0x1 = Interrupt line 1 selected for this interrupt (if enabled)
2	RF0FL	R/W	0x0	Rx FIFO 0 Full Line 0x0 = Interrupt line 0 selected for this interrupt (if enabled) 0x1 = Interrupt line 1 selected for this interrupt (if enabled)
1	RF0WL	R/W	0x0	Rx FIFO 0 Watermark Reached Line 0x0 = Interrupt line 0 selected for this interrupt (if enabled) 0x1 = Interrupt line 1 selected for this interrupt (if enabled)

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Table 9-43. ILS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RF0NL	R/W	0x0	Rx FIFO 0 New Message Line 0x0 = Interrupt line 0 selected for this interrupt (if enabled) 0x1 = Interrupt line 1 selected for this interrupt (if enabled)

9.4.18 ILE Register (Address = 0x105C) [Reset = 0x00000000]

ILE is shown in Figure 9-38 and described in Table 9-44.

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Enable interrupt outputs from the CAN controller.#NOTE#m_can_int0 (INT0) is routed to the main device nINT pin. M_can_int1 (INT1) by default is not routed to any pin, but can be routed to nWKRQ as an active low output for the INT1 line. This feature is enabled in register 0x0800[10].#/NOTE#

Figure 9-38. ILE Register

31	30	29	28	27	26	25	24
RESERVED							
R-0x0							
23	22	21	20	19	18	17	16
RESERVED							
R-0x0							
15	14	13	12	11	10	9	8
RESERVED							
R-0x0							
7	6	5	4	3	2	1	0
RESERVED						EINT1	EINT0
R-0x0						R/W-0x0	R/W-0x0

Table 9-44. ILE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0x0	Reserved
1	EINT1	R/W	0x0	Enable Interrupt Line 1 0x0 = Interrupt line m_can_int1 disabled 0x1 = Interrupt line m_can_int1 enabled
0	EINT0	R/W	0x0	Enable Interrupt Line 0 0x0 = Interrupt line m_can_int0 disabled 0x1 = Interrupt line m_can_int0 enabled

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9.4.19 GFC Register (Address = 0x1080) [Reset = 0x00000000]

GFC is shown in Figure 9-39 and described in Table 9-45.

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Figure 9-39. GFC Register

31	30	29	28	27	26	25	24
RESERVED							
R-0x0							
23	22	21	20	19	18	17	16
RESERVED							
R-0x0							
15	14	13	12	11	10	9	8
RESERVED							
R-0x0							
7	6	5	4	3	2	1	0
RESERVED		ANFS		ANFE		RRFS	RRFE
R-0x0		R/WP-0x0		R/WP-0x0		R/WP-0x0	R/WP-0x0

Table 9-45. GFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0x0	Reserved
5-4	ANFS	R/WP	0x0	Accept Non-matching Frames Standard ID Defines how received messages with 11-bit IDs that do not match any element of the filter list are treaded. 0x0 = Accept in Rx FIFO 0 0x1 = Accept in Rx FIFO 1 0x2 = Reject 0x3 = Reject
3-2	ANFE	R/WP	0x0	Accept Non-matching Frames Extended ID Defines how received messages with 29-bit IDs that do not match any element of the filter list are treaded. 0x0 = Accept in Rx FIFO 0 0x1 = Accept in Rx FIFO 1 0x2 = Reject 0x3 = Reject
1	RRFS	R/WP	0x0	Reject Remote Frames Standard ID 0x0 = Filter remote frames with 11-bit standard IDs 0x1 = Reject all remote frames with 11-bit standard IDs
0	RRFE	R/WP	0x0	Reject Remote Frames Extended ID 0x0 = Filter remote frames with 29-bit extended IDs 0x1 = Reject all remote frames with 29-bit extended IDs

9.4.20 SIDFC Register (Address = 0x1084) [Reset = 0x00000000]

SIDFC is shown in Figure 9-40 and described in Table 9-46.

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Figure 9-40. SIDFC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								LSS								FLSSA															
R-0x0								R/WP-0x0								R/WP-0x0															

Table 9-46. SIDFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0x0	Reserved
23-16	LSS	R/WP	0x0	List Size Standard 0 = No standard Message ID Filter 1- 128 = Number of standard Message ID filter elements # 62# 128 = Values greater than 128 are interpreted as 128
15-0	FLSSA	R/WP	0x0	Filter List Standard Start Address Start address of standard Message ID filter list.#NOTE#The MRAM and start address for this register, FLSSA, has special consideration. The start address must be word aligned (32-bit) in the MRAM. The 2 least significant bits are ignored on a write to make sure of this behavior. When entering the MRAM start address, the 0x8000 prefix is not necessary. For example, if the desired start address is 0x8634, then the value to enter into bits SA[15:0] must be 0x0634#/NOTE#

ADVANCE INFORMATION

9.4.21 XIDFC Register (Address = 0x1088) [Reset = 0x00000000]

XIDFC is shown in Figure 9-41 and described in Table 9-47.

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Figure 9-41. XIDFC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									LSE							FLSEA															
R-0x0									R/WP-0x0							R/WP-0x0															

Table 9-47. XIDFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R	0x0	Reserved
22-16	LSE	R/WP	0x0	List Size Extended 0 = No standard Message ID Filter 1- 128 = Number of standard Message ID filter elements # 62# 128 = Values greater than 128 are interpreted as 128
15-0	FLSEA	R/WP	0x0	Filter List Extended Start Address Start address of Extended Message ID filter list.#NOTE#The MRAM and start address for this register, FLSSA, has special consideration. The start address must be word aligned (32-bit) in the MRAM. The 2 least significant bits are ignored on a write to make sure of this behavior. When entering the MRAM start address, the 0x8000 prefix is not necessary. For example, if the desired start address is 0x8634, then the value to enter into bits SA[15:0] must be 0x0634#/NOTE#

ADVANCE INFORMATION

9.4.22 XIDAM Register (Address = 0x1090) [Reset = 0x3FFFFFFF]

XIDAM is shown in Figure 9-42 and described in Table 9-48.

Return to the Summary Table.

Figure 9-42. XIDAM Register

31	30	29	28	27	26	25	24
RESERVED		Extended					
R-0x0		R/WP-0x3FFFFFFF					
23	22	21	20	19	18	17	16
Extended							
R/WP-0x3FFFFFFF							
15	14	13	12	11	10	9	8
Extended							
R/WP-0x3FFFFFFF							
7	6	5	4	3	2	1	0
Extended							
R/WP-0x3FFFFFFF							

Table 9-48. XIDAM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0x0	Reserved
29-0	Extended	R/WP	0x3FFFFFFF	Extended ID Mask For acceptance filtering of extended frames the Extended ID AND Mask is ANDed with the Message ID of a received frame. Intended for masking of 29-bit IDs in SAE J1939. With the reset value of all bits set to one the mask is not active.

ADVANCE INFORMATION

9.4.23 HPMS Register (Address = 0x1094) [Reset = 0x00000000]

HPMS is shown in Figure 9-43 and described in Table 9-49.

Return to the Summary Table.

Figure 9-43. HPMS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0x0							
23	22	21	20	19	18	17	16
RESERVED							
R-0x0							
15	14	13	12	11	10	9	8
FLST	FIDX						
R-0x0	R-0x0						
7	6	5	4	3	2	1	0
MSI		BIDX					
R-0x0		R-0x0					

Table 9-49. HPMS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0x0	Reserved
15	FLST	R	0x0	Filter List Indicates the filter list of the matching filter element 0x0 = Standard filter list 0x1 = Extended filter list
14-8	FIDX	R	0x0	Filter Index Index of matching filter element. Range is 0 to SIDFC.LSS - 1 to XIDFC.LSE -1
7-6	MSI	R	0x0	Message Storage Indicator 0x0 = No FIFO Selected 0x1 = FIFO message lost 0x2 = Message stored in FIFO0 0x3 = Message stored in FIFO1
5-0	BIDX	R	0x0	Buffer Index Index of Rx FIFO element to which the message was stored. Only valid when MSI[1] = '1'

9.4.24 NDAT1 Register (Address = 0x1098) [Reset = 0x00000000]

NDAT1 is shown in Figure 9-44 and described in Table 9-50.

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Figure 9-44. NDAT1 Register

31	30	29	28	27	26	25	24
ND31	ND30	ND29	ND28	ND27	ND26	ND25	ND24
R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0
23	22	21	20	19	18	17	16
ND23	ND22	ND21	ND20	ND19	ND18	ND17	ND16
R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0
15	14	13	12	11	10	9	8
ND15	ND14	ND13	ND12	ND11	ND10	ND9	ND8
R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0
7	6	5	4	3	2	1	0
ND7	ND6	ND5	ND4	ND3	ND2	ND1	ND0
R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0

Table 9-50. NDAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ND31	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
30	ND30	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
29	ND29	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
28	ND28	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
27	ND27	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
26	ND26	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
25	ND25	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
24	ND24	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
23	ND23	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
22	ND22	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
21	ND21	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
20	ND20	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
19	ND19	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
18	ND18	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
17	ND17	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
16	ND16	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
15	ND15	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message

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Table 9-50. NDAT1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	ND14	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
13	ND13	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
12	ND12	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
11	ND11	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
10	ND10	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
9	ND9	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
8	ND8	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
7	ND7	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
6	ND6	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
5	ND5	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
4	ND4	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
3	ND3	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
2	ND2	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
1	ND1	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
0	ND0	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message

9.4.25 NDAT2 Register (Address = 0x109C) [Reset = 0x00000000]

NDAT2 is shown in Figure 9-45 and described in Table 9-51.

Return to the Summary Table.

Figure 9-45. NDAT2 Register

31	30	29	28	27	26	25	24
ND63	ND62	ND61	ND60	ND59	ND58	ND57	ND56
R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0
23	22	21	20	19	18	17	16
ND55	ND54	ND53	ND52	ND51	ND50	ND49	ND48
R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0
15	14	13	12	11	10	9	8
ND47	ND46	ND45	ND44	ND43	ND42	ND41	ND40
R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0
7	6	5	4	3	2	1	0
ND39	ND38	ND37	ND36	ND35	ND34	ND33	ND32
R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0	R/W1C-0x0

Table 9-51. NDAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ND63	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
30	ND62	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
29	ND61	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
28	ND60	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
27	ND59	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
26	ND58	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
25	ND57	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
24	ND56	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
23	ND55	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
22	ND54	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
21	ND53	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
20	ND52	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
19	ND51	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
18	ND50	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
17	ND49	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
16	ND48	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
15	ND47	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message

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Table 9-51. NDAT2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	ND46	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
13	ND45	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
12	ND44	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
11	ND43	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
10	ND42	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
9	ND41	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
8	ND40	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
7	ND39	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
6	ND38	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
5	ND37	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
4	ND36	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
3	ND35	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
2	ND34	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
1	ND33	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message
0	ND32	R/W1C	0x0	0x0 = Rx Buffer not updated 0x1 = Rx Buffer updated with new message

9.4.26 RXF0C Register (Address = 0x10A0) [Reset = 0x00000000]

RXF0C is shown in Figure 9-46 and described in Table 9-52.

Return to the Summary Table.

Figure 9-46. RXF0C Register

31	30	29	28	27	26	25	24
F0OM	F0WM						
R/WP-0x0	R/WP-0x0						
23	22	21	20	19	18	17	16
RESERVED	F0S						
R-0x0	R/WP-0x0						
15	14	13	12	11	10	9	8
F0SA							
R/WP-0x0							
7	6	5	4	3	2	1	0
F0SA							
R/WP-0x0							

Table 9-52. RXF0C Register Field Descriptions

Bit	Field	Type	Reset	Description
31	F0OM	R/WP	0x0	FIFO 0 Operation Mode Sets the defined behavior for new messages when the FIFO is full 0x0 = FIFO 0 is in rejecting new messages mode 0x1 = FIFO 0 is in overwrite old messages mode
30-24	F0WM	R/WP	0x0	FIFO 0 Watermark 0 = Watermark interrupt disabled 1- 64 = Level for Rx FIFO 0 watermark interrupt (IR.RF 0W) # 62# 64 = Watermark interrupt disabled
23	RESERVED	R	0x0	Reserved
22-16	F0S	R/WP	0x0	FIFO 0 Size How many Rx FIFO 0 elements there are. 0 = No Rx FIFO 0 1- 64 = Number of Rx FIFO 0 elements # 62# 64 = Interpreted as 64
15-0	F0SA	R/WP	0x0	Rx FIFO 0 Start Address Start address of the Rx FIFO0 #NOTE#The MRAM and start address for this register has special consideration. The start address must be word aligned (32-bit) in the MRAM. The 2 least significant bits are ignored on a write to make sure of this behavior. When entering the MRAM start address, the 0x8000 prefix is not necessary. For example, if the desired start address is 0x8634, then the value to enter into bits SA[15:0] must be 0x0634#/NOTE#

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9.4.27 RXF0S Register (Address = 0x10A4) [Reset = 0x00000000]

RXF0S is shown in Figure 9-47 and described in Table 9-53.

Return to the Summary Table.

Figure 9-47. RXF0S Register

31	30	29	28	27	26	25	24
RESERVED						RF0L	RF0F
R-0x0						R-0x0	R-0x0
23	22	21	20	19	18	17	16
RESERVED		F0PI					
R-0x0		R-0x0					
15	14	13	12	11	10	9	8
RESERVED		F0GI					
R-0x0		R-0x0					
7	6	5	4	3	2	1	0
RESERVED	F0FL						
R-0x0	R-0x0						

Table 9-53. RXF0S Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0x0	Reserved

25	RF0L	R	0x0	Rx FIFO 0 Message Lost This bit is a copyo of the interrupt flag IR.RF0L.
				When IR.RF0L is reset, this bit is also reset #NOTE#Overwriting the oldest message with RXF0C.F0OM = 1 does not set this flag#/ NOTE#
				0x0 = No Rx FIFO 0 message Lost
				0x1 = Rx FIFO 0 message lost, also set after write attempt to Rx FIFO 0 of size zero

24	RF0F	R	0x0	Rx FIFO 0 Full This bit is a copy of the interrupt flag IR.RF0F. When IR.RF0F is cleared, this bit is also reset 0x0 = Rx FIFO 0 not full 0x1 = Rx FIFO 0 full
23-22	RESERVED	R	0x0	Reserved
21-16	F0PI	R	0x0	Rx FIFO 0 Put Index Valid range is 0 to 63
15-14	RESERVED	R	0x0	Reserved
13-8	F0GI	R	0x0	Rx FIFO 0 Get Index Valid range is 0 to 63
7	RESERVED	R	0x0	Reserved
6-0	F0FL	R	0x0	Rx FIFO 0 Fill Level Number of elements stored in Rx FIFO 0, valid range is 0 to 64

9.4.28 RXF0A Register (Address = 0x10A8) [Reset = 0x00000000]

RXF0A is shown in Figure 9-48 and described in Table 9-54.

Return to the Summary Table.

Figure 9-48. RXF0A Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										F0AI					
R-0x0																										R/W-0x0					

Table 9-54. RXF0A Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0x0	Reserved
5-0	F0AI	R/W	0x0	Rx FIFO 0 Acknowledge Index After the host has read a message or a sequence of messages from Rx FIFO 0, it must write the buffer index of the last element read from the Rx FIFO 0 to F0AI. This will set the Rx FIFO 0 Get Index to F0AI + 1 and update the fill level shown in RXF0S.F0FL

9.4.29 RXBC Register (Address = 0x10AC) [Reset = 0x00000000]

RXBC is shown in Figure 9-49 and described in Table 9-55.

Return to the Summary Table.

Figure 9-49. RXBC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RBSA															
R-0x0																R/WP-0x0															

Table 9-55. RXBC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0x0	Reserved
15-0	RBSA	R/WP	0x0	Rx Buffer Start Address Start address of the Rx Buffer #NOTE#The MRAM and start address for this register has special consideration. The start address must be word aligned (32-bit) in the MRAM. The 2 least significant bits are ignored on a write to make sure of this behavior. When entering the MRAM start address, the 0x8000 prefix is not necessary. For example, if the desired start address is 0x8634, then the value to enter into bits SA[15:0] must be 0x0634#/NOTE#

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9.4.30 RXF1C Register (Address = 0x10B0) [Reset = 0x00000000]

RXF1C is shown in Figure 9-50 and described in Table 9-56.

Return to the Summary Table.

Figure 9-50. RXF1C Register

31	30	29	28	27	26	25	24
F1OM	F1WM						
R/WP-0x0	R/WP-0x0						
23	22	21	20	19	18	17	16
RESERVED	F1S						
R-0x0	R/WP-0x0						
15	14	13	12	11	10	9	8
F1SA							
R/WP-0x0							
7	6	5	4	3	2	1	0
F1SA							
R/WP-0x0							

Table 9-56. RXF1C Register Field Descriptions

Bit	Field	Type	Reset	Description
31	F1OM	R/WP	0x0	FIFO 1 Operation Mode Sets the defined behavior for new messages when the FIFO is full 0x0 = FIFO 1 is in rejecting new messages mode 0x1 = FIFO 1 is in overwrite old messages mode
30-24	F1WM	R/WP	0x0	FIFO 1 Watermark 0 = Watermark interrupt disabled 1- 64 = Level for Rx FIFO 1 watermark interrupt (IR.RF 1W) # 62# 64 = Watermark interrupt disabled
23	RESERVED	R	0x0	Reserved
22-16	F1S	R/WP	0x0	FIFO 1 Size How many Rx FIFO 1 elements there are. 0 = No Rx FIFO 1 1- 64 = Number of Rx FIFO 1 elements # 62# 64 = Interpreted as 64
15-0	F1SA	R/WP	0x0	Rx FIFO 1 Start Address Start address of the Rx FIFO1 #NOTE#The MRAM and start address for this register has special consideration. The start address must be word aligned (32-bit) in the MRAM. The 2 least significant bits are ignored on a write to make sure of this behavior. When entering the MRAM start address, the 0x8000 prefix is not necessary. For example, if the desired start address is 0x8634, then the value to enter into bits SA[15:0] must be 0x0634#/NOTE#

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9.4.31 RXF1S Register (Address = 0x10B4) [Reset = 0x00000000]

RXF1S is shown in Figure 9-51 and described in Table 9-57.

Return to the Summary Table.

Figure 9-51. RXF1S Register

31	30	29	28	27	26	25	24
RESERVED						RF1L	RF1F
R-0x0						R-0x0	R-0x0
23	22	21	20	19	18	17	16
RESERVED		F1PI					
R-0x0		R-0x0					
15	14	13	12	11	10	9	8
RESERVED		F1GI					
R-0x0		R-0x0					
7	6	5	4	3	2	1	0
RESERVED	F1FL						
R-0x0	R-0x0						

Table 9-57. RXF1S Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0x0	Reserved

25	RF1L	R	0x0	Rx FIFO 1 Message Lost This bit is a copyo of the interrupt flag IR.RF1L.
				When IR.RF1L is reset, this bit is also reset #NOTE#Overwriting the oldest message with RXF1C.F1OM = 1 does not set this flag#/ NOTE#
				0x0 = No Rx FIFO 1 message Lost
				0x1 = Rx FIFO 1 message lost, also set after write attempt to Rx FIFO 1 of size zero

24	RF1F	R	0x0	Rx FIFO 1 Full This bit is a copy of the interrupt flag IR.RF1F. When IR.RF1F is cleared, this bit is also reset 0x0 = Rx FIFO 1 not full 0x1 = Rx FIFO 1 full
23-22	RESERVED	R	0x0	Reserved
21-16	F1PI	R	0x0	Rx FIFO 1 Put Index Valid range is 0 to 63
15-14	RESERVED	R	0x0	Reserved
13-8	F1GI	R	0x0	Rx FIFO 1 Get Index Valid range is 0 to 63
7	RESERVED	R	0x0	Reserved
6-0	F1FL	R	0x0	Rx FIFO 1 Fill Level Number of elements stored in Rx FIFO 1, valid range is 0 to 64

9.4.32 RXF1A Register (Address = 0x10B8) [Reset = 0x00000000]

RXF1A is shown in Figure 9-52 and described in Table 9-58.

Return to the Summary Table.

Figure 9-52. RXF1A Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										F1AI					
R-0x0																										R/W-0x0					

Table 9-58. RXF1A Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0x0	Reserved
5-0	F1AI	R/W	0x0	Rx FIFO 1 Acknowledge Index After the host has read a message or a sequence of messages from Rx FIFO 1, it must write the buffer index of the last element read from the Rx FIFO 1 to F1AI. This will set the Rx FIFO 1 Get Index to F1AI + 1 and update the fill level shown in RXF1S.F1FL

9.4.33 RXESC Register (Address = 0x10BC) [Reset = 0x00000000]

RXESC is shown in Figure 9-53 and described in Table 9-59.

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Figure 9-53. RXESC Register

31	30	29	28	27	26	25	24
RESERVED							
R-0x0							
23	22	21	20	19	18	17	16
RESERVED							
R-0x0							
15	14	13	12	11	10	9	8
RESERVED					RBDS		
R-0x0					R/WP-0x0		
7	6	5	4	3	2	1	0
RESERVED	F1DS			RESERVED	F0DS		
R-0x0	R/WP-0x0			R-0x0	R/WP-0x0		

Table 9-59. RXESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0x0	Reserved
10-8	RBDS	R/WP	0x0	Rx Buffer Data Field Size 0x0 = 8 byte data field 0x1 = 12 byte data field 0x2 = 16 byte data field 0x3 = 20 byte data field 0x4 = 24 byte data field 0x5 = 32 byte data field 0x6 = 48 byte data field 0x7 = 64 byte data field
7	RESERVED	R	0x0	Reserved
6-4	F1DS	R/WP	0x0	Rx FIFO 1 Data Field Size 0x0 = 8 byte data field 0x1 = 12 byte data field 0x2 = 16 byte data field 0x3 = 20 byte data field 0x4 = 24 byte data field 0x5 = 32 byte data field 0x6 = 48 byte data field 0x7 = 64 byte data field
3	RESERVED	R	0x0	Reserved
2-0	F0DS	R/WP	0x0	Rx FIFO 0 Data Field Size 0x0 = 8 byte data field 0x1 = 12 byte data field 0x2 = 16 byte data field 0x3 = 20 byte data field 0x4 = 24 byte data field 0x5 = 32 byte data field 0x6 = 48 byte data field 0x7 = 64 byte data field

9.4.34 TXBC Register (Address = 0x10C0) [Reset = 0x00000000]

TXBC is shown in Figure 9-54 and described in Table 9-60.

Return to the Summary Table.

Figure 9-54. TXBC Register

31	30	29	28	27	26	25	24
RESERVED	TFQM	TFQS					
R-0x0	R/WP-0x0	R/WP-0x0					
23	22	21	20	19	18	17	16
RESERVED		NDTB					
R-0x0		R/WP-0x0					
15	14	13	12	11	10	9	8
TBSA							
R/WP-0x0							
7	6	5	4	3	2	1	0
TBSA							
R/WP-0x0							

Table 9-60. TXBC Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0x0	Reserved
30	TFQM	R/WP	0x0	Tx FIFO/Queue Mode 0x0 = Tx FIFO operation 0x1 = Tx Queue operation
29-24	TFQS	R/WP	0x0	Transmit FIFO/Queue Size 0 = No Tx FIFO/Queue 1- 32 = Number of Tx Buffers used for Tx FIFO/Queue # 62# 32 = Values greater than 32 are interpreted as 32
23-22	RESERVED	R	0x0	Reserved
21-16	NDTB	R/WP	0x0	Number of Dedicated Transmit Buffers 0 = No Tx FIFO/Queue 1- 32 = Number of Tx Buffers used for Tx FIFO/Queue # 62# 32 = Values greater than 32 are interpreted as 32
15-0	TBSA	R/WP	0x0	Tx Buffers Start Address Start address of Tx Buffers section in Message RAM #NOTE#The MRAM and start address for this register has special consideration. The start address must be word aligned (32-bit) in the MRAM. The 2 least significant bits are ignored on a write to make sure of this behavior. When entering the MRAM start address, the 0x8000 prefix is not necessary. For example, if the desired start address is 0x8634, then the value to enter into bits SA[15:0] must be 0x0634#/NOTE#

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9.4.35 TXFQS Register (Address = 0x10C4) [Reset = 0x00000000]

TXFQS is shown in Figure 9-55 and described in Table 9-61.

Return to the Summary Table.

Figure 9-55. TXFQS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0x0							
23	22	21	20	19	18	17	16
RESERVED		TFQF	TFQPI				
R-0x0		R-0x0	R-0x0				
15	14	13	12	11	10	9	8
RESERVED			TFGI				
R-0x0			R-0x0				
7	6	5	4	3	2	1	0
RESERVED		TFFL					
R-0x0		R-0x0					

Table 9-61. TXFQS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R	0x0	Reserved
21	TFQF	R	0x0	Tx FIFO/Queue Full 0x0 = Tx FIFO/Queue not full 0x1 = Tx FIFO/Queue full
20-16	TFQPI	R	0x0	Tx FIFO/Queue Put Index Tx FIFO/Queue write index pointer, range 0 to 31
15-13	RESERVED	R	0x0	Reserved
12-8	TFGI	R	0x0	Tx FIFO Get Index Tx FIFO read index pointer, range 0 to 31. Read as zero when Tx Queue operation is configured (TXBC.TFQM = 1)
7-6	RESERVED	R	0x0	Reserved
5-0	TFFL	R	0x0	Tx FIFO Free Level Number of consecutive Tx FIFO elements starting from the TFGI (range 0 to 32). Read as zero when Tx Queue operation is configured (TXBC.TFQM = 1) #NOTE#In case of mixed configurations where dedicated Tx Buffers are combined with a Tx FIFO or a Tx Queue, the Put and Get Indices indicate the number of the Tx Buffer Starting with the first dedicated Tx Buffers. Example: For a configuration of 12 dedicated Tx Buffers and a Tx FIFO of 20 BUffers, a Put Index of 15 points to the fourth buffer of the Tx FIFO#/NOTE#

9.4.36 TXESC Register (Address = 0x10C8) [Reset = 0x00000000]

TXESC is shown in Figure 9-56 and described in Table 9-62.

Return to the Summary Table.

Figure 9-56. TXESC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0x0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													TBDS		
R-0x0													R/WP-0x0		

Table 9-62. TXESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0x0	Reserved

2-0	TBDS	R/WP	0x0	Tx Buffer Data Field Size #NOTE#In case the data length code DLC of a Tx Buffer element is configured to a value higher than the Tx Buffer data field size TXESC.TBDS, the bytes not defined by the Tx Buffer are transmitted as "0xCC" (padding bytes)#/NOTE#
				0x0 = 8 byte data field
				0x1 = 12 byte data field
				0x2 = 16 byte data field
				0x3 = 20 byte data field
				0x4 = 24 byte data field
				0x5 = 32 byte data field
				0x6 = 48 byte data field
				0x7 = 64 byte data field

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9.4.37 TXBRP Register (Address = 0x10CC) [Reset = 0x00000000]

TXBRP is shown in Figure 9-57 and described in Table 9-63.

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Transmission Request Pending register Each Tx Buffer has its own Transmission Request Pending bit. The bits are set via register TXBAR. The bits are reset after a requested transmission has completed or has been cancelled via register TXBCR. TXBRP bits are set only for those Tx Buffers configured via TXBC. After a TXBRP bit has been set, a Tx scan is started to check for the pending Tx request with the highest priority (Tx Buffer with lowest Message ID). A cancellation request resets the corresponding transmission request pending bit of register TXBRP. In case a transmission has already been started when a cancellation is requested, this is done at the end of the transmission, regardless whether the transmission was successful or not. The cancellation request bits are reset directly after the corresponding TXBRP bit has been reset. After a cancellation has been requested, a finished cancellation is signaled via TXBCF when 1) after successful transmission together with the corresponding TXBTO bit 2) when the transmission has not yet been started at the point of cancellation 3) when the transmission has been aborted due to lost arbitration 4) when an error occured during frame transmission In DAR mode all transmissions are automatically cancelled if they are nto successful. The corresponding TXBCF bit is set for all unsuccessful transmissions. #NOTE#TXBRP bits which are set while a Tx scan is in progress are not considered during this particular Tx scan. In case a cancellation is requested for such a Tx Buffer, this Add Request is cancelled immediately, and the corresponding TXBRP bit is reset.#/NOTE#

Figure 9-57. TXBRP Register

31	30	29	28	27	26	25	24
TRP31	TRP30	TRP29	TRP28	TRP27	TRP26	TRP25	TRP24
R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0
23	22	21	20	19	18	17	16
TRP23	TRP22	TRP21	TRP20	TRP19	TRP18	TRP17	TRP16
R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0
15	14	13	12	11	10	9	8
TRP15	TRP14	TRP13	TRP12	TRP11	TRP10	TRP9	TRP8
R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0
7	6	5	4	3	2	1	0
TRP7	TRP6	TRP5	TRP4	TRP3	TRP2	TRP1	TRP0
R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0

Table 9-63. TXBRP Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TRP31	R	0x0	Transmission Request Pending See above note 0x0 = No transmission request pending 0x1 = Transmission request pending
30	TRP30	R	0x0	Transmission Request Pending See above note 0x0 = No transmission request pending 0x1 = Transmission request pending
29	TRP29	R	0x0	Transmission Request Pending See above note 0x0 = No transmission request pending 0x1 = Transmission request pending
28	TRP28	R	0x0	Transmission Request Pending See above note 0x0 = No transmission request pending 0x1 = Transmission request pending
27	TRP27	R	0x0	Transmission Request Pending See above note 0x0 = No transmission request pending 0x1 = Transmission request pending
26	TRP26	R	0x0	Transmission Request Pending See above note 0x0 = No transmission request pending 0x1 = Transmission request pending

Table 9-63. TXBRP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	TRP25	R	0x0	Transmission Request Pending See above note 0x0 = No transmission request pending 0x1 = Transmission request pending
24	TRP24	R	0x0	Transmission Request Pending See above note 0x0 = No transmission request pending 0x1 = Transmission request pending
23	TRP23	R	0x0	Transmission Request Pending See above note 0x0 = No transmission request pending 0x1 = Transmission request pending
22	TRP22	R	0x0	Transmission Request Pending See above note 0x0 = No transmission request pending 0x1 = Transmission request pending
21	TRP21	R	0x0	Transmission Request Pending See above note 0x0 = No transmission request pending 0x1 = Transmission request pending
20	TRP20	R	0x0	Transmission Request Pending See above note 0x0 = No transmission request pending 0x1 = Transmission request pending
19	TRP19	R	0x0	Transmission Request Pending See above note 0x0 = No transmission request pending 0x1 = Transmission request pending
18	TRP18	R	0x0	Transmission Request Pending See above note 0x0 = No transmission request pending 0x1 = Transmission request pending
17	TRP17	R	0x0	Transmission Request Pending See above note 0x0 = No transmission request pending 0x1 = Transmission request pending
16	TRP16	R	0x0	Transmission Request Pending See above note 0x0 = No transmission request pending 0x1 = Transmission request pending
15	TRP15	R	0x0	Transmission Request Pending See above note 0x0 = No transmission request pending 0x1 = Transmission request pending
14	TRP14	R	0x0	Transmission Request Pending See above note 0x0 = No transmission request pending 0x1 = Transmission request pending
13	TRP13	R	0x0	Transmission Request Pending See above note 0x0 = No transmission request pending 0x1 = Transmission request pending
12	TRP12	R	0x0	Transmission Request Pending See above note 0x0 = No transmission request pending 0x1 = Transmission request pending
11	TRP11	R	0x0	Transmission Request Pending See above note 0x0 = No transmission request pending 0x1 = Transmission request pending
10	TRP10	R	0x0	Transmission Request Pending See above note 0x0 = No transmission request pending 0x1 = Transmission request pending
9	TRP9	R	0x0	Transmission Request Pending See above note 0x0 = No transmission request pending 0x1 = Transmission request pending
8	TRP8	R	0x0	Transmission Request Pending See above note 0x0 = No transmission request pending 0x1 = Transmission request pending
7	TRP7	R	0x0	Transmission Request Pending See above note 0x0 = No transmission request pending 0x1 = Transmission request pending

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Table 9-63. TXBRP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	TRP6	R	0x0	Transmission Request Pending See above note 0x0 = No transmission request pending 0x1 = Transmission request pending
5	TRP5	R	0x0	Transmission Request Pending See above note 0x0 = No transmission request pending 0x1 = Transmission request pending
4	TRP4	R	0x0	Transmission Request Pending See above note 0x0 = No transmission request pending 0x1 = Transmission request pending
3	TRP3	R	0x0	Transmission Request Pending See above note 0x0 = No transmission request pending 0x1 = Transmission request pending
2	TRP2	R	0x0	Transmission Request Pending See above note 0x0 = No transmission request pending 0x1 = Transmission request pending
1	TRP1	R	0x0	Transmission Request Pending See above note 0x0 = No transmission request pending 0x1 = Transmission request pending
0	TRP0	R	0x0	Transmission Request Pending See above note 0x0 = No transmission request pending 0x1 = Transmission request pending

9.4.38 TXBAR Register (Address = 0x10D0) [Reset = 0x00000000]

TXBAR is shown in Figure 9-58 and described in Table 9-64.

Return to the Summary Table.

Tx Buffer Add Request Each Tx Buffer has its own Add Request bit. Writing a 1 will set the corresponding Add Request bit; writing a 0 has no impact. This enables the host to set transmission requests for multiple Tx Buffers with one write to TXBAR. TXBAR bits are set only for those Tx Buffers configured via TXBC. When no Tx scan is running, the bits are reset immediately, else the bits remain set until the Tx scan process has completed.#NOTE#If an add request is applied for a Tx Buffer with pending transmission request (corresponding TXBRP bit is already set), then this add request is ignored#/NOTE#

Figure 9-58. TXBAR Register

31	30	29	28	27	26	25	24
AR31	AR30	AR29	AR28	AR27	AR26	AR25	AR24
RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0
23	22	21	20	19	18	17	16
AR23	AR22	AR21	AR20	AR19	AR18	AR17	AR16
RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0
15	14	13	12	11	10	9	8
AR15	AR14	AR13	AR12	AR11	AR10	AR9	AR8
RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0
7	6	5	4	3	2	1	0
AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0
RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0

Table 9-64. TXBAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AR31	RH/W1S	0x0	Add Request 0x0 = No transmission request added 0x1 = Transmission request added
30	AR30	RH/W1S	0x0	Add Request 0x0 = No transmission request added 0x1 = Transmission request added
29	AR29	RH/W1S	0x0	Add Request 0x0 = No transmission request added 0x1 = Transmission request added
28	AR28	RH/W1S	0x0	Add Request 0x0 = No transmission request added 0x1 = Transmission request added
27	AR27	RH/W1S	0x0	Add Request 0x0 = No transmission request added 0x1 = Transmission request added
26	AR26	RH/W1S	0x0	Add Request 0x0 = No transmission request added 0x1 = Transmission request added
25	AR25	RH/W1S	0x0	Add Request 0x0 = No transmission request added 0x1 = Transmission request added
24	AR24	RH/W1S	0x0	Add Request 0x0 = No transmission request added 0x1 = Transmission request added
23	AR23	RH/W1S	0x0	Add Request 0x0 = No transmission request added 0x1 = Transmission request added

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Table 9-64. TXBAR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	AR22	RH/W1S	0x0	Add Request 0x0 = No transmission request added 0x1 = Transmission request added
21	AR21	RH/W1S	0x0	Add Request 0x0 = No transmission request added 0x1 = Transmission request added
20	AR20	RH/W1S	0x0	Add Request 0x0 = No transmission request added 0x1 = Transmission request added
19	AR19	RH/W1S	0x0	Add Request 0x0 = No transmission request added 0x1 = Transmission request added
18	AR18	RH/W1S	0x0	Add Request 0x0 = No transmission request added 0x1 = Transmission request added
17	AR17	RH/W1S	0x0	Add Request 0x0 = No transmission request added 0x1 = Transmission request added
16	AR16	RH/W1S	0x0	Add Request 0x0 = No transmission request added 0x1 = Transmission request added
15	AR15	RH/W1S	0x0	Add Request 0x0 = No transmission request added 0x1 = Transmission request added
14	AR14	RH/W1S	0x0	Add Request 0x0 = No transmission request added 0x1 = Transmission request added
13	AR13	RH/W1S	0x0	Add Request 0x0 = No transmission request added 0x1 = Transmission request added
12	AR12	RH/W1S	0x0	Add Request 0x0 = No transmission request added 0x1 = Transmission request added
11	AR11	RH/W1S	0x0	Add Request 0x0 = No transmission request added 0x1 = Transmission request added
10	AR10	RH/W1S	0x0	Add Request 0x0 = No transmission request added 0x1 = Transmission request added
9	AR9	RH/W1S	0x0	Add Request 0x0 = No transmission request added 0x1 = Transmission request added
8	AR8	RH/W1S	0x0	Add Request 0x0 = No transmission request added 0x1 = Transmission request added
7	AR7	RH/W1S	0x0	Add Request 0x0 = No transmission request added 0x1 = Transmission request added
6	AR6	RH/W1S	0x0	Add Request 0x0 = No transmission request added 0x1 = Transmission request added
5	AR5	RH/W1S	0x0	Add Request 0x0 = No transmission request added 0x1 = Transmission request added
4	AR4	RH/W1S	0x0	Add Request 0x0 = No transmission request added 0x1 = Transmission request added

Table 9-64. TXBAR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	AR3	RH/W1S	0x0	Add Request 0x0 = No transmission request added 0x1 = Transmission request added
2	AR2	RH/W1S	0x0	Add Request 0x0 = No transmission request added 0x1 = Transmission request added
1	AR1	RH/W1S	0x0	Add Request 0x0 = No transmission request added 0x1 = Transmission request added
0	AR0	RH/W1S	0x0	Add Request 0x0 = No transmission request added 0x1 = Transmission request added

9.4.39 TXBCR Register (Address = 0x10D4) [Reset = 0x00000000]

TXBCR is shown in Figure 9-59 and described in Table 9-65.

Return to the Summary Table.

Each Tx Buffer has its own cancellation request bit. Writing a 1 will set the corresponding Cancellation Request bit; writing a 0 has no impact. This enables the host to set cancellation requests for multiple Tx Buffers with one write to TXBCR. TXBCR bits are only set for those Tx Buffers configured via TXBC. The bits remain set until the corresponding bit of TXBRP is reset#NOTE#This must NOT be used when in CAN FD Light Commander mode#/NOTE#

Figure 9-59. TXBCR Register

31	30	29	28	27	26	25	24
CR31	CR30	CR29	CR28	CR27	CR26	CR25	CR24
RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0
23	22	21	20	19	18	17	16
CR23	CR22	CR21	CR20	CR19	CR18	CR17	CR16
RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0
15	14	13	12	11	10	9	8
CR15	CR14	CR13	CR12	CR11	CR10	CR9	CR8
RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0
7	6	5	4	3	2	1	0
CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0	RH/W1S-0x0

Table 9-65. TXBCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CR31	RH/W1S	0x0	Cancellation Request 0x0 = No cancellation pending 0x1 = Cancellation pending
30	CR30	RH/W1S	0x0	Cancellation Request 0x0 = No cancellation pending 0x1 = Cancellation pending
29	CR29	RH/W1S	0x0	Cancellation Request 0x0 = No cancellation pending 0x1 = Cancellation pending
28	CR28	RH/W1S	0x0	Cancellation Request 0x0 = No cancellation pending 0x1 = Cancellation pending
27	CR27	RH/W1S	0x0	Cancellation Request 0x0 = No cancellation pending 0x1 = Cancellation pending
26	CR26	RH/W1S	0x0	Cancellation Request 0x0 = No cancellation pending 0x1 = Cancellation pending
25	CR25	RH/W1S	0x0	Cancellation Request 0x0 = No cancellation pending 0x1 = Cancellation pending
24	CR24	RH/W1S	0x0	Cancellation Request 0x0 = No cancellation pending 0x1 = Cancellation pending
23	CR23	RH/W1S	0x0	Cancellation Request 0x0 = No cancellation pending 0x1 = Cancellation pending
22	CR22	RH/W1S	0x0	Cancellation Request 0x0 = No cancellation pending 0x1 = Cancellation pending

Table 9-65. TXBCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	CR21	RH/W1S	0x0	Cancellation Request 0x0 = No cancellation pending 0x1 = Cancellation pending
20	CR20	RH/W1S	0x0	Cancellation Request 0x0 = No cancellation pending 0x1 = Cancellation pending
19	CR19	RH/W1S	0x0	Cancellation Request 0x0 = No cancellation pending 0x1 = Cancellation pending
18	CR18	RH/W1S	0x0	Cancellation Request 0x0 = No cancellation pending 0x1 = Cancellation pending
17	CR17	RH/W1S	0x0	Cancellation Request 0x0 = No cancellation pending 0x1 = Cancellation pending
16	CR16	RH/W1S	0x0	Cancellation Request 0x0 = No cancellation pending 0x1 = Cancellation pending
15	CR15	RH/W1S	0x0	Cancellation Request 0x0 = No cancellation pending 0x1 = Cancellation pending
14	CR14	RH/W1S	0x0	Cancellation Request 0x0 = No cancellation pending 0x1 = Cancellation pending
13	CR13	RH/W1S	0x0	Cancellation Request 0x0 = No cancellation pending 0x1 = Cancellation pending
12	CR12	RH/W1S	0x0	Cancellation Request 0x0 = No cancellation pending 0x1 = Cancellation pending
11	CR11	RH/W1S	0x0	Cancellation Request 0x0 = No cancellation pending 0x1 = Cancellation pending
10	CR10	RH/W1S	0x0	Cancellation Request 0x0 = No cancellation pending 0x1 = Cancellation pending
9	CR9	RH/W1S	0x0	Cancellation Request 0x0 = No cancellation pending 0x1 = Cancellation pending
8	CR8	RH/W1S	0x0	Cancellation Request 0x0 = No cancellation pending 0x1 = Cancellation pending
7	CR7	RH/W1S	0x0	Cancellation Request 0x0 = No cancellation pending 0x1 = Cancellation pending
6	CR6	RH/W1S	0x0	Cancellation Request 0x0 = No cancellation pending 0x1 = Cancellation pending
5	CR5	RH/W1S	0x0	Cancellation Request 0x0 = No cancellation pending 0x1 = Cancellation pending
4	CR4	RH/W1S	0x0	Cancellation Request 0x0 = No cancellation pending 0x1 = Cancellation pending
3	CR3	RH/W1S	0x0	Cancellation Request 0x0 = No cancellation pending 0x1 = Cancellation pending

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Table 9-65. TXBCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	CR2	RH/W1S	0x0	Cancellation Request 0x0 = No cancellation pending 0x1 = Cancellation pending
1	CR1	RH/W1S	0x0	Cancellation Request 0x0 = No cancellation pending 0x1 = Cancellation pending
0	CR0	RH/W1S	0x0	Cancellation Request 0x0 = No cancellation pending 0x1 = Cancellation pending

9.4.40 TXBTO Register (Address = 0x10D8) [Reset = 0x00000000]

TXBTO is shown in Figure 9-60 and described in Table 9-66.

Return to the Summary Table.

Each Tx Buffer has its own Transmission Occurred bit. The bits are set when the corresponding TXBRP bit is cleared after a successful transmission. The bits are reset when a new transmission is requested by writing a 1 to the corresponding bit of register TXBAR

Figure 9-60. TXBTO Register

31	30	29	28	27	26	25	24
TO31	TO30	TO29	TO28	TO27	TO26	TO25	TO24
R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0
23	22	21	20	19	18	17	16
TO23	TO22	TO21	TO20	TO19	TO18	TO17	TO16
R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0
15	14	13	12	11	10	9	8
TO15	TO14	TO13	TO12	TO11	TO10	TO9	TO8
R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0
7	6	5	4	3	2	1	0
TO7	TO6	TO5	TO4	TO3	TO2	TO1	TO0
R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0

Table 9-66. TXBTO Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TO31	R	0x0	Transmission Occurred 0x0 = No transmission occurred 0x1 = Transmission occurred
30	TO30	R	0x0	Transmission Occurred 0x0 = No transmission occurred 0x1 = Transmission occurred
29	TO29	R	0x0	Transmission Occurred 0x0 = No transmission occurred 0x1 = Transmission occurred
28	TO28	R	0x0	Transmission Occurred 0x0 = No transmission occurred 0x1 = Transmission occurred
27	TO27	R	0x0	Transmission Occurred 0x0 = No transmission occurred 0x1 = Transmission occurred
26	TO26	R	0x0	Transmission Occurred 0x0 = No transmission occurred 0x1 = Transmission occurred
25	TO25	R	0x0	Transmission Occurred 0x0 = No transmission occurred 0x1 = Transmission occurred
24	TO24	R	0x0	Transmission Occurred 0x0 = No transmission occurred 0x1 = Transmission occurred
23	TO23	R	0x0	Transmission Occurred 0x0 = No transmission occurred 0x1 = Transmission occurred
22	TO22	R	0x0	Transmission Occurred 0x0 = No transmission occurred 0x1 = Transmission occurred

Table 9-66. TXBTO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	TO21	R	0x0	Transmission Occurred 0x0 = No transmission occurred 0x1 = Transmission occurred
20	TO20	R	0x0	Transmission Occurred 0x0 = No transmission occurred 0x1 = Transmission occurred
19	TO19	R	0x0	Transmission Occurred 0x0 = No transmission occurred 0x1 = Transmission occurred
18	TO18	R	0x0	Transmission Occurred 0x0 = No transmission occurred 0x1 = Transmission occurred
17	TO17	R	0x0	Transmission Occurred 0x0 = No transmission occurred 0x1 = Transmission occurred
16	TO16	R	0x0	Transmission Occurred 0x0 = No transmission occurred 0x1 = Transmission occurred
15	TO15	R	0x0	Transmission Occurred 0x0 = No transmission occurred 0x1 = Transmission occurred
14	TO14	R	0x0	Transmission Occurred 0x0 = No transmission occurred 0x1 = Transmission occurred
13	TO13	R	0x0	Transmission Occurred 0x0 = No transmission occurred 0x1 = Transmission occurred
12	TO12	R	0x0	Transmission Occurred 0x0 = No transmission occurred 0x1 = Transmission occurred
11	TO11	R	0x0	Transmission Occurred 0x0 = No transmission occurred 0x1 = Transmission occurred
10	TO10	R	0x0	Transmission Occurred 0x0 = No transmission occurred 0x1 = Transmission occurred
9	TO9	R	0x0	Transmission Occurred 0x0 = No transmission occurred 0x1 = Transmission occurred
8	TO8	R	0x0	Transmission Occurred 0x0 = No transmission occurred 0x1 = Transmission occurred
7	TO7	R	0x0	Transmission Occurred 0x0 = No transmission occurred 0x1 = Transmission occurred
6	TO6	R	0x0	Transmission Occurred 0x0 = No transmission occurred 0x1 = Transmission occurred
5	TO5	R	0x0	Transmission Occurred 0x0 = No transmission occurred 0x1 = Transmission occurred
4	TO4	R	0x0	Transmission Occurred 0x0 = No transmission occurred 0x1 = Transmission occurred
3	TO3	R	0x0	Transmission Occurred 0x0 = No transmission occurred 0x1 = Transmission occurred

Table 9-66. TXBTO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	TO2	R	0x0	Transmission Occurred 0x0 = No transmission occurred 0x1 = Transmission occurred
1	TO1	R	0x0	Transmission Occurred 0x0 = No transmission occurred 0x1 = Transmission occurred
0	TO0	R	0x0	Transmission Occurred 0x0 = No transmission occurred 0x1 = Transmission occurred

9.4.41 TXBCF Register (Address = 0x10DC) [Reset = 0x00000000]

TXBCF is shown in Figure 9-61 and described in Table 9-67.

Return to the Summary Table.

Each Tx Buffer has its own Cancellation Finished bit. The bits are set when the corresponding TXBRP bit is cleared after a cancellation was requested via TXBCR. In case the corresponding TXBRP bit was not set at the point of cancellation, CF is set immediately. The bits are reset when a new transmission is requested by writing a 1 to the corresponding bit of register TXBAR.

Figure 9-61. TXBCF Register

31	30	29	28	27	26	25	24
CF31	CF30	CF29	CF28	CF27	CF26	CF25	CF24
R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0
23	22	21	20	19	18	17	16
CF23	CF22	CF21	CF20	CF19	CF18	CF17	CF16
R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0
15	14	13	12	11	10	9	8
CF15	CF14	CF13	CF12	CF11	CF10	CF9	CF8
R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0
7	6	5	4	3	2	1	0
CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0
R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0

Table 9-67. TXBCF Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CF31	R	0x0	Cancellation Finished 0x0 = No transmit buffer cancellation 0x1 = Transmit buffer cancellation finished
30	CF30	R	0x0	Cancellation Finished 0x0 = No transmit buffer cancellation 0x1 = Transmit buffer cancellation finished
29	CF29	R	0x0	Cancellation Finished 0x0 = No transmit buffer cancellation 0x1 = Transmit buffer cancellation finished
28	CF28	R	0x0	Cancellation Finished 0x0 = No transmit buffer cancellation 0x1 = Transmit buffer cancellation finished
27	CF27	R	0x0	Cancellation Finished 0x0 = No transmit buffer cancellation 0x1 = Transmit buffer cancellation finished
26	CF26	R	0x0	Cancellation Finished 0x0 = No transmit buffer cancellation 0x1 = Transmit buffer cancellation finished
25	CF25	R	0x0	Cancellation Finished 0x0 = No transmit buffer cancellation 0x1 = Transmit buffer cancellation finished
24	CF24	R	0x0	Cancellation Finished 0x0 = No transmit buffer cancellation 0x1 = Transmit buffer cancellation finished
23	CF23	R	0x0	Cancellation Finished 0x0 = No transmit buffer cancellation 0x1 = Transmit buffer cancellation finished
22	CF22	R	0x0	Cancellation Finished 0x0 = No transmit buffer cancellation 0x1 = Transmit buffer cancellation finished

Table 9-67. TXBCF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	CF21	R	0x0	Cancellation Finished 0x0 = No transmit buffer cancellation 0x1 = Transmit buffer cancellation finished
20	CF20	R	0x0	Cancellation Finished 0x0 = No transmit buffer cancellation 0x1 = Transmit buffer cancellation finished
19	CF19	R	0x0	Cancellation Finished 0x0 = No transmit buffer cancellation 0x1 = Transmit buffer cancellation finished
18	CF18	R	0x0	Cancellation Finished 0x0 = No transmit buffer cancellation 0x1 = Transmit buffer cancellation finished
17	CF17	R	0x0	Cancellation Finished 0x0 = No transmit buffer cancellation 0x1 = Transmit buffer cancellation finished
16	CF16	R	0x0	Cancellation Finished 0x0 = No transmit buffer cancellation 0x1 = Transmit buffer cancellation finished
15	CF15	R	0x0	Cancellation Finished 0x0 = No transmit buffer cancellation 0x1 = Transmit buffer cancellation finished
14	CF14	R	0x0	Cancellation Finished 0x0 = No transmit buffer cancellation 0x1 = Transmit buffer cancellation finished
13	CF13	R	0x0	Cancellation Finished 0x0 = No transmit buffer cancellation 0x1 = Transmit buffer cancellation finished
12	CF12	R	0x0	Cancellation Finished 0x0 = No transmit buffer cancellation 0x1 = Transmit buffer cancellation finished
11	CF11	R	0x0	Cancellation Finished 0x0 = No transmit buffer cancellation 0x1 = Transmit buffer cancellation finished
10	CF10	R	0x0	Cancellation Finished 0x0 = No transmit buffer cancellation 0x1 = Transmit buffer cancellation finished
9	CF9	R	0x0	Cancellation Finished 0x0 = No transmit buffer cancellation 0x1 = Transmit buffer cancellation finished
8	CF8	R	0x0	Cancellation Finished 0x0 = No transmit buffer cancellation 0x1 = Transmit buffer cancellation finished
7	CF7	R	0x0	Cancellation Finished 0x0 = No transmit buffer cancellation 0x1 = Transmit buffer cancellation finished
6	CF6	R	0x0	Cancellation Finished 0x0 = No transmit buffer cancellation 0x1 = Transmit buffer cancellation finished
5	CF5	R	0x0	Cancellation Finished 0x0 = No transmit buffer cancellation 0x1 = Transmit buffer cancellation finished
4	CF4	R	0x0	Cancellation Finished 0x0 = No transmit buffer cancellation 0x1 = Transmit buffer cancellation finished
3	CF3	R	0x0	Cancellation Finished 0x0 = No transmit buffer cancellation 0x1 = Transmit buffer cancellation finished

Table 9-67. TXBCF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	CF2	R	0x0	Cancellation Finished 0x0 = No transmit buffer cancellation 0x1 = Transmit buffer cancellation finished
1	CF1	R	0x0	Cancellation Finished 0x0 = No transmit buffer cancellation 0x1 = Transmit buffer cancellation finished
0	CF0	R	0x0	Cancellation Finished 0x0 = No transmit buffer cancellation 0x1 = Transmit buffer cancellation finished

9.4.42 TXBTIE Register (Address = 0x10E0) [Reset = 0x00000000]

TXBTIE is shown in Figure 9-62 and described in Table 9-68.

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Each TX Buffer has its own Transmission Interrupt Enable

Figure 9-62. TXBTIE Register

31	30	29	28	27	26	25	24
TIE31	TIE30	TIE29	TIE28	TIE27	TIE26	TIE25	TIE24
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0
23	22	21	20	19	18	17	16
TIE23	TIE22	TIE21	TIE20	TIE19	TIE18	TIE17	TIE16
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0
15	14	13	12	11	10	9	8
TIE15	TIE14	TIE13	TIE12	TIE11	TIE10	TIE9	TIE8
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0
7	6	5	4	3	2	1	0
TIE7	TIE6	TIE5	TIE4	TIE3	TIE2	TIE1	TIE0
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0

Table 9-68. TXBTIE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TIE31	R/W	0x0	Transmission Interrupt Enable 0x0 = Transmission interrupt disabled 0x1 = Transmission interrupt enabled
30	TIE30	R/W	0x0	Transmission Interrupt Enable 0x0 = Transmission interrupt disabled 0x1 = Transmission interrupt enabled
29	TIE29	R/W	0x0	Transmission Interrupt Enable 0x0 = Transmission interrupt disabled 0x1 = Transmission interrupt enabled
28	TIE28	R/W	0x0	Transmission Interrupt Enable 0x0 = Transmission interrupt disabled 0x1 = Transmission interrupt enabled
27	TIE27	R/W	0x0	Transmission Interrupt Enable 0x0 = Transmission interrupt disabled 0x1 = Transmission interrupt enabled
26	TIE26	R/W	0x0	Transmission Interrupt Enable 0x0 = Transmission interrupt disabled 0x1 = Transmission interrupt enabled
25	TIE25	R/W	0x0	Transmission Interrupt Enable 0x0 = Transmission interrupt disabled 0x1 = Transmission interrupt enabled
24	TIE24	R/W	0x0	Transmission Interrupt Enable 0x0 = Transmission interrupt disabled 0x1 = Transmission interrupt enabled
23	TIE23	R/W	0x0	Transmission Interrupt Enable 0x0 = Transmission interrupt disabled 0x1 = Transmission interrupt enabled
22	TIE22	R/W	0x0	Transmission Interrupt Enable 0x0 = Transmission interrupt disabled 0x1 = Transmission interrupt enabled
21	TIE21	R/W	0x0	Transmission Interrupt Enable 0x0 = Transmission interrupt disabled 0x1 = Transmission interrupt enabled

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Table 9-68. TXBTIE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	TIE20	R/W	0x0	Transmission Interrupt Enable 0x0 = Transmission interrupt disabled 0x1 = Transmission interrupt enabled
19	TIE19	R/W	0x0	Transmission Interrupt Enable 0x0 = Transmission interrupt disabled 0x1 = Transmission interrupt enabled
18	TIE18	R/W	0x0	Transmission Interrupt Enable 0x0 = Transmission interrupt disabled 0x1 = Transmission interrupt enabled
17	TIE17	R/W	0x0	Transmission Interrupt Enable 0x0 = Transmission interrupt disabled 0x1 = Transmission interrupt enabled
16	TIE16	R/W	0x0	Transmission Interrupt Enable 0x0 = Transmission interrupt disabled 0x1 = Transmission interrupt enabled
15	TIE15	R/W	0x0	Transmission Interrupt Enable 0x0 = Transmission interrupt disabled 0x1 = Transmission interrupt enabled
14	TIE14	R/W	0x0	Transmission Interrupt Enable 0x0 = Transmission interrupt disabled 0x1 = Transmission interrupt enabled
13	TIE13	R/W	0x0	Transmission Interrupt Enable 0x0 = Transmission interrupt disabled 0x1 = Transmission interrupt enabled
12	TIE12	R/W	0x0	Transmission Interrupt Enable 0x0 = Transmission interrupt disabled 0x1 = Transmission interrupt enabled
11	TIE11	R/W	0x0	Transmission Interrupt Enable 0x0 = Transmission interrupt disabled 0x1 = Transmission interrupt enabled
10	TIE10	R/W	0x0	Transmission Interrupt Enable 0x0 = Transmission interrupt disabled 0x1 = Transmission interrupt enabled
9	TIE9	R/W	0x0	Transmission Interrupt Enable 0x0 = Transmission interrupt disabled 0x1 = Transmission interrupt enabled
8	TIE8	R/W	0x0	Transmission Interrupt Enable 0x0 = Transmission interrupt disabled 0x1 = Transmission interrupt enabled
7	TIE7	R/W	0x0	Transmission Interrupt Enable 0x0 = Transmission interrupt disabled 0x1 = Transmission interrupt enabled
6	TIE6	R/W	0x0	Transmission Interrupt Enable 0x0 = Transmission interrupt disabled 0x1 = Transmission interrupt enabled
5	TIE5	R/W	0x0	Transmission Interrupt Enable 0x0 = Transmission interrupt disabled 0x1 = Transmission interrupt enabled
4	TIE4	R/W	0x0	Transmission Interrupt Enable 0x0 = Transmission interrupt disabled 0x1 = Transmission interrupt enabled
3	TIE3	R/W	0x0	Transmission Interrupt Enable 0x0 = Transmission interrupt disabled 0x1 = Transmission interrupt enabled
2	TIE2	R/W	0x0	Transmission Interrupt Enable 0x0 = Transmission interrupt disabled 0x1 = Transmission interrupt enabled

Table 9-68. TXBTIE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	TIE1	R/W	0x0	Transmission Interrupt Enable 0x0 = Transmission interrupt disabled 0x1 = Transmission interrupt enabled
0	TIE0	R/W	0x0	Transmission Interrupt Enable 0x0 = Transmission interrupt disabled 0x1 = Transmission interrupt enabled

9.4.43 TXBCIE Register (Address = 0x10E4) [Reset = 0x00000000]

TXBCIE is shown in Figure 9-63 and described in Table 9-69.

Return to the Summary Table.

Each Tx Buffer has its own Cancellation Finished Interrupt Enable

Figure 9-63. TXBCIE Register

31	30	29	28	27	26	25	24
CFIE31	CFIE30	CFIE29	CFIE28	CFIE27	CFIE26	CFIE25	CFIE24
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0
23	22	21	20	19	18	17	16
CFIE23	CFIE22	CFIE21	CFIE20	CFIE19	CFIE18	CFIE17	CFIE16
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0
15	14	13	12	11	10	9	8
CFIE15	CFIE14	CFIE13	CFIE12	CFIE11	CFIE10	CFIE9	CFIE8
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0
7	6	5	4	3	2	1	0
CFIE7	CFIE6	CFIE5	CFIE4	CFIE3	CFIE2	CFIE1	CFIE0
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0

Table 9-69. TXBCIE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CFIE31	R/W	0x0	Cancellation Finished Interrupt Enable 0x0 = Cancellation finished interrupt disabled 0x1 = Cancellation finished interrupt enabled
30	CFIE30	R/W	0x0	Cancellation Finished Interrupt Enable 0x0 = Cancellation finished interrupt disabled 0x1 = Cancellation finished interrupt enabled
29	CFIE29	R/W	0x0	Cancellation Finished Interrupt Enable 0x0 = Cancellation finished interrupt disabled 0x1 = Cancellation finished interrupt enabled
28	CFIE28	R/W	0x0	Cancellation Finished Interrupt Enable 0x0 = Cancellation finished interrupt disabled 0x1 = Cancellation finished interrupt enabled
27	CFIE27	R/W	0x0	Cancellation Finished Interrupt Enable 0x0 = Cancellation finished interrupt disabled 0x1 = Cancellation finished interrupt enabled
26	CFIE26	R/W	0x0	Cancellation Finished Interrupt Enable 0x0 = Cancellation finished interrupt disabled 0x1 = Cancellation finished interrupt enabled
25	CFIE25	R/W	0x0	Cancellation Finished Interrupt Enable 0x0 = Cancellation finished interrupt disabled 0x1 = Cancellation finished interrupt enabled
24	CFIE24	R/W	0x0	Cancellation Finished Interrupt Enable 0x0 = Cancellation finished interrupt disabled 0x1 = Cancellation finished interrupt enabled
23	CFIE23	R/W	0x0	Cancellation Finished Interrupt Enable 0x0 = Cancellation finished interrupt disabled 0x1 = Cancellation finished interrupt enabled
22	CFIE22	R/W	0x0	Cancellation Finished Interrupt Enable 0x0 = Cancellation finished interrupt disabled 0x1 = Cancellation finished interrupt enabled
21	CFIE21	R/W	0x0	Cancellation Finished Interrupt Enable 0x0 = Cancellation finished interrupt disabled 0x1 = Cancellation finished interrupt enabled

Table 9-69. TXBCIE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	CFIE20	R/W	0x0	Cancellation Finished Interrupt Enable 0x0 = Cancellation finished interrupt disabled 0x1 = Cancellation finished interrupt enabled
19	CFIE19	R/W	0x0	Cancellation Finished Interrupt Enable 0x0 = Cancellation finished interrupt disabled 0x1 = Cancellation finished interrupt enabled
18	CFIE18	R/W	0x0	Cancellation Finished Interrupt Enable 0x0 = Cancellation finished interrupt disabled 0x1 = Cancellation finished interrupt enabled
17	CFIE17	R/W	0x0	Cancellation Finished Interrupt Enable 0x0 = Cancellation finished interrupt disabled 0x1 = Cancellation finished interrupt enabled
16	CFIE16	R/W	0x0	Cancellation Finished Interrupt Enable 0x0 = Cancellation finished interrupt disabled 0x1 = Cancellation finished interrupt enabled
15	CFIE15	R/W	0x0	Cancellation Finished Interrupt Enable 0x0 = Cancellation finished interrupt disabled 0x1 = Cancellation finished interrupt enabled
14	CFIE14	R/W	0x0	Cancellation Finished Interrupt Enable 0x0 = Cancellation finished interrupt disabled 0x1 = Cancellation finished interrupt enabled
13	CFIE13	R/W	0x0	Cancellation Finished Interrupt Enable 0x0 = Cancellation finished interrupt disabled 0x1 = Cancellation finished interrupt enabled
12	CFIE12	R/W	0x0	Cancellation Finished Interrupt Enable 0x0 = Cancellation finished interrupt disabled 0x1 = Cancellation finished interrupt enabled
11	CFIE11	R/W	0x0	Cancellation Finished Interrupt Enable 0x0 = Cancellation finished interrupt disabled 0x1 = Cancellation finished interrupt enabled
10	CFIE10	R/W	0x0	Cancellation Finished Interrupt Enable 0x0 = Cancellation finished interrupt disabled 0x1 = Cancellation finished interrupt enabled
9	CFIE9	R/W	0x0	Cancellation Finished Interrupt Enable 0x0 = Cancellation finished interrupt disabled 0x1 = Cancellation finished interrupt enabled
8	CFIE8	R/W	0x0	Cancellation Finished Interrupt Enable 0x0 = Cancellation finished interrupt disabled 0x1 = Cancellation finished interrupt enabled
7	CFIE7	R/W	0x0	Cancellation Finished Interrupt Enable 0x0 = Cancellation finished interrupt disabled 0x1 = Cancellation finished interrupt enabled
6	CFIE6	R/W	0x0	Cancellation Finished Interrupt Enable 0x0 = Cancellation finished interrupt disabled 0x1 = Cancellation finished interrupt enabled
5	CFIE5	R/W	0x0	Cancellation Finished Interrupt Enable 0x0 = Cancellation finished interrupt disabled 0x1 = Cancellation finished interrupt enabled
4	CFIE4	R/W	0x0	Cancellation Finished Interrupt Enable 0x0 = Cancellation finished interrupt disabled 0x1 = Cancellation finished interrupt enabled
3	CFIE3	R/W	0x0	Cancellation Finished Interrupt Enable 0x0 = Cancellation finished interrupt disabled 0x1 = Cancellation finished interrupt enabled
2	CFIE2	R/W	0x0	Cancellation Finished Interrupt Enable 0x0 = Cancellation finished interrupt disabled 0x1 = Cancellation finished interrupt enabled

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Table 9-69. TXBCIE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CFIE1	R/W	0x0	Cancellation Finished Interrupt Enable 0x0 = Cancellation finished interrupt disabled 0x1 = Cancellation finished interrupt enabled
0	CFIE0	R/W	0x0	Cancellation Finished Interrupt Enable 0x0 = Cancellation finished interrupt disabled 0x1 = Cancellation finished interrupt enabled

9.4.44 TXEFC Register (Address = 0x10F0) [Reset = 0x00000000]

TXEFC is shown in Figure 9-64 and described in Table 9-70.

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Figure 9-64. TXEFC Register

31	30	29	28	27	26	25	24
RESERVED		EFWM					
R-0x0		R/WP-0x0					
23	22	21	20	19	18	17	16
RESERVED		EFS					
R-0x0		R/WP-0x0					
15	14	13	12	11	10	9	8
EFSA							
R/WP-0x0							
7	6	5	4	3	2	1	0
EFSA							
R/WP-0x0							

Table 9-70. TXEFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0x0	Reserved
29-24	EFWM	R/WP	0x0	Event FIFO Watermark 0 = Watermark interrupt disabled 1- 32 = Level for Tx Event FIFO watermark interrupt (IR.TEFW) # 62# 32 = Watermark interrupt disabled
23-22	RESERVED	R	0x0	Reserved
21-16	EFS	R/WP	0x0	Event FIFO Size 0 = Tx Event FIFO disabled 1- 32 = Number of Tx Event FIFO elements # 62# 32 = Interpreted as 32
15-0	EFSA	R/WP	0x0	Event FIFO Start Address#NOTE#The MRAM and start address for this register has special consideration. The start address must be word aligned (32-bit) in the MRAM. The 2 least significant bits are ignored on a write to make sure of this behavior. When entering the MRAM start address, the 0x8000 prefix is not necessary. For example, if the desired start address is 0x8634, then the value to enter into bits SA[15:0] must be 0x0634#/NOTE#

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9.4.45 TXEFS Register (Address = 0x10F4) [Reset = 0x00000000]

TXEFS is shown in Figure 9-65 and described in Table 9-71.

Return to the Summary Table.

Figure 9-65. TXEFS Register

31	30	29	28	27	26	25	24
RESERVED						TEFL	TEFF
R-0x0						R-0x0	R-0x0
23	22	21	20	19	18	17	16
RESERVED			EFPI				
R-0x0			R-0x0				
15	14	13	12	11	10	9	8
RESERVED			REFGI				
R-0x0			R-0x0				
7	6	5	4	3	2	1	0
RESERVED		EFFL					
R-0x0		R-0x0					

Table 9-71. TXEFS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0x0	Reserved
25	TEFL	R	0x0	Tx Event FIFO Element Lost This bit is a copy of interrupt flag IR.TEFL. When IR.TEFL is reset, this bit is also reset 0x0 = No Tx Event FIFO element lost 0x1 = Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero
24	TEFF	R	0x0	Tx Event FIFO Full This bit is a copy of interrupt flag IR.TEFF. When IR.TEFF is reset, this bit is also res 0x0 = Tx Event FIFO not full 0x1 = Tx Event FIFO is full
23-21	RESERVED	R	0x0	Reserved
20-16	EFPI	R	0x0	Tx Event FIFO Put Index Tx Event FIFO write index pointer, range 0 to 31
15-13	RESERVED	R	0x0	Reserved
12-8	REFGI	R	0x0	Tx Event FIFO Get Index Tx Event FIFO read index pointer, range 0 to 31
7-6	RESERVED	R	0x0	Reserved
5-0	EFFL	R	0x0	Tx Event FIFO Fill Level Number of elements stored in the Tx Event FIFO, range 0 to 32

9.4.46 TXEFA Register (Address = 0x10F8) [Reset = 0x00000000]

TXEFA is shown in Figure 9-66 and described in Table 9-72.

Return to the Summary Table.

Figure 9-66. TXEFA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											EFAI				
R-0x0																											R0/W-0x0				

Table 9-72. TXEFA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0x0	Reserved
4-0	EFAI	R0/W	0x0	Event FIFO Acknowledge Index After the host has read an element or a sequence of elements from the Tx Event FIFO, it must write the index of the last element read from the Tx Event FIFO to EFAI. This will set the Tx Event FIFO Get Index TXEFS.EFGI to EFAI + 1 and update the Event FIFO Fill Level TXEFS.EFFL

ADVANCE INFORMATION

ADVANCE INFORMATION

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

10.1.1.1 CAN Transceiver Physical Layer Standards:

- ISO 11898-2:2016: High speed medium access unit with low power mode
- ISO 8802-3: CSMA/CD – referenced for collision detection from ISO11898-2
- CAN FD 1.0 Spec and Papers
- Bosch “Configuration of CAN Bit Timing”, Paper from 6th International CAN Conference (ICC), 1999. This is repeated a lot in the DCAN IP CAN Controller spec copied into this system spec.
- SAE J2284-2: High Speed CAN (HSC) for Vehicle Applications at 250 kbps
- SAE J2284-3: High Speed CAN (HSC) for Vehicle Applications at 500 kbps
- Bosch M_CAN Controller Area Network Revision 3.2.1.1 (3/24/2016)

10.1.1.2 EMC requirements:

- SAE J2962-2: US3 requirements for CAN Transceivers
- HW Requirements for CAN, LIN,FR V1.3:

10.1.1.3 Conformance Test requirements:

- HS_TRX_Test_Spec_V_1_0: GIFT / ICT CAN test requirements for High Speed Physical Layer

10.1.1.4 Support Documents

- TCAN45xx Software User's Guide
- “A Comprehensible Guide to Controller Area Network”, Wilfried Voss, Copperhill Media Corporation
- “CAN System Engineering: From Theory to Practical Applications”, 2nd Edition, 2013; Dr. Wolfhard Lawrenz, Springer.

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2026	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

12.1 Packaging Information

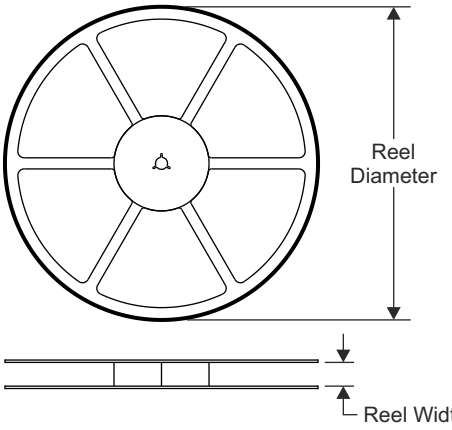
Orderable part number	Status(1)	Material type(2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/Ball material(4)	MSL rating/Peak reflow(5)	Op temp (°C)	Part marking(6)
TCAN4572-Q1	Active	Production	VQFN (RGY)/20	3000 / Tray	RoHS and Green	CU NIPDAU	Level-1-260C-1 YEAR	-40 to 85	TBD

(1) **Status:** For more details on status, see our product life cycle.
(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

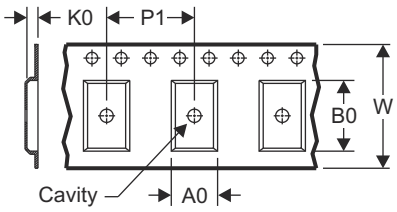
ADVANCE INFORMATION

12.2 Tape and Reel Information

REEL DIMENSIONS

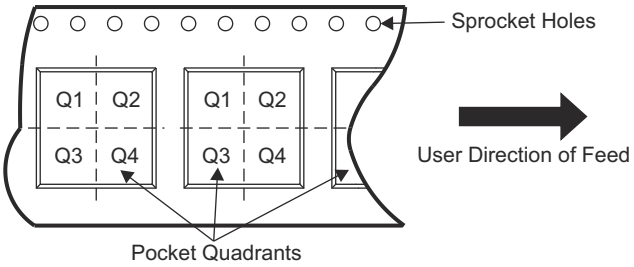


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

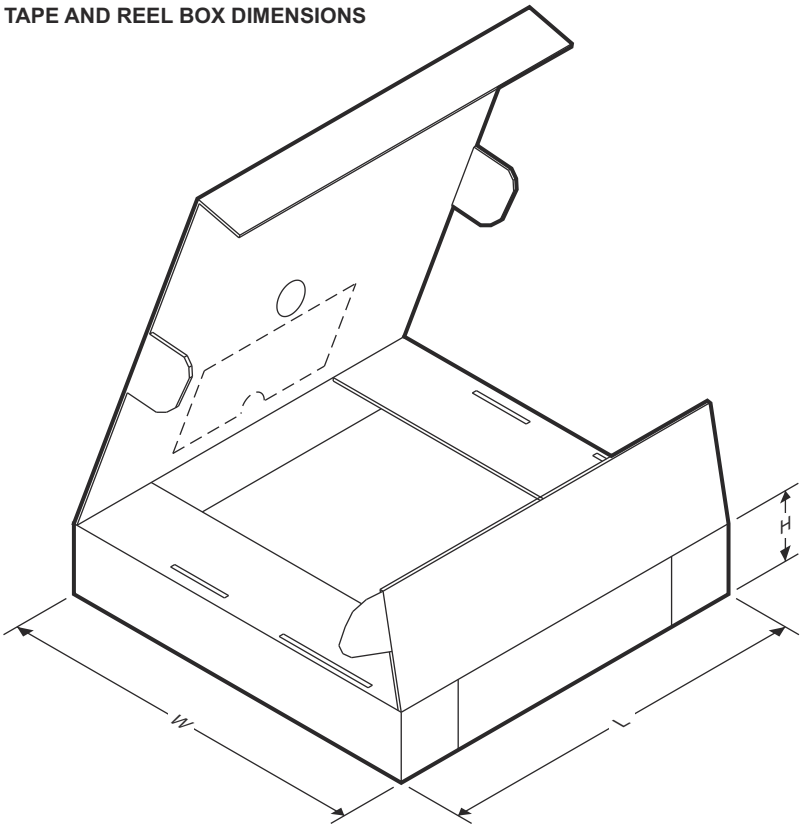


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCAN4572-Q1	SOT	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3

ADVANCE INFORMATION

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



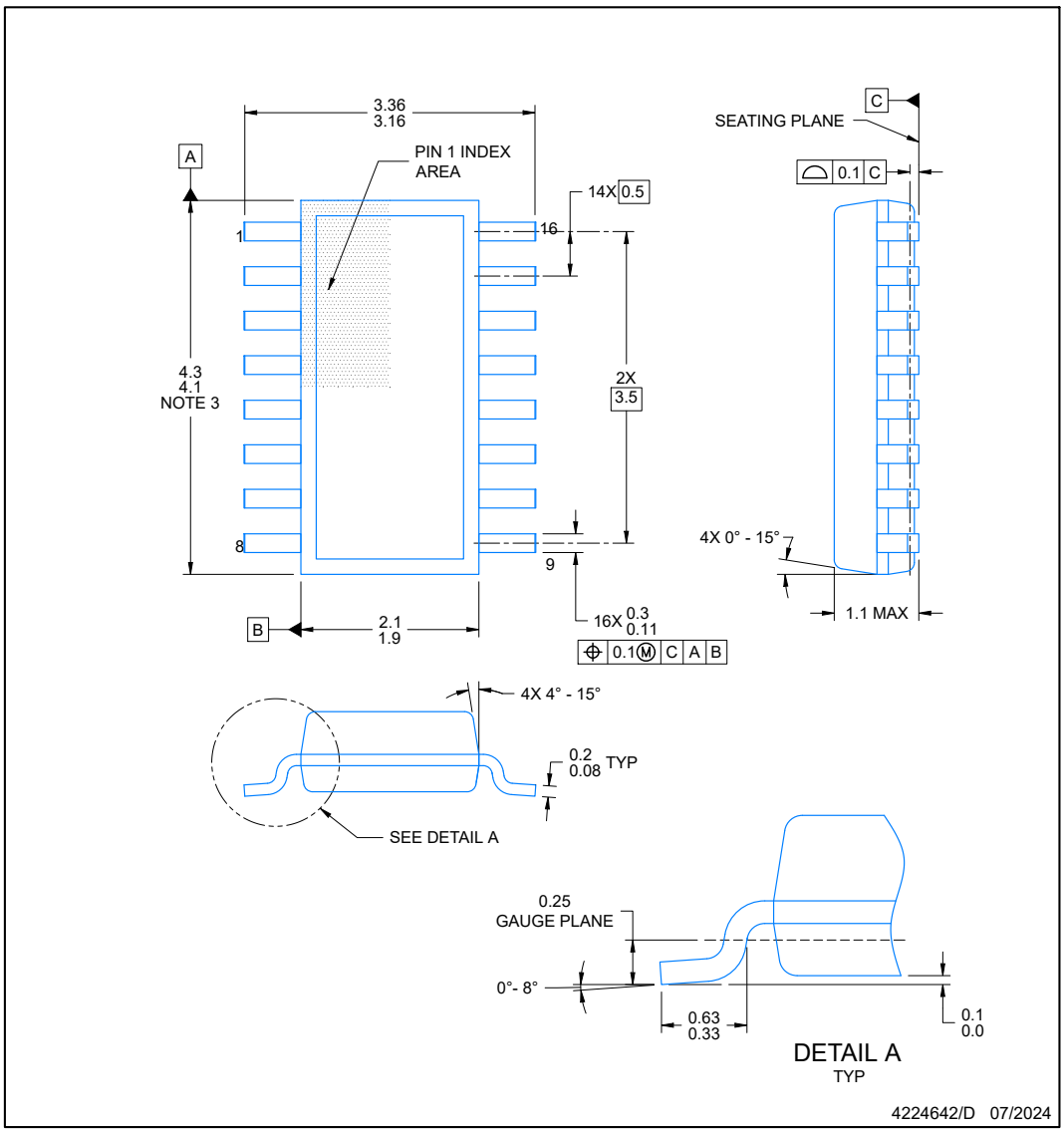
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCAN4572-Q1	SOT	DYY	16	3000	336.6	336.6	31.8

12.3 Mechanical Data

PACKAGE OUTLINE

DYY0016A — **SOT-23-THIN - 1.1 mm max height**

PLASTIC SMALL OUTLINE



NOTES:

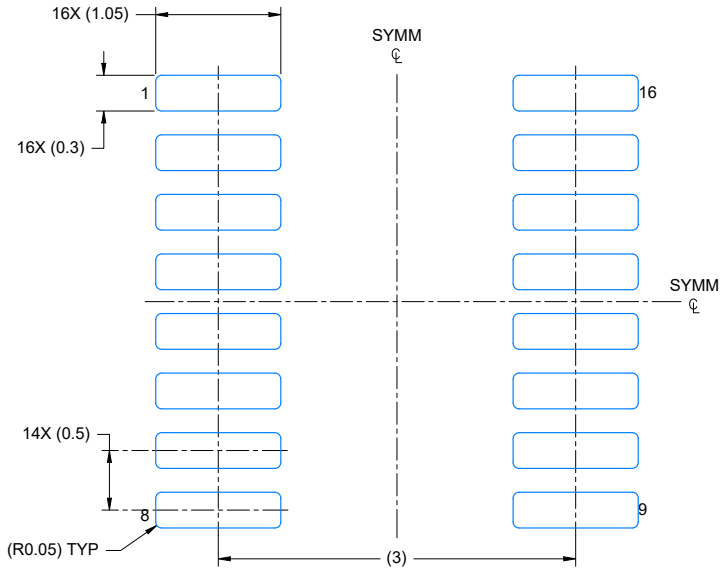
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA

ADVANCE INFORMATION

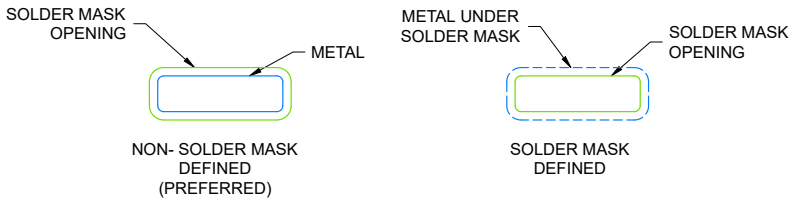
EXAMPLE BOARD LAYOUT

DYY0016A — **SOT-23-THIN - 1.1 mm max height**

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4224642/D 07/2024

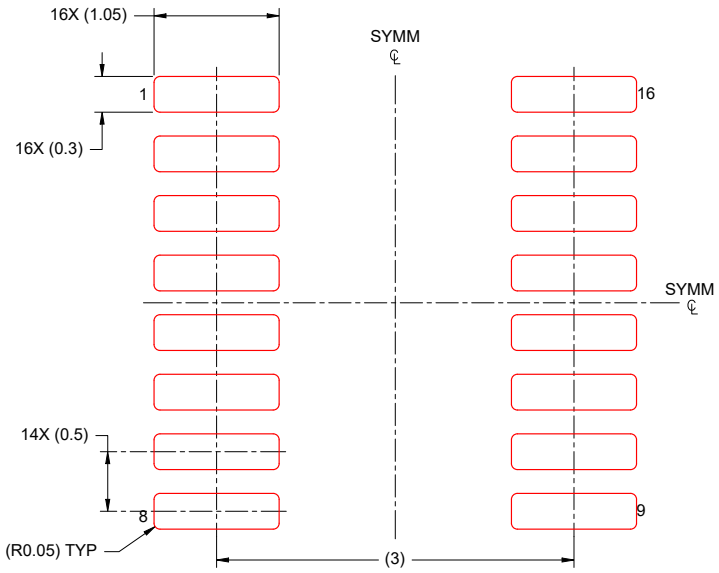
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DYY0016A — **SOT-23-THIN - 1.1 mm max height**

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224642/D 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTCAN4572DYYRQ1	Active	Preproduction	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

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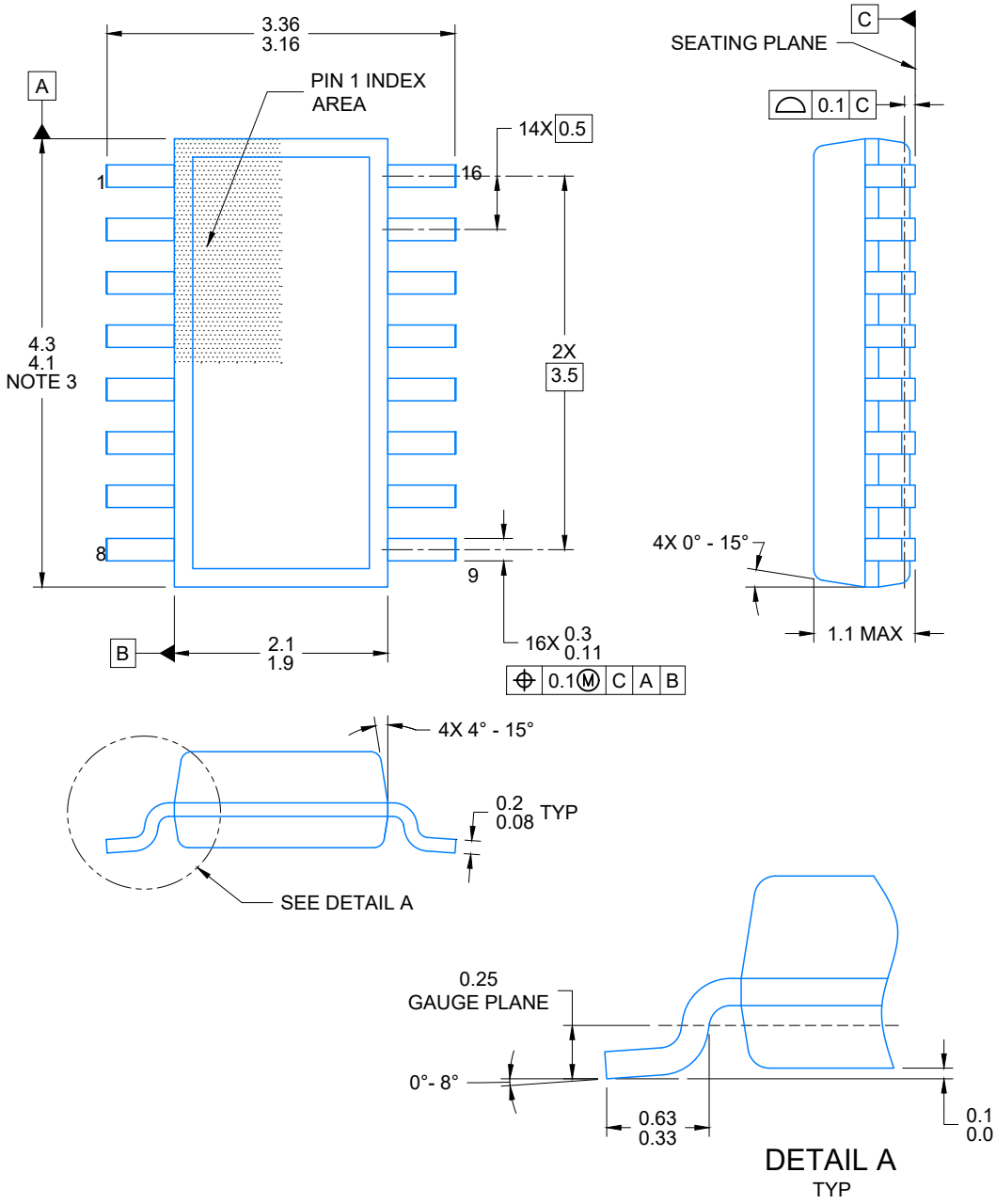
PACKAGE OUTLINE

DYY0016A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



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2. This drawing is subject to change without notice.
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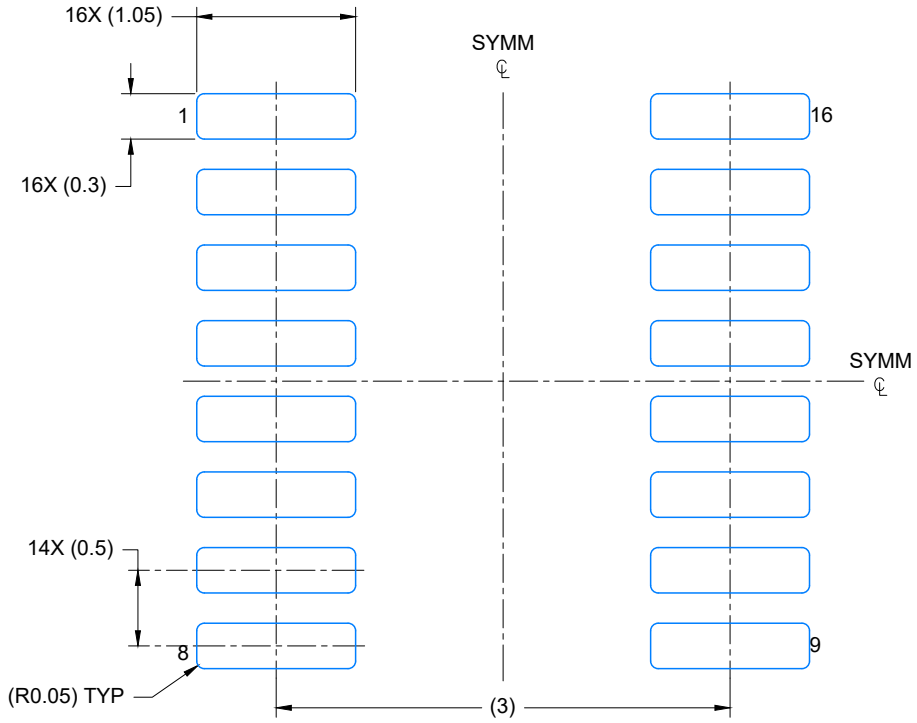
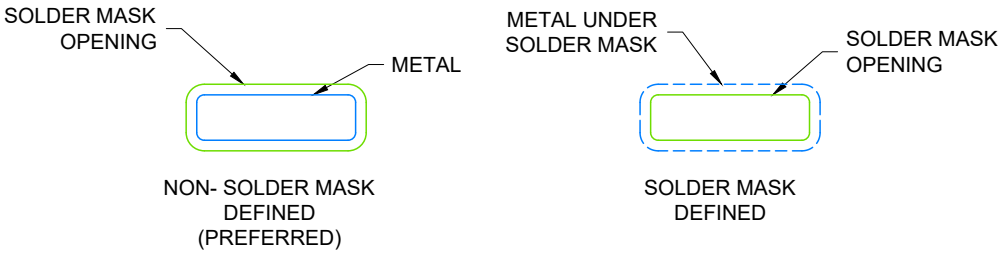


LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4224642/D 07/2024

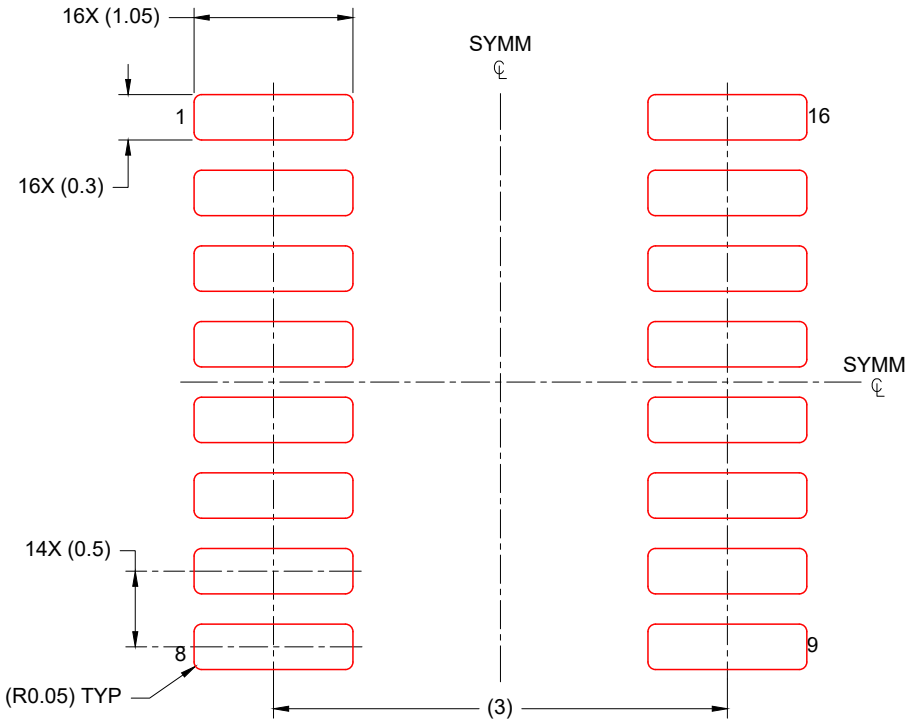
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224642/D 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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