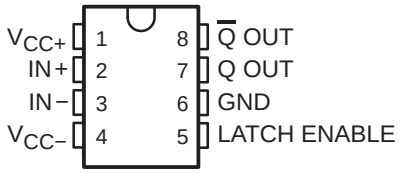
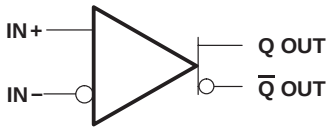
- **Ultra-Fast Operation . . . 10 ns (typ)**
- **Low Positive Supply Current 12.7 mA (Typ)**
- **Operates From a Single 5-V Supply or From a Split ±5-V Supply**
- **Complementary Outputs**
- **Input Common-Mode Voltage Includes Negative Rail**
- **Low Offset Voltage**
- **No Minimum Slew Rate Requirement**
- **Output Latch Capability**
- **Functional Replacement to the LT1116**

D AND PW PACKAGE
(TOP VIEW)



symbol (each comparator)



description

The TL3116 is an ultra-fast comparator designed to interface directly to TTL logic while operating from either a single 5-V power supply or dual ±5-V supplies. The input common-mode voltage extends to the negative rail for ground sensing applications. It features extremely tight offset voltage and high gain for precision applications. It has complementary outputs that can be latched using the LATCH ENABLE terminal. Figure 1 shows the positive supply current of the comparator. The TL3116 only requires 12.7 mA (typical) to achieve a propagation delay of 10 ns.

The TL3116 is a pin-for-pin functional replacement for the LT1116 comparator, offering high-speed operation but consuming much less power.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		CHIP FORM‡ (Y)
	SMALL OUTLINE† (D)	TSSOP (PW)	
0°C to 70°C	TL3116CD	TL3116CPWLE	TL3116Y
−40°C to 85°C	TL3116ID	TL3116IPWLE	—

† The PW packages are available left-ended taped and reeled only.
‡ Chip forms are tested at T_A = 25°C only.

POSITIVE SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

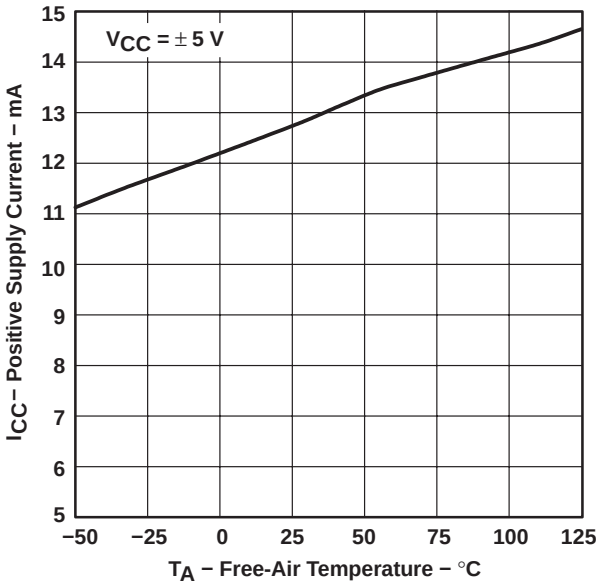


Figure 1

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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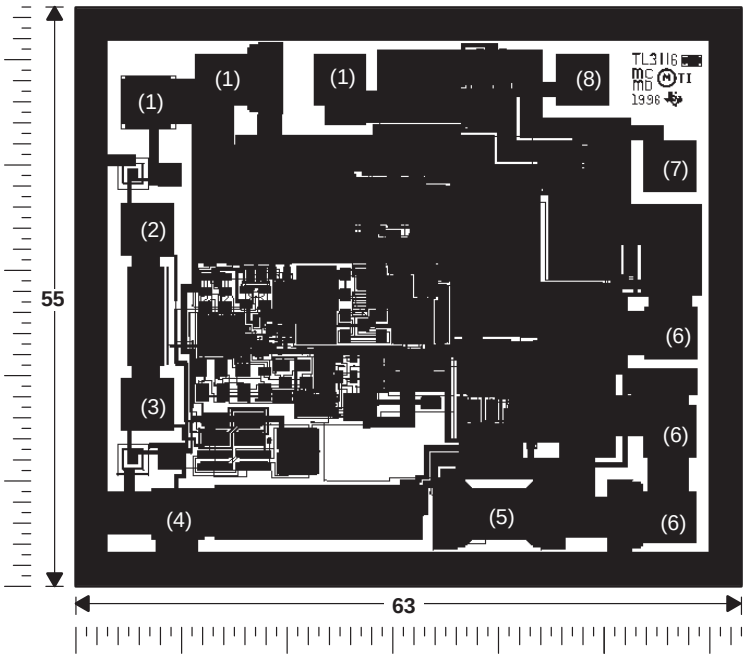
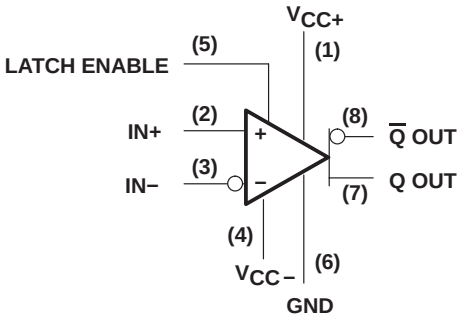
TL3116Y chip information

This chip, when properly assembled, displays characteristics similar to the TL3116C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 10 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

T_J max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

TERMINALS 1 AND 6 CAN BE CONNECTED TO MULTIPLE PADS.

COMPONENT COUNT	
Bipolars	53
MOSFETs	49
Resistors	46
Capacitors	14

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . − 7 V to 7 V
Differential input voltage, V_{ID} (see Note 2) . . . . . 7 V
Input voltage range, V_I . . . . . 7 V
Input voltage, V_I (LATCH ENABLE) . . . . . 7 V
Output current, I_O . . . . . ± 20 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . −40°C to 85°C
Storage temperature range, T_{stg} . . . . . − 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at IN+ with respect to IN−.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
PW	525 mW	4.2 mW/°C	336 mW

electrical characteristics at specified operating free-air temperature, V_{DD} = ±5 V, V_{LE} = 0 (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	TL3116C			TL3116I			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IO}	Input offset voltage	T_A = 25°C		0.5	3		0.5	3	mV
		T_A = full range			3.5			3.5	
α_{VIO}	Temperature coefficient of input offset voltage			−2.5			−2.8		µV/°C
I_{IO}	Input offset current	T_A = 25°C		0.1	0.2		0.1	0.2	µA
		T_A = full range			0.3			0.35	
I_{IB}	Input bias current	T_A = 25°C		0.7	1.1		0.7	1.1	µA
		T_A = full range			1.2			1.5	
V_{ICR}	Common-mode input voltage range	V_{DD} = ±5 V	−5		2.5	−5		2.5	V
		V_{DD} = 5 V	0		2.5	0		2.5	
CMRR	Common-mode rejection ratio	− 5 ≤ V_{IC} ≤ 2.5 V	75	100		75	100		dB
k_{SVR}	Supply-voltage rejection ratio	Positive supply: 4.6 V ≤ +V_{DD} ≤ 5.4 V, T_A = 25°C	60	80		60	80		dB
		Negative supply: − 7 V ≤ −V_{DD} ≤ − 2 V, T_A = 25°C	80	100		80	100		
V_{OL}	Low-level output voltage	$I_{(sink)}$ = 4 mA, V+ ≤ 4.6 V, T_A = 25°C		400	600		400	600	mV
		$I_{(sink)}$ = 10 mA, V+ ≤ 4.6 V, T_A = 25°C		750			750		
V_{OH}	High-level output voltage	V+ ≤ 4.6 V, I_O = 1 mA, T_A = 25°C	3.6	3.9		3.6	3.9		V
		V+ ≤ 4.6 V, I_O = 10 mA, T_A = 25°C	3.4	3.8		3.4	3.8		
I_{CC}	Positive supply current	T_A = full range		12.7	14.7		12.7	15	mA
	Negative supply current		−2.6			−3			
V_{IL}	Low-level input voltage (LATCH ENABLE)				0.8			0.8	V
V_{IH}	High-level input voltage (LATCH ENABLE)		2			2			V
I_{IL}	Low-level input current (LATCH ENABLE)	V_{LE} = 0		0	1		0	1	µA
		V_{LE} = 2 V		24	39		24	45	µA

† Full range for the TL3116C is T_A = 0°C to 70°C. Full range for the TL3116I is T_A = −40°C to 85°C.
‡ All typical values are measures with T_A = 25°C.

switching characteristics, $V_{DD} = \pm 5$ V, $V_{LE} = 0$

PARAMETER		TEST CONDITIONS†		TL3116C			TL3116I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd1}	Propagation delay time‡	ΔV_I = 100 mV, V_{OD} = 5 mV	T_A = 25°C		9.9	12		9.9	12	ns
			T_A = full range		9.9	14		9.9	15	
		ΔV_I = 100 mV, V_{OD} = 20 mV	T_A = 25°C		8.2	10.3		8.2	10.3	
			T_A = full range		8.2	12.7		8.2	13.7	
$t_{sk(p)}$	Pulse skew ($\lvert t_{pd+} - t_{pd-} \rvert$)	ΔV_I = 100 mV, T_A = 25°C	V_{OD} = 5 mV,		0.5			0.5		ns
t_{su}	Setup time, LATCH ENABLE				3.4			3.4		ns

† Full range for the TL3116C is 0°C to 70°C. Full range for the TL3116I is −40°C to 85°C.

‡ t_{pd1} cannot be measured in automatic handling equipment with low values of overdrive. The TL3116 is 100% tested with a 1-V step and 500-mV overdrive at T_A = 25°C only. Correlation tests have shown that t_{pd1} limits given can be ensured with this test, if additional dc tests are performed to ensure that all internal bias conditions are correct. For low overdrive conditions, V_{OS} is added to the overdrive.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_{CC}	Positive supply current	vs Input voltage	2
		vs Frequency	3
		vs Free-air temperature	4
I_{CC}	Negative supply current	vs Free-air temperature	5
t_{pd}	Propagation delay time	vs Overdrive voltage	6
		vs Supply voltage	7
		vs Input impedance	8
		vs Load capacitance	9
		vs Free-air temperature	10
V_{IC}	Common-mode input voltage	vs Free-air temperature	11
V_{IT}	Input threshold voltage (LATCH ENABLE)	vs Free-air temperature	12
V_O	Output voltage	vs Output source current	13
		vs Output sink current	14
I_I	Input current (LATCH ENABLE)	vs Input voltage	15

TYPICAL CHARACTERISTICS

POSITIVE SUPPLY CURRENT vs INPUT VOLTAGE

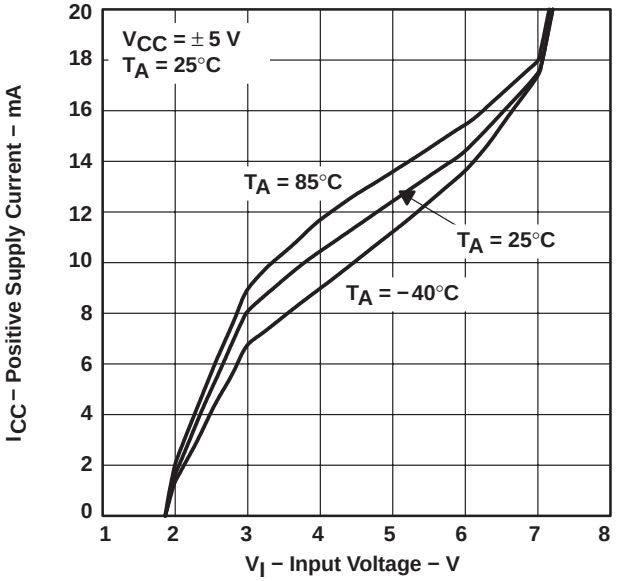


Figure 2

POSITIVE SUPPLY CURRENT vs FREQUENCY

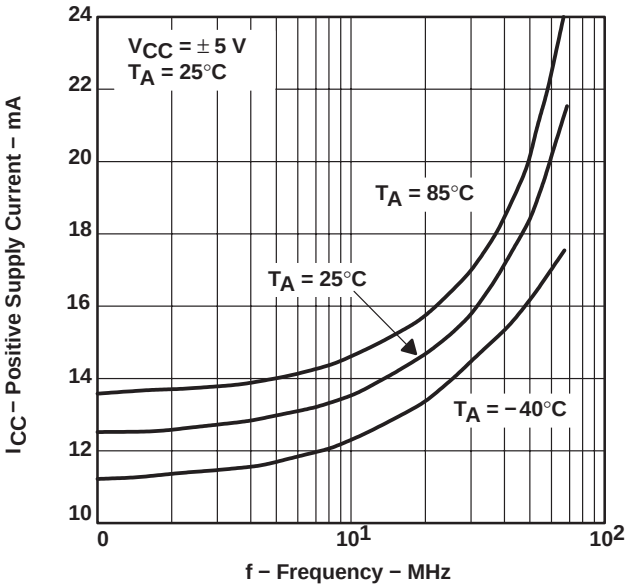


Figure 3

POSITIVE SUPPLY CURRENT vs FREE-AIR TEMPERATURE

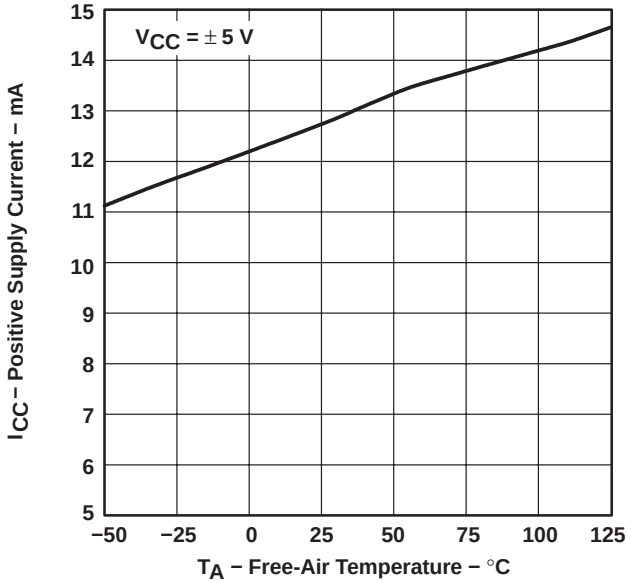


Figure 4

NEGATIVE SUPPLY CURRENT vs FREE-AIR TEMPERATURE

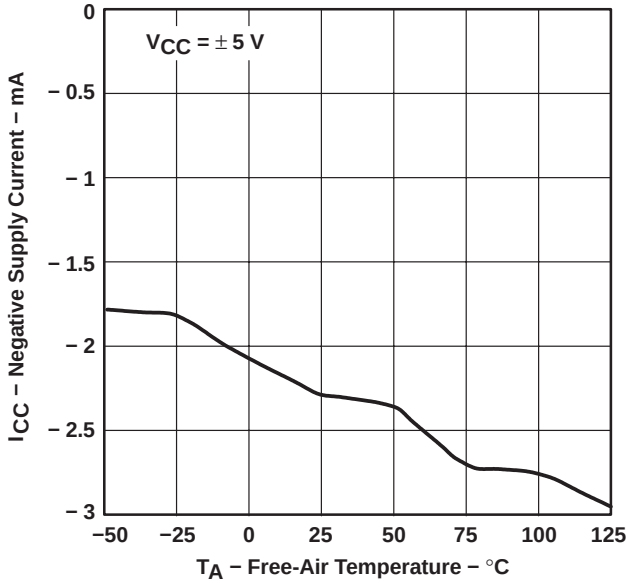


Figure 5

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME vs OVERDRIVE VOLTAGE

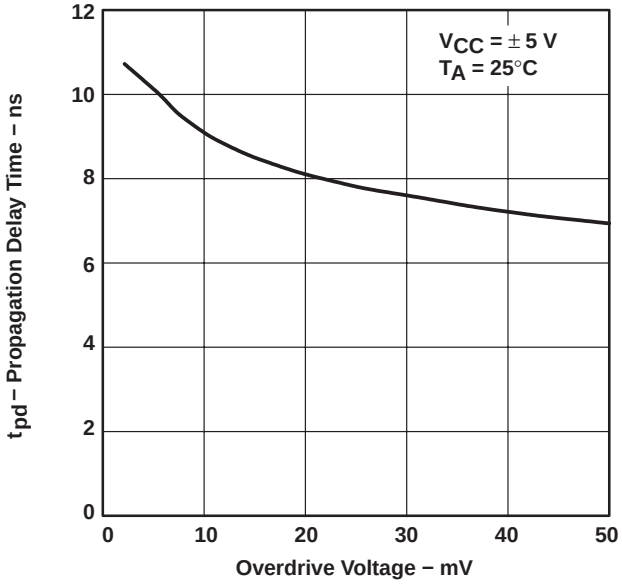


Figure 6

PROPAGATION DELAY TIME vs SUPPLY VOLTAGE

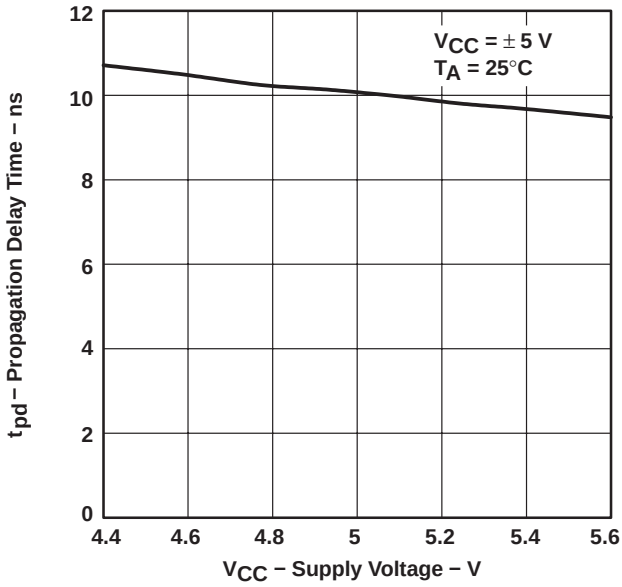


Figure 7

PROPAGATION DELAY TIME vs INPUT IMPEDANCE

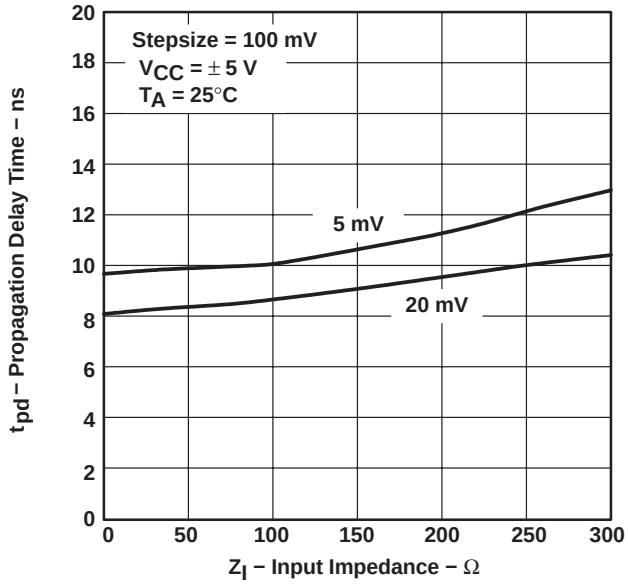


Figure 8

PROPAGATION DELAY TIME vs LOAD CAPACITANCE

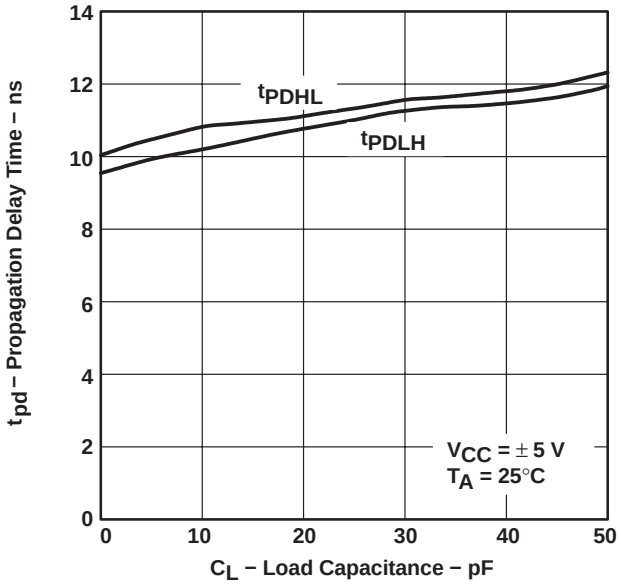


Figure 9

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

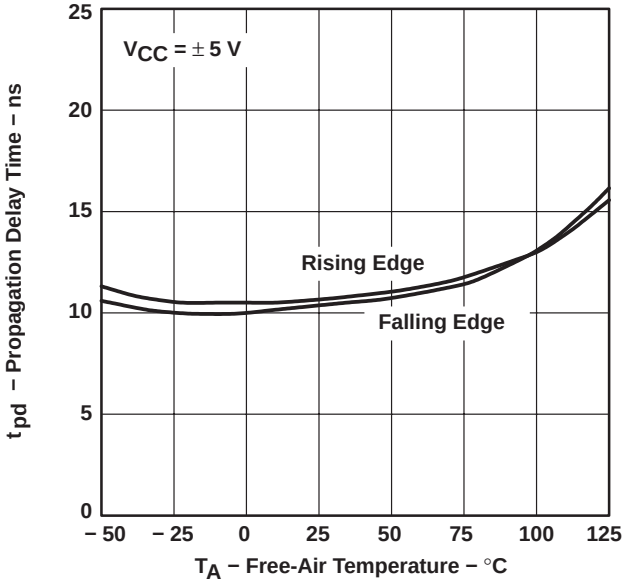


Figure 10

COMMON-MODE INPUT VOLTAGE vs FREE-AIR TEMPERATURE

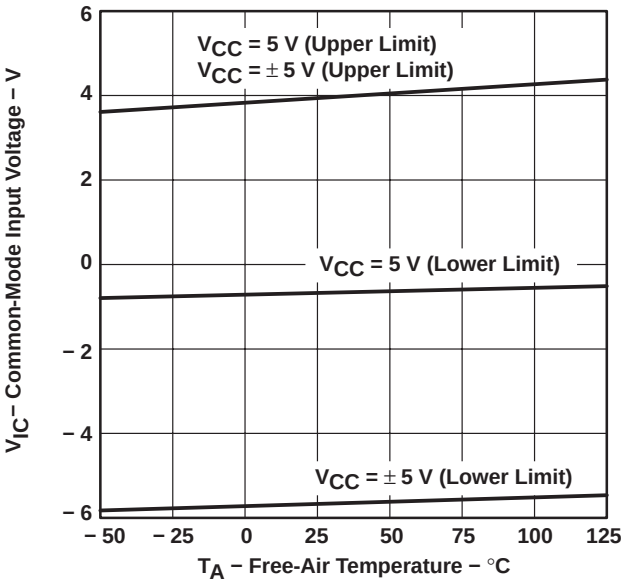


Figure 11

INPUT THRESHOLD VOLTAGE (LATCH ENABLE) vs FREE-AIR TEMPERATURE

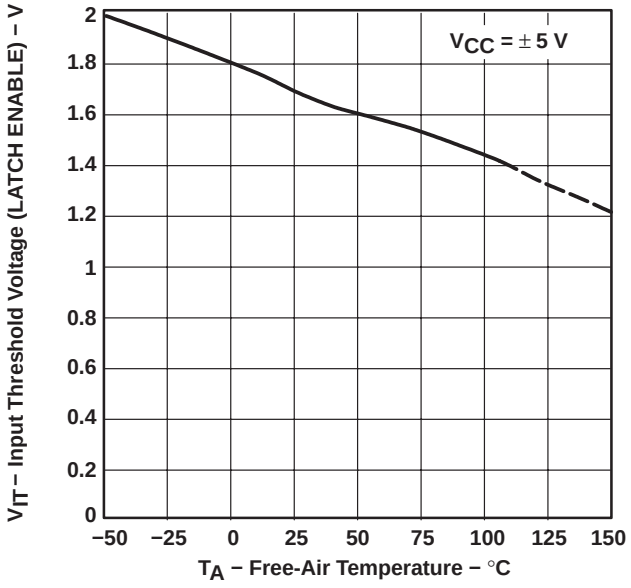


Figure 12

OUTPUT VOLTAGE vs OUTPUT SOURCE CURRENT

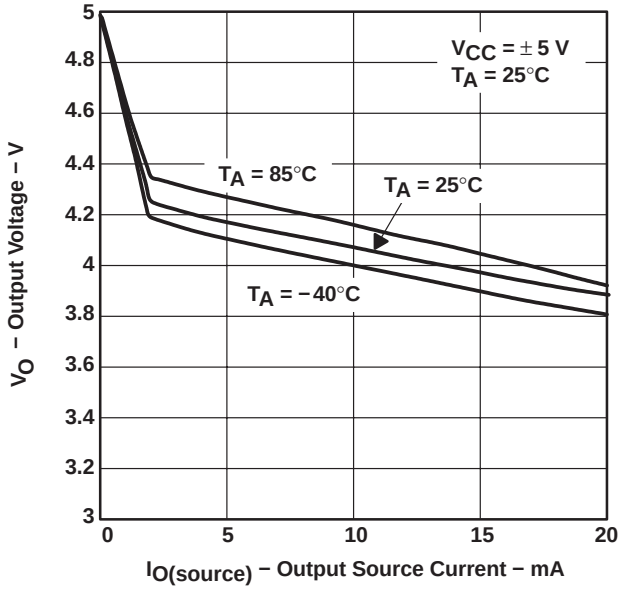


Figure 13

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE vs OUTPUT SINK CURRENT

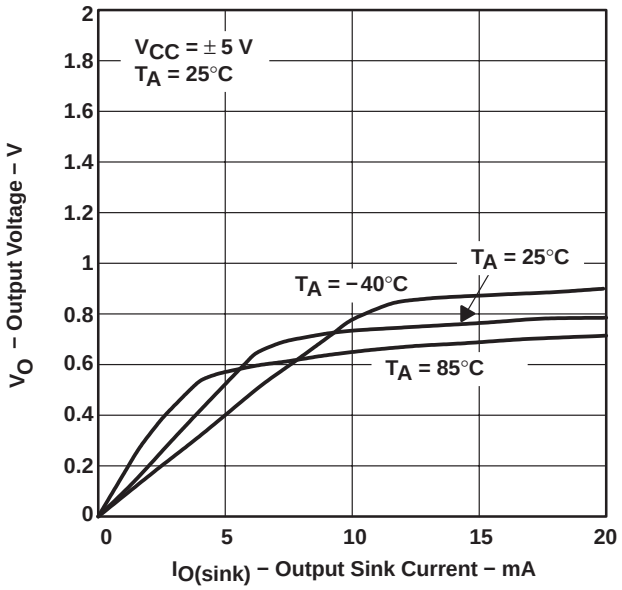


Figure 14

INPUT CURRENT (LATCH ENABLE) vs INPUT VOLTAGE

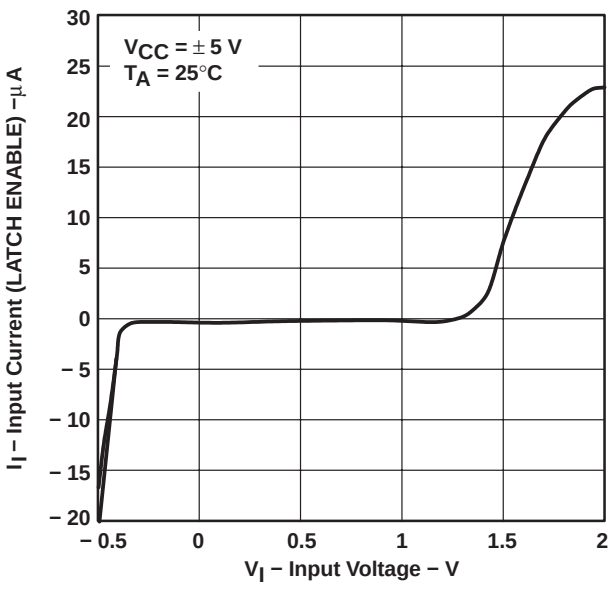


Figure 15

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL3116CD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	3116C
TL3116CDR	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	3116C
TL3116CPW	Obsolete	Production	TSSOP (PW) | 8	-	-	Call TI	Call TI	0 to 70	T3116
TL3116CPWR	Obsolete	Production	TSSOP (PW) | 8	-	-	Call TI	Call TI	0 to 70	T3116
TL3116ID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	3116I
TL3116IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3116I
TL3116IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3116I
TL3116IPW	Obsolete	Production	TSSOP (PW) | 8	-	-	Call TI	Call TI	-40 to 85	Z3116
TL3116IPWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z3116
TL3116IPWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z3116

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

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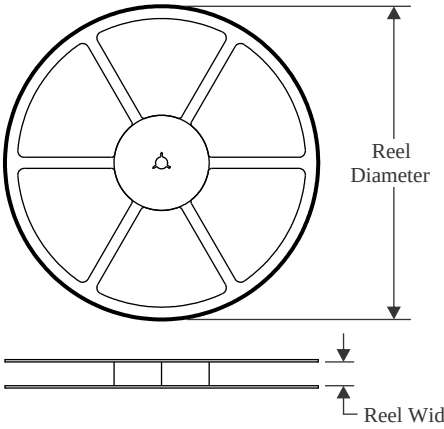
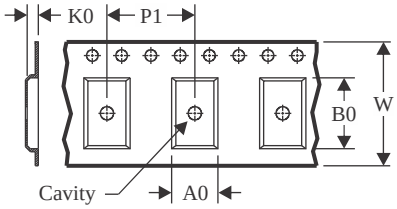
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

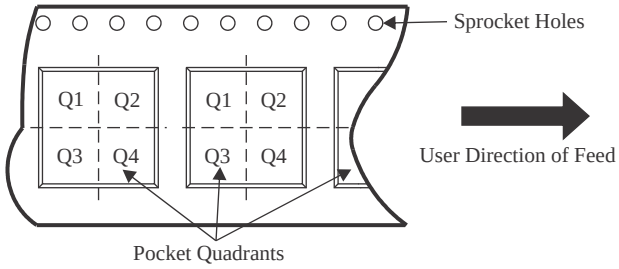


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

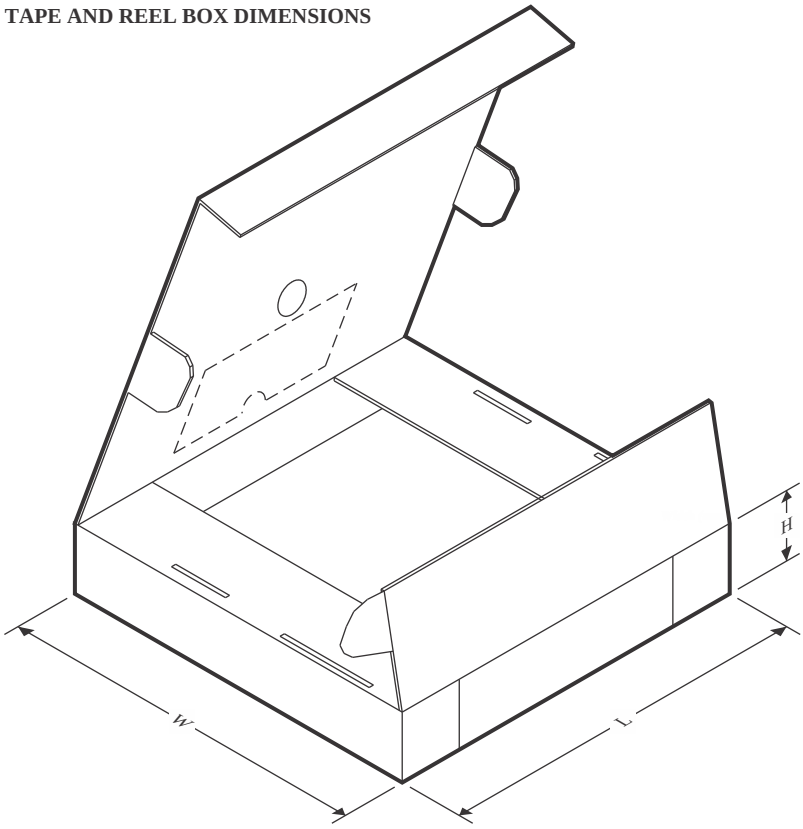
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

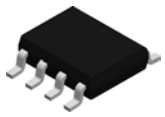
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL3116IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL3116IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL3116IDR	SOIC	D	8	2500	350.0	350.0	43.0
TL3116IPWR	TSSOP	PW	8	2000	353.0	353.0	32.0

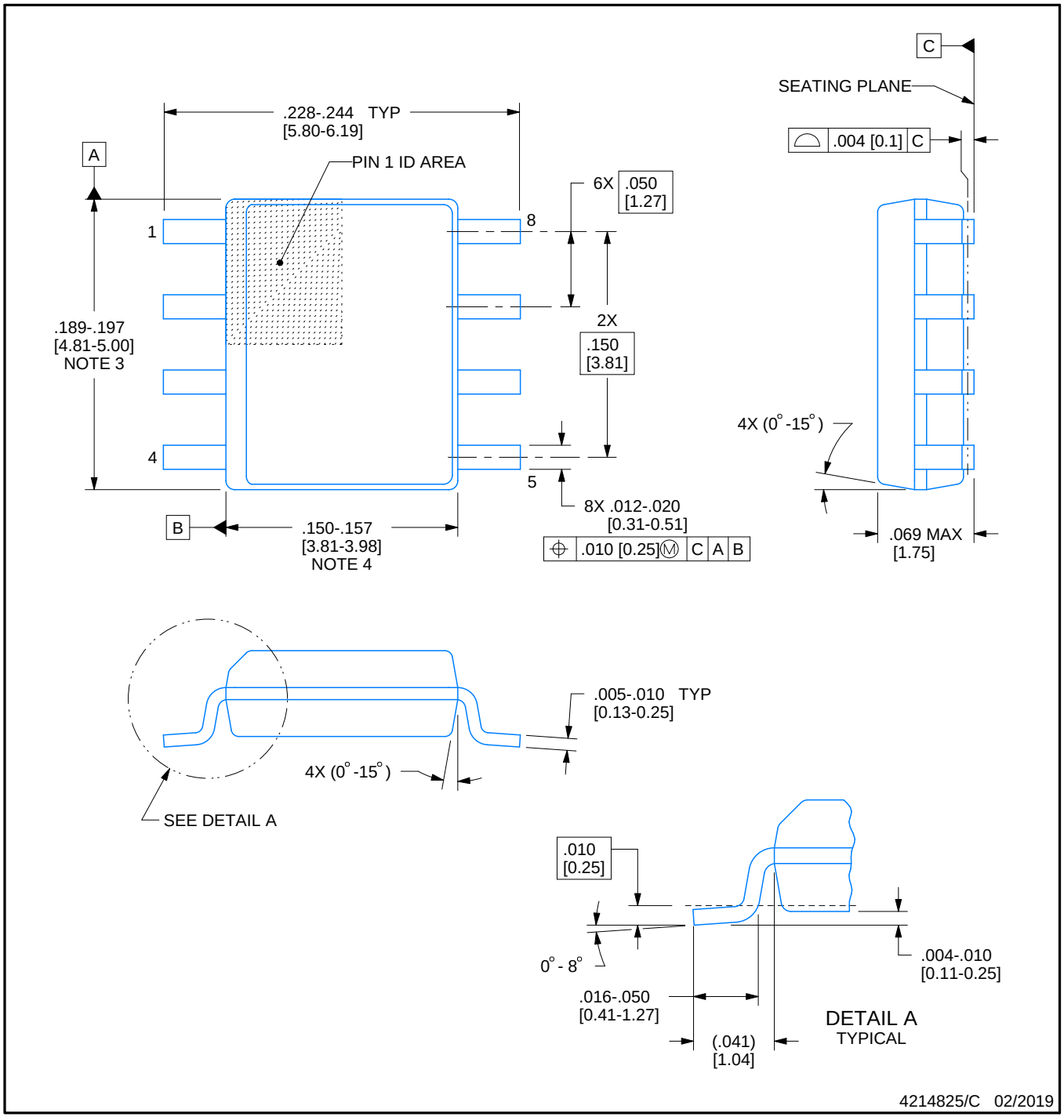


PACKAGE OUTLINE

D0008A

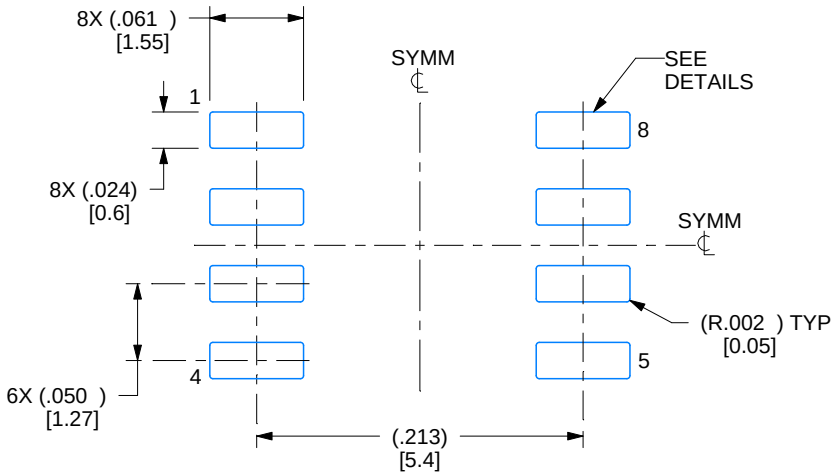
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

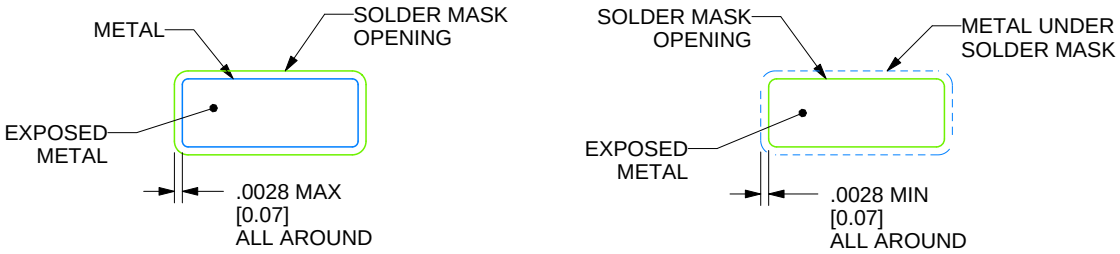


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

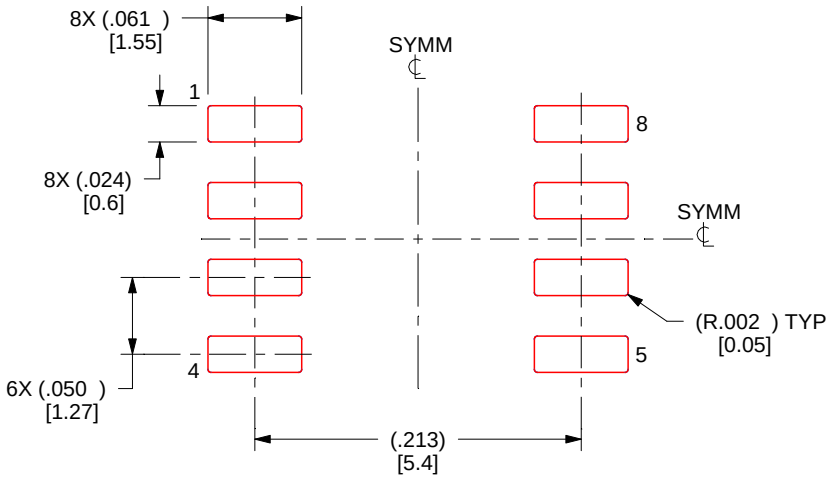
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

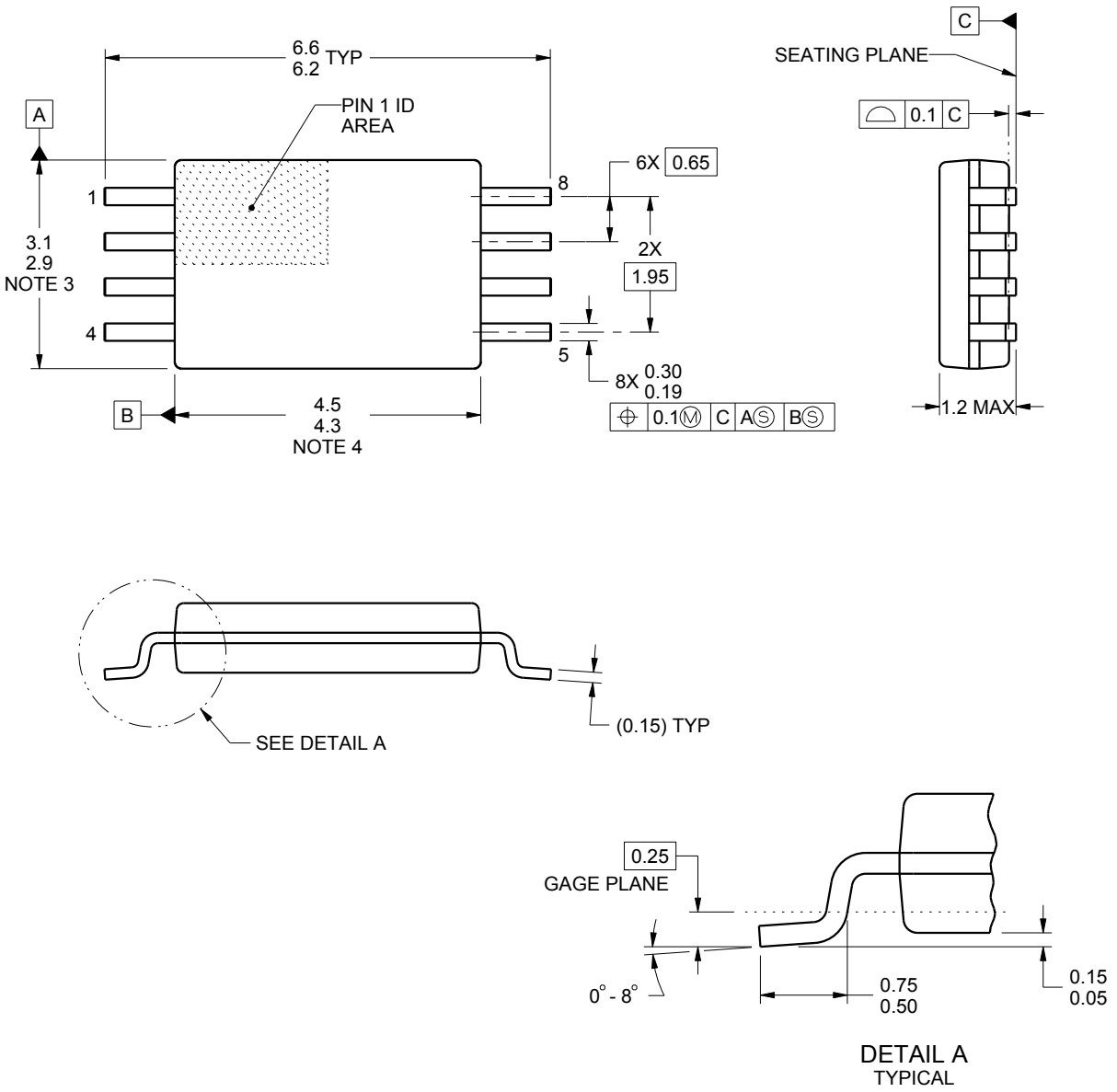
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0008A

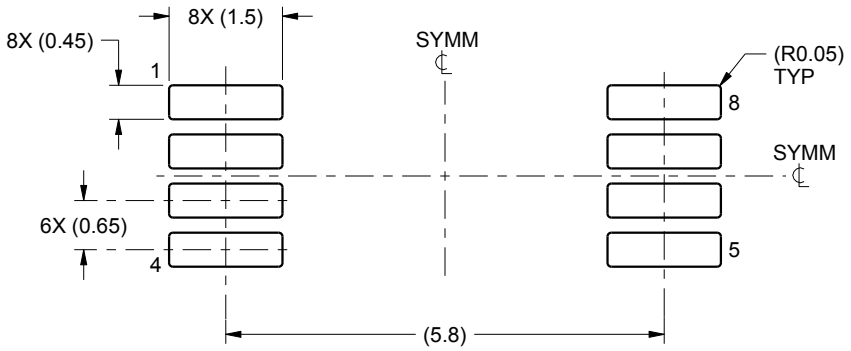
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

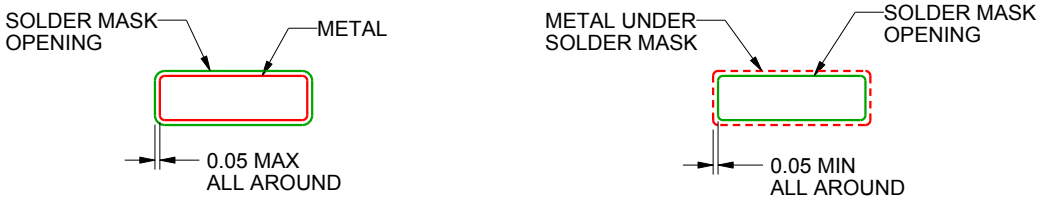


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

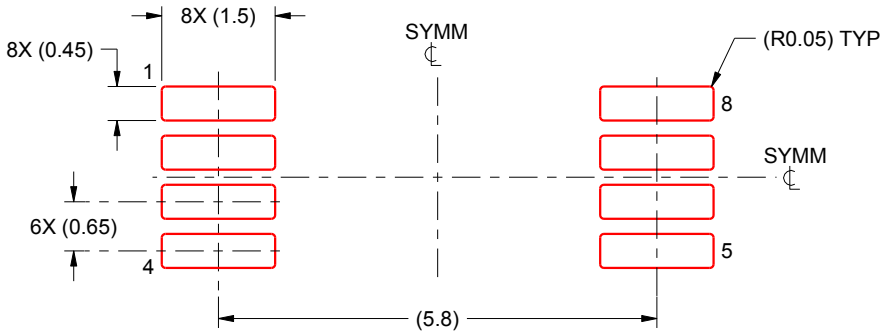


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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