TLV181x-Q1 and TLV182x-Q1 Family of 40V Automotive Rail-to-Rail Input Comparators with Push-Pull or Open-Drain Output Options

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to 125°C ambient operating temperature range
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C3
- Wide 2.4V to 40V supply range
- Low quiescent current 5µA per channel
- Rail-to-Rail input
- Power-On Reset (POR) for known start-up
- Low input offset voltage 500µV
- 420ns typical propagation delay
- Push-pull output option (TLV181x-Q1)
- Open-drain output option (TLV182x-Q1)
- Functional Safety-Capable
  - Documentation available to aid functional safety system design

2 Applications

- HEV/EV and power train
- Infotainment and cluster
- Body control module

3 Description

The TLV181x-Q1 and TLV182x-Q1 are a family of Automotive grade 40 volt single, dual and quad channel comparators with multiple output options. The family offers rail-to-rail inputs with push-pull or open-drain output options. The family has an excellent speed-to-power combination with a propagation delay of 420ns with a full supply voltage range of 2.4V to 40V with a quiescent supply current of only 5µA per channel.

All devices include a Power-On Reset (POR) feature. This makes sure the output is in a known state until the minimum supply voltage has been reached before the output responds to the inputs, thus preventing false outputs during system power-up and power-down.

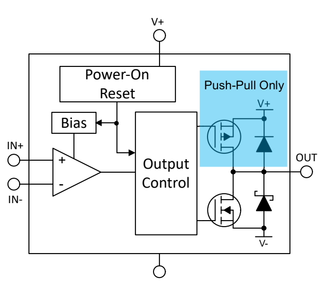
The TLV181x-Q1 comparators have a push-pull output stage capable of sinking and sourcing milliamps of current when controlling an LED or driving a capacitive load such as a MOSFET gate.

The TLV182x-Q1 comparators have an open-drain output stage that can be pulled up to 40V independent of comparator supply voltage.

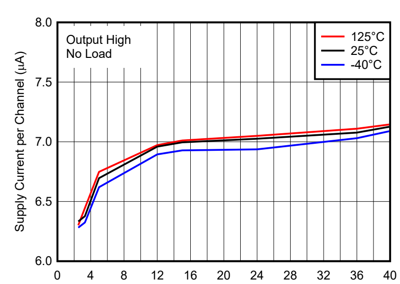
Package Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM) (2)
TLV1811-Q1, TLV1821-Q1 (Single)	SC-70 (5)	1.25mm × 2.00mm
	SOT-23 (5)	1.60mm × 2.90mm
TLV1811L-Q1, TLV1821L-Q1 (Single - alt pinout)	SOT-23 (5)	1.60mm × 2.90mm
TLV1812-Q1, TLV1822-Q1 (Dual)	SOIC (8)	3.91mm × 4.90mm
	TSSOP (8)	3.00mm × 4.40mm
	VSSOP (8)	3.00mm × 3.00mm
	WSON (8) (Preview)	2.00mm × 2.00mm
	SOT-23 (8)	1.60mm × 2.90mm
TLV1814-Q1, TLV1824-Q1 (Quad)	SOIC (14)	3.91mm × 8.65mm
	TSSOP (14)	4.40mm × 5.00mm
	SOT-23 (14)	4.20mm × 2.00mm
	WQFN (16)	3.00mm × 3.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



TLV18xx-Q1 Block Diagram



TLV18xx-Q1 Supply Current vs. Supply Voltage

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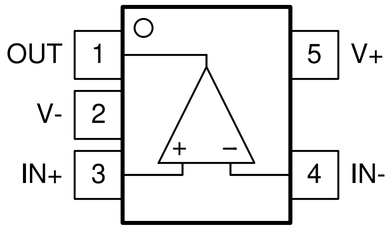
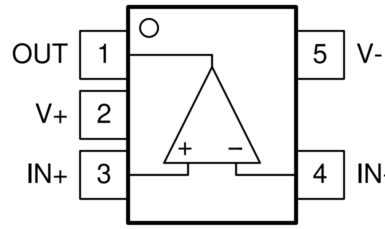
4 Pin Configuration and Functions

Pin Functions:TLV18x1-Q1 TLV18x1L-Q1



TLV18x1-Q1 TLV18x1L-Q1
Standard "North West" pinout
DBV, DCK Packages,
SOT-23-5, SC-70-5
Top View

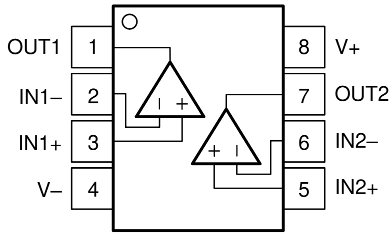


TLV1811L-Q1 and TLV1821L-Q1 DBV Package,
"LMC72x1/TLV72x1 type" pinout with reversed supplies
SOT-23-5,
Top View

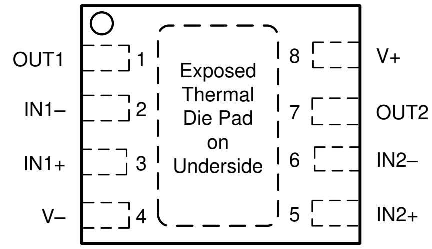
Table 4-1. Pin Functions: TLV1811-Q1, TLV1821-Q1, TLV1811L-Q1 and TLV1821L-Q1

NAME	TLV18x1-Q1		TLV18x1L-Q1	I/O	DESCRIPTION
	PINS		PINS		
	SOT-23	SC-70	SOT-23		
OUT	1	1	1	O	Output
V-	2	2	**5**	-	Negative Supply Voltage
IN+	3	3	3	I	Non-Inverting (+) Input
IN-	4	4	4	I	Inverting (-) Input
V+	5	5	**2**	-	Positive Supply Voltage

Pin Functions:TLV1812-Q1 and TLV1822-Q1



D, DGK, PW, DDF Packages
8-Pin SOIC, VSSOP, TSSOP, SOT-23-8
Top View



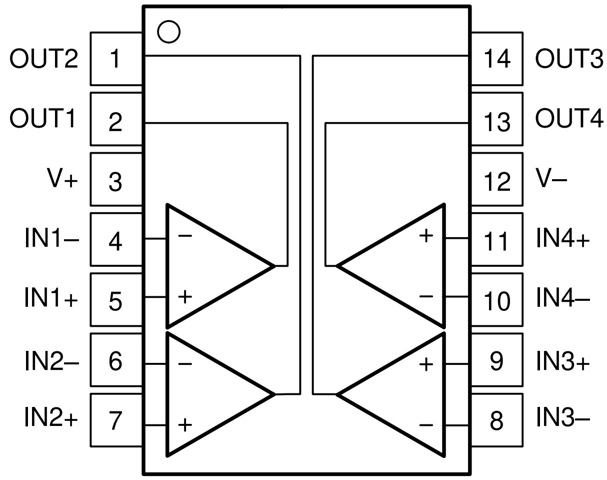
NOTE: Connect exposed thermal pad directly to V- pin.

DSG Package,
8-Pad WSON With Exposed Thermal Pad,
Top View

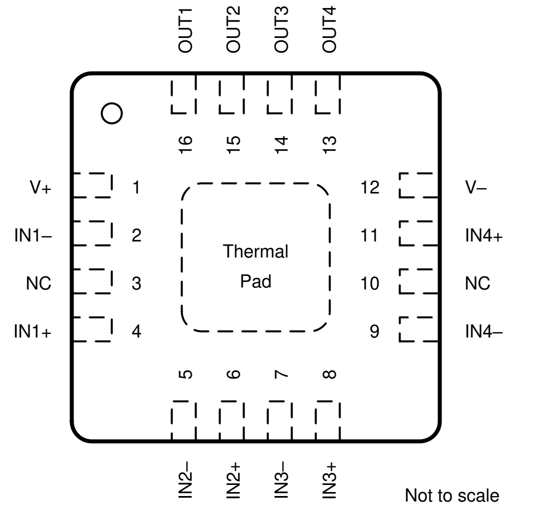
Table 4-2. Pin Functions: TLV1812-Q1 and TLV1822-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT1	1	O	Output pin of the comparator 1
IN1–	2	I	Inverting input pin of comparator 1
IN1+	3	I	Noninverting input pin of comparator 1
V-	4	—	Negative (low) supply
IN2+	5	I	Noninverting input pin of comparator 2
IN2–	6	I	Inverting input pin of comparator 2
OUT2	7	O	Output pin of the comparator 2
V+	8	—	Positive supply
Thermal Pad	—	—	Connect directly to V- pin

Pin Functions: TLV1814-Q1 and TLV1824-Q1



D, PW, DYY Package,
14-Pin SOIC, TSSOP, SOT-23,
Top View



NOTE: Connect exposed thermal pad directly to V- pin.

NOTE: Wettable flank for devices with "W" in package suffix.

RTE Package,
16-Pad WQFN With Exposed Thermal Pad,
Top View

Table 4-3. Pin Functions: TLV1814-Q1 and TLV1824-Q1

PIN			I/O	DESCRIPTION
NAME	SOIC	WQFN		
OUT2(1)	1	15	O	Output pin of the comparator 2
OUT1(1)	2	16	O	Output pin of the comparator1
V+	3	1	—	Positive supply
IN1–	4	2	I	Negative input pin of the comparator 1
IN1+	5	4	I	Positive input pin of the comparator 1
IN2–	6	5	I	Negative input pin of the comparator 2
IN2+	7	6	I	Positive input pin of the comparator 2
IN3–	8	7	I	Negative input pin of the comparator 3
IN3+	9	8	I	Positive input pin of the comparator 3
IN4–	10	9	I	Negative input pin of the comparator 4
IN4+	11	11	I	Positive input pin of the comparator 4
V-	12	12	—	Negative supply
OUT4	13	13	O	Output pin of the comparator 4
OUT3	14	14	O	Output pin of the comparator 3
NC	—	3	—	No Internal Connection - Leave floating or GND
NC	—	10	—	No Internal Connection - Leave floating or GND
Thermal Pad	—	PAD	—	Connect directly to V- pin.

(1) Some manufacturers transpose the names of channels 1 and 2. Electrically the pinouts are identical, just a difference in channel naming convention.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

	MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (V–)	–0.3	42	V
Input pins (IN+, IN–) from (V–) [(2)]	–0.3	(V+) + 0.3	V
Current into Input pins (IN+, IN–)	–10	10	mA
Output (OUT) voltage (Open-Drain) from (V–)[(3)]	–0.3	42	V
Output (OUT) voltage (Push-Pull) from (V–)	–0.3	(V+) + 0.3	V
Output (OUT) current [(4)] [(5)] [(6)]	-10	10	mA
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings can cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input terminals are diode-clamped to (V–). Input signals that can swing more than 0.3V beyond the supply rails must be current-limited to 10mA or less.
(3) Output (OUT) for open drain can be greater than (V+) and inputs (IN+, IN–) as long as within the –0.3V to 42V range
(4) The output is diode-clamped to (V-) for both output options, and diode clamped to (V+) for the push-pull output option. The open drain version does not have a clamp to V+. Please see the *Outputs* and *ESD Protection* section of the *Application Information* Section for more information.
(5) Output sinking and sourcing current is internally limited to <35mA when operating within the Absolute Maximum output voltage limits. The Absolute Maximum Output Current limit specified here is the maximum current through the clamp structure when exceeding the supply voltage below (V-) for both output options, or above (V+) for the push-pull option.
(6) Short-circuit from output to (V–) or (V+). Continuous output short circuits at elevated supply voltages can result in excessive heating and exceeding the maximum allowed junction temperature, leading to eventual device destruction.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[(1)]	±2000	V
		Charged-device model (CDM), per AEC Q100-0111	±1000	
		Charged-device model (CDM), per AEC Q100-0111, TLV1822-Q1 Only	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (V–)		2.4	40	V
Input voltage range from (V–)		–0.2	(V+) + 0.2	V
Output voltage range from (V–)	Open Drain	–0.2	40	V
Output voltage range from (V–)	Push Pull	–0.2	(V+) + 0.2	V
Ambient temperature, T_A		–40	125	°C

5.4 Thermal Information - Single

THERMAL METRIC[(1)]		TLV18x1-Q1		UNIT
		DCK (SC-70)	DBV (SOT-23)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	226.0	203.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	129.5	105.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	78.6	106.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	51.5	54.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	78.3	106.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	–	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Thermal Information - Dual

THERMAL METRIC[(1)]		TLV18x2-Q1					UNIT
		D (SOIC)	PW (TSSOP)	DDF (SOT-23)	DSG (WSON)	DGK (VSSOP)	
		8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	136.1	187.5	170.4	79.9	178.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	76.8	76.7	90.3	100.1	66.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	79.7	118.1	88.1	46.4	100.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	26.8	14.4	7.5	5.3	9.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	78.9	116.4	87.6	46.4	98.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	–	–	21.6	–	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.6 Thermal Information - Quad

THERMAL METRIC[(1)]		TLV18x4-Q1				UNIT
		D (SOIC)	PW (TSSOP)	DYY (SOT-23-THN)	RTE (WQFN)	
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	104.2	124.1	119.9	53.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60.3	52.4	60.6	58.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.2	67.2	79.0	29.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	20.7	7.5	3.3	2.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	59.8	66.6	41.2	28.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	–	–	13.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.7 Electrical Characteristics

For V_S (Total Supply Voltage) = (V+) – (V–) = 12V, V_{CM} = V_S / 2 at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage		–3	±0.5	3	mV
V_{OS}	Input offset voltage	T_A = –40°C to +125°C	–4		4	mV
dV_{IO}/dT	Input offset voltage drift	T_A = –40°C to +125°C		±1.2		µV/°C
PSRR	Power supply rejection ratio	V_S = 2.4V to 40V, V_{CM} = (V–)		100		dB
POWER SUPPLY						
I_Q	Quiescent current, No Load	Output Low, T_A = 25°C TLV1811-Q1 Only		6	7.5	µA
		Output Low, T_A = –40°C to +125°C TLV1811-Q1 Only			8.5	
		Output High, T_A = 25°C TLV1811-Q1 Only		8	10	
		Output High, T_A = –40°C to +125°C TLV1811-Q1 Only			11	
I_Q	Quiescent current per comparator, No Load	Output Low, T_A = 25°C		6	7.5	µA
		Output Low, T_A = –40°C to +125°C			8.5	
		Output High, T_A = 25°C		7	9	
		Output High, T_A = –40°C to +125°C			10	
V_{POR}	Power On Reset Voltage			1.7		V
INPUT BIAS CURRENT						
I_B	Input bias current			150		fA
I_B	Input bias current	T_A = –40°C to +125°C	–1.2		1.2	nA
I_{OS}	Input offset current			10		fA
INPUT CAPACITANCE						
C_{ID}	Input Capacitance, Differential			2		pF
C_{IC}	Input Capacitance, Common Mode			8		pF
INPUT COMMON MODE RANGE						
$V_{CM\text{-}Range}$	Common-mode voltage range	V_S = 2.4V to 40V T_A = –40°C to +125°C	(V–) – 0.2		(V+) + 0.2	V
OUTPUT						
V_{OL}	Voltage swing from (V–)	I_{SINK} = 4mA T_A = –40°C to +125°C			250	mV
V_{OH}	Voltage swing from (V+) (for Push-Pull only)	I_{SOURCE} = 4mA T_A = –40°C to +125°C			250	mV
I_{LKG}	Open-drain output leakage current	V_{ID} = +0.1V, V_{PULLUP} = (V+) T_A = –40°C to +125°C		0.1		nA
I_{OL}	Short-circuit current	Sinking	15	30		mA
I_{OH}	Short-circuit current	Sourcing (for Push-Pull only)	15	30		mA

5.8 Switching Characteristics

For V_S (Total Supply Voltage) = (V+) – (V–) = 12V, V_{CM} = V_S / 2 at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
T_{PD-HL}	Propagation delay time, high-to-low	V_{OD} = 10mV, C_L = 50pF		900		ns
T_{PD-HL}	Propagation delay time, high-to-low	V_{OD} = 100mV, C_L = 50pF		450		ns
T_{PD-LH}	Propagation delay time, low-to-high, push-pull output	V_{OD} = 10mV, C_L = 50pF		900		ns
T_{PD-LH}	Propagation delay time, low-to-high, push-pull output	V_{OD} = 100mV, C_L = 50pF		420		ns
T_{RISE}	Output Rise Time, 20% to 80%, push-pull output	C_L = 50pF		15		ns
T_{FALL}	Output Fall Time, 80% to 20%	C_L = 50pF		15		ns
F_{TOGGLE}	Toggle Frequency	V_{ID} = 100mV, C_L = 50pF		500		kHz
POWER ON TIME						
P_{ON}	Power on-time			200		µs

6 Typical Characteristics

T_A = 25°C, V_S = 12V, R_{PULLUP} = 2.5k, C_L = 20pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

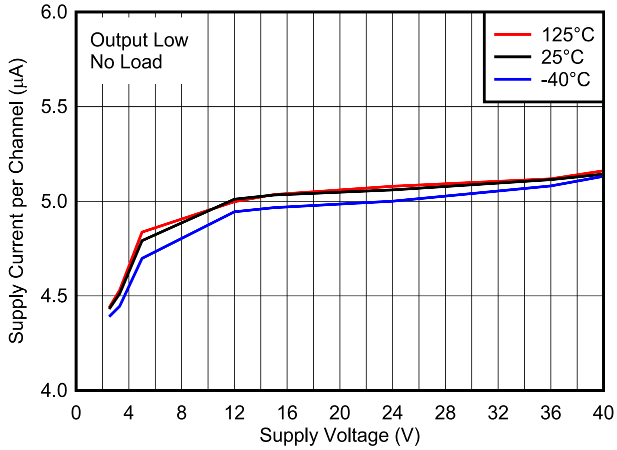


Figure 6-1. Supply Current per Channel vs. Supply Voltage, Output Low

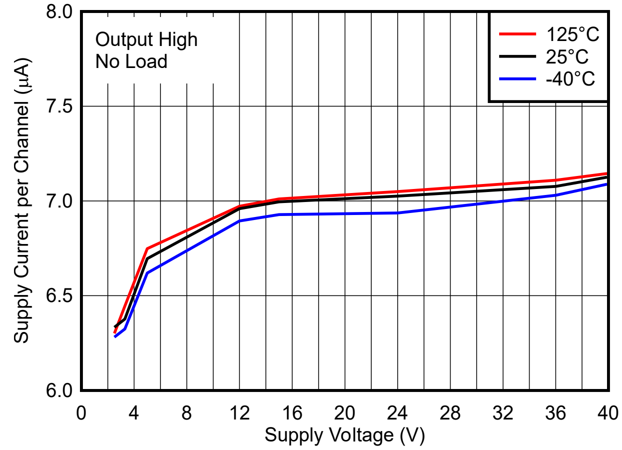


Figure 6-2. Supply Current per Channel vs. Supply Voltage, Output High

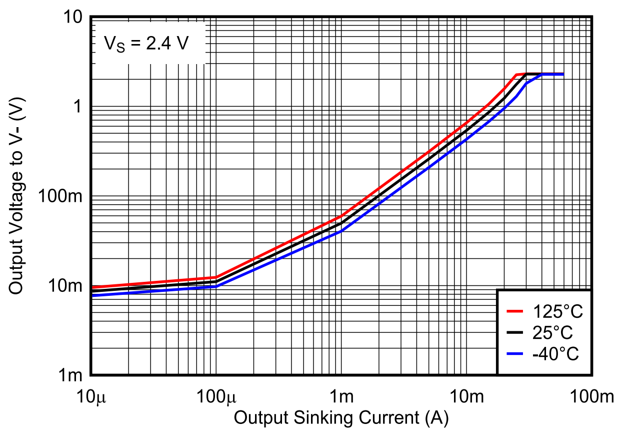


Figure 6-3. Output Voltage vs. Output Sinking Current, 2.4V

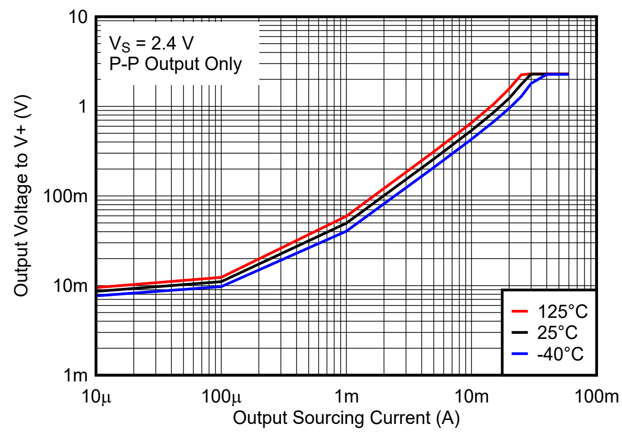


Figure 6-4. Output Voltage vs. Output Sourcing Current, 2.4V

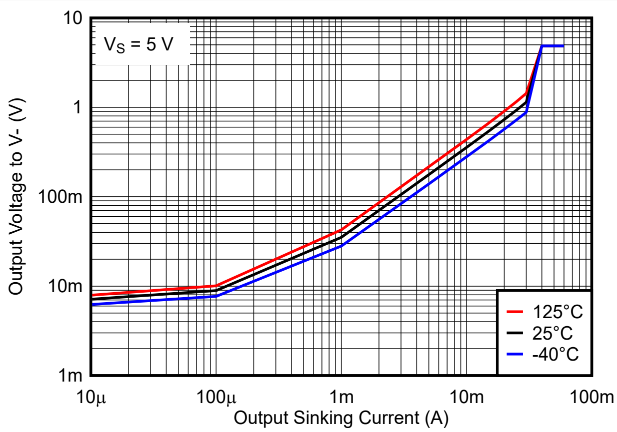


Figure 6-5. Output Voltage vs. Output Sinking Current, 5V

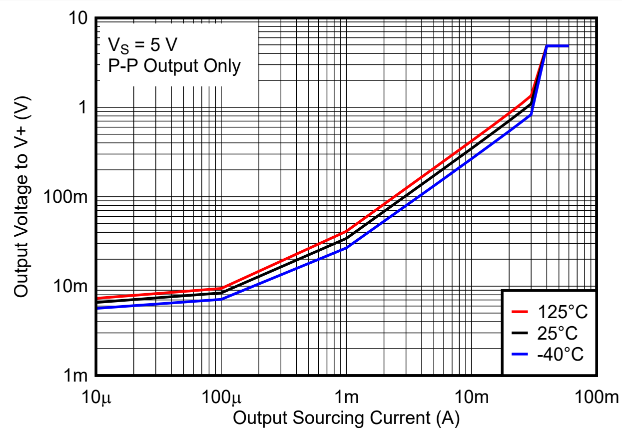


Figure 6-6. Output Voltage vs. Output Sourcing Current, 5V

6 Typical Characteristics (continued)

T_A = 25°C, V_S = 12V, R_{PULLUP} = 2.5k, C_L = 20pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

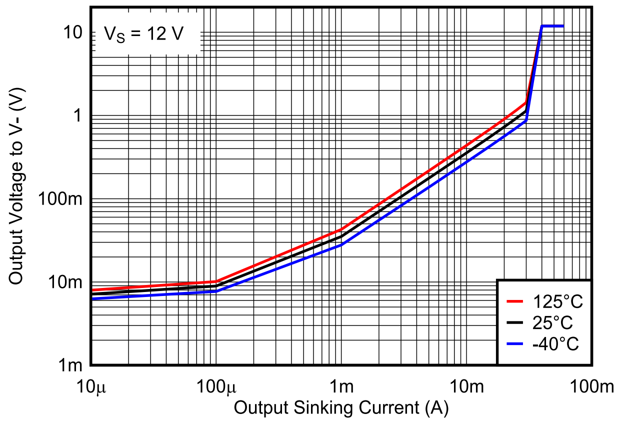


Figure 6-7. Output Voltage vs. Output Sinking Current, 12V

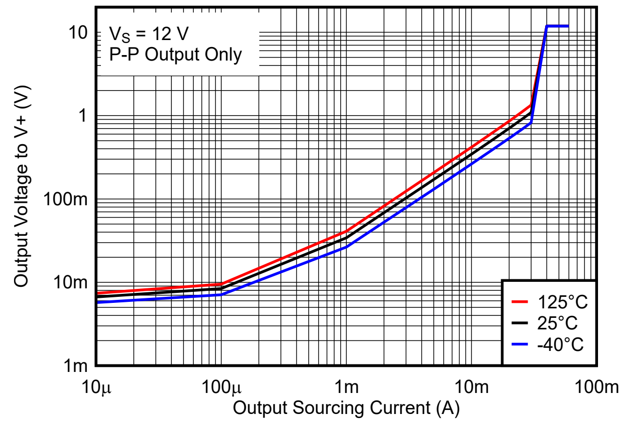


Figure 6-8. Output Voltage vs. Output Sourcing Current, 12V

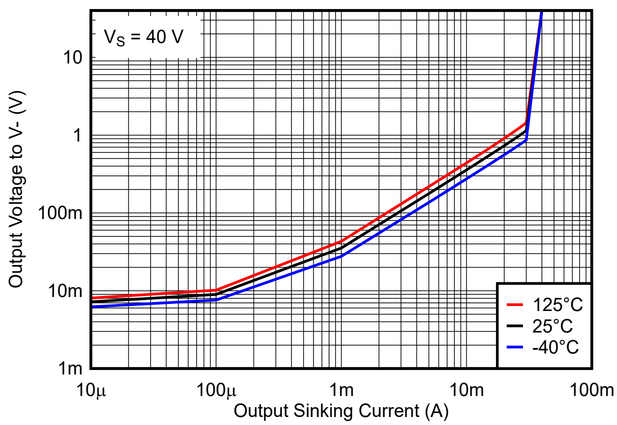


Figure 6-9. Output Voltage vs. Output Sinking Current, 40V

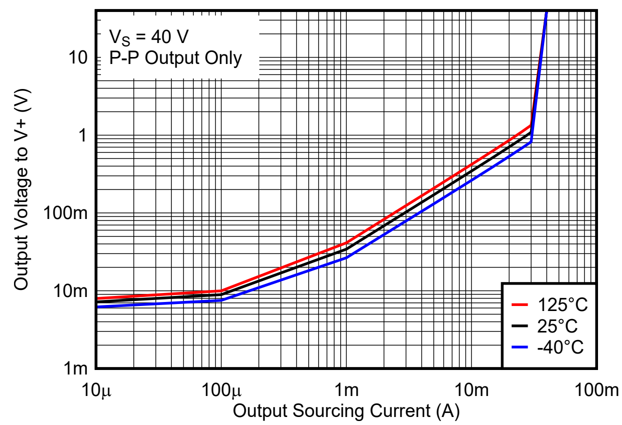


Figure 6-10. Output Voltage vs. Output Sourcing Current, 40V

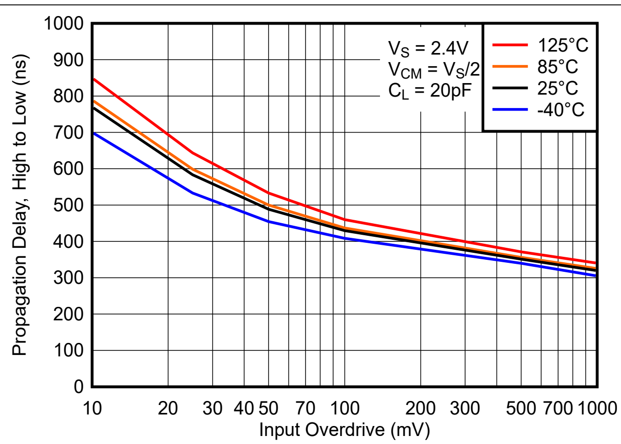


Figure 6-11. Propagation Delay, High to Low, 2.4V

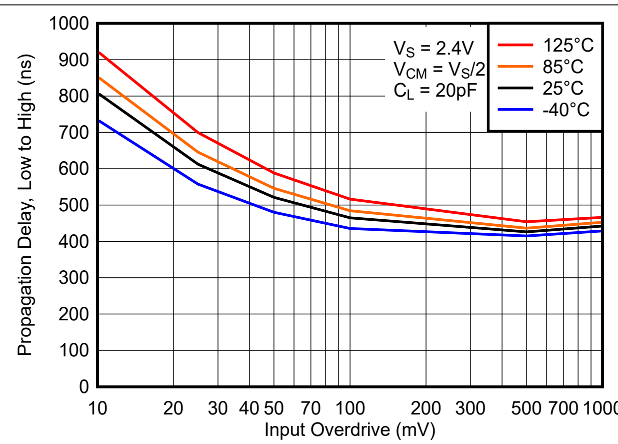


Figure 6-12. Propagation Delay, Low to High, 2.4V

6 Typical Characteristics (continued)

T_A = 25°C, V_S = 12V, R_{PULLUP} = 2.5k, C_L = 20pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

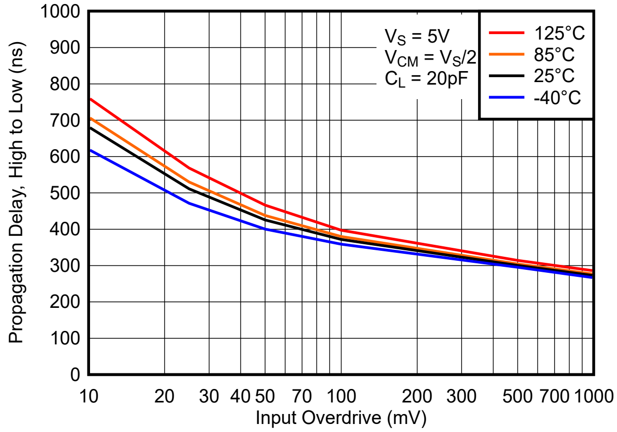


Figure 6-13. Propagation Delay, High to Low, 5V

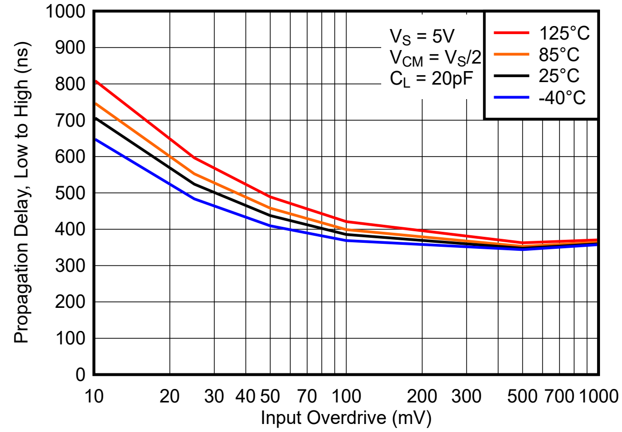


Figure 6-14. Propagation Delay, Low to High, 5V

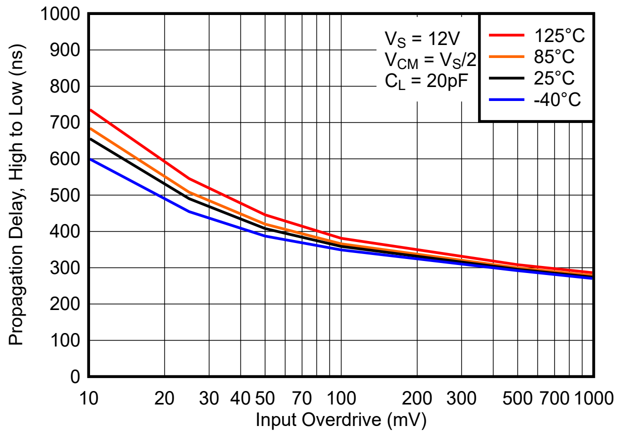


Figure 6-15. Propagation Delay, High to Low, 12V

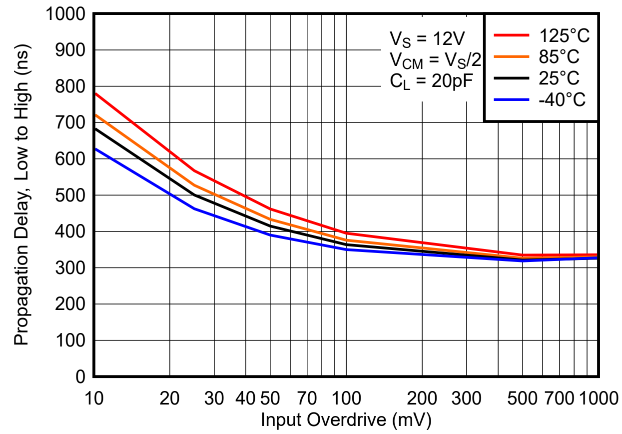


Figure 6-16. Propagation Delay, Low to High, 12V

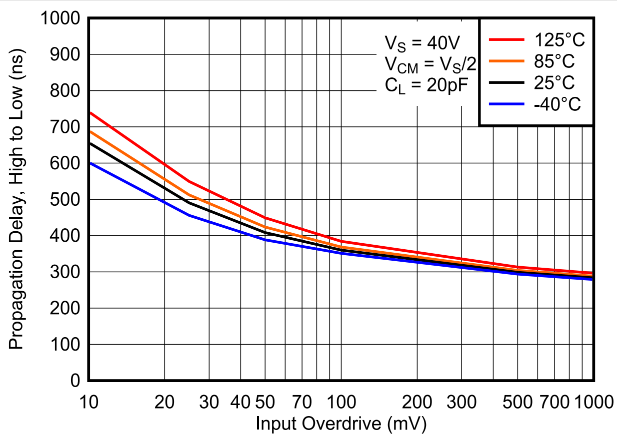


Figure 6-17. Propagation Delay, High to Low, 40V

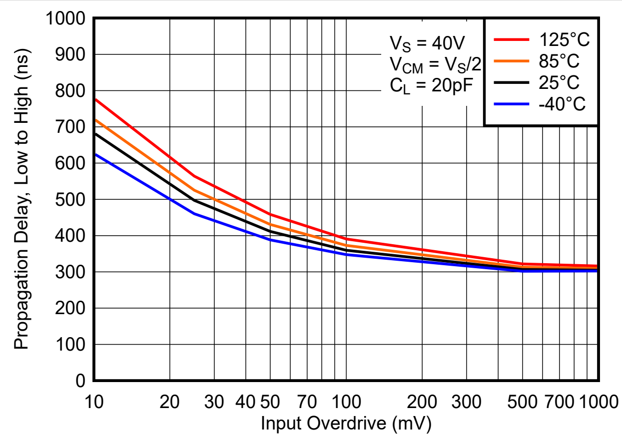


Figure 6-18. Propagation Delay, Low to High, 40V

7 Detailed Description

7.1 Overview

The TLV181x-Q1 and TLV182x-Q1 devices are micro-power comparators with push-pull and open-drain output options. Operating down to 2.4V while only consuming only 5µA per channel, the TLV181x-Q1 and TLV182x-Q1 are well suited for portable, automotive and industrial applications. An internal power-on reset circuit is designed so that the output remains in a known state during power-up and power-down.

7.2 Functional Block Diagrams

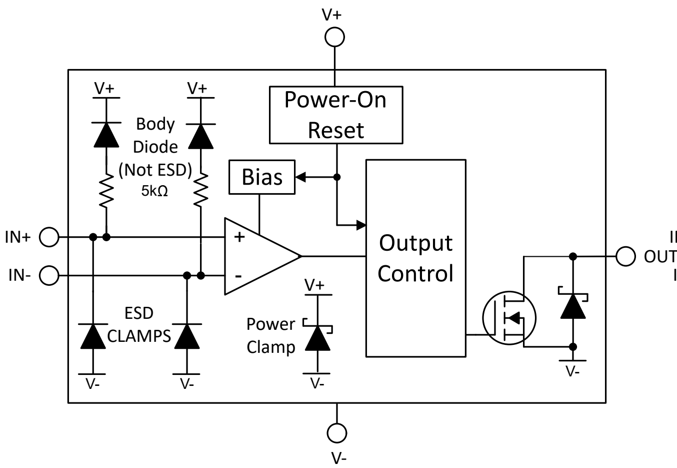


Figure 7-1. TLV182x-Q1 Open-Drain Block Diagram

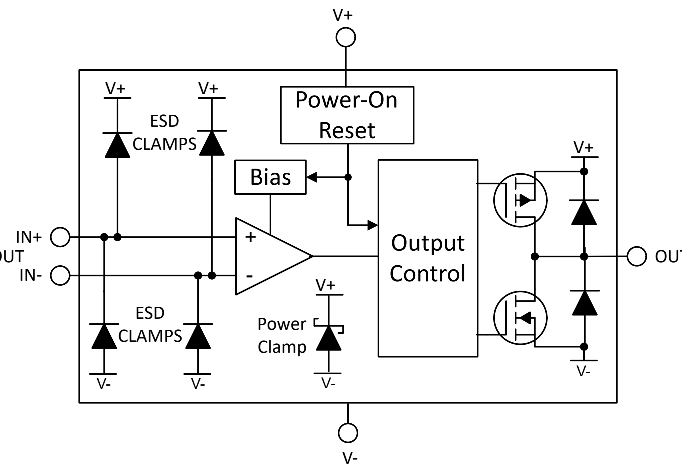


Figure 7-2. TLV181x-Q1 Push-Pull Block Diagram

7.3 Feature Description

TLV18xx Family Options

The TLV18xxy family consists of several output and pinout options, all featuring 40V operation, micro-power 5µA supply currents, 420ns propagation delay, and a Power-On Reset (POR) function.

The TLV18xx family has two output options:

The TLV18**1**x-Q1 has a **push-pull** (sink-source) output.

The TLV18**2**x-Q1 has a **open-drain** (sink only) output, capable of being pulled-up to any voltage up to 40V, independent of comparator supply voltage.

The TLV1811L-Q1 and TLV1821L-Q1 are alternate pinouts of the TLV1811-Q1 and TLV1821-Q1 that allow upgrading older devices such as the TLV7211, TLV7221, LMC7211 and LMC7221 family.

7.4 Device Functional Modes

7.4.1 Inputs

7.4.1.1 TLV18xx Rail-to-Rail Input

The TLV18xx-Q1 input voltage range extends from 200mV below V- to 200mV above V+. The differential input voltage (V_{ID}) can be any voltage within these limits. No phase-inversion of the comparator output occurs when the input voltages stay within the specified range.

The Rail-to-Rail input does have an ESD clamp to the V+ supply line and therefore the input voltage must not exceed the supply voltages by more than 200mV. TI does not recommend applying signals to the rail to rail inputs with no supply voltage.

7.4.1.2 ESD Protection

The TLV182x open-drain option ESD protection consists of a snapback ESD clamp between the output and V- to allow the output to be pulled above V+ to a maximum of 40V. For the inputs, there is a "lower" ESD clamp between V- and the inputs and there is also a parasitic "upper" ESD soft-clamp diode between the input and V+ with a 5kΩ equivelent resistance (as shown in Figure 7-1). These are not traditional ESD cells and current must be limited to 1mA or less across the this upper diode junction and resistance. External diode clamping is recommended if the input voltage can exceed V+ during operation.

The TLV181x push-pull inputs and output ESD protection contains a conventional diode-type "upper" ESD clamp between the I/O pins and V+, and a "lower" ESD clamp between the I/O pins and V-. The inputs or output must not exceed the supply rails by more than 200mV.

If the inputs are to be connected to a low impedance source, such as a power supply or buffered reference line, TI recommends adding a current-limiting resistor in series with the input to limit any currents when the clamps conduct. The current must be limited 10mA or less, though TI recommends limitng the current to 1mA or less. This series resistance can be part of any resistive input dividers or networks.

7.4.1.3 Unused Inputs

If a channel is not to be used, DO NOT tie the inputs together. Due to the high equivalent bandwidth and low offset voltage, tying the inputs directly together can cause high frequency chatter as the device triggers on it's own internal wideband noise. Instead, the inputs must be tied to any available voltage that resides within the specified input voltage range and provides a minimum of 50mV differential voltage. For example, one input can be grounded and the other input connected to a reference voltage, or even V+ (as long as the input is directly connected to the V+ pin to avoid transients).

7.4.2 Outputs

7.4.2.1 TLV181x-Q1 Push-Pull Output

The TLV181x-Q1 features a push-pull output stage capable of both sinking and sourcing current. This allows driving loads such as LED's and MOSFET gates, as well as eliminating the need for a power-wasting external pull-up resistor. The push-pull output must never be connected to another output.

Directly shorting the output to the opposite supply rail (V+ when output "low" or V- when output "High") can result in thermal runaway and eventual device destruction at high (>12V) supply voltages. If output shorts are possible, a series current limiting resistor is recommended to limit the power dissipation.

Unused push-pull outputs mustbe left floating, and never tied to a supply, ground, or another output.

7.4.2.2 TLV182x-Q1 Open-Drain Output

The TLV182x-Q1 features an open-drain (also commonly called open collector) sinking-only output stage enabling the output logic levels to be pulled up to an external voltage from 0V up to 40V, independent of the comparator supply voltage (V+). The open-drain output allows logical OR'ing of multiple open drain outputs and logic level translation. TI recommends setting the pull-up resistor current to between 100uA and 1mA. Lower value pull-up resistor values can help increase the rising edge rise-time, but at the expense of increasing V_{OL} and higher power dissipation. The rise-time is dependent on the time constant of the total pull-up resistance and total load capacitance. Large value pull-up resistors (>1 MΩ) creates an exponential rising edge due to the output RC time constant and increase the rise-time.

Directly shorting the output to V+ can result in thermal runaway and eventual device destruction at high (>12V) pull-up voltages. If output shorts are possible, a series current limiting resistor is recommended to limit the power dissipation.

Unused open drain outputs can be left floating, or can be tied to the V- pin if floating pins are not desired.

7.4.3 Power-On Reset (POR)

The TLV18xx -Q1 family has an internal Power-on-Reset (POR) circuit for known start-up or power-down conditions. While the power supply (V+) is ramping up or ramping down, the POR circuitry is activated for up to 200μs after the minimum supply voltage threshold of 2.4V is crossed, or immediately when the supply voltage drops below 2.4V. When the supply voltage is equal to or greater than the minimum supply voltage, and after the delay period, the comparator output reflects the state of the differential input (V_{ID}).

For the TLV181x-Q1 push-pull output devices, the output is held low during the POR period (t_{on}).

For the TLV182x-Q1 open drain output option the POR circuit keeps the output high impedance (Hi-Z) during the POR period (t_{on}).

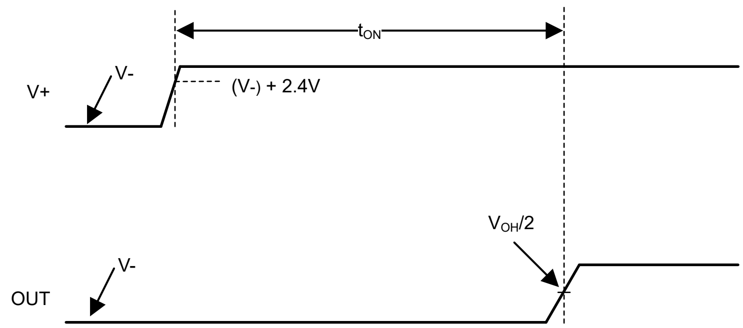


Figure 7-3. Power-On Reset Timing Diagram

Note: The output voltage rises with the pull-up voltage during the POR period.

7.4.4 Hysteresis

The TLV18xx-Q1 family does not have internal hysteresis. Due to the wide effective bandwidth and low input offset voltage, there is a possibility for the output to "chatter" when the absolute differential voltage is near zero as the comparator triggers on internal wideband noise. This is normal comparator behavior and is expected. TI recommends that the user add external hysteresis if slow moving signals are expected. See Section 8.1.2 in the following section.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Basic Comparator Definitions

8.1.1.1 Operation

The basic comparator compares the input voltage (V_{IN}) on one input to a reference voltage (V_{REF}) on the other input. In the Figure 8-1 example below, if V_{IN} is less than V_{REF}, the output voltage (V_O) is logic low (V_{OL}). If V_{IN} is greater than V_{REF}, the output voltage (V_O) is at logic high (V_{OH}). Table 8-1 summarizes the output conditions. The output logic can be inverted by simply swapping the input pins.

Table 8-1. Output Conditions

Inputs Condition	Output
IN+ > IN-	HIGH (V_{OH})
IN+ = IN-	Indeterminate (chatters - see Section 8.1.2)
IN+ < IN-	LOW (V_{OL})

8.1.1.2 Propagation Delay

There is a delay between from when the input crosses the reference voltage and the output responds. This is called the Propagation Delay. Propagation delay can be different between high-to low and low-to-high input transitions. This is shown as t_{pLH} and t_{pHL} in the Comparator Timing Diagram and is measured from the mid-point of the input to the midpoint of the output. Likewise, propagation varies with what is called overdrive (V_{OD}) and underdrive (V_{UD}) voltage levels (see Overdrive and Underdrive Voltage).

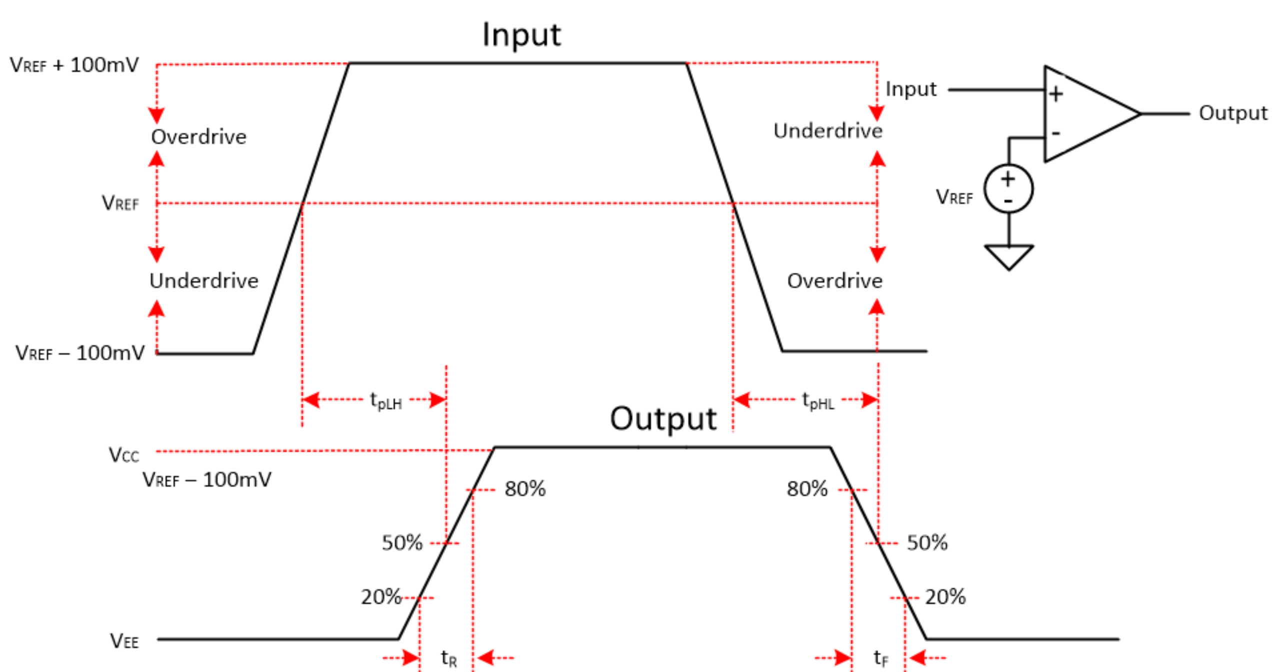


Figure 8-1. Comparator Timing Diagram

8.1.1.3 Overdrive and Underdrive Voltage

The overdrive voltage, V_{OD}, is the amount of input voltage beyond the reference voltage (and not the total input peak-to-peak voltage). The overdrive voltage is 100mV as shown in the Figure 8-1 example. Similarly, underdrive voltage, V_{UD}, is how far below REF the input starts. The overdrive and underdrive voltages influence the propagation delay (t_p). See curves in the Typical Characteristics section for more details. The smaller the overdrive voltage, the longer the propagation delay, particularly when <100mV. If the fastest speeds are desired, apply the highest amount of overdrive possible. Contrary to overdrive voltage, larger underdrive voltage causes tp to increase. This is particulary important in applications where rail-to-rail input swings are present at the comparator inputs. The result can be skewed propagation delay (difference between tp_{LH} and tp_{HL}). As a low power comparator, TI does not recommend using this comparator family if variation in propagation delay is critical.

The risetime (t_r) and falltime (t_f) is the time from the 20% and 80% points of the output waveform.

8.1.2 Hysteresis

The basic comparator configuration can oscillate or produce a noisy "chatter" output if the applied differential input voltage is near the comparator's offset voltage. This typically occurs when the input signal is moving very slowly across the switching threshold of the comparator.

This problem can be prevented by the addition of hysteresis or positive feedback.

The hysteresis transfer curve is shown in Figure 8-2. This curve is a function of three components: V_{TH}, V_{OS}, and V_{HYST}:

- V_{TH} is the actual set voltage or threshold trip voltage.
- V_{OS} is the internal offset voltage between V_{IN+} and V_{IN-}. This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST} is the hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

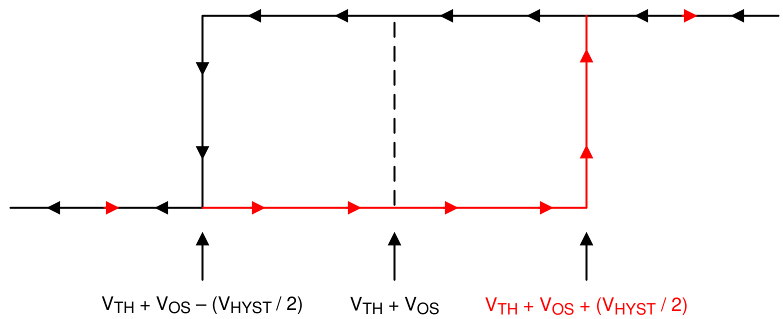


Figure 8-2. Hysteresis Transfer Curve

For more information, please see the Comparator with and without hysteresis circuit application note.

8.1.2.1 Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V_{CC}), as shown in Figure 8-3.

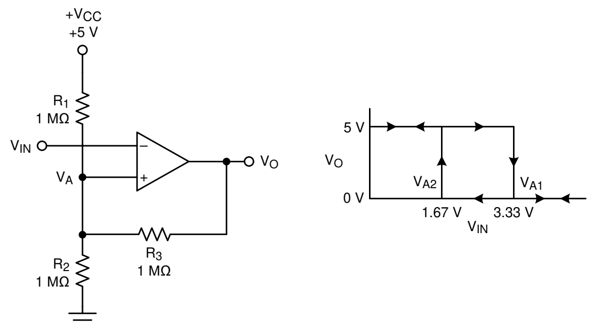


Figure 8-3. TLV181x-Q1in an Inverting Configuration With Hysteresis

The equivalent resistor networks when the output is high and low are shown in Figure 8-3.

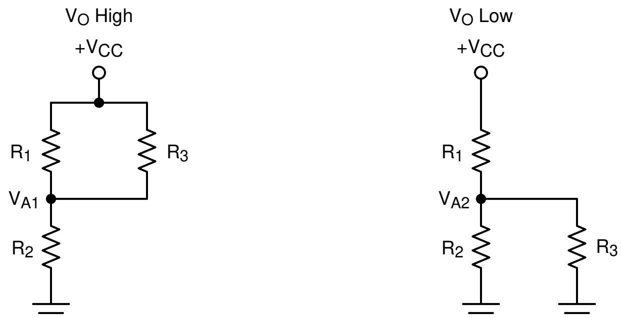


Figure 8-4. Inverting Configuration Resistor Equivalent Networks

When V_{IN} is less than V_A, the output voltage is high (for simplicity, assume V_O switches as high as V_{CC}). The three network resistors can be represented as R1 || R3 in series with R2, as shown in Figure 8-4.

Equation 1 below defines the high-to-low trip voltage (V_{A1}).

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2} \tag{1}$$

When V_{IN} is greater than V_A, the output voltage is low. In this case, the three network resistors can be presented as R2 || R3 in series with R1, as shown in Equation 2.

Use Equation 2 to define the low to high trip voltage (V_{A2}).

$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)} \tag{2}$$

Equation 3 defines the total hysteresis provided by the network.

$$\Delta V_A = V_{A1} - V_{A2} \tag{3}$$

8.1.2.2 Non-Inverting Comparator With Hysteresis

A non-inverting comparator with hysteresis requires a two-resistor network and a voltage reference (V_{REF}) at the inverting input, as shown in Figure 8-5,

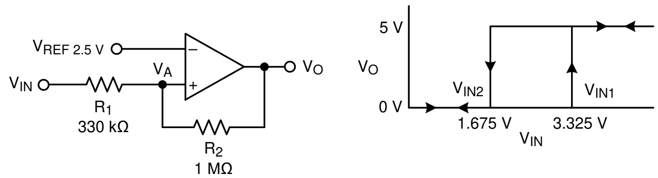


Figure 8-5. TLV181x-Q1 in a Non-Inverting Configuration With Hysteresis

The equivalent resistor networks when the output is high and low are shown in Figure 8-6.

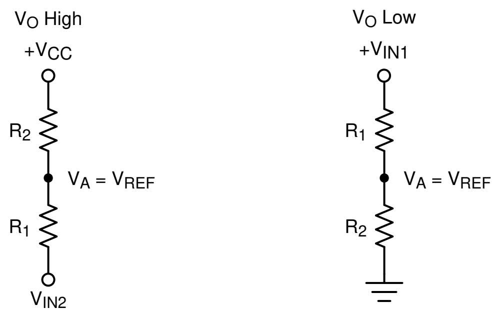


Figure 8-6. Non-Inverting Configuration Resistor Networks

When V_{IN} is less than V_{REF}, the output is low. For the output to switch from low to high, V_{IN} must rise above the V_{IN1} threshold. Use Equation 4 to calculate V_{IN1}.

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} + V_{REF} \tag{4}$$

When V_{IN} is greater than V_{REF}, the output is high. For the comparator to switch back to a low state, V_{IN} must drop below V_{IN2}. Use Equation 5 to calculate V_{IN2}.

$$V_{IN2} = \frac{V_{REF}\,(R1 + R2) - V_{CC} \times R1}{R2} \tag{5}$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}, as shown in Equation 6.

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \tag{6}$$

For more information, please see Application Notes SNOA997 "Inverting comparator with hysteresis circuit" and SBOA313 "Non-Inverting Comparator With Hysteresis Circuit".

8.1.2.3 Inverting and Non-Inverting Hysteresis using Open-Drain Output

An open drain output device, such as the TLV182x-Q1, can also be used, but the output pull-up resistor must also be taken into account in the calculations. The pull-up resistor is seen in series with the feedback resistor when the output is high. Thus, the feedback resistor is actually seen as R2 + R_{PULLUP}. TI recommends that the pull-up resistor be at least 10 times less than the feedback resistor value.

8.2 Typical Applications

8.2.1 Window Comparator

Window comparators are commonly used to detect undervoltage and overvoltage conditions. Figure 8-7 shows a simple window comparator circuit. Window comparators require open drain outputs (TLV182x-Q1) if the outputs are directly connected together.

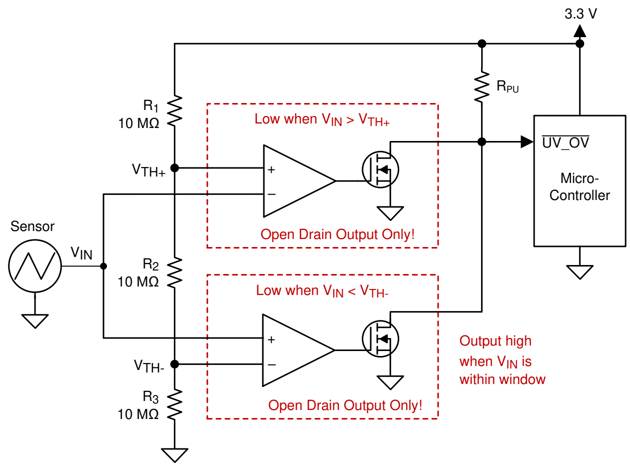


Figure 8-7. Window Comparator

8.2.1.1 Design Requirements

For this design, follow these design requirements:

- UV_Alert (logic low output) when the 24V suply is less than 19.2V
- OV_Alert (logic low output) when the 24V suply is greater than 30V
- Current dissipated in the resistor string is 30uA
- Comparator operates from the 5V supply
- 2.5V external reference is used

8.2.1.2 Detailed Design Procedure

Configure the circuit as shown in the circuit above where the 2.5V REF from the TLC3702-EP is used as the reference voltage and the resistor string of R1, R2, and R3 define the upper and lower threshold voltages for the 24V PLC power supply. When the comparator detects that the 24V supply has exceeded the maximum voltage of 30V or has drooped below the minimum voltage of 19.2V, OV_Alert and UV_Alert nets are pulled to a logic LOW state.

The first step is to determine the sum total resistance of the resistor string (R1, R2, R3) using the dissipation limit of 30uA. With a maximum operating voltage of 30V, the resistor string draws 30uA if the total resistance of R1+R2+R3 is 1Mohm.

The second step is to set the value of R3 such that the lower comparator changes output state from HIGH to LOW when the 24V supply reaches 30V. This is achieved when the voltage at the junction of R2 and R3 is equal to the reference voltage of 2.5V. Since 30uA is passing through the resistor string at 30V, R3 can be calculated from 2.5V / 30uA which is approximately 83.3kΩ.

The third step is to set the value of R2 such that the upper comparator changes output state from HIGH to LOW when the 24V supply reaches 19.2V. This is achieved when the voltage at the junction of R1 and R2 is equal to the reference voltage of 2.5V. Since 19.2uA passes through the resistor string at 19.2V, R2 can be calculated from (2.5V /19.2uA) - R3 which is approximately 46.9kΩ.

Lastly, the value of R1 is calculated from 1Mohm - (R2 + R3) which is approximately 870kΩ. Please note that standard 1% resistor values are selected for the circuit

The respective comparator outputs (OV_Alert and UV_Alert) are LOW when the 24V PLC power supply is less than 19.2V or greater than 30V. Likewise, the respective comparator outputs are HIGH when the 24V supply is within the range of 19.2V to 30V (within the "window"), as shown below.

8.2.1.3 Application Curve

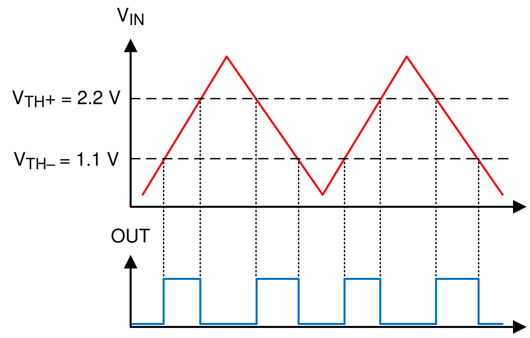


Figure 8-8. Window Comparator Results

For more information, please see Application note SBOA221 "Window comparator circuit".

8.2.2 Square-Wave Oscillator

Square-wave oscillator can be used as low cost timing reference or system supervisory clock source. A push-pull output (TLV181x-Q1) is recommended for best symmetry.

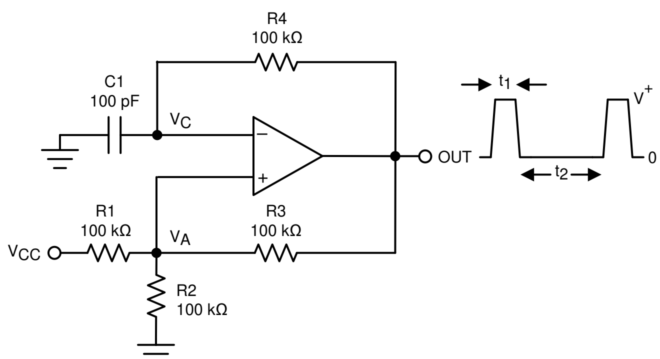


Figure 8-9. Square-Wave Oscillator

8.2.2.1 Design Requirements

The square-wave period is determined by the RC time constant of the capacitor C_1 and resistor R_4. The maximum frequency is limited by propagation delay of the device and the capacitance load on the output. The low input bias current allows a lower capacitor value and larger resistor value combination for a given oscillator frequency, which helps to reduce BOM cost and board space. TI recommends that R4 be over several kiloΩ to minimize loading the output.

8.2.2.2 Detailed Design Procedure

The oscillation frequency is determined by the resistor and capacitor values. The following calculation provides details of the steps.

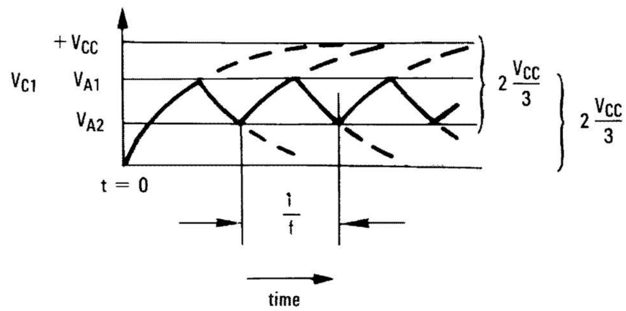


Figure 8-10. Square-Wave Oscillator Timing Thresholds

First consider the output of Figure Figure 8-9 as high, which indicates the inverted input V_C is lower than the noninverting input (V_A). This causes the C_1 to be charged through R_4, and the voltage V_C increases until equal to the noninverting input. The value of V_A at the point is calculated by Equation 7.

$$V_{A1} = \frac{V_{CC} \times R_2}{R_2 + R_1 \| R_3} \tag{7}$$

if $R_1 = R_2 = R_3$, then $V_{A1} = 2V_{CC} / 3$

At this time the comparator output trips pulling down the output to the negative rail. The value of $V_A$at this point is calculated by Equation 8.

$$V_{A2} = \frac{V_{CC}(R_2 \| R_3)}{R_1 + R_2 \| R_3} \tag{8}$$

if $R_1 = R_2 = R_3$, then $V_{A2} = V_{CC}/3$

The C_1 now discharges though the R_4, and the voltage V_{CC} decreases until reaching V_{A2}. At this point, the output switches back to the starting state. The oscillation period equals to the time duration from for C_1 from $2V_{CC}/3$ to V_{CC} / 3 then back to $2V_{CC}/3$, which is given by R_4C_1 × ln 2 for each trip. Therefore, the total time duration is calculated as $2R_4C_1$ × ln 2.

The oscillation frequency can be obtained by Equation 9:

$$f = 1 / (2\ R4 \times C1 \times \ln 2) \tag{9}$$

8.2.2.3 Application Curve

Figure 8-11 shows the simulated results of an oscillator using the following component values:

- $R_1 = R_2 = R_3 = R_4 = 100k\Omega$
- $C_1 = 100pF$, $C_L = 20pF$
- V+ = 5V, V– = GND
- C_{stray} (not shown) from V_A TO GND = 10pF

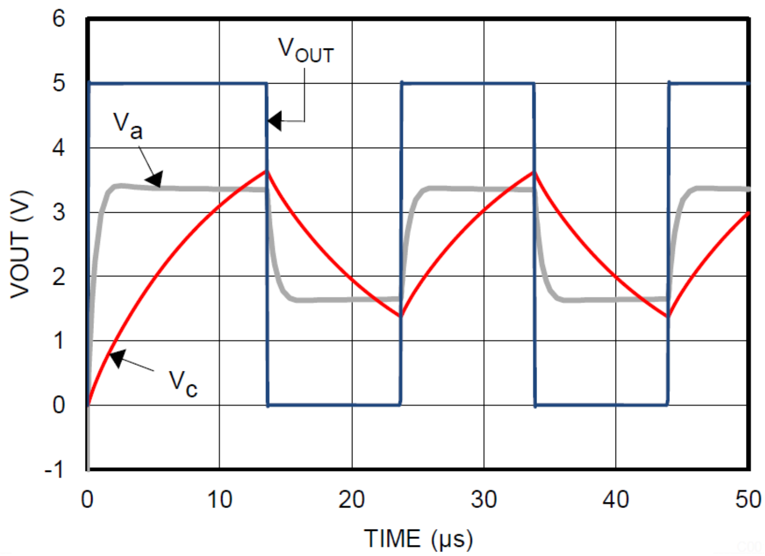


Figure 8-11. Square-Wave Oscillator Output Waveform

8.2.3 Adjustable Pulse Width Generator

Figure 8-12 is a variation on the Section 8.2.2 that allows adjusting the pulse widths.

R_4 and R_5 provide separate charge and discharge paths for the capacitor C depending on the output state.

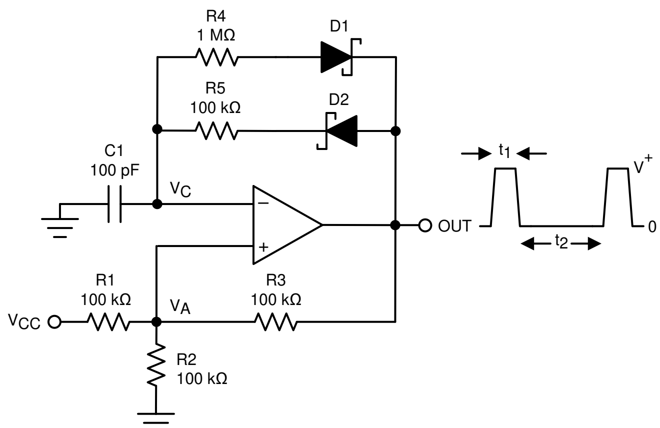


Figure 8-12. Adjustable Pulse Width Generator

The charge path is set through R_5 and D_2 when the output is high. Similarly, the discharge path for the capacitor is set by R_4 and D_1 when the output is low.

The pulse width t_1 is determined by the RC time constant of R_5 and C. Thus, the time t_2 between the pulses can be changed by varying R_4, and the pulse width can be altered by R_5. The frequency of the output can be changed by varying both R_4 and R_5. At low voltages, the effects of the diode forward drop (0.8V, or 0.15V for Shottky) must be taken into account by altering output high and low voltages in the calculations.

8.2.4 Time Delay Generator

The circuit shown in Figure 8-13 provides output signals at a prescribed time interval from a time reference and automatically resets the output low when the input returns to 0V. This is useful for sequencing a "power on" signal to trigger a controlled start-up of power supplies.

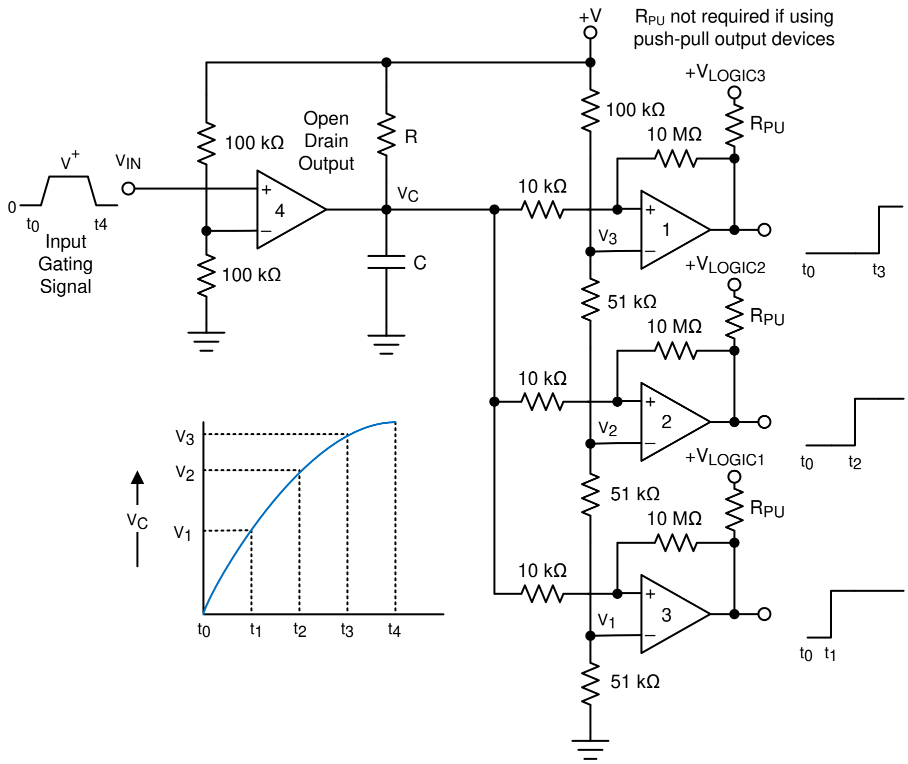


Figure 8-13. Time Delay Generator

Consider the case of V_{IN} = 0. The output of comparator 4 is also at ground, "shorting" the capacitor and holding the node at 0V. This implies that the outputs of comparators 1, 2, and 3 are also at 0V. When an input signal is applied, the output of open drain comparator 4 goes High-Z and C charges exponentially through R. This is indicated in the graph. The output voltages of comparators 1, 2, and 3 switch to the high state in sequence when V_C rises above the reference voltages V_1, V_2 and V_3. A small amount of hysteresis has been provided by the 10kΩ and 10MΩ resistors to insure fast switching when the RC time constant is chosen to give long delay times. A good starting point is R = 100kΩ and C = 0.01µF to 1µF.

All outputs immediately go low when V_{IN} falls to 0V, due to the comparator output going low and immediately discharging the capacitor.

Comparator 4 must be a open-drain type output (TLV182x-Q1), whereas comparators 1 though 3 can be either open drain or push-pull output, depending on system requirements. R_{PU} is not required for push-pull output devices.

8.2.5 Logic Level Shifter

The output of the TLV182x-Q1 is the uncommitted drain of the output transistor. Many open-drain outputs can be tied together to provide an output OR'ing function if desired.

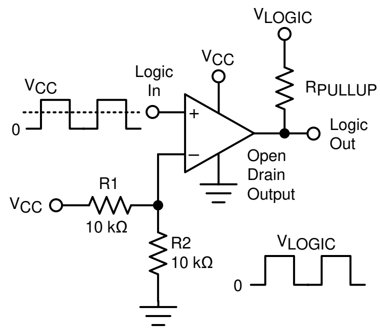


Figure 8-14. Universal Logic Level Shifter

The two 10kΩ resistors bias the input to half of the input logic supply level to set the threshold in the mid-point of the input logic levels. Only one shared output pull-up resistor is needed and can be connected to any pull-up voltage between 0V and 5.5V. The pullup voltage (V_{LOGIC}) must match the driven logic input "high" level.

8.2.6 One-Shot Multivibrator

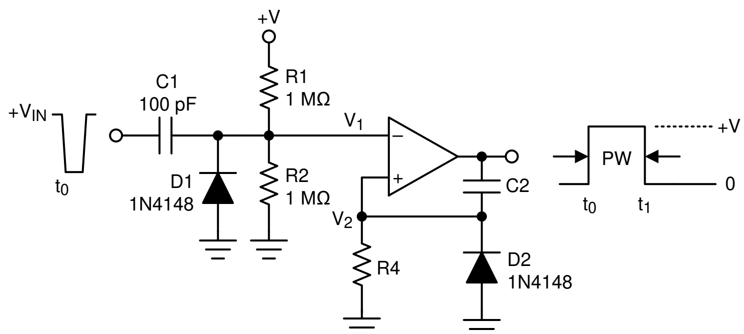


Figure 8-15. One-Shot Multivibrator

A monostable multivibrator has one stable state in which the circuit can remain indefinitely. The circuit can be triggered externally to another quasi-stable state. A monostable multivibrator can thus be used to generate a pulse of desired width.

The desired pulse width is set by adjusting the values of C_2 and R_4. The resistor divider of R_1 and R_2 can be used to determine the magnitude of the input trigger pulse. The output changes state when $V_1 < V_2$. Diode D_2 provides a rapid discharge path for capacitor C_2 to reset at the end of the pulse. The diode also prevents the non-inverting input from being driven below ground.

8.2.7 Bi-Stable Multivibrator

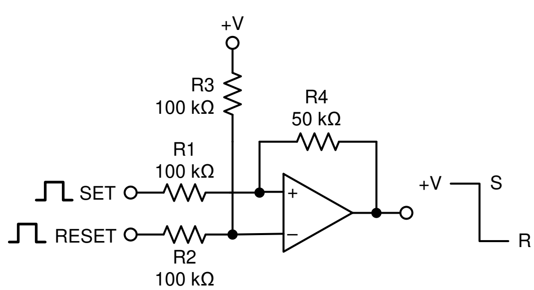


Figure 8-16. Bi-Stable Multivibrator

A bi-stable multivibrator has two stable states. The reference voltage is set up by the voltage divider of R_2 and R_3. A pulse applied to the SET terminal switches the output of the comparator high. The resistor divider of R_1

and R4 now sets the non-inverting input to a voltage greater than the reference voltage. A pulse applied to RESET toggles the output low.

8.2.8 Zero Crossing Detector

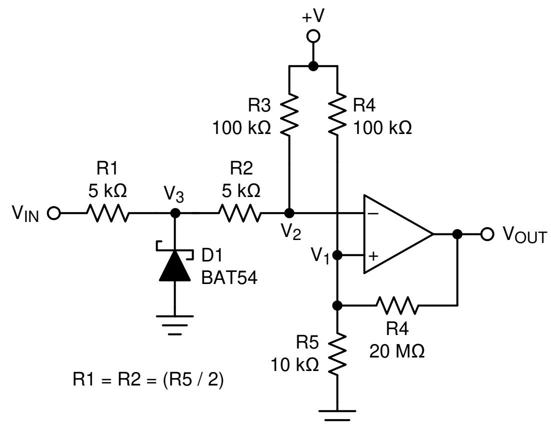


Figure 8-17. Zero Crossing Detector

A voltage divider of R_4 and R_5 establishes a reference voltage V_1 at the non-inverting input. By making the series resistance of R_1 and R_2 equal to R_5, the comparator output switches when V_{IN} = 0V. Diode D_1 clamps V_3 near ground. The voltage divider of R_2 and R_3 then prevents V_2 from going below ground. A small amount of hysteresis is setup to maintain rapid output voltage transitions.

8.2.9 Pulse Slicer

A Pulse Slicer is a variation of the Zero Crossing Detector and is used to detect the zero crossings on an input signal with a varying baseline level. This circuit works best with symmetrical waveforms. The RC network of R_1 and C_1 establishes an mean reference voltage V_{REF}, which tracks the mean amplitude of the V_{IN} signal. The non-inverting input is directly connected to V_{REF} through R2. R2 and R3 are used to produce hysteresis to keep transitions free of spurious toggles. The time constant is a tradeoff between long-term symmetry and response time to changes in amplitude.

If the waveform is data, the data can be encoded in the recommended NRZ (Non-Return to Zero) format to maintain proper average baseline. Asymmetrical inputs can suffer from timing distortions caused by the changing V_{REF} average voltage.

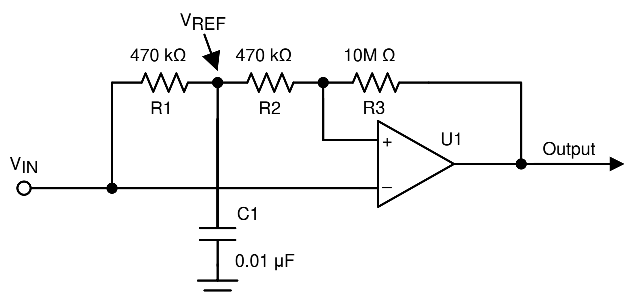


Figure 8-18. Pulse Slicer

For this design, follow these design requirements:

- The RC constant value (R_2 and C_1) must support the targeted data rate to maintain a valid tripping threshold.
- The hysteresis introduced with R_2 and R_{43} helps to avoid spurious output toggles.

The TLV182x-Q1 can also be used, but with the addition of a pull-up resistor on the output (not shown for clarity).

Figure 8-19 shows the results of a 9600 baud data signal riding on a varying baseline.

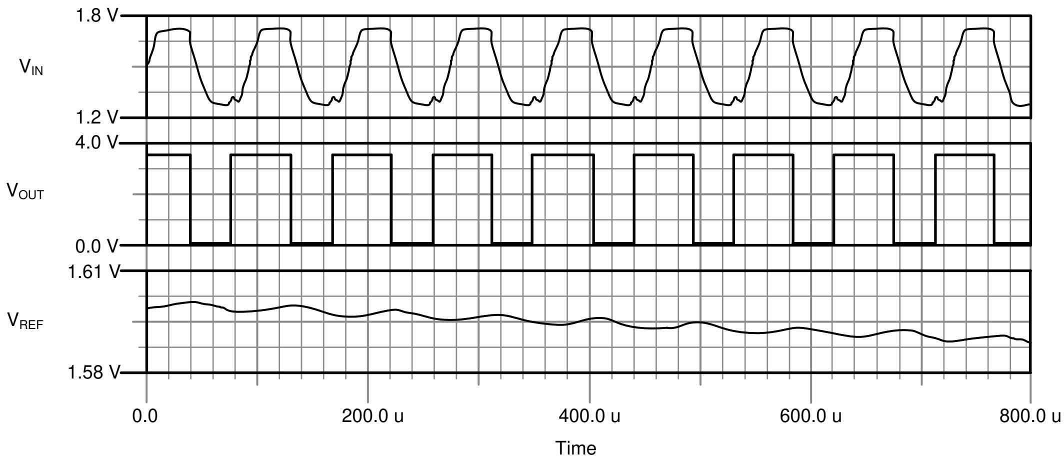


Figure 8-19. Pulse Slicer Waveforms

8.3 Power Supply Recommendations

Due to the fast output edge rates, bypass capacitors are critical on the supply pin to prevent supply ringing and false triggers and oscillations. Bypass the supply directly at *each* device with a low ESR 0.1μF ceramic bypass capacitor directly between V_{CC} pin and ground pins. Narrow, peak currents are drawn during the output transition time, particularly for the push-pull output device. These narrow pulses can cause un-bypassed supply lines and poor grounds to ring, possibly causing variation that can eat into the input voltage range and create an inaccurate comparison or even oscillations.

The device can be powered from both "split" supplies (V+ and V-), or "single" supplies (V+ and GND), with GND applied to the V- pin. Input signals must stay within the specified input range (between V+ and V-) for either type. Note that with a "split" supply the output swings "low" (V_{OL}) to V- potential and not GND.

8.4 Layout

8.4.1 Layout Guidelines

For accurate comparator applications, a clean, stable power supply is important to minimize output glitches. Output rise and fall times are in the tens of nanoseconds, and must be treated as high speed logic devices. The bypass capacitor must be as close to the supply pin as possible and connected to a solid ground plane, and preferably directly between the V_{CC} and GND pins.

Minimize coupling between outputs and inputs to prevent output oscillations. Do not run output and input traces in parallel unless there is a V_{CC} or GND trace between output to reduce coupling. When series resistance is added to inputs, place resistor close to the device. A low value (≤100Ω) resistor can also be added in series with the output to dampen any ringing or reflections on long, non-impedance controlled traces. For best edge shapes, controlled impedance traces with back-terminations can be used when routing long distances.

8.4.2 Layout Example

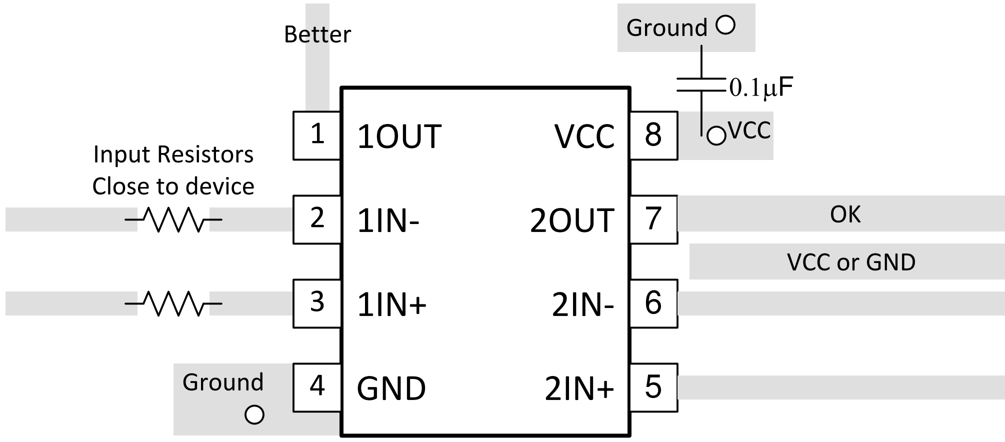


Figure 8-20. Dual Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

- Texas Instruments, *Analog Engineers Circuit Cookbook: Amplifiers* (See Comparators section) - SLYY137
- Texas Instruments, *Precision Design, Comparator with Hysteresis Reference Design*— TIDU020
- Texas Instruments, *Window comparator circuit* - SBOA221
- Texas Instruments, *Reference Design, Window Comparator Reference Design*— TIPD178
- Texas Instruments, *Comparator with and without hysteresis circuit* - SBOA219
- Texas Instruments, *Inverting comparator with hysteresis circuit* - SNOA997
- Texas Instruments, *Non-Inverting Comparator With Hysteresis Circuit* - SBOA313
- Texas Instruments, *Zero crossing detection using comparator circuit* - SNOA999
- Texas Instruments, *PWM generator circuit* - SBOA212
- Texas Instruments, *How to Implement Comparators for Improving Performance of Rotary Encoder in Industrial Drive Applications* - SNOAA41
- Texas Instruments, *A Quad of Independently Func Comparators* - SNOA654

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (December 2024) to Revision D (May 2026)	Page
• Removed Preview from Quad WQFN	1
• Restored missing rows and tables	6

Changes from Revision B (September 2023) to Revision C (December 2024)	Page
• Replaced block digram and added graph	1

Changes from Revision A (March 2023) to Revision B (September 2023)	Page
• Removed previews for Duals and SOIC Quad releases	1

Changes from Revision * (October 2022) to Revision A (March 2023)	Page
• Removed previews for Single releases	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.