3-Pin Voltage Supervisors with Active-High, Push-Pull Reset

1 FEATURES

- 3-Pin SOT23 Package
- Supply Current: 9 µA (Typical)
- Precision Supply Voltage Monitor: 2.5 V, 3 V, 3.3 V, 5 V
- Power-On Reset Generator with Fixed Delay Time of 200 ms
- Pin-for-Pin Compatible with MAX810
- Temperature Range: –40°C to +125°C
- Push-Pull, RESET Output

2 APPLICATIONS

- DSPs, Microcontrollers, and Microprocessors
- Wireless Communication Systems
- Portable/Battery-Powered Equipment
- Programmable Controls
- Intelligent Instruments
- Industrial Equipment
- Notebook and Desktop Computers
- Automotive Systems

DEVICE FAMILY COMPARISON

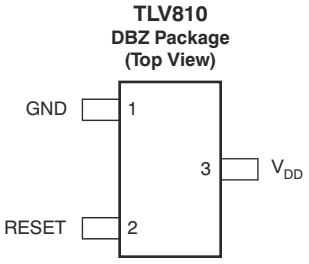
DEVICE	FUNCTION
TLV803	Open-Drain, $\overline{\text{RESET}}$ Output
TLV809	Push-Pull, $\overline{\text{RESET}}$ Output
TLV810	Push-Pull, RESET Output

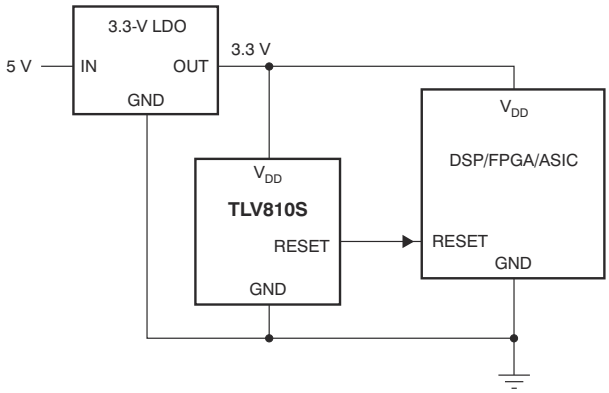
3 DESCRIPTION

The TLV810 family of supervisory circuits provides circuit initialization and timing supervision, primarily for DSPs and processor-based systems.

During power-on, RESET is asserted when the supply voltage (V_{DD}) becomes higher than 1.1 V. Thereafter, the supervisory circuit monitors V_{DD} and keeps RESET active as long as V_{DD} remains below the threshold voltage V_{IT}. An internal timer delays the return of the output to the inactive state (low) to ensure proper system reset. The delay time ($t_{d(typ)}$ = 200 ms) starts after V_{DD} has risen above the threshold voltage, V_{IT}. When the supply voltage drops below the V_{IT} threshold voltage, the output becomes active (high) again. No external components are required. All the devices in this family have a fixed sense-threshold voltage (V_{IT}) set by an internal voltage divider.

The product spectrum is designed for supply voltages of 2.5 V, 3 V, 3.3 V, and 5 V. The circuits are available in a 3-pin SOT-23 package. The TLV810 devices are characterized for operation over a temperature range of –40°C to +125°C.





TYPICAL APPLICATION

4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5 PACKAGE/ORDERING INFORMATION (1)

PRODUCT	THRESHOLD VOLTAGE	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED OPERATING TEMPERATURE	PACKAGE MARKING	ORDERING INFORMATION	TRANSPORT MEDIA, QUANTITY
TLV810Z	2.25 V	SOT23-3	DBZ	–40°C to +125°C	VOVQ	TLV810ZDBZR	Tape and Reel, 3000
						TLV810ZDBZT	Tape and Reel, 250
TLV810R	2.64 V	SOT23-3	DBZ	–40°C to +125°C	VOWQ	TLV810RDBZR	Tape and Reel, 3000
						TLV810RDBZT	Tape and Reel, 250
TLV810S	2.93 V	SOT23-3	DBZ	–40°C to +125°C	VOXQ	TLV810SDBZR	Tape and Reel, 3000
						TLV810SDBZT	Tape and Reel, 250
TLV810M	4.38 V	SOT23-3	DBZ	–40°C to +125°C	VOYQ	TLV810MDBZR	Tape and Reel, 3000
						TLV810MDBZT	Tape and Reel, 250

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or visit the device product folders at www.ti.com.

6 ABSOLUTE MAXIMUM RATINGS (1)

Over operating free-air temperature range (unless otherwise noted).

		VALUE		UNIT
		MIN	MAX	
Voltage	V_{DD} (2)	0	7	V
	All other pins(2)	–0.3	7	V
Current	Maximum low output current, I_{OL}		5	mA
	Maximum high output current, I_{OH}		–5	mA
	Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD})		±20	mA
	Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD})		±20	mA
Temperature	Operating free-air temperature range, T_A	–40	+125	°C
	Storage temperature range, T_{stg}	–65	+150	°C
	Soldering temperature		+260	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND. For reliable operation the device should not be operated at 7 V for more than t = 1000h continuously.

7 THERMAL INFORMATION

THERMAL METRIC[1]		TLV810 DBZ 3 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	286.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	105.6	
θ_{JB}	Junction-to-board thermal resistance	124.4	
ψ_{JT}	Junction-to-top characterization parameter	25.8	
ψ_{JB}	Junction-to-board characterization parameter	107.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	—	

8 RECOMMENDED OPERATING CONDITIONS

At specified temperature range (unless otherwise noted).

		MIN	MAX	UNIT
V_{DD}	Supply voltage	1.1	6	V
T_A	Operating free-air temperature range	–40	+125	°C

9 ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		V_{DD} = 2.0 V to 6 V,I_{OH} = –500 µA	V_{DD} – 0.2			V
			V_{DD} = 3.3 V,I_{OH} = –2 mA	V_{DD} – 0.4			
			V_{DD} = 6 V,I_{OH} = –4 mA, T_A = –40°C to +85°C	V_{DD} – 0.4			
			V_{DD} = 6 V,I_{OH} = –4 mA, T_A = +85°C to +125°C	V_{DD} – 0.5			
V_{OL}	Low-level output voltage		V_{DD} = 2.5 V to 6 V,I_{OL} = 500 µA			0.2	V
			V_{DD} = 3.3 V,I_{OL} = 2 mA			0.4	
			V_{DD} = 6 V, I_{OL} = 4 mA			0.4	
	Power-up reset voltage[1]		$V_{OH} \geq V_{DD}$ – 0.2 V, I_{OH} = –50 µA	1.1			V
$V_{IT–}$	Negative-going input threshold voltage[2]	TLV810Z		2.20	2.25	2.30	V
		TLV810R		2.58	2.64	2.70	
		TLV810S		2.87	2.93	2.99	
		TLV810M		4.28	4.38	4.48	
V_{hys}	Hysteresis	TLV810Z	I_{OH} = –50 µA, T_A = +25°C		30		mV
		TLV810R			35		
		TLV810S			40		
		TLV810M			60		
I_{DD}	Supply current		V_{DD} = 2 V, output unconnected		9	15	µA
			V_{DD} = 6 V, output unconnected		20	30	

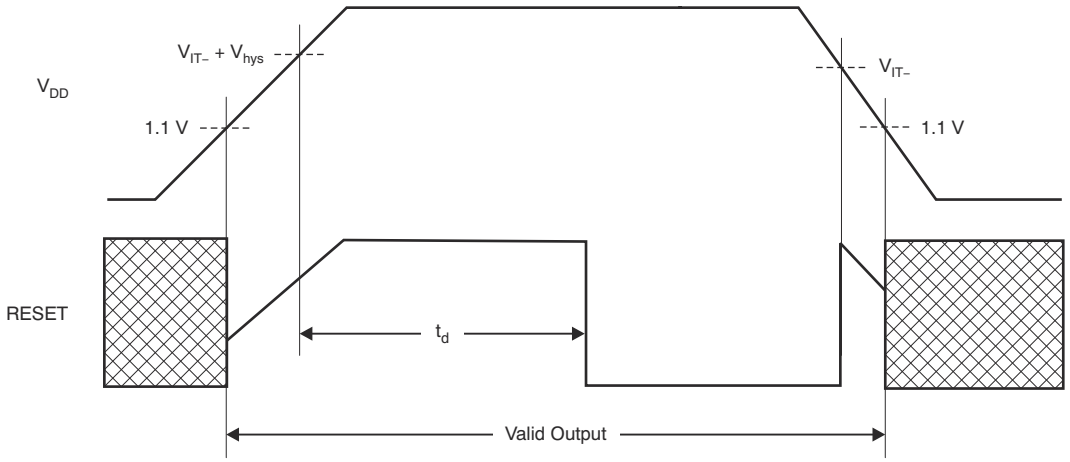
(1) The lowest supply voltage at which RESET becomes valid. $t_{r, VDD} \leq 66.7$ ms/V.
(2) To ensure best stability of the threshold voltage, a bypass capacitor (0.1-µF ceramic) should be placed near the supply terminals.

10 SWITCHING CHARACTERISTICS

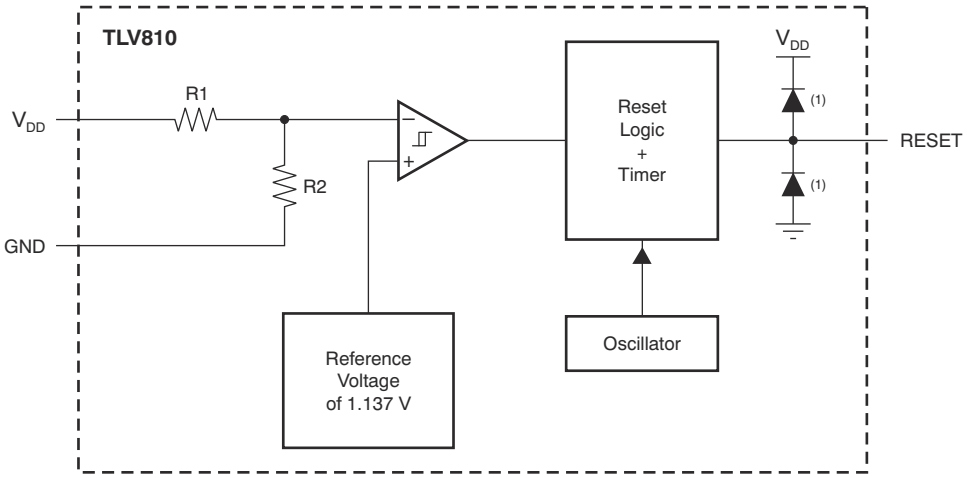
At T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w	Pulse width at V_{DD}	V_{DD} = 1.08 V_{IT-} to 0.92 V_{IT-}		1		µs
t_d	Delay time	V_{DD} ≥ V_{IT-} + 0.2 V; see Timing Diagram	120	200	280	ms

11 TIMING DIAGRAM



12 FUNCTIONAL BLOCK DIAGRAM



A. Parasitic diode.

13 TYPICAL CHARACTERISTICS

At T_A = +25°C, V_{IT-} = 4.38 V, and V_{DD} = 5.0 V, unless otherwise noted.

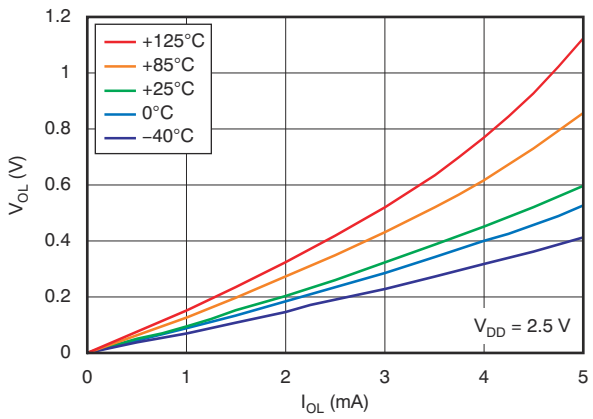


Figure 13-1. LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

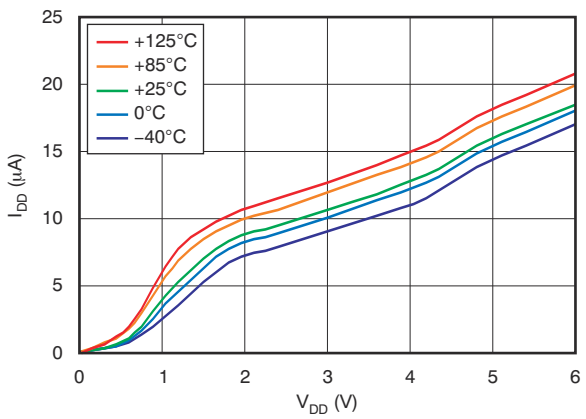


Figure 13-2. SUPPLY CURRENT vs SUPPLY VOLTAGE

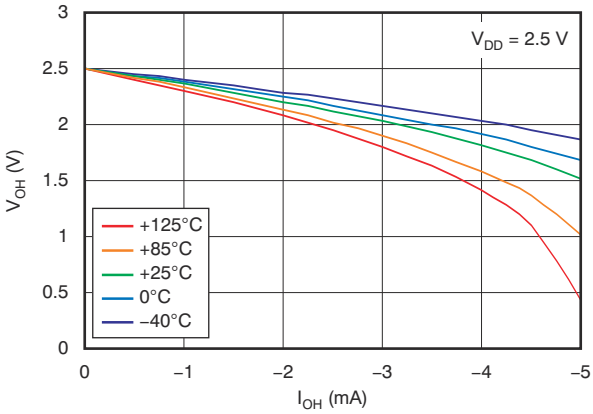


Figure 13-3. HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

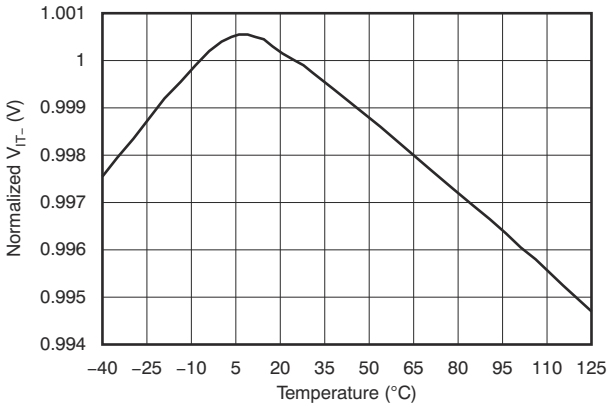


Figure 13-4. NORMALIZED INPUT THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE AT V_{DD}

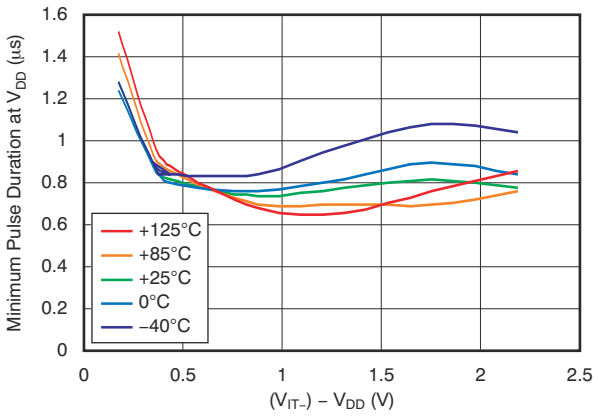


Figure 13-5. MINIMUM PULSE DURATION AT V_{DD} vs V_{DD} THRESHOLD OVERDRIVE VOLTAGE(TLV810M)

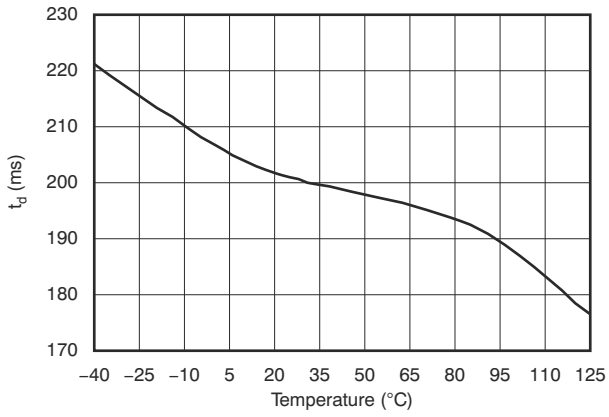


Figure 13-6. DELAY TIME vs TEMPERATURE

14 APPLICATION INFORMATION

14.1 V_{DD} TRANSIENT REJECTION

The TLV810 has built-in rejection of fast transients on the V_{DD} pin. The rejection of transients depends on both the duration and the amplitude of the transient. The amplitude of the transient is measured from the bottom of the transient to the negative threshold voltage of the TLV810, as shown in Figure 14-1.

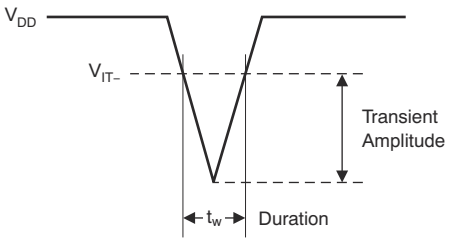


Figure 14-1. Voltage Transient Measurement

The TLV810 does not respond to transients that are fast duration/low amplitude or long duration/small amplitude. Figure 13-5 shows the relationship between the transient amplitude and the duration needed to trigger a reset. Any combination of duration and amplitude above the curve generates a reset signal.

14.2 RESET DURING POWER UP/DOWN

The TLV810 output is valid when V_{DD} is greater than 1.1 V. When V_{DD} is less than 1.1 V, the output is undefined. Figure 14-2 shows a typical waveform for the power-up sequence.

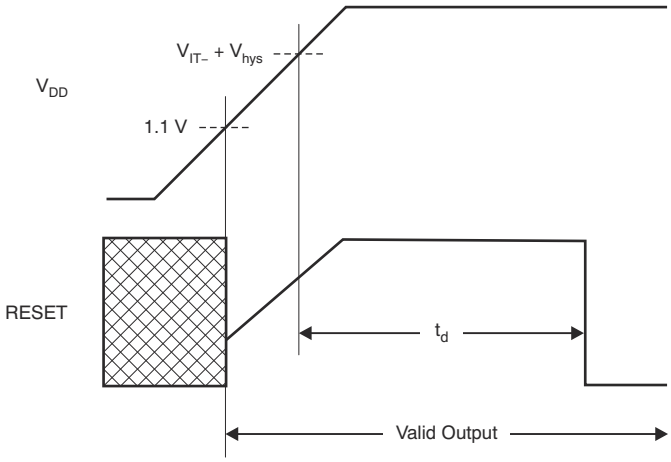


Figure 14-2. Power-Up Response

14.3 BIDIRECTIONAL RESET PINS

Some microcontrollers have bidirectional reset pins that act as both inputs and outputs. In a situation where both the TLV810 and the microcontroller are attempting to drive the RESET line, a series resistor should be placed between the output of the TLV810 and the RESET pin of the microcontroller to protect against excessive current flow. Figure 14-3 shows the connection of the TLV810 to a microcontroller using a series resistor to drive a bidirectional RESET line.

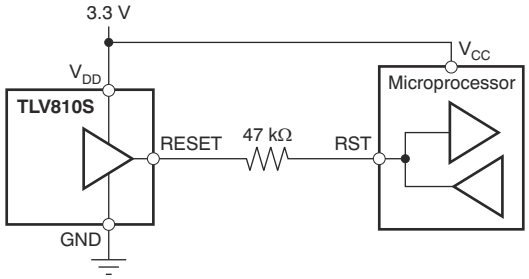


Figure 14-3. Connection to Bidirectional Reset Pin

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV810MDBZR	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VOYQ
TLV810MDBZR.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VOYQ
TLV810MDBZT	Active	Production	SOT-23 (DBZ) | 3	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VOYQ
TLV810MDBZT.A	Active	Production	SOT-23 (DBZ) | 3	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VOYQ
TLV810RDBZR	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VOWQ
TLV810RDBZR.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VOWQ
TLV810RDBZT	Active	Production	SOT-23 (DBZ) | 3	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VOWQ
TLV810RDBZT.A	Active	Production	SOT-23 (DBZ) | 3	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VOWQ
TLV810ZDBZR	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VOVQ
TLV810ZDBZR.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VOVQ
TLV810ZDBZT.A	Active	Production	SOT-23 (DBZ) | 3	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VOVQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

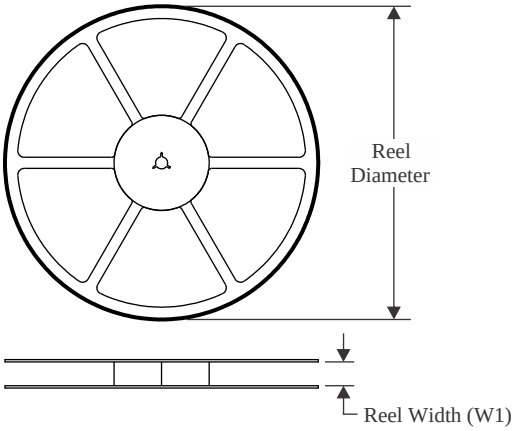
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

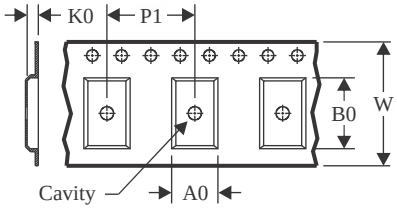
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

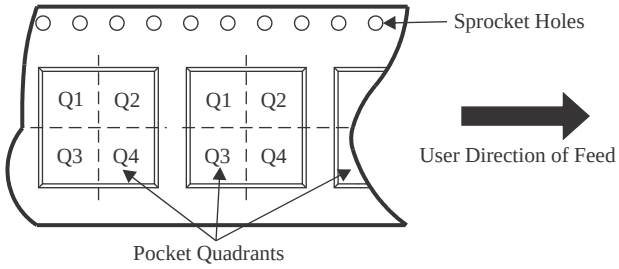


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

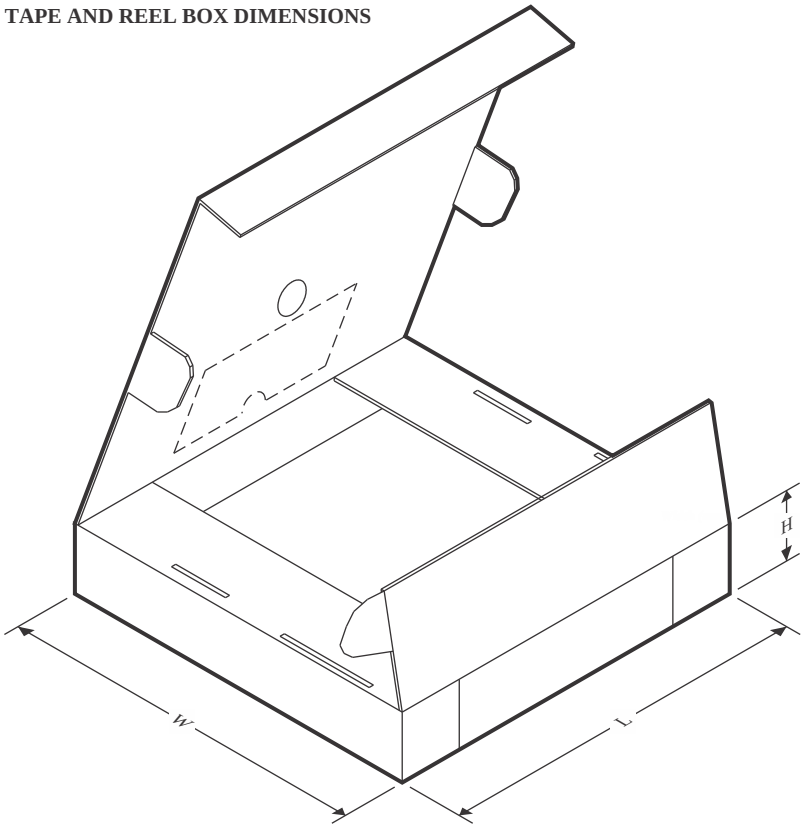
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV810MDBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV810MDBZT	SOT-23	DBZ	3	250	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV810RDBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV810RDBZT	SOT-23	DBZ	3	250	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV810ZDBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

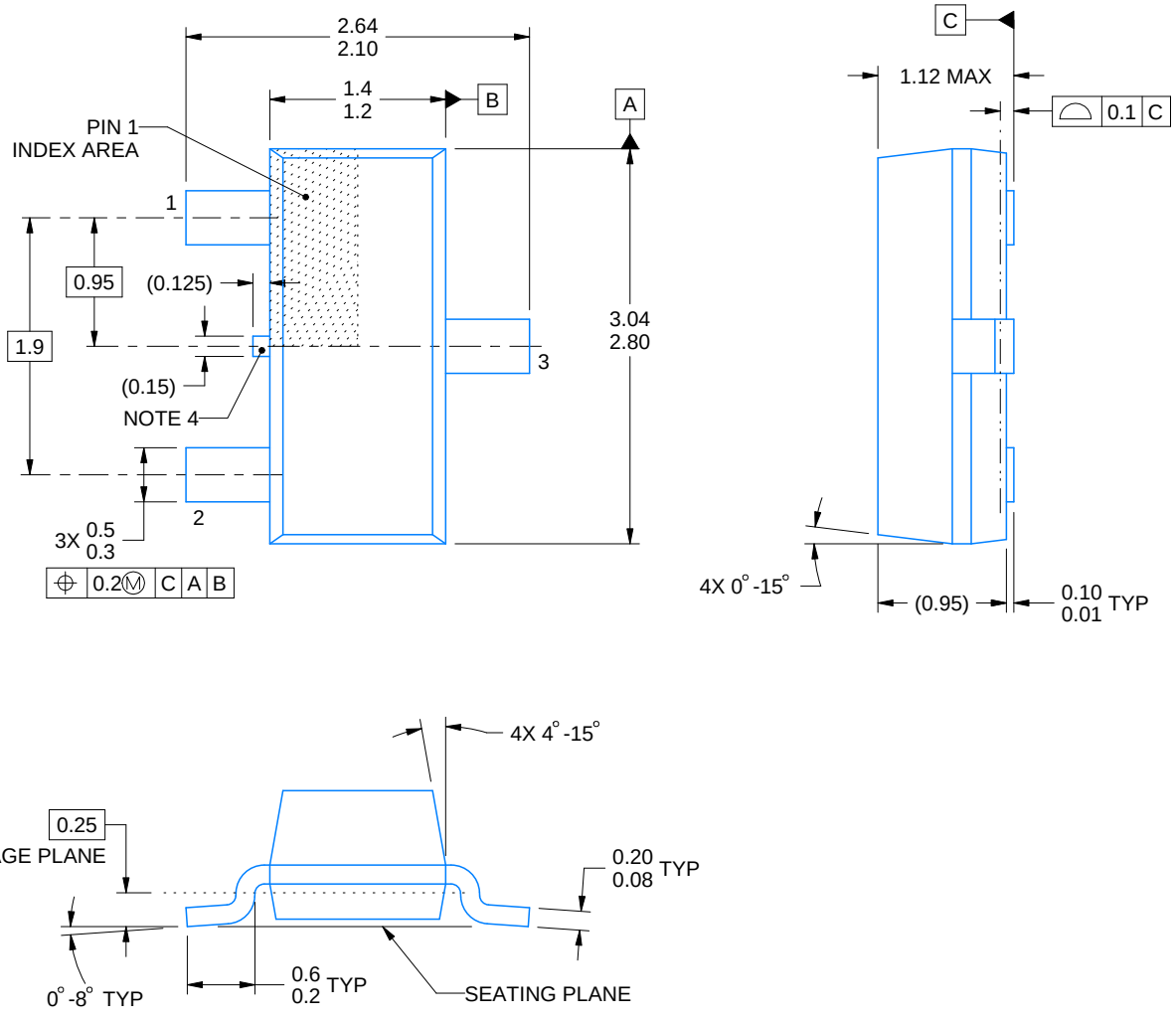
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV810MDBZR	SOT-23	DBZ	3	3000	200.0	183.0	25.0
TLV810MDBZT	SOT-23	DBZ	3	250	203.0	203.0	35.0
TLV810RDBZR	SOT-23	DBZ	3	3000	200.0	183.0	25.0
TLV810RDBZT	SOT-23	DBZ	3	250	200.0	183.0	25.0
TLV810ZDBZR	SOT-23	DBZ	3	3000	203.0	203.0	35.0

PACKAGE OUTLINE

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



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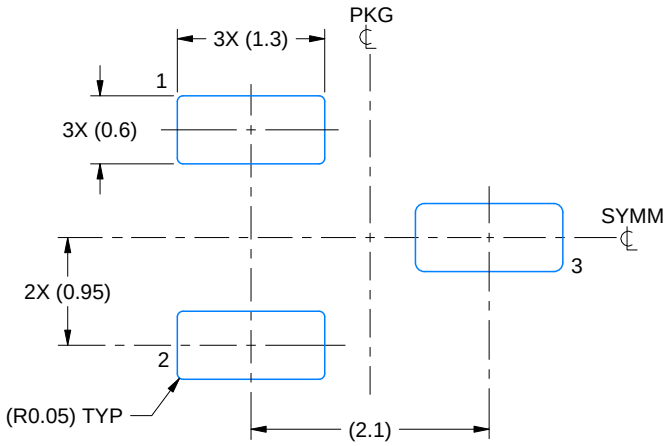
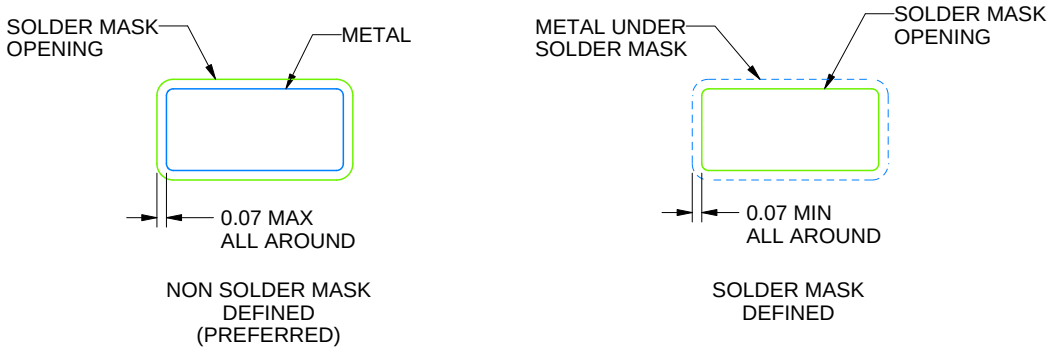
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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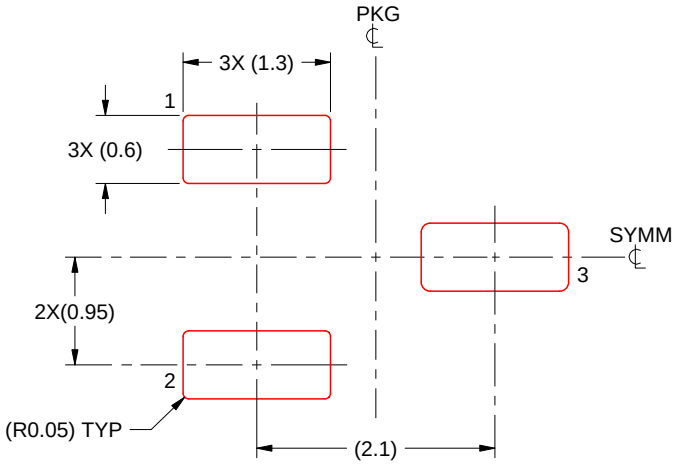
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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