TMP4719-Q1 High-Accuracy 3-Channel (2-Remote and 1-Local) 1.2V Logic Compatible Temperature Sensor With η-Factor

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to 125°C ambient operating temperature range
- Supply range: 1.62V to 5.5V
- Wide operating range: –40°C to 125°C
- Remote channel accuracy: 0.8°C
  - Resolution: 12-bit (0.0625°C)
- Local channel accuracy: 1°C
  - Resolution: 8-bit (1°C)
- Support I^2C and SMBus interface
- Low power consumption
- Additional features for improved temperature measurement accuracy:
  - Diode non-ideality factor (η-factor) correction
  - Series resistance cancellation
  - Programmable digital filter
- Remote diode fault detection
- 1.2V logic-compatible input thresholds independent of supply
- Footprint compatible with the TMP432

2 Applications

- HVAC
- Automotive infotainment systems
- Lighting
- ADAS
- Telematics control unit temperature monitoring
- Body Electronics
- Engine Control

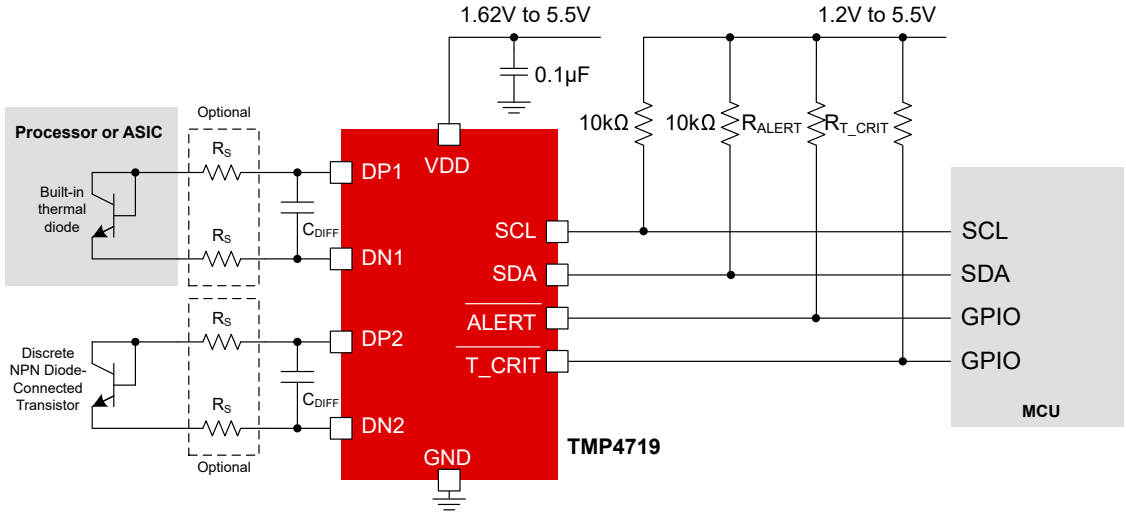
3 Description

The TMP4719-Q1 device is a high-accuracy 0.8°C temperature sensor with one local integrated sensor and two remote temperature sensor channels that can be connected to diode-connected transistors, such as the popular MMBT3904 NPN transistor, to replace traditional thermistors or thermocouples. The remote channels can also be connected to a substrate thermal transistor or diode integrated inside microprocessors, microcontrollers, or FPGAs to monitor the die temperature of the IC.

The TMP4719-Q1 supports series resistance cancellation, programmable ideality factor (η-factor), configurable temperature limits, and programmable digital filters to improve the noise immunity and provide a robust design for complex thermal environment monitoring applications. The device supports I^2C and SMBus communication with logic levels down to 1.2V regardless of the main supply rail, enabling interoperability with low-voltage MCUs without needing a secondary low-voltage supply or a bus level shifter.

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TMP4719-Q1	DGS (VSSOP, 10)	4.9mm × 3.0mm

(1) For more information, see the *Mechanical, Packaging, and Orderable* addendum.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Block Diagram

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4 Device Comparison

Table 4-1. Device Comparison

Feature	TMP4719-Q1	TMP422-Q1	TMP432	TMP442	TMP512
V_{DD} (V)	1.62 to 5.5	2.7 to 5.5	2.7 to 5.5	2.7 to 5.5	3 to 26
Local Temperature Accuracy (°C)					
-40°C (max)	±1.0	±2.5	±2.5	±2.5	±2.5
0°C (max)	±1.0	±2.5	±1.0 (1), ±2.5	±1.0 (1), ±2.5	±2.5
15°C (max)	±1.0	±1.5 (1), ±2.5	±1.0 (1), ±2.5	±1.0 (1), ±2.5	±1.0 (2), ±2.5
85°C (max)	±1.0	±1.5 (1), ±2.5	±1.0 (1), ±2.5	±1.0 (1), ±2.5	±1.0 (2), ±2.5
100°C (max)	±1.0	±2.5	±1.0 (1), ±2.5	±1.0 (1), ±2.5	±2.5
125°C (max)	±1.0	±2.5	±2.5	±2.5	±2.5
Remote Temperature Accuracy (°C)					
-40°C (max)	±1.0 (3), ±1.5 (4)	±3 (1), ±5	±1.5 (1), ±5	±1.5 (1), ±5	±3 (2), ±5
-10°C (max)	±0.8	±3 (1), ±5	±1.5 (1), ±5	±1.5 (1), ±5	±3 (2), ±5
0°C (max)	±0.8	±3 (1), ±5	±1 (1), ±5	±1 (1), ±5	±3 (2), ±5
15°C (max)	±0.8	±1 (1), ±5	±1 (1), ±5	±1 (1), ±5	±1 (2), ±5
85°C (max)	±0.8	±1 (1), ±5	±1 (1), ±5	±1 (1), ±5	±1 (2), ±5
100°C (max)	±1.0 (3), ±1.5 (4)	±3 (1), ±5	±1 (1), ±5	±1 (1), ±5	±3 (2), ±5
125°C (max)	±1.0 (3), ±1.5 (4)	±5	±5	±5	±5
Digital Input/Output					
Resolution (Bit)	12	12	12	12	13
V_{IH}/V_{IL}	0.9/0.4	2.1/0.8 70%/30%	2.1/0.8	2.1/0.8 70%/30%	2.1/0.8
Current Consumption and Conversion Time (Typ: V_{DD}=3.3V/12V and 25°C)					
T_{Conv} (ms) (per remote ch)	17	115	93	93	115
I_{AVG} at 0.0625Hz (µA)	1.53	32	35	35	-
I_{SD} (µA)	0.5	3	3	3	-
Features: R_S Cancellation, N-Factor Correction, Diode Fault Detection, Digital Filter					
I^2C Addresses	1 OPN	4 OPNs	2 OPNs	2 OPNs	4 (A0 pin)
Packaging Dimension					
Dimensions [mm × mm × mm]	**VSSOP** (10-pin) 4.9 × 3 × 1.1	**SOT-23** (8-pin) 2.9 × 2.8 × 1.1	**VSSOP** (10-pin) 4.9 × 3 × 1.1	**SOT-23** (8-pin) 2.9 × 2.8 × 1.1	**SOIC** (14-pin) 8.65 × 6 × 1.75 **VQFN** (16-pin) 4 × 4× 1

1. Temperature accuracy is specified over V_{DD}= 3.3V.
2. Temperature accuracy is specified over V_{DD}= 12V.
3. Remote temperature accuracy is specified over T_A = –10°C to 85°C.
4. Remote temperature accuracy is specified over T_A = –40°C to 125°C.

5 Pin Configuration and Functions

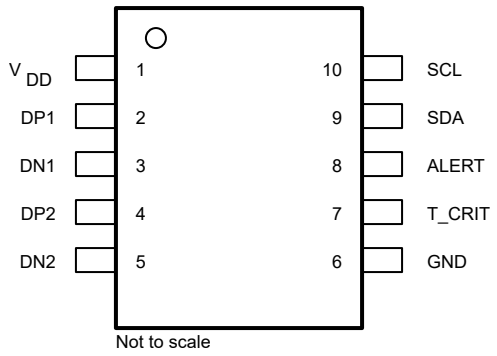


Figure 5-1. DGS Package 10-Pin VSSOP Top View

Table 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
V_{DD}	1	P	Supply Pin. Bypass to GND with a 0.1µF capacitor.
DP1	2	I/O	Positive (anode) connection to the remote diode for channel 1. Leave DP1 and DN1 open if no remote diode is used. Place a 470pF capacitor between DP1 and DN1 for noise filtering (if needed).
DN1	3	I/O	Negative (cathode) connection to the remote diode for channel 1. Leave DP1 and DN1 open if no remote diode is used. Place a 470pF capacitor between DP1 and DN1 for noise filtering (if needed).
DP2	4	I/O	Positive (anode) connection to the remote diode for channel 2. Leave DP2 and DN2 open if no remote diode is used. Place a 470pF capacitor between DP2 and DN2 for noise filtering (if needed).
DN2	5	I/O	Negative (cathode) connection to the remote diode for channel 2. Leave DP2 and DN2 open if no remote diode is used. Place a 470pF capacitor between DP2 and DN2 for noise filtering (if needed).
GND	6	G	Ground connection
$\overline{T\_CRIT}$	7	I/O	Open-drain critical temperature alert pin. A pullup resistor to V_{DD} (or a separate bus) is required. T_CRIT and ALERT pins can be floating if not in use.
ALERT	8	O	Open-drain temperature alert pin. A pullup resistor to VDD (or a separate bus) is required. T_CRIT and ALERT pins can be floating if not in use.
SDA	9	I/O	Open-drain serial data line. Requires a pullup resistor.
SCL	10	I	Input serial data line clock. Note I^2C clock stretching is not supported.

(1) I = Input; O = Output; I/O = Input or Output; G = Ground; P = Power/Supply

6 Specifications

6.1 Absolute Maximum Ratings

Over free-air temperature range unless otherwise noted(1)

		MIN	MAX	UNIT
Supply voltage	VDD	–0.3	6	V
I/O voltage	DP1, DP2	–0.3	1.65	V
	DN1, DN2	–0.3	0.3	V
	$\overline{\text{ALERT}}$, $\overline{\text{T\_CRIT}}$, SCL, SDA	–0.3	6	V
I/O current	$\overline{\text{ALERT}}$, $\overline{\text{T\_CRIT}}$, SDA	–10	10	mA
Operating junction temperature, T_J		–55	150	°C
Storage temperature, T_{stg}		–65	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±750	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	1.62	3.3	5.5	V
$V_{I/O}$	DP1, DP2	0		1.2	
	DN1, DN2	0		0	
	$\overline{\text{ALERT}}$, $\overline{\text{T\_CRIT}}$, SCL, SDA	0		5.5	
$I_{I/O}$	$\overline{\text{ALERT}}$, $\overline{\text{T\_CRIT}}$, SDA			3	mA
T_A	Operating ambient temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TMP4719-Q1 DGS (VSSOP) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	155.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	62.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	91.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	90.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.5 Electrical Characteristics

Over free-air temperature range at T_A = –40°C to 125°C and V_{DD} = 1.62V to 5.5V (unless otherwise noted); Typical specifications are at T_A = 25°C and V_{DD} = 3.3V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
TEMPERATURE SENSOR							
T_{ERR_L}	Local temperature accuracy	T_A = –40°C to 125°C		–1		1	°C
T_{ERR_R}	Remote temperature accuracy (Optimized for 2N3904 NPN Transistor)	T_D = –10°C to 85°C, T_A = –10°C to 85°C		–0.8		0.8	°C
		T_D = –55°C to 125°C,	T_A = –10°C to 85°C	–1.0		1.0	°C
			T_A = –40°C to 125°C	–1.5		1.5	°C
PSR	Supply Sensitivity on accuracy	Remote temperature sensor, one-shot mode, V_{DD} = 1.62V to 5.5V			0.05		°C/V
T_{RES_L}	Temperature resolution (local)	Including sign bit			8		Bits
		LSB			1		°C
T_{RES_R}	Temperature resolution (remote)	Including sign bit			12		Bits
		LSB			0.0625		°C
T_{REPEAT}	Repeatability[1]	V_{DD} = 3.3V, 1Hz conversion cycle, no averaging			1.5		LSB
t_{RT}	Response time (Stirred Liquid, mounted on 2-layer 62-mil PCB)	τ = 63% 25°C to 75°C	Local temperature sensor		1.5		s
		τ = 63% 25°C to75 °C	Remote temperature sensor (MMBT3904 NPN Transistor)		0.5		s
V_{FMAX}	Forward diode voltage	Supported voltage applied to remote diode				1.1	V
R_S	Series resistor	Supported series resistance on remote channel				1000	Ω
C_{DIFF}	Differential filter capacitor	Supported capacitive filter connected across DP and DN				1.5	nF
t_{CONV}	Conversion time	Local conversion only, one-shot mode			18.2		ms
		Remote (2-ch) + local conversion, one-shot mode			52		ms
t_{VAR}	Timing variation	Conversion period and conversion time		–10		10	%
DIGITAL INPUT/OUTPUT							
C_{IN}	Input capacitance	ALERT, T_CRIT, SCL, SDA	f = 100kHz		7		pF
V_{IH}	Input logic high level	SCL, SDA		0.9			V
V_{IL}	Input logic low level	SCL, SDA				0.4	V
V_{HYS}	Input logic level hysteresis	SCL, SDA			100		mV
I_{LI}	Input leakage current	$\overline{ALERT}$, $\overline{T\_CRIT}$, SCL, SDA		–0.1		0.1	µA
I_{LO}	Output leakage current	$\overline{ALERT}$, $\overline{T\_CRIT}$, SDA		–0.1		0.1	µA
V_{OL}	Output low level	$\overline{ALERT}$, $\overline{T\_CRIT}$, SDA, I_{OL} = 3mA			0.15	0.4	V
POWER SUPPLY							
I_{DD_ACTIVE}	Active conversion current	T_A = –40°C to 125°C Serial bus inactive	Local conversion stage		100	150	µA
			Remote conversion stage		220	320	µA
I_{DD_AVG}	Average current consumption	Serial bus inactive, continuous conversion	Conversion period = 1s, all channels		11		µA
			Conversion period = 0.125 s, all channels		75		µA
I_{DD_SB}	Standby current[2]	Serial bus inactive	T_A = 25°C		1	1.5	µA
			T_A = –40°C to 125°C			5.5	µA

6.5 Electrical Characteristics (continued)

Over free-air temperature range at T_A = –40°C to 125°C and V_{DD} = 1.62V to 5.5V (unless otherwise noted); Typical specifications are at T_A = 25°C and V_{DD} = 3.3V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DD_SD}	Shutdown current	Serial bus inactive	T_A = 25°C		0.5	0.8	µA
			T_A = –40°C to 125°C			5	µA
		Serial bus active. fs = 400kHz			6.9		µA
		Serial bus active. fs = 1MHz			15.2		µA
V_{POR}	Power-on reset threshold voltage	Supply rising			1.2	1.4	V
	Brownout detect	Supply falling		1.0	1.1		V
t_{POR}	Device initialization time after power up(3)				15		ms

(1) Repeatability is the ability to reproduce a reading when the measured temperature is applied consecutively, under the same conditions.
(2) Quiescent current between conversions in continuous conversion mode
(3) Refer to Device Initialization and Default Temperature Conversion for additional details

6.6 I²C Interface Timing

minimum and maximum specifications are over –40 °C to 125 °C and V_{DD} = 1.62 V to 5.5 V (unless otherwise noted)(1)

		STANDARD MODE		FAST MODE		UNIT
		MIN	MAX	MIN	MAX	
$f_{(SCL)}$	SCL operating frequency(2)	1	100	1	400	kHz
$t_{(BUF)}$	Bus free time between STOP and START condition	4.7	–	1.3	–	µs
$t_{(HDSTA)}$	Hold time after repeated START condition. After this period, the first clock is generated.	4.0	–	0.6	–	µs
$t_{(SUSTA)}$	Repeated START condition setup time	4.7	–	0.6	–	µs
$t_{(SUSTO)}$	STOP condition setup time	4.0	–	0.6	–	µs
$t_{(HDDAT)}$	Data hold time(3)	0	3450	0	900	ns
$t_{(SUDAT)}$	Data setup time	250	–	100	–	ns
$t_{(LOW)}$	SCL clock LOW period	4.7	–	1.3	–	µs
$t_{(HIGH)}$	SCL clock HIGH period	4.0	–	0.6	–	µs
$t_{(VDAT)}$	Data valid time (data response time)(4)	–	3.45	–	0.9	µs
t_F	Clock and data fall time(5)	–	300	20 × (V_{DD} / 5.5 V)	300	ns
t_R	Clock and data rise time(5)	–	1000	20	300	ns
$t_{timeout}$	Timeout (SCL = GND)	20	30	20	30	ms

(1) The controller and target have the same I/O supply value. Values are based on statistical analysis of samples tested during initial release.
(2) Device is equipped with a 50-ns spike filter on both SCL and SDA lines. The filter allows the device to be used alongside I3C devices without impacting the communication.
(3) The maximum $t_{(HDDAT)}$ can be 3.45 µs and 0.9 µs for Standard Mode and Fast Mode, but must be less than the maximum of $t_{(VDAT)}$ by a transition time.
(4) $t_{(VDAT)}$ = time for data signal from SCL LOW to SDA output (HIGH to LOW, depending on which is worse).
(5) Device is not sensitive to rise and fall time. Violation of rise and fall time does not lead to communication failure.

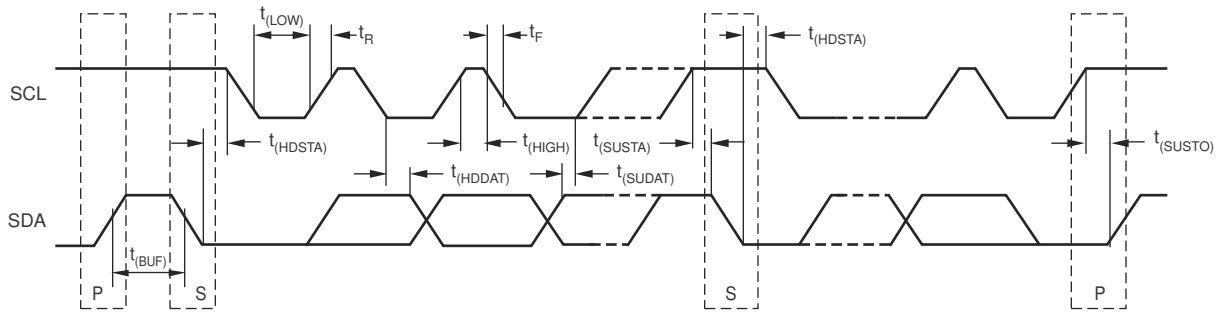
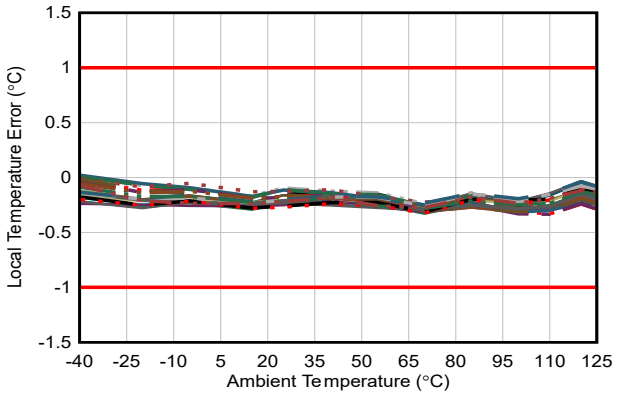


Figure 6-1. Two-Wire Timing Diagram

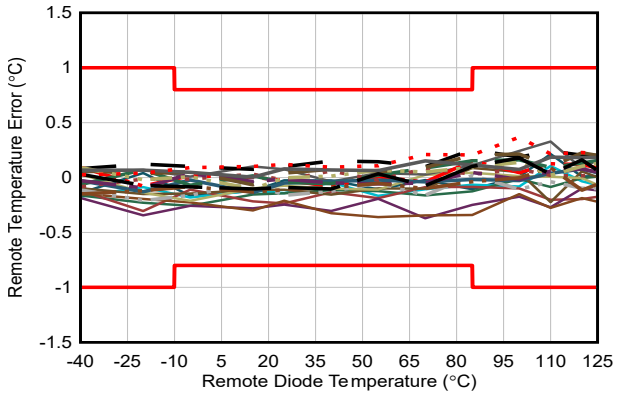
6.8 Typical Characteristics

at T_A = 25°C and V_{DD} = 3.3V (unless otherwise noted)



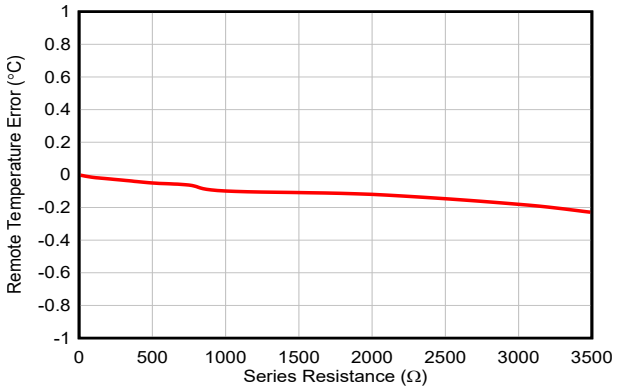
V_{DD} = 1.62V to 5.5V

Figure 6-2. Local Temperature Error vs Temperature



Characterized with MMBT3904 NPN Transistor; T_A = 25°C; 30 units

Figure 6-3. Remote Temperature Error vs Temperature



Characterized with MMBT3904 NPN Transistor; 7 units averaged

Figure 6-4. Remote Temperature Error vs Series Resistance

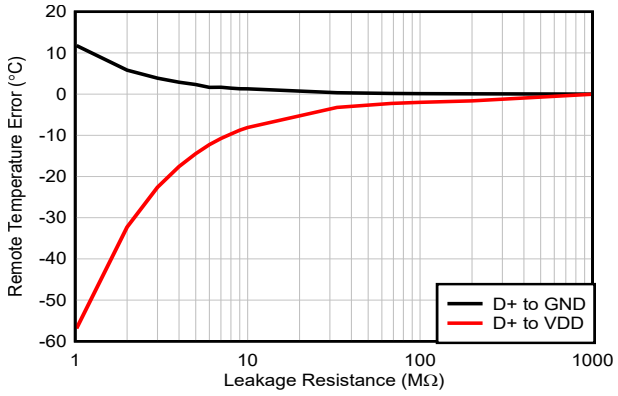
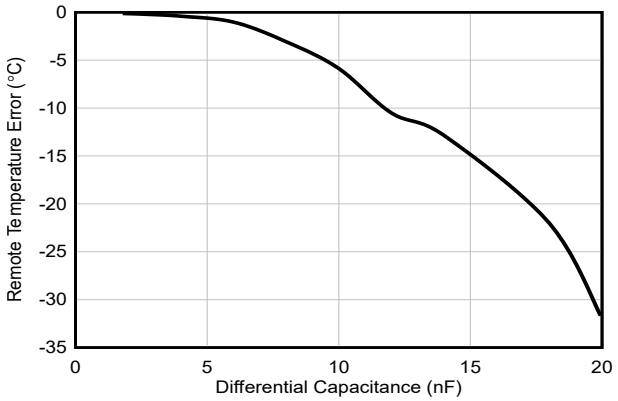
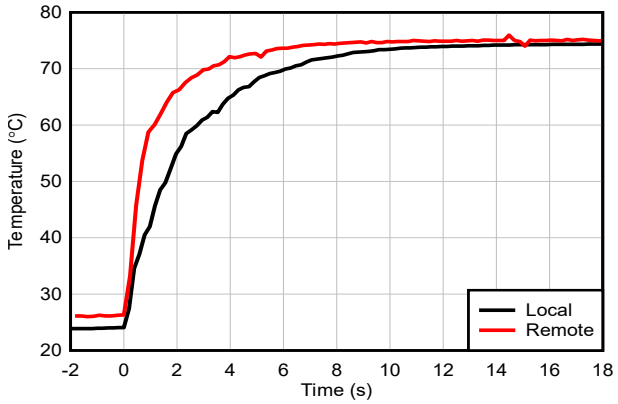


Figure 6-5. Remote Temperature Error vs Diode Parallel Leakage Resistance



Characterized with MMBT3904 NPN Transistor

Figure 6-6. Remote Temperature Error vs Differential Capacitance

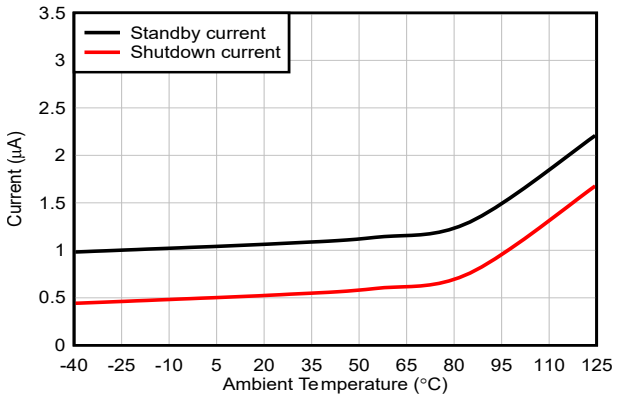


Local: soldered devices on 62mil 2-layer FR4 PCB
Remote: characterized with MMBT3904 NPN Transistor
Temperature Step: T_A jumps from 25°C to 75°C

Figure 6-7. Response Time (Stirred Liquid)

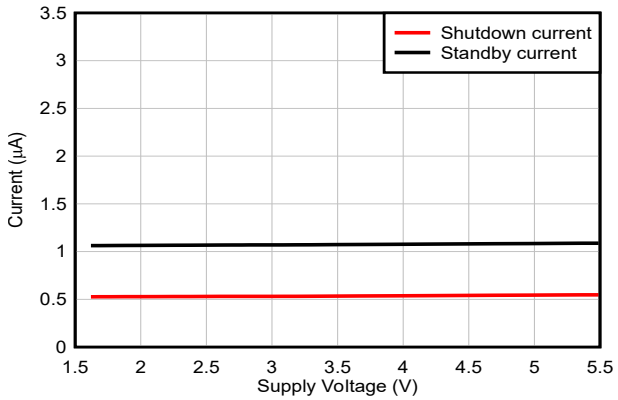
6.8 Typical Characteristics (continued)

at T_A = 25°C and V_{DD} = 3.3V (unless otherwise noted)



Serial Bus Inactive

Figure 6-8. Standby and Shutdown Current vs Temperature



Serial Bus Inactive, V_{DD} = 1.62V to 5.5V

Figure 6-9. Standby and Shutdown Current vs Supply Voltage

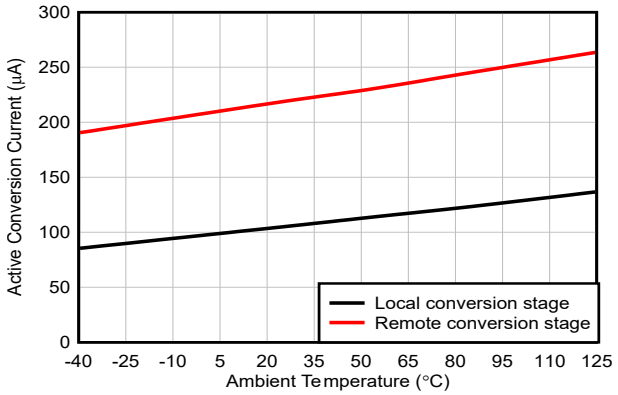
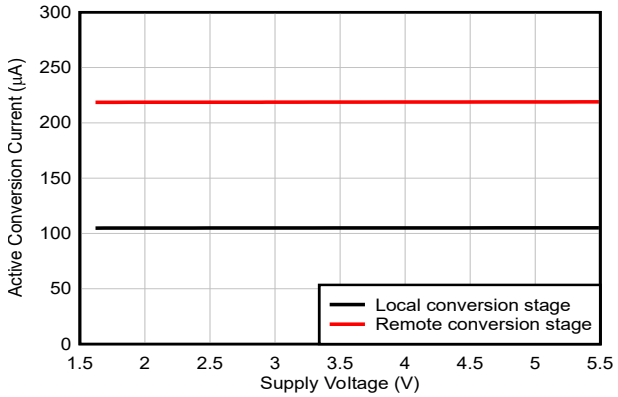


Figure 6-10. Active Current vs Temperature



V_{DD} = 1.62V to 5.5V

Figure 6-11. Active Current vs Supply Voltage

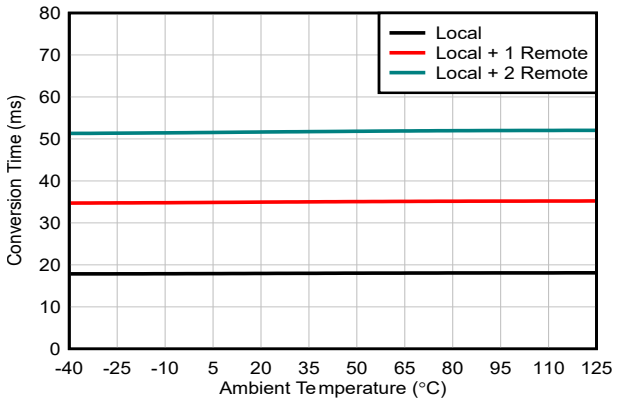
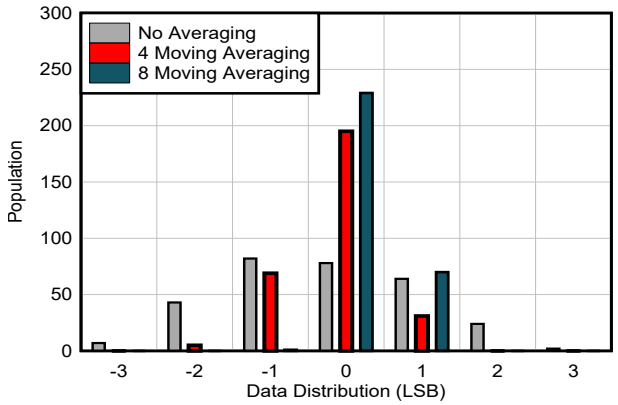


Figure 6-12. Conversion Time vs Temperature



Characterized with MMBT3904 NPN Transistor

Figure 6-13. Remote Temperature Noise Data Distribution (300 Samples)

7 Detailed Description

7.1 Overview

The TMP4719-Q1 is a digital temperature sensor that combines a local temperature measurement channel and 2 remote-junction temperature measurement channels in a single 10-pin package. The device is I^2C and SMBus compatible and is specified over a temperature range of –40°C to 125°C. The device supports various features to improve the noise immunity of the device and provide a robust design for complex thermal environment monitoring applications, including series resistance cancellation, programmable ideality factor (η-factor), programmable temperature limits, and programmable digital filters. The device supports I^2C and SMBus communication with logic levels down to 1.2V regardless of the main supply rail, enabling interoperability with low-voltage MCUs without needing a secondary low-voltage supply.

7.2 Functional Block Diagram

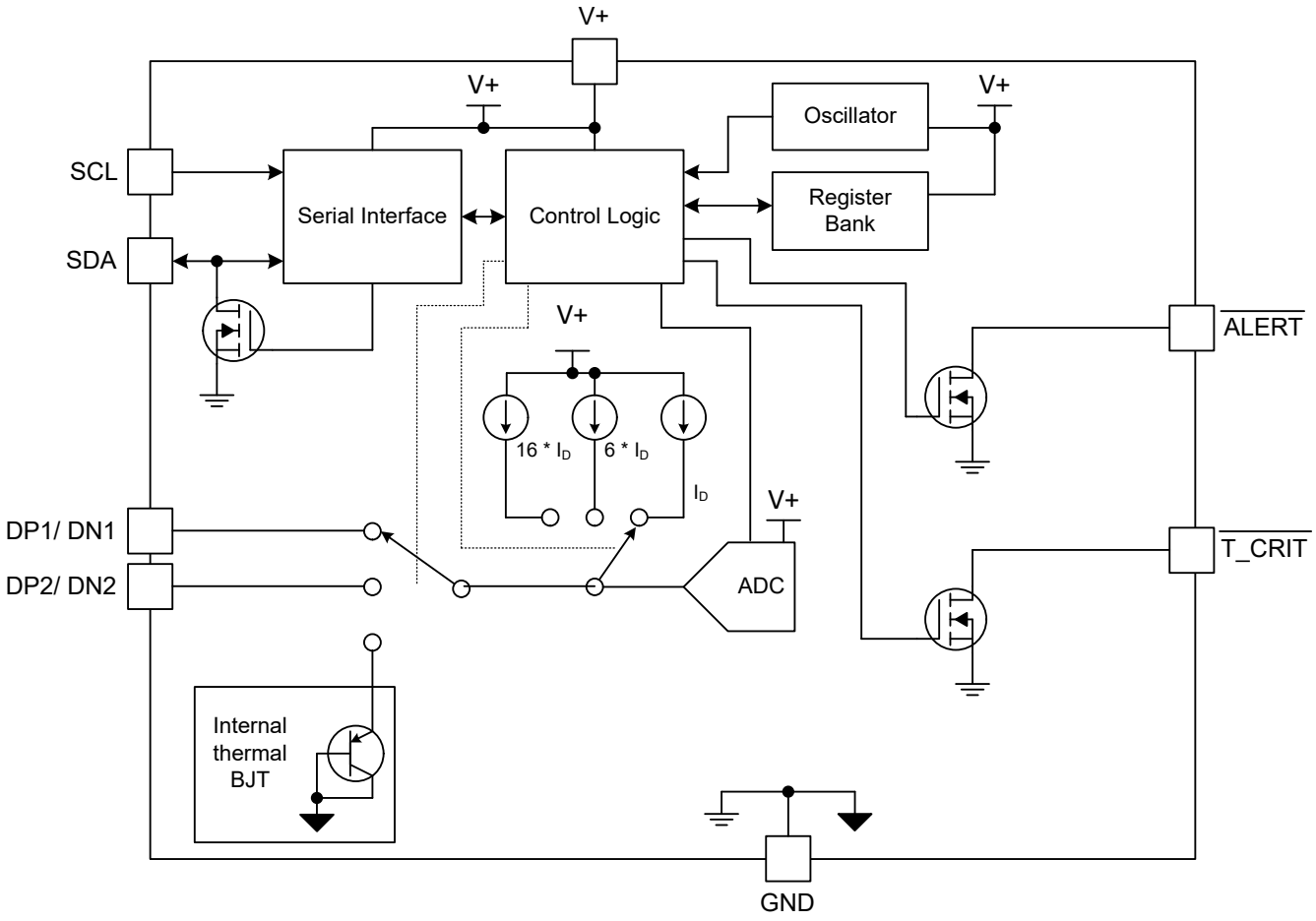


Figure 7-1. Functional Block Diagram

7.3 Feature Description

7.3.1 Device Initialization and Default Temperature Conversion

When V_{DD} goes above V_{POR} (power-on reset threshold), the device initiates the power-on reset (POR) sequence and starts loading default configuration settings into the device. After the device initialization is complete, the device starts default local (1 channel) and remote (2 channels) temperature conversion. The converted result and corresponding output ($\overline{ALERT}$ or $\overline{T\_CRIT}$) are asserted if the corresponding limit is crossed.

The device initialization and default conversion take approximately 67ms. During device initialization, the supply voltage V_{DD} is held stable and above V_{POR} (falling) to avoid any device misbehavior. Figure 7-2 depicts the details timing sequence for the device initialization and default temperature conversion.

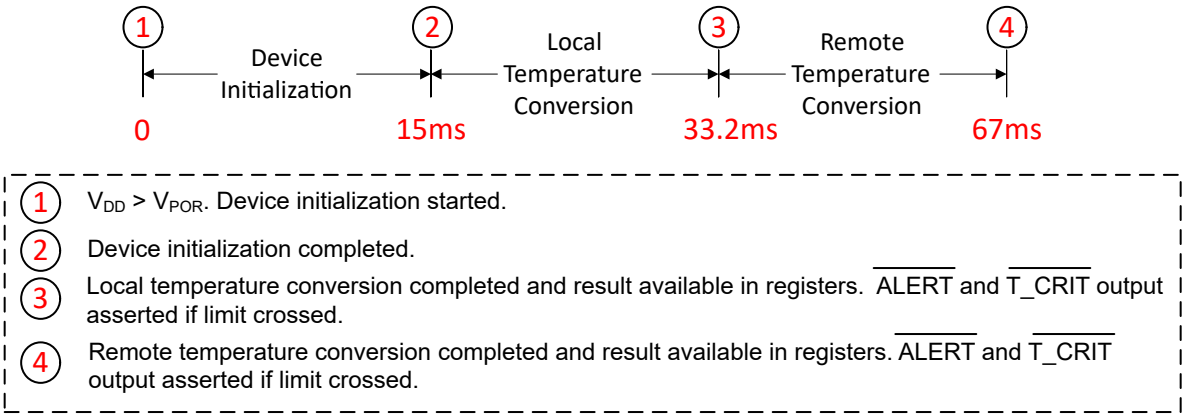


Figure 7-2. Device Initialization and Default Temperature Conversion Timing

7.3.2 Series Resistance Cancellation

Series resistance cancellation automatically eliminates the temperature error caused by the resistance of the routing to the remote transistor or by the resistors of the optional external low-pass filter. A total of up to 1kΩ of series resistance can be canceled by the device, thus eliminating the need for additional characterization and temperature offset correction.

7.3.3 $\overline{ALERT}$ and $\overline{T\_CRIT}$ Output

The TMP4719-Q1 $\overline{ALERT}$ and $\overline{T\_CRIT}$ pins are active-low open-drain outputs. The $\overline{ALERT}$ pin is asserted at the end of a conversion cycle when the measured temperature exceeds a High Alert Limit or goes below a Low Alert Limit. The $\overline{T\_CRIT}$ pin is asserted at the end of a conversion cycle when the measured temperature exceeds the T_CRIT limit defined in the limit register. The $\overline{ALERT}$ and $\overline{T\_CRIT}$ pins can be used to notify the system of overtemperature or undertemperature conditions and protect from thermally induced system damage. Note that the $\overline{ALERT}$ and $\overline{T\_CRIT}$ outputs are activated only when the corresponding bits are not masked in the Alert_Mask register.

7.3.4 1.2V Logic Compatible Inputs

The device includes static input thresholds independent of supply to maintain compatibility with a 1.2V logic I^2C or SMBus. This removes the need for a translator when operating with a bus voltage different from the supply voltage of the device.

7.3.5 Digital Filter

Remote junction temperature sensors are typically implemented in a noisy environment. Noise is most often created by fast digital signals that can corrupt measurements. A digital filter is available for the remote temperature measurements to reduce the effect of noise. This filter is programmable and has two levels when enabled. Level 1 performs a moving average of four consecutive samples. Level 2 performs a moving average of eight consecutive samples. After POR, the output of the digital filter starts with a default ZERO without previous data. The output of the digital filter is stored in the remote temperature result register, and the temperature limits are compared to this value. The filter responses to impulse and step inputs are shown in Figure 7-3 and Figure 7-4, respectively. The filter can be enabled or disabled by programming the desired levels in register settings. The digital filter is disabled by default.

The averages are cleared after the filter is set to 00h. Filtering can be used with both continuous conversions and one-shot conversions.

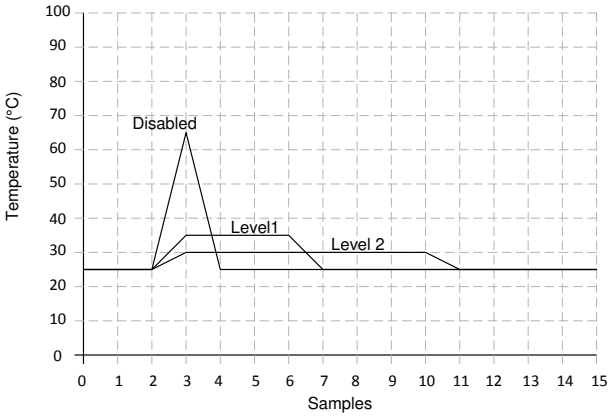


Figure 7-3. Filter Response to Impulse Inputs

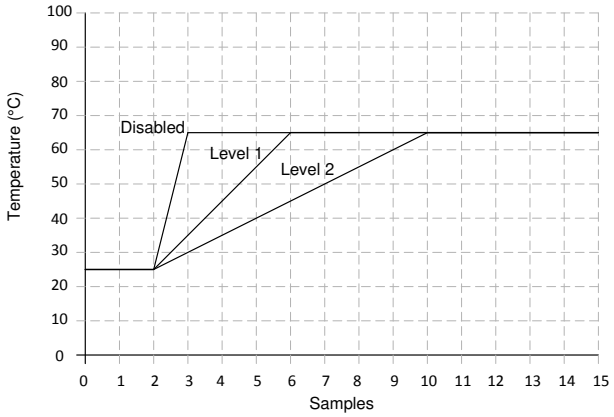


Figure 7-4. Filter Response to Step Inputs

In addition to the built-in digital filter of the device, TI recommends the user add an external capacitor between the DP and DN pins on the remote channel. The capacitor acts as a bypass filter to help reduce high-frequency EMI noise when the device is operating in a noisy environment. The recommended optimal value for the capacitor is 470pF, and the value must not exceed 3nF to allow proper operation of the temperature sensor.

7.3.6 One-Shot Conversions

Users can write any data to the one-shot register to trigger a manual single one-shot conversion. This allows for greater control of the device and flexibility of system implementation. This feature is only available in Shutdown mode, and writes to the one-shot register has no effect in continuous conversion mode. For best performance in one-shot mode, have the communication bus idle during temperature conversion (within t_{CONV} after a conversion is triggered).

7.4 Device Functional Modes

The device can be configured to operate in different modes of operation through the configuration register.

7.4.1 Interrupt and Comparator Mode

The $\overline{\text{ALERT}}$ pin of the device can be programmed into two different $\overline{\text{ALERT}}$ output modes. In the interrupt mode, the device asserts the $\overline{\text{ALERT}}$ pin if the temperature exceeds the limits set by the temperature limit registers. After the Alert Status is read and interrupt bits cleared, the $\overline{\text{ALERT}}$ pin is deasserted. In Comparator Mode, the device asserts the $\overline{\text{ALERT}}$ pin if the measured temperature exceeds the limits and clears when the temperature returns below the limits.

7.4.1.1 Interrupt Mode

When the Alert Mode Setting bit in the Configuration Register is set to 0, the Alert Mode is set to Interrupt mode. In this mode, the $\overline{\text{ALERT}}$ pin is asserted at the end of a conversion cycle if the measured temperature exceeds a High Alert Limit or goes below a Low Alert Limit defined in the limit registers. In this mode, the TMP4719-Q1 sets the $\overline{\text{ALERT}}$ mask bit of the Configuration Register during a read of the Status Register if any flag in the Status Register, except the ADC_Busy flag and Remote Diode Fault flag, is set. This prevents the $\overline{\text{ALERT}}$ pin from triggering until the controller has reset the ALERT mask bit (write 0 to the Alert_MASK bit in Configuration Register).

The $\overline{\text{ALERT}}$ High Status flag is set at the end of a conversion cycle when a measured temperature exceeds the respective High Alert Limit register limit. There are separate High Limit values and status register flags for the remote and local temperature measurements. The High Limit Status register flags are only set based on respective temperature measurements. Refer to Section 8.30 .

The $\overline{\text{ALERT}}$ Low Status flag is set at the end of a conversion cycle when a measured temperature is below the respective Low Alert Limit register limit. There are separate Low Limit values and status register flags for the remote and local temperature measurements. The Low Limit Status register flags are only set based on respective temperature measurements. Refer to Section 8.31 .

The Status Register limit flags are cleared after a read command of the Status Register from the controller and are set again at the end of a preceding temperature conversion cycle if the measured temperature is outside the set limits.

Figure 7-5 shows the behavior of the ALERT pin and flags while in Interrupt mode.

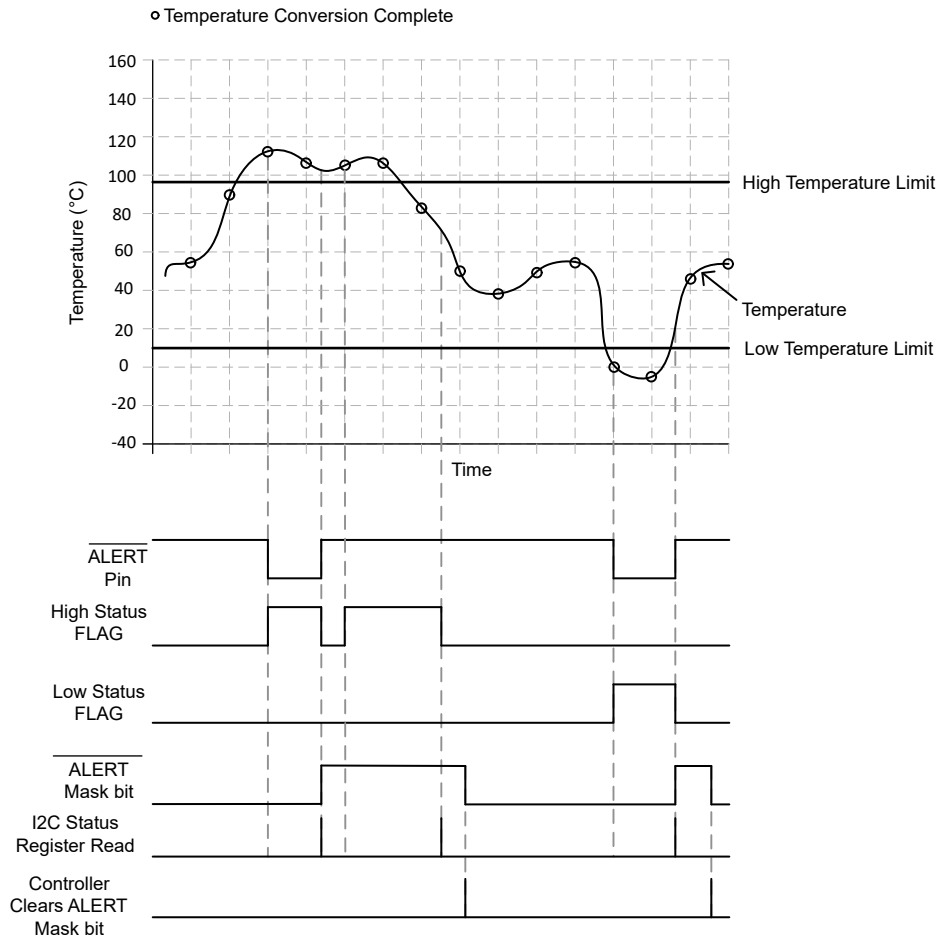


Figure 7-5. Alert Interrupt Mode Timing Diagram

7.4.1.2 Comparator Mode

When the Alert Mode Setting bit in the Configuration Register is set to 1, the Alert Mode is set to Comparator mode. In this mode, the $\overline{\text{ALERT}}$ pin is asserted at the end of a conversion cycle if the measured temperature exceeds a High Alert Limit or goes below a Low Alert Limit defined in the limit registers. The $\overline{\text{ALERT}}$ pin deasserts at the end of the preceding conversion cycle if the measured temperature is equal to or below a High Alert limit minus hysteresis and equal to or above a Low Alert limit plus hysteresis defined in the limit registers. The $\overline{\text{ALERT}}$ mask bit does not set after reading the status register in comparator mode.

The $\overline{\text{ALERT}}$ High Status flag sets at the end of a conversion cycle when the measured temperature exceeds a High Alert Limit register limit and clear at the end of a conversion cycle when the measured temperature is equal to or below the High Limit value minus hysteresis. There are separate High Limit values and status register flags for the remote and local temperature measurements. The status register flags only set or clear to the respective temperature measurements. Refer to Section 8.30 .

The $\overline{\text{ALERT}}$ Low Status flag sets at the end of a conversion cycle when the measured temperature is below a Low Alert Limit register limit and clears at the end of a conversion cycle when the measured temperature is equal to or above the Low Limit value plus hysteresis. There are separate Low Limit values and status register flags for the remote and local temperature measurements. The status register flags only set or clear to the respective temperature measurements. Refer to Section 8.31 .

Figure 7-6 shows the behavior of the $\overline{\text{ALERT}}$ pin and flags while in Comparator mode.

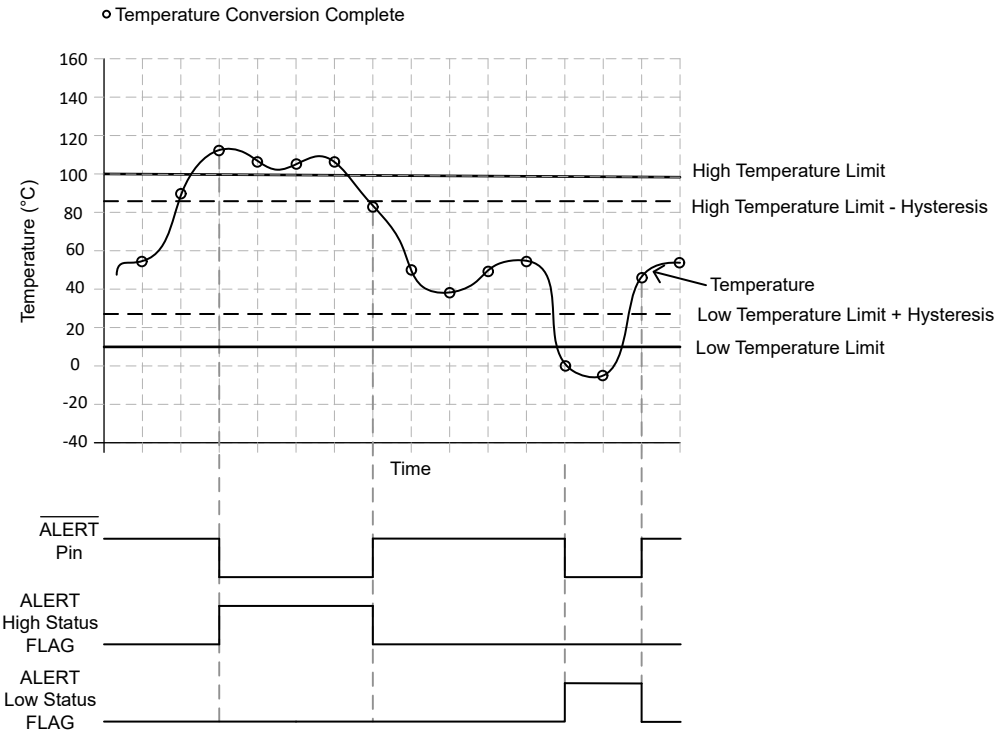


Figure 7-6. Alert Comparator Mode Timing Diagram

7.4.1.3 $\overline{\text{T\_CRIT}}$ Output

The TMP4719-Q1 $\overline{\text{T\_CRIT}}$ pin is an active-low, open-drain output which is asserted at the end of a conversion cycle when the measured temperature exceeds a $\overline{\text{T\_CRIT}}$ Limit defined in the $\overline{\text{T\_CRIT}}$ limit registers. A $\overline{\text{T\_CRIT}}$ Status Register flag is set at the end of a conversion cycle when the measured temperature exceeds a $\overline{\text{T\_CRIT}}$ Limit. The $\overline{\text{T\_CRIT}}$ pin deasserts at the end of a conversion cycle if the temperature measurement is less than the $\overline{\text{T\_CRIT}}$ limit – $\overline{\text{T\_CRIT}}$ Hysteresis. The $\overline{\text{T\_CRIT}}$ Hysteresis is set in the Hysteresis register.

When the TMP4719-Q1 is set in interrupt mode, the status register flag is cleared by reading the status register. The Status Register flag continues to set after the end of a conversion cycle until the temperature measurement

is below the T_CRIT limit – T_CRIT Hysteresis value or the device is reset. T_CRIT has no mask bit. Note that reading the Status Register sets the ALERT mask bit of the Configuration Register if any flag in the Status Register, except the ADC_Busy flag and Remote Diode Fault flag, is set. The ALERT mask bit does not mask the T_CRIT pin, which means the clearance of ALERT mask bit has no influence on T_CRIT pin, and T_CRIT has no mask bit. There are separate T_CRIT Limit values and status register flags for the remote and local temperature measurements.

Figure 7-7 shows the behavior of the T_CRIT pin and flags in interrupt mode.

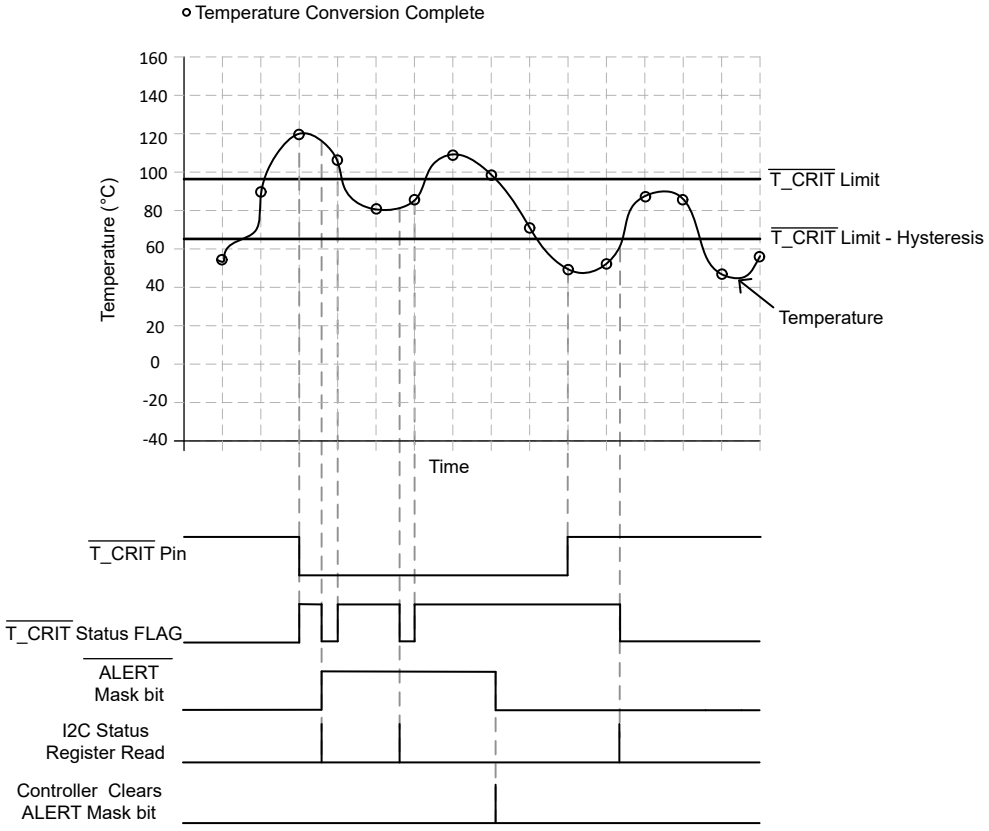


Figure 7-7. T_CRIT Output Timing Diagram-Interrupt Mode

When the TMP4719-Q1 is in comparator mode, the status register flag is only cleared at the end of a conversion cycle if the temperature measurement is below the T_CRIT limit – T_CRIT Hysteresis value. Figure 7-8 shows the behavior of the T_CRIT pin and flags in comparator mode.

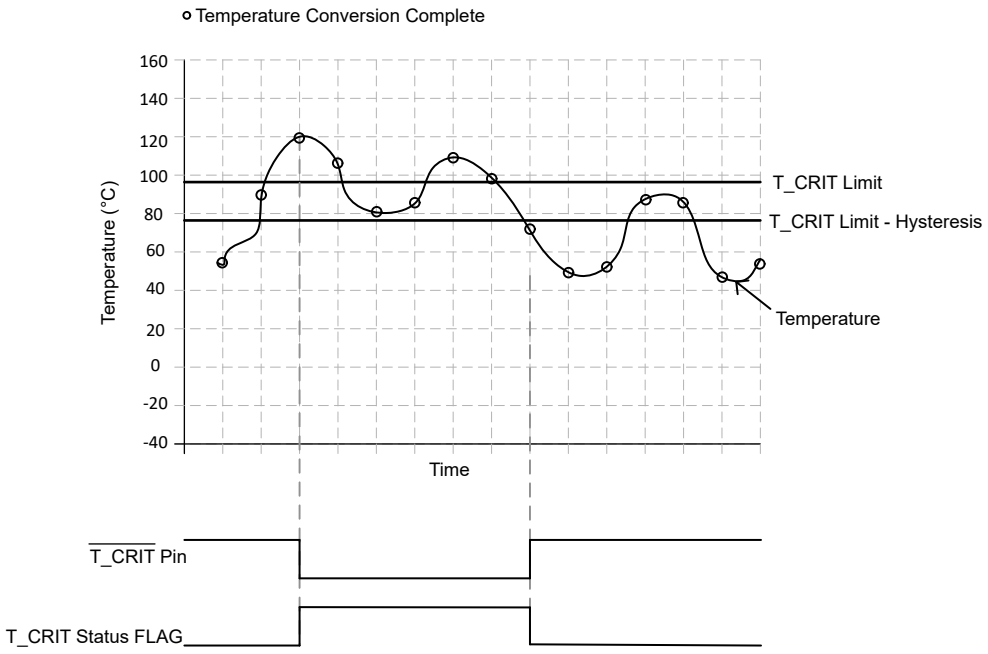


Figure 7-8. T_CRIT Output Timing Diagram-Comparator Mode

7.4.2 Shutdown Mode

When the Mode bit is set to 1 in the Configuration register, the device immediately enters the low-power shutdown mode. If the device is making a temperature conversion, the device stops the conversion and discard the partial result. In this mode, the device powers down all active circuitry and can be used in conjunction with the One_Shot bit to perform temperature conversions. Engineers can use the device for battery-operated systems and other low-power consumption applications because the device typically only consumes 0.5µA in Shutdown mode.

Entering Shutdown mode does not clear any active Alerts and does not deassert the ALERT or T_CRIT pins.

7.4.3 Continuous Conversion Mode

When the Mode bit is set to 0 in the Configuration register, the device operates in continuous conversion mode. The device continuously performs temperature conversions in this mode. The device does not wait until the end of the conversion period to update the temperature; instead, the temperature result register is updated at the end of the temperature conversion. While the ADC is converting, the ADC_Busy bit is set to 1 in the Status register.

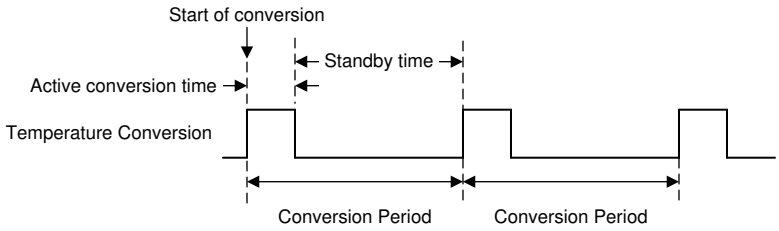


Figure 7-9. Conversion Period Timing Diagram

7.5 Programming

7.5.1 Temperature Data Format

Remote Temperature data is represented by an 12-bit, two's complement word with an LSB (Least Significant Bit) equal to 0.0625°C.

Table 7-1. Remote Temperature Data Format

TEMPERATURE	DIGITAL OUTPUT	
	BINARY	HEX
-127.875°C	1000 0000 0010 0000	8020
−25.750°C	1110 0110 0100 0000	E640
−2.250°C	1111 1101 1100 0000	FDC0
−1.125°C	1111 1110 1110 0000	FEE0
0°C	0000 0000 0000 0000	0000
1.125°C	0000 0001 0010 0000	0120
2.250°C	0000 0010 0100 0000	0240
25.750°C	0001 1001 1100 0000	19C0
127.875°C	0111 1111 1110 0000	7FE0

Local Temperature data is represented by an 8-bit, two's complement word with an LSB (Least Significant Bit) equal to 1°C.

Table 7-2. Local Temperature Data Format

TEMPERATURE	DIGITAL OUTPUT	
	BINARY	HEX
-128°C	1000 0000	80
−25°C	1110 0110	E6
−2°C	1111 1101	FD
−1°C	1111 1110	FE
0°C	0000 0000	00
1°C	0000 0001	01
2°C	0000 0010	02
25°C	0001 1001	19
127°C	0111 1111	7F

Refer to the *How to Read and Interpret Digital Temperature Sensor Output Data* application note for more information about data encoding.

7.5.2 I²C and SMBus Interface

The TMP4719-Q1 has a standard bidirectional I²C interface that can be configured or read by a controller. Each target on the I²C bus has a specific device address to differentiate between other target devices that are on the same I²C bus. Target devices require configuration upon start-up to set the behavior of the device. This is typically done when the controller accesses internal register maps of the target, which have unique register addresses. A device can have one or multiple registers where data is stored, written, or read. The TMP4719-Q1 includes 50ns glitch suppression filters, allowing the device to coexist on I3C mixed bus.

The physical I²C interface consists of the serial clock (SCL) and serial data (SDA) lines. Both SDA and SCL lines must be connected to a bus supply through a pullup resistor. The size of the pullup resistor is determined by the amount of capacitance on the I²C lines and communication speed. See also the *I2C Bus Pullup Resistor Calculation* application note. Data transfer can be initiated only when the bus is idle. A bus is considered idle if both SDA and SCL lines are high after a STOP condition (see Figure 7-10 and Figure 7-11). See the *Writes* and *Reads* sections for detailed procedures on how the controller can access the TMP4719-Q1.

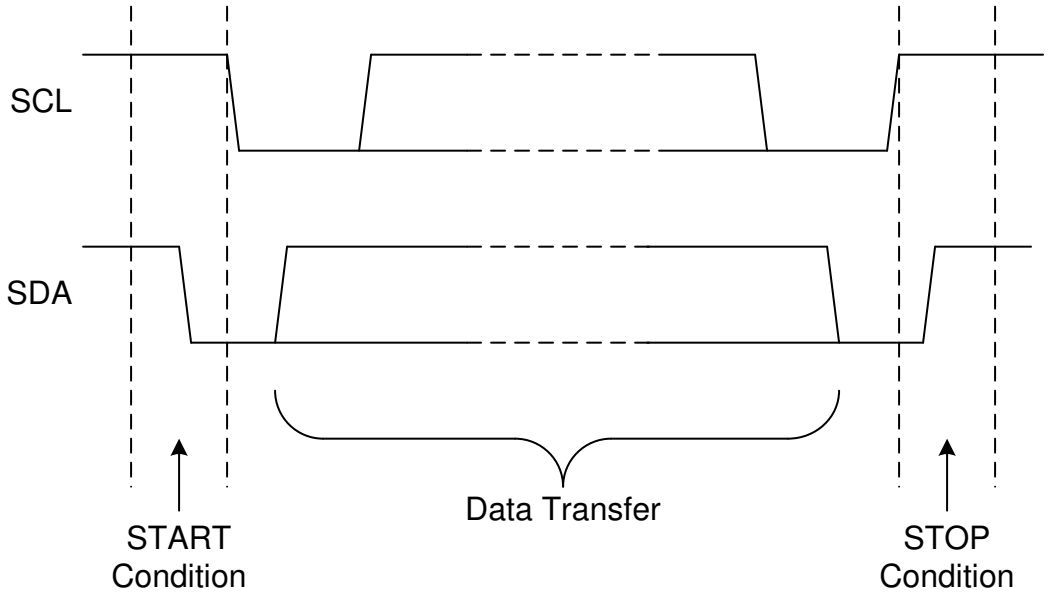


Figure 7-10. Definition of Start and Stop Conditions

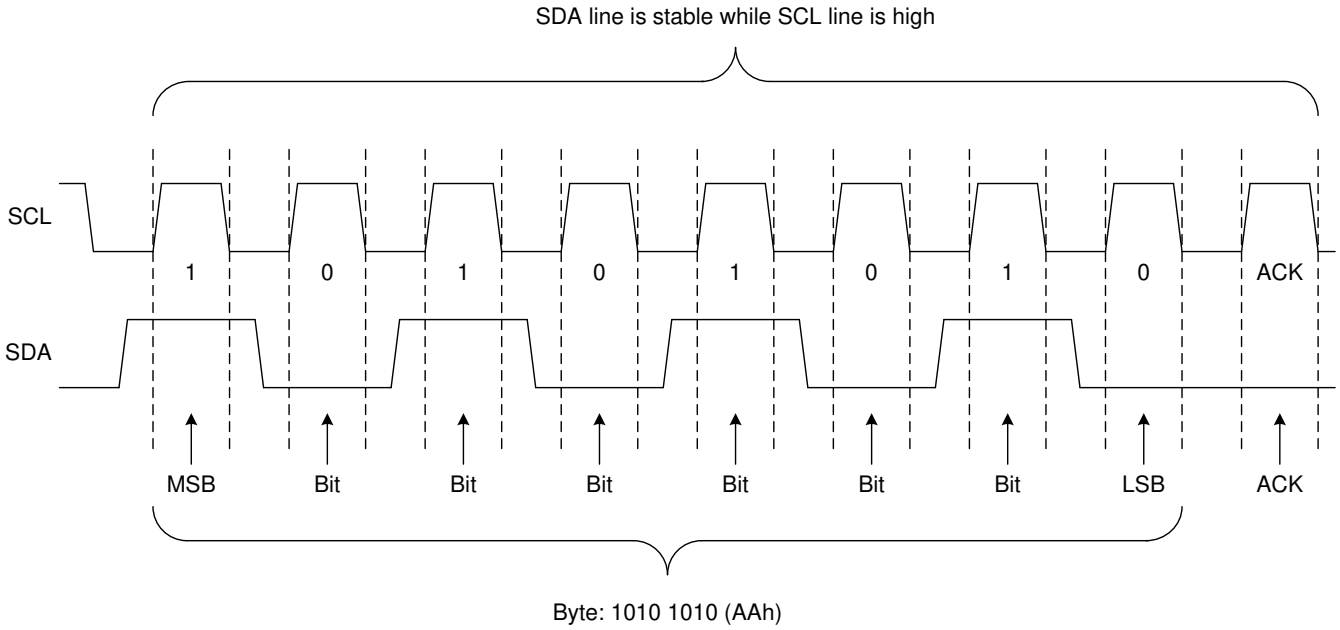


Figure 7-11. Bit Transfer

7.5.3 Serial Bus Address

The serial bus address consists of a 7-bit value, followed by an 8th bit that indicates whether the controller is issuing a Read or a Write command. If the 8th bit is a logic '0', the controller is writing data to the target device. If the 8th bit is a logic '1', the controller is reading data from the target device.

The 7-bit serial bus address for TMP4719 is 4Dh (1001101b).

7.5.4 Bus Transactions

Registers are locations in the memory of the target that contain information, including configuration information and sampled data to send back to the controller. The controller must write information to these registers to instruct the target device to perform a task.

7.5.4.1 Writes

To write on the I^2C bus, the controller sends a START condition on the bus with the address of the target, as well as the last bit (the R/W bit) set to 0, which signifies a write. The target acknowledges, letting the controller know the target is ready. After this, the controller starts sending the register pointer followed by the register data to the target. The controller terminates the transmission with a STOP condition.

Writes to read-only registers or register locations outside of the register map are ignored, and the TMP4719-Q1 performs a NACK to the data that the controller tries to send.

Figure 7-12 shows an example of writing a single-byte write communication. TMP4719-Q1 does not support multiple-byte writes.

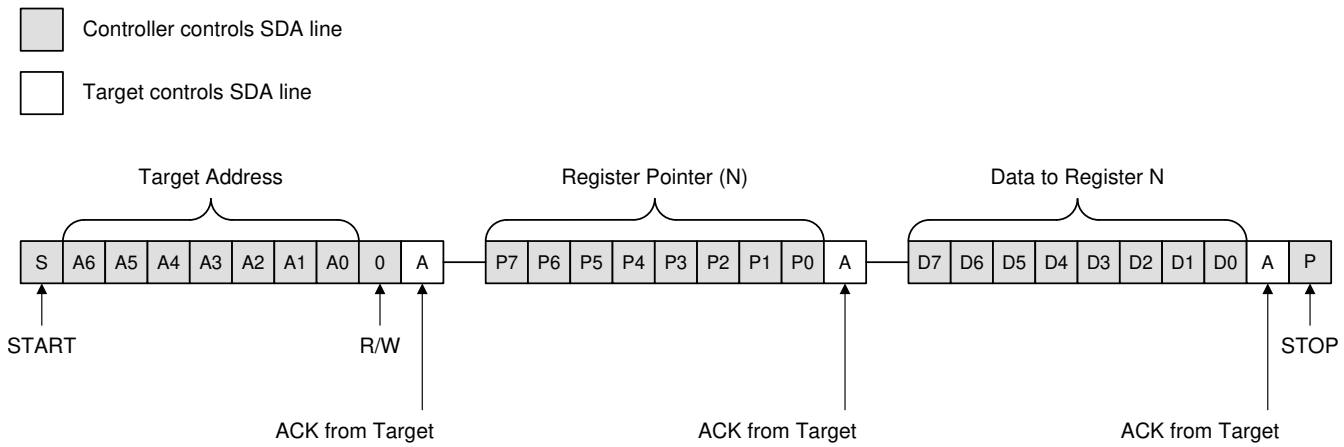


Figure 7-12. Write to Single Register

7.5.4.2 Reads

For a read operation, the controller sends a START condition followed by the target address with the R/W bit set to 0 (signifying a write). The target acknowledges the write request, and the controller sends the Register Pointer. After the Register Pointer, the host initiates a restart, followed by the target address with the R/W bit set to 1 (signifying a read). The controller continues to send out clock pulses, but releases the SDA line so that the target can transmit data. At the end of every byte of data, the controller sends an ACK to the target, letting the target know that the controller is ready for more data. Figure 7-13 shows an example of reading a single byte from a target register. The TMP4719-Q1 does not support multiple register reads with a single transaction.

If repeated reads from the same register are desired, the pointer register bytes do not have to be continually sent, as shown in Figure 7-14. The TMP4719-Q1 remembers the pointer register value until the value is changed by the next write operation. Note that after the device POR, the pointer address is defaulted to 0h. Therefore, the controller can read (and re-read) the Temp_Local register content without setting the pointer value.

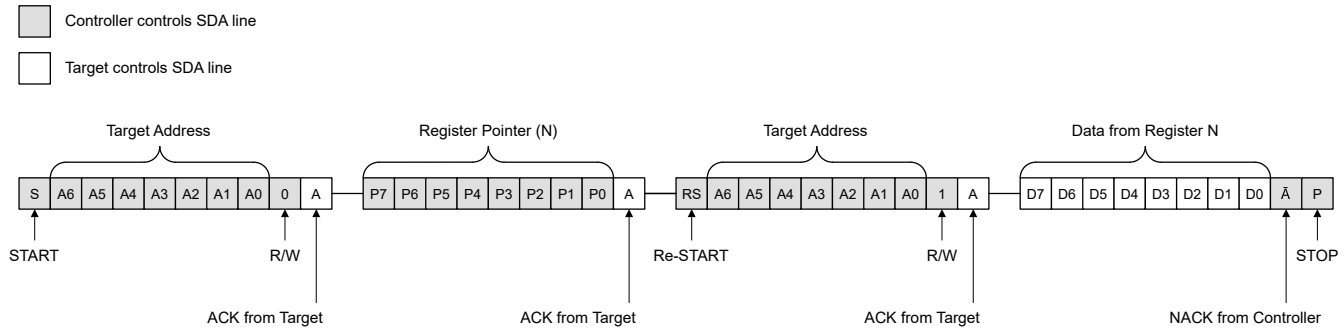


Figure 7-13. Read from Single Register

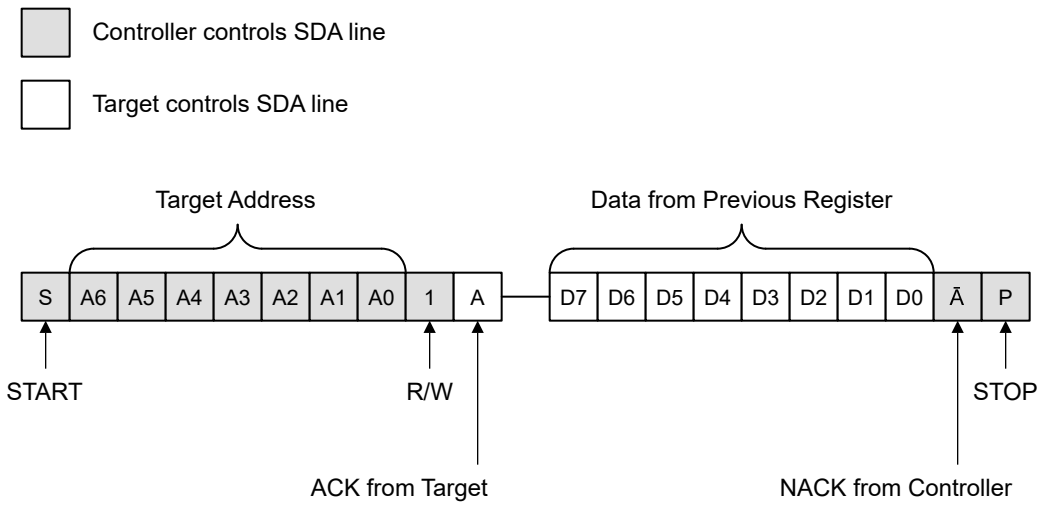


Figure 7-14. Repeated Read from Single Register

7.5.5 SMBus Alert Mode

When the Alert Mode Setting bit in the Configuration Register is set to 0, the Interrupt/SMBus Alert mode is enabled. In this mode, the $\overline{\text{ALERT}}$ pin is asserted at the end of a conversion cycle if the measured temperature exceeds a High Alert Limit or goes below a Low Alert Limit defined in the limit registers. In this mode, the TMP4719-Q1 sets the $\overline{\text{ALERT}}$ mask bit of the Configuration Register during a read of the Status Register if any flag in the Status Register, except the ADC_Busy flag and Remote Diode Fault flag, is set. This prevents the $\overline{\text{ALERT}}$ pin from triggering until the controller resets the $\overline{\text{ALERT}}$ mask bit (write 0 to the Alert_MASK bit).

The $\overline{\text{ALERT}}$ High Status flag is set at the end of a conversion cycle when the measured temperature exceeds a High Alert Limit register limit. There are separate High Limit values and status register flags for the remote and local temperature measurements. The High Limit Status register flags are only set to the respective temperature measurements.

The $\overline{\text{ALERT}}$ Low Status flag is set at the end of a conversion cycle when the measured temperature is below a Low Alert Limit register limit. There are separate Low Limit values and status register flags for the remote and local temperature measurements. The Low Limit Status register flags are only set to the respective temperature measurements.

The Status Register limit flags are cleared after a read command of the Status Register from the controller and are set again at the end of a temperature conversion cycle if the measured temperature is outside the set limits.

When the $\overline{\text{ALERT}}$ pin is connected to the SMBus alert line, there can be multiple devices on the same output. For the controller to resolve which target is generating an alert, the controller can send an SMBus ALERT Response Address (ARA) command. If the TMP4719-Q1 is generating an alert, and an ARA command is sent, the TMP4719-Q1 sets the ALERT MASK bit in the Configuration register and sends the target address to the controller. An ARA command does not clear any Status register flags. A read command of the Status Register from the controller is required to clear the Status Register limit flags.

Figure 7-15 shows the behavior of the $\overline{\text{ALERT}}$ pin and flags while in SMBus Alert mode.

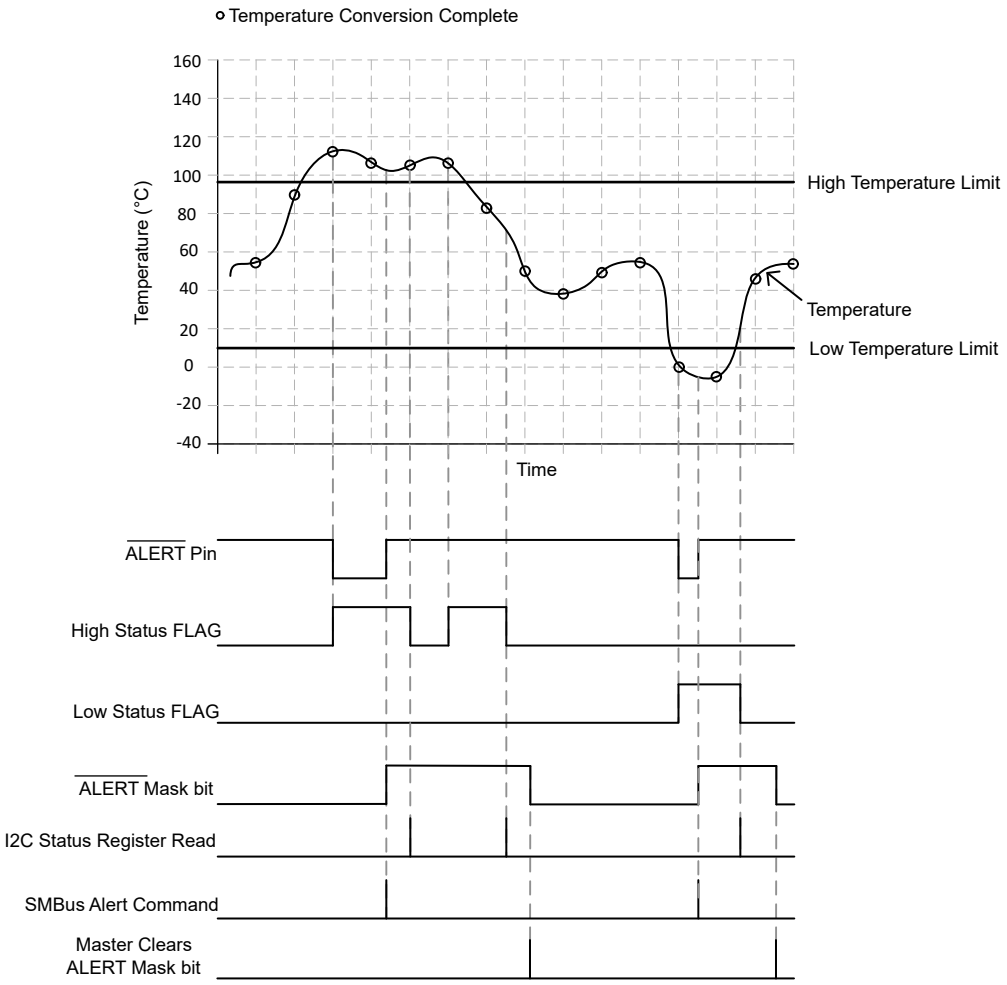


Figure 7-15. Alert SMBus Mode Timing Diagram

8 Register Map

Table 8-1. TMP4719-Q1 Registers

REGISTER ADDRESS	SHARED ADDRESS	TYPE	RESET	ACRONYM	REGISTER NAME	SECTION
00h	N/A	R	00h	Temp_Local	Local temperature register	GO
01h	N/A	R	00h	Temp_Remote_Ch1_High	Remote (Channel 1) temperature (high byte) register	GO
02h	N/A	R	00h	Status	Status register	GO
03h	09h	R/W	00h	Configuration	Configuration register	GO
04h	0Ah	R/W	06h	Conv_Period	Conversion period register	GO
05h	0Bh	R/W	55h	THigh_Limit_Local	Local temperature high limit register	GO
06h	0Ch	R/W	00h	TLow_Limit_Local	Local temperature low limit register	GO
07h	0Dh	R/W	55h	THigh_Limit_Remote_Ch1_High	Remote (Channel 1) high limit (high byte) register	GO
08h	0Eh	R/W	00h	TLow_Limit_Remote_Ch1_High	Remote (Channel 1) low limit (high byte) register	GO
0Fh	N/A	W	00h	One_Shot	One shot conversion register	GO
10h	N/A	R	00h	Temp_Remote_Ch1_Low	Remote (Channel 1) temperature (low byte) register	GO
11h	N/A	R/W	00h	Scratchpad1	Scratchpad 1 register	GO
12h	N/A	R/W	00h	Scratchpad2	Scratchpad 2 register	GO
13h	N/A	R/W	00h	THigh_Limit_Remote_Ch1_Low	Remote (Channel 1) high limit (low byte) register	GO
14h	N/A	R/W	00h	TLow_Limit_Remote_Ch1_Low	Remote (Channel 1) low limit (low byte) register	GO
15h	N/A	R/W	55h	THigh_Limit_Remote_Ch2_High	Remote (Channel 2) high limit (high byte) register	GO
16h	N/A	R/W	00h	TLow_Limit_Remote_Ch2_High	Remote (Channel 2) low limit (high byte) register	GO
17h	N/A	R/W	00h	THigh_Limit_Remote_Ch2_Low	Remote (Channel 2) high limit (low byte) register	GO
18h	N/A	R/W	00h	TLow_Limit_Remote_Ch2_Low	Remote (Channel 2) low limit (low byte) register	GO
19h	N/A	R/W	55h	THigh_Crit_Remote_Ch1	Remote (Channel 1) T_CRIT limit register	GO
1Ah	N/A	R/W	55h	THigh_Crit_Remote_Ch2	Remote (Channel 2) T_CRIT limit register	GO
1Bh	N/A	R	00h	Diode_Fault	Remote diode open/short fault indicator register	GO
1Fh	N/A	R/W	00h	Alert_Mask	Remote channel alert masking register	GO
20h	N/A	R/W	55h	THigh_Crit_Local	Local T_CRIT limit register	GO
21h	N/A	R/W	0Ah	Hysteresis	Hysteresis register for ALERT and T_CRIT	GO
23h	N/A	R	00h	Temp_Remote_Ch2_High	Remote (Channel 2) temperature (high byte) register	GO
24h	N/A	R	00h	Temp_Remote_Ch2_Low	Remote (Channel 2) temperature (low byte) register	GO
27h	N/A	R/W	12h	η-Factor_Ch1	Remote (Channel 1) η-Factor correction register	GO

Table 8-1. TMP4719-Q1 Registers (continued)

REGISTER ADDRESS	SHARED ADDRESS	TYPE	RESET	ACRONYM	REGISTER NAME	SECTION
28h	N/A	R/W	12h	η-Factor_Ch2	Remote (Channel 2) η-Factor correction register	GO
35h	N/A	RC	00h	THigh_Limit_Status	High limit status register	GO
36h	N/A	RC	00h	TLow_Limit_Status	Low limit status register	GO
37h	N/A	R	00h	TCRIT_Limit_Status	T_CRIT limit status register	GO
40h	N/A	R/W	00h	Filter_Control	Digital filter setting register	GO
FDh	N/A	R	21h	Chip_ID	Chip ID register	GO
FEh	N/A	R	60h	Vendor_ID	Vendor ID register	GO
FFh	N/A	R	A0h	Device_Rev_ID	Device and Revision ID register	GO

Table 8-2. TMP4719-Q1 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.1 Temp_Local Register(Address = 00h) [reset = 00h]

This register stores the byte of the latest temperature conversion result for the local temperature sensor in a 8-bit two's complement format with a LSB (Least Significant Bit) equal to 1°C.

Return to Register Map.

Figure 8-1. Temp_Local Register

7	6	5	4	3	2	1	0
Temp_Local[7:0]							
R-00h							

Table 8-3. Temp_Local Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Temp_Local[7:0]	R	00h	8-bit local temperature conversion result.

8.2 Temp_Remote_Ch1_High Register (Address = 01h) [reset = 00h]

This register stores the high byte of the latest temperature conversion result for channel 1 of the remote temperature sensor in a 8-bit two's complement format with a LSB (Least Significant Bit) equal to 1°C.

Return to Register Map.

Figure 8-2. Temp_Remote_Ch1_High Register

7	6	5	4	3	2	1	0
Temp_Remote_Ch1[11:4]							
R-00h							

Table 8-4. Temp_Remote_Ch1_High Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Temp_Remote_Ch1[11:4]	R	00h	High-byte (bits 11:4) of the 12-bit temperature conversion result for remote channel 1. Use the Temp_Remote_Ch1_High register together with the Temp_Remote_Ch1_Low register to get the full 12-bit temperature data of the remote channel 1 temperature sensor.

8.3 Status Register (Address = 02h) [reset = 00h]

This register shows the current status of the device.

Return to Register Map.

Figure 8-3. Status Register

7	6	5	4	3	2	1	0
ADC_Busy	Reserved		THigh	TLow	Remote_Fault	TCrit	Reserved
R-0h	R-0h		R-0h	R-0h	R-0h	R-0h	R-0h

Table 8-5. Status Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ADC_Busy	R	0h	Indicates if the ADC is busy in the middle of a conversion 0h = The ADC is idle 1h = The ADC is converting
6-5	Reserved	R	0h	Reserved
4	THigh	R	0h	Indicates if any of the temperature channel (local or remote) result is higher than the high limit register setting. When set, this bit asserts the $\overline{\text{ALERT}}$ pin. 0h = All temperature results are below the high limit 1h = Any one of the temperature result exceeds the high limit
3	TLow	R	0h	Indicates if any of the temperature channel (local or remote) result is lower than the low limit register setting. When set, this bit asserts the $\overline{\text{ALERT}}$ pin. 0h = All temperature results are above the low limit 1h = Any one of the temperature result drops below the low limit
2	Remote_Fault	R	0h	Indicates if either one of the remote channels is disconnected or shorted. 0h = Both remote channels are connected 1h = Either one of the remote channels is disconnected or shorted.
1	TCrit	R	0h	Indicates if any of the temperature channel (local or remote) result is above the corresponding $\overline{\text{T\_CRIT}}$ limit. When set, this bit asserts the $\overline{\text{T\_CRIT}}$ pin. 0h = All temperature results are below the configured $\overline{\text{T\_CRIT}}$ limits. 1h = Any one of the temperature result exceeds the configured $\overline{\text{T\_CRIT}}$ limits.
0	Reserved	R	0h	Reserved

8.4 Configuration Register (Address = 03h or 09h) [reset = 00h]

This register is used to configure the operation of the device, including the alert pin behavior, temperature conversion mode and operation mode. Changes to the configuration register does not disrupt an on-going conversion (except when configuring the device into Shutdown mode) and is serviced after completion of the current conversion.

Return to Register Map.

Figure 8-4. Configuration Register

7	6	5	4	3	2	1	0
Alert_Mask	Mode	Alert_Mode	Reserved				
R/W-0h	R/W-0h	R/W-0h	R-0h				

Table 8-6. Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Alert_Mask	R/W	0h	Masks the $\overline{\text{ALERT}}$ pin from asserting. 0h = The $\overline{\text{ALERT}}$ pin assertion is enabled. 1h = The $\overline{\text{ALERT}}$ pin is masked and does not assert low, unless the device is configured to operate in comparator mode. The Status register continues to get updated normally.
6	Mode	R/W	0h	Controls the operation mode of the device 0h = Continuous mode enabled 1h = Shutdown mode enabled. One-shot conversation can be started in this mode.
5	Alert_Mode	R/W	0h	Configures the $\overline{\text{ALERT}}$ pin output mode of the device. 0h = Interrupt mode enabled for the $\overline{\text{ALERT}}$ pin 1h = Comparator mode enabled for the $\overline{\text{ALERT}}$ pin
4-0	Reserved	R	0h	Reserved

8.5 Conv_Period Register (Address = 04h or 0Ah) [reset = 06h]

This register is used to configure the conversion period of the device.

Return to Register Map.

Figure 8-5. Conv_Period Register

7	6	5	4	3	2	1	0
Reserved				Conv_Period[3:0]			
R-0h				R/W-6h			

Table 8-7. Conv_Period Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	Reserved	R	0h	Reserved
3:0	Conv_Period[3:0]	R/W	6h	Conversion period setting. This bit field changes the conversion period of the device at the next possible interval but does not restart an on-going conversion period. Writing an unsupported value to this setting puts the device in Shutdown mode. 0h = 16s / 0.0625Hz 1h = 8s / 0.125Hz 2h = 4s / 0.25Hz 3h = 2s / 0.5Hz 4h = 1s / 1Hz 5h = 0.5s / 2Hz 6h = 0.25s / 4Hz 7h = 0.125s / 8Hz 8h = 0.0625s / 16Hz 9h-Fh = 1s / 1Hz

8.6 THigh_Limit_Local Register (Address = 05h or 0Bh) [reset = 55h]

This register is used to configure Local temperature high limit. The default value 55h corresponds to a limit setting of 85°C.

Return to Register Map.

Figure 8-6. THigh_Limit_Local Register

7	6	5	4	3	2	1	0
THigh_Limit_Local[7:0]							
R/W-55h							

Table 8-8. THigh_Limit_Local Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	THigh_Limit_Local[7:0]	R/W	55h	8-bit local temperature alert high limit setting. The temperature alert limit format is an 8-bit two's complement byte with a least significant bit equal to 1°C

8.7 TLow_Limit_Local Register (Address = 06h or 0Ch) [reset = 00h]

This register is used to configure Local temperature low limit. The default value 00h corresponds to a limit setting of 0°C.

Return to Register Map.

Figure 8-7. TLow_Limit_Local Register

7	6	5	4	3	2	1	0
TLow_Limit_Local[7:0]							
R/W-00h							

Table 8-9. TLow_Limit_Local Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TLow_Limit_Local[7:0]	R/W	00h	8-bit local temperature alert low limit setting. The temperature alert limit format is an 8-bit two's complement byte with a least significant bit equal to 1°C

8.8 THigh_Limit_Remote_Ch1_High Register (Address = 07h or 0Dh) [reset = 55h]

This register is used to configure the high byte (bits 11:4) of the temperature high limit for remote channel 1. The default value 55h corresponds to a limit setting of 85°C.

Return to Register Map.

Figure 8-8. THigh_Limit_Remote_Ch1_High Register

7	6	5	4	3	2	1	0
THigh_Limit_Remote_Ch1_High[11:4]							
R/W-55h							

Table 8-10. THigh_Limit_Remote_Ch1_High Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	THigh_Limit_Remote_Ch1_High[11:4]	R/W	55h	High-byte (bits 11:4) of the 12-bit temperature alert high limit setting for remote channel 1. Use the THigh_Limit_Remote_Ch1_High register together with the THigh_Limit_Remote_Ch1_Low register to get the full 12-bit temperature alert high limit for remote channel 1.

8.9 TLow_Limit_Remote_Ch1_High Register (Address = 08h or 0Eh) [reset = 00h]

This register is used to configure the high byte (bits 11:4) of the temperature low limit for remote channel 1. The default value 00h corresponds to a limit setting of 0°C.

Return to Register Map.

Figure 8-9. TLow_Limit_Remote_Ch1_High Register

7	6	5	4	3	2	1	0
TLow_Limit_Remote_Ch1_High[11:4]							
R/W-00h							

Table 8-11. TLow_Limit_Remote_Ch1_High Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TLow_Limit_Remote_Ch1_High[11:4]	R/W	00h	High-byte (bits 11:4) of the 12-bit temperature alert low limit setting for remote channel 1. Use the TLow_Limit_Remote_Ch1_High register together with theTLow_Limit_Remote_Ch1_Low register to get the full 12-bit temperature alert low limit for remote channel 1.

8.10 One_Shot Register (Address = 0Fh) [reset = 00h]

Write to this register to trigger a One Shot conversion in Shutdown Mode (that is, Bit 6 of the Configuration Register written to 1).

Return to Register Map.

Figure 8-10. One_Shot Register

7	6	5	4	3	2	1	0
One_Shot[7:0]							
W-00h							

Table 8-12. One_Shot Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	One_Shot[7:0]	W	00h	Writing any value to this register triggers a One_Shot conversion while in Shutdown Mode. In continuous mode there is no effect.

8.11 Temp_Remote_Ch1_Low Register (Address = 10h) [reset = 00h]

This register stores the low byte (bits 3:0) of the latest temperature conversion result for channel 1 of the remote temperature sensor.

Return to Register Map.

Figure 8-11. Temp_Remote_Ch1_Low Register

7	6	5	4	3	2	1	0
Temp_Remote_Ch1_Low[3:0]				Reserved			
R-0h				R-0h			

Table 8-13. Temp_Remote_Ch1_Low Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	Temp_Remote_Ch1_Low[3:0]	R	0h	Low-byte (bits 3:0) of the 12-bit temperature conversion result for remote channel 1. Use the Temp_Remote_Ch1_High register together with the Temp_Remote_Ch1_Low register to get the full 12-bit temperature data of the remote channel 1 temperature sensor.
3:0	Reserved	R	0h	Reserved

8.12 Scratchpad1 Register (Address = 11h) [reset = 00h]

This is one of the two Scratchpad registers that are editable and readable to store user-programmable data, such as serial number and system calibration data. The Scratchpad registers are volatile.

Return to Register Map.

Figure 8-12. Scratchpad1 Register

7	6	5	4	3	2	1	0
Scratchpad1[7:0]							
R/W-00h							

Table 8-14. Scratchpad1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Scratchpad1[7:0]	R/W	00h	8-bit Scratchpad data to store user-programmable data. Reading the register returns the previously programmed content. The data is volatile and power needs to be supplied to the device for the programmed data to be retained.

8.13 Scratchpad2 Register (Address = 12h) [reset = 00h]

This is one of the two Scratchpad registers that are editable and readable to store user-programmable data, such as serial number and system calibration data. The Scratchpad registers are volatile.

Return to Register Map.

Figure 8-13. Scratchpad2 Register

7	6	5	4	3	2	1	0
Scratchpad2[7:0]							
R/W-00h							

Table 8-15. Scratchpad2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Scratchpad2[7:0]	R/W	00h	8-bit Scratchpad data to store user-programmable data. Reading the register returns the previously programmed content. The data is volatile and power needs to be supplied to the device for the programmed data to be retained.

8.14 THigh_Limit_Remote_Ch1_Low Register (Address = 13h) [reset = 00h]

This register is used to configure the low byte (bits 3:0) of the temperature high limit for remote channel 1.

Return to Register Map.

Figure 8-14. THigh_Limit_Remote_Ch 1_Low Register

7	6	5	4	3	2	1	0
THigh_Limit_Remote_Ch1_Low[3:0]				Reserved			
R/W-0h				R-0h			

Table 8-16. THigh_Limit_Remote_Ch 1_Low Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	THigh_Limit_Remote_Ch1_Low[3:0]	R/W	0h	Low-byte (bits 3:0) of the 12-bit temperature alert high limit setting for remote channel 1. Use the THigh_Limit_Remote_Ch1_High register together with the THigh_Limit_Remote_Ch1_Low register to get the full 12-bit temperature alert high limit for remote channel 1.
3:0	Reserved	R	0h	Reserved

8.15 TLow_Limit_Remote_Ch1_Low Register (Address = 14h) [reset = 00h]

This register is used to configure the low byte (bits 3:0) of the temperature low limit for remote channel 1.

Return to Register Map.

Figure 8-15. TLow_Limit_Remote_Ch1_Low Register

7	6	5	4	3	2	1	0
TLow_Limit_Remote_Ch1_Low[3:0]				Reserved			
R/W-0h				R-0h			

Table 8-17. TLow_Limit_Remote_Ch1_Low Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	TLow_Limit_Remote_Ch1_Low [3:0]	R/W	0h	Low-byte (bits 3:0) of the 12-bit temperature alert low limit setting for remote channel 1. Use the TLow_Limit_Remote_Ch1_High register together with the TLow_Limit_Remote_Ch1_Low register to get the full 12-bit temperature alert low limit for remote channel 1.
3:0	Reserved	R	0h	Reserved

8.16 THigh_Limit_Remote_Ch2_High Register (Address = 15h) [reset = 55h]

This register is used to configure the high byte (bits 11:4) of the temperature high limit for remote channel 2. The default value 55h corresponds to a limit setting of 85°C.

Return to Register Map.

Figure 8-16. THigh_Limit_Remote_Ch2_High Register

7	6	5	4	3	2	1	0
THigh_Limit_Remote_Ch2_High[11:4]							
R/W-55h							

Table 8-18. THigh_Limit_Remote_Ch2_High Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	THigh_Limit_Remote_Ch2_High[11:4]	R/W	55h	High-byte (bits 11:4) of the 12-bit temperature alert high limit setting for remote channel 2. Use the THigh_Limit_Remote_Ch2_High register together with the THigh_Limit_Remote_Ch2_Low register to get the full 12-bit temperature alert high limit for remote channel 2.

8.17 TLow_Limit_Remote_Ch2_High Register Register (Address = 16h) [reset = 00h]

This register is used to configure the high byte (bits 11:4) of the temperature low limit for remote channel 2. The default value 00h corresponds to a limit setting of 0°C.

Return to Register Map.

Figure 8-17. TLow_Limit_Remote_Ch2_High Register

7	6	5	4	3	2	1	0
TLow_Limit_Remote_Ch2_High[11:4]							
R/W-00h							

Table 8-19. TLow_Limit_Remote_Ch2_High Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TLow_Limit_Remote_Ch2_High[11:4]	R/W	00h	High-byte (bits 11:4) of the 12-bit temperature alert low limit setting for remote channel 2. Use the TLow_Limit_Remote_Ch2_High register together with theTLow_Limit_Remote_Ch2_Low register to get the full 12-bit temperature alert low limit for remote channel 2.

8.18 THigh_Limit_Remote_Ch2_Low Register (Address = 17h) [reset = 00h]

This register is used to configure the low byte (bits 3:0) of the temperature high limit for remote channel 2.

Return to Register Map.

Figure 8-18. THigh_Limit_Remote_Ch2_Low Register

7	6	5	4	3	2	1	0
THigh_Limit_Remote_Ch2_Low[3:0]				Reserved			
R/W-0h				R-0h			

Table 8-20. THigh_Limit_Remote_Ch2_Low Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	THigh_Limit_Remote_Ch2_Low[3:0]	R/W	0h	Low-byte (bits 3:0) of the 12-bit temperature alert high limit setting for remote channel 2. Use the THigh_Limit_Remote_Ch2_High register together with the THigh_Limit_Remote_Ch2_Low register to get the full 12-bit temperature alert high limit for remote channel 2.
3:0	Reserved	R	0h	Reserved

8.19 TLow_Limit_Remote_Ch2_Low Register (Address = 18h) [reset = 00h]

This register is used to configure the low byte (bits 3:0) of the temperature low limit for remote channel 1.

Return to Register Map.

Figure 8-19. TLow_Limit_Remote_Ch2_Low Register

7	6	5	4	3	2	1	0
TLow_Limit_Remote_Ch2_Low[3:0]				Reserved			
R/W-0h				R-0h			

Table 8-21. TLow_Limit_Remote_Ch2_Low Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	TLow_Limit_Remote_Ch2_Low [3:0]	R/W	0h	Low-byte (bits 3:0) of the 12-bit temperature alert low limit setting for remote channel 2. Use the TLow_Limit_Remote_Ch2_High register together with the TLow_Limit_Remote_Ch2_Low register to get the full 12-bit temperature alert low limit for remote channel 2.
3:0	Reserved	R	0h	Reserved

8.20 THigh_Crit_Remote_Ch1 Register (Address = 19h) [reset = 55h]

This register is used to configure the critical limit for remote channel 1. The default value 55h corresponds to a limit setting of 85°C.

Return to Register Map.

Figure 8-20. THigh_Crit_Remote_Ch1 Register

7	6	5	4	3	2	1	0
THigh_Crit_Remote_Ch1[7:0]							
R/W-55h							

Table 8-22. THigh_Crit_Remote_Ch1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	THigh_Crit_Remote_Ch1[7:0]	R/W	55h	8-bit remote channel 1 temperature crit limit setting. Temperature crit limit format is an 8-bit two's complement word with a least significant bit equal to 1°C

8.21 THigh_Crit_Remote_Ch2 Register (Address = 1Ah) [reset = 55h]

This register is used to configure the critical limit for remote channel 2. The default value 55h corresponds to a limit setting of 85°C.

Return to Register Map.

Figure 8-21. THigh_Crit_Remote_Ch2 Register

7	6	5	4	3	2	1	0
THigh_Crit_Remote_Ch2[7:0]							
R/W-55h							

Table 8-23. THigh_Crit_Remote_Ch2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	THigh_Crit_Remote_Ch2[7:0]	R/W	55h	8-bit remote channel 2 temperature crit limit setting. Temperature crit limit format is an 8-bit two's complement word with a least significant bit equal to 1°C

8.22 Diode_Fault (Address = 1Bh) [reset = 00h]

This register is used to indicate whether either of the remote channels have a diode improperly connected.

A diode fault is identified when diode short condition occurs. When diode short is detected on any channel, the respective remote channel temperature conversion result gets is 0000h. Short bit in Diode_Fault is set to 1 and Alert pin is asserted (if no channel masks of both remote channels are set in Interrupt Mode). Short bit in Diode_Fault is unset when diode short condition clears. Alert pin can be cleared by reading Diode_Fault register and Alert Masks of both remote channels are set in both interrupt Mode and Comparator Mode, which is a special case.

Diode open condition is identified as DP open and DN open or connected to GND. When diode open condition occurs, the respective remote channel temperature conversion result gets is 0000h. Open bit in Diode_Fault is set to 1 while Alert pin is NOT asserted. Open bit in Diode_Fault is unset when diode open condition clears (diode gets connected back and a conversion happens that identifies it).

Return to Register Map.

Figure 8-22. Diode_Fault Register

7	6	5	4	3	2	1	0
Reserved				Short	Ch2_Open	Ch1_Open	Reserved
R-00h				R-0h	R-0h	R-0h	R-0h

Table 8-24. Diode_Fault Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	Reserved	R	00h	Reserved
3	Short	R	0h	This bit, when flagged to 1b, indicates remote channel 1 and(or) remote channel 2 are(is) shorted.
2	Ch2_Open	R	0h	This bit, when flagged to 1b, indicates remote channel 2 has a open condition.
1	Ch1_Open	R	0h	This bit, when flagged to 1b, indicates remote channel 1 has a open condition.
0	Reserved	R	0h	Reserved

8.23 Alert_Mask Register (Address = 1Fh) [reset = 00h]

This register controls whether either of remote channel or the local channel is masked. Masking an alert prevents the ALERT pin from being asserted low in Interrupt Mode.

Return to Register Map.

Figure 8-23. Alert_Mask Register

7	6	5	4	3	2	1	0
Reserved					Mask_Ch2	Mask_Ch1	Mask_L
R-00h					R/W-0h	R/W-0h	R/W-0h

Table 8-25. Alert_Mask Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	Reserved	R	00h	Reserved
2	Mask_Ch2	R/W	0h	Setting this bit to 1 prevents the ALERT pin from being asserted low when remote channel 2 is out of the temperature limit or encounters a diode fault condition.
1	Mask_Ch1	R/W	0h	Setting this bit to 1 prevents the ALERT pin from being asserted low when remote channel 1 is out of the temperature limit or encounters a diode fault condition.
0	Mask_L	R/W	0h	Setting this bit to 1 prevents the ALERT pin from being asserted low when the local channel is out of the temperature limit.

8.24 THigh_Crit_Local Register (Address = 20h) [reset = 55h]

This register is used to configure the critical limit for the local channel. The default value 55h corresponds to a limit setting of 85°C.

Return to Register Map.

Figure 8-24. THigh_Crit_Local Register

7	6	5	4	3	2	1	0
THigh_Crit_Local[7:0]							
R/W-55h							

Table 8-26. THigh_Crit_Local Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	THigh_Crit_Local[7:0]	R/W	55h	8-bit local channel temperature crit limit setting. Temperature crit limit format is an 8-bit two's complement word with a least significant bit equal to 1°C

8.25 Hysteresis Register (Address = 21h) [reset = 0Ah]

This register is used to configure the hysteresis of ALERT and TCRIT for both remote and local channels. The value for this register is a 5-bit integer value with a least significant bit equal to 1°C. Default value is 10°C.

Return to Register Map.

Figure 8-25. Hysteresis Register

7	6	5	4	3	2	1	0
Reserved			Hysteresis[4:0]				
R-0h			R/W-0Ah				

Table 8-27. Hysteresis Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	Reserved	R	0h	Reserved
4:0	Hysteresis[4:0]	R/W	0Ah	5-bit temperature hysteresis. Temperature hysteresis format is an 5-bit integer byte with a least significant bit equal to 1°C

8.26 Temp_Remote_Ch2_High Register (Address = 23h) [reset = 00h]

This register stores the high byte of the latest temperature conversion result for channel 2 of the remote temperature sensor in a 8-bit two's complement format with a LSB (Least Significant Bit) equal to 1°C.

Return to Register Map.

Figure 8-26. Temp_Remote_Ch2_High Register

7	6	5	4	3	2	1	0
Temp_Remote_Ch2[11:4]							
R-00h							

Table 8-28. Temp_Remote_Ch2_High Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Temp_Remote_Ch2[11:4]	R	00h	High-byte (bits 11:4) of the 12-bit temperature conversion result for remote channel 2. Use the Temp_Remote_Ch2_High register together with the Temp_Remote_Ch2_Low register to get the full 12-bit temperature data of the remote channel 2 temperature sensor.

8.27 Temp_Remote_Ch2_Low Register (Address = 24h) [reset = 00h]

This register stores the low byte (bits 3:0) of the latest temperature conversion result for channel 2 of the remote temperature sensor.

Return to Register Map.

Figure 8-27. Temp_Remote_Ch2_Low Register

7	6	5	4	3	2	1	0
Temp_Remote_Ch2_Low[3:0]				Reserved			
R-0h				R-0h			

Table 8-29. Temp_Remote_Ch2_Low Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	Temp_Remote_Ch2_Low[3:0]	R	0h	Low-byte (bits 3:0) of the 12-bit temperature conversion result for remote channel 1. Use the Temp_Remote_Ch2_High register together with the Temp_Remote_Ch2_Low register to get the full 12-bit temperature data of the remote channel 2 temperature sensor.
3:0	Reserved	R	0h	Reserved

8.28 η-Factor_Ch1 Register (Address = 27h) [reset = 12h]

This register is used to configure the diode ideality factor for remote channel 1 according to settings in Table 8-30. The default value 12h corresponds to the ideality factor of 1.004.

Return to Register Map.

Table 8-30. η-Factor Lookup Table

Setting	η-Factor	Setting	η-Factor
8	0.9911	20	1.0225
9	0.9923	21	1.0238
A	0.9936	22	1.0251
B	0.9949	23	1.0263
C	0.9962	24	1.0277
D	0.9975	25	1.0290
E	0.9987	26	1.0302
F	1.0001	27	1.0316
10	1.0013	28	1.0328
11	1.0026	29	1.0341
12	1.004	2A	1.0354
13	1.0053	2B	1.0367
14	1.0066	2C	1.0379
15	1.0079	2D	1.0393
16	1.0092	2E	1.0405
17	1.0105	2F	1.0419
18	1.0118	30	1.0431
19	1.0131	31	1.0445
1A	1.0144	32	1.0456
1B	1.0159	33	1.0470
1C	1.0171	34	1.0482
1D	1.0185	35	1.0496
1E	1.0198	36	1.0508
1F	1.0211	37	1.0522

Figure 8-28. η-Factor_Ch1 Register

7	6	5	4	3	2	1	0
η-Factor_Ch1[7:0]							
R/W-12h							

Table 8-31. η-Factor_Ch1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	η-Factor_Ch1[7:0]	R/W	12h	This register is used to configure the diode ideality factor for remote channel 1. Refer to Table 8-30 for the specific settings.

8.29 η-Factor_Ch2 Register (Address = 28h) [reset = 12h]

This register is used to configure the diode ideality factor for remote channel 2 according to settings in η-Factor Lookup Table.

The default value 12h corresponds to the ideality factor of 1.004.

Return to Register Map.

Figure 8-29. η-Factor_Ch2 Register

7	6	5	4	3	2	1	0
η-Factor_Ch2[7:0]							
R/W-12h							

Table 8-32. η-Factor_Ch2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	η-Factor_Ch2[7:0]	R/W	12h	This register is used to configure the diode ideality factor for remote channel 2. Refer to Table 8-30 for the specific settings.

8.30 High_Limit_Status Register (Address = 35h) [reset = 00h]

The High_Limit_Status Register contains the status bits that are set when a temperature channel high limit is exceeded. If any of these bits are set, the THigh status bit in the Status Register is also set, and the $\overline{\text{ALERT}}$ pin is asserted low.

In Interrupt Mode, reading from the High_Limit_Status Register clear all bits in the register, while also clearing the THigh status bit in the Status Register. Note that the flag is set again in the next conversion if a temperature channel high limit is exceeded. In Comparator Mode, all bits in the register and the THigh status bit in the Status Register get cleared when temperature drops below High Temperature Limit minus Hysteresis.

Return to Register Map.

Figure 8-30. High_Limit_Status Register

7	6	5	4	3	2	1	0
Reserved					Ch2_High	Ch1_High	Local_High
R-00h					RC-0h	RC-0h	RC-0h

Table 8-33. High_Limit_Status Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	Reserved	R	00h	Reserved
2	Ch2_High	RC	0h	This bit is set when the remote temperature channel 2 rises above the configured high limit.
1	Ch1_High	RC	0h	This bit is set when the remote temperature channel 1 rises above the configured high limit.
0	Local_High	RC	0h	This bit is set when the local temperature channel rises above the configured high limit.

8.31 Low_Limit_Status Register (Address = 36h) [reset = 00h]

The Low_Limit_Status Register contains the status bits that are set when a temperature channel low limit is exceeded. If any of these bits are set, the TLow status bit in the Status Register is also set, and the $\overline{\text{ALERT}}$ pin is asserted low.

In Interrupt Mode, reading from the Low_Limit_Status Register clear all bits in the register, while also clearing the TLow status bit in the Status Register. Note that the flag is set again in the next conversion if a temperature channel low limit is exceeded. In Comparator Mode, all bits in the register and the TLow status bit in the Status Register get cleared when temperature increases above Low Temperature Limit plus Hysteresis.

Return to Register Map.

Figure 8-31. Low_Limit_Status Register

7	6	5	4	3	2	1	0
Reserved					Ch2_Low	Ch1_Low	Local_Low
R-00h					RC-0h	RC-0h	RC-0h

Table 8-34. Low_Limit_Status Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	Reserved	R	00h	Reserved
2	Ch2_Low	RC	0h	This bit is set when the remote temperature channel 2 drops below the configured low limit.
1	Ch1_Low	RC	0h	This bit is set when the remote temperature channel 1 drops below the configured low limit.
0	Local_Low	RC	0h	This bit is set when the local temperature channel drops below the configured low limit.

8.32 TCRIT_Limit_Status Register (Address = 37h) [reset = 00h]

The TCRIT_Limit_Status Register contains the status bits that are set when a temperature channel's TCRIT limit is exceeded. If any of these bits are set, the TCRIT status bit in the Status Register is also set, and the $\overline{\text{TCRIT}}$ pin is asserted low.

Reading from the TCRIT_Limit_Status Register does not clear the bits in the register. Once the temperature drops below TCRIT limit minus the TCRIT hysteresis, the corresponding status bit is automatically cleared. The TCRIT bit in Status Register is also automatically cleared when all individual channel bits are cleared in the TCRIT_Limit_Status register.

Return to Register Map.

Figure 8-32. TCRIT_Limit_Status Register

7	6	5	4	3	2	1	0
Reserved					Ch2_TCRIT	Ch1_TCRIT	Local_TCRIT
R-00h					R-0h	R-0h	R-0h

Table 8-35. TCRIT_Limit_Status Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	Reserved	R	00h	Reserved
2	Ch2_TCRIT	R	0h	This bit is set when the remote temperature channel 2 exceeds the configured TCRIT limit.
1	Ch1_TCRIT	R	0h	This bit is set when the remote temperature channel 1 exceeds the configured TCRIT limit.
0	Local_TCRIT	R	0h	This bit is set when the local temperature channel exceeds the configured TCRIT limit.

8.33 Filter_Control Register (Address = 40h) [reset = 00h]

This register controls the remote diode filter level.

Return to Register Map.

Figure 8-33. Filter_Control Register

7	6	5	4	3	2	1	0
Reserved						Filter_Control[1:0]	
R-00h						R/W-0h	

Table 8-36. Filter_Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	Reserved	R	00h	Reserved
1:0	Filter_Control[1:0]	R/W	0h	Controls the filter level. The filter is a moving average of the Remote temperature conversion results. 0h = 0 moving average (default) 1h = 4 moving average (level 1) 2h = 4 moving average (level 1) 3h = 8 moving average (level 2)

8.34 Chip_ID Register (Address = FDh) [reset = 21h]

This register contains the Chip ID for identifying the device.

Return to Register Map.

Figure 8-34. Chip_ID Register

7	6	5	4	3	2	1	0
Chip_ID[7:0]							
R-21h							

Table 8-37. Chip_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Chip_ID[7:0]	R	21h	Chip ID of the device.

8.35 Vendor_ID Register (Address = FEh) [reset = 60h]

This register contains the Vendor ID for identifying the device.

Return to Register Map.

Figure 8-35. Vendor_ID Register

7	6	5	4	3	2	1	0
Vendor_ID[7:0]							
R-60h							

Table 8-38. Vendor_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Vendor_ID[7:0]	R	60h	Vendor ID of the device.

8.36 Device_Rev_ID Register (Address = FFh) [reset = A0h]

This register contains the Device and Revision ID for identifying the device.

Return to Register Map.

Figure 8-36. Device_Rev_ID Register

7	6	5	4	3	2	1	0
Device_ID[3:0]				Rev_ID[3:0]			
R-xh				R-xh			

Table 8-39. Device_Rev_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	Device_ID[3:0]	R	Ah	Device ID of the device.
3:0	Rev_ID[3:0]	R	0h	Revision ID of the device.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TMP4719-Q1 operates with a two-wire I²C or SMBus compatible interface. The interfaces support static input thresholds independent of supply to maintain compatibility with a 1.2V logic I²C or SMBus. The following section shows an example implementation of proper device operation.

9.2 Typical Application

Figure 9-1 depicts the completed design.

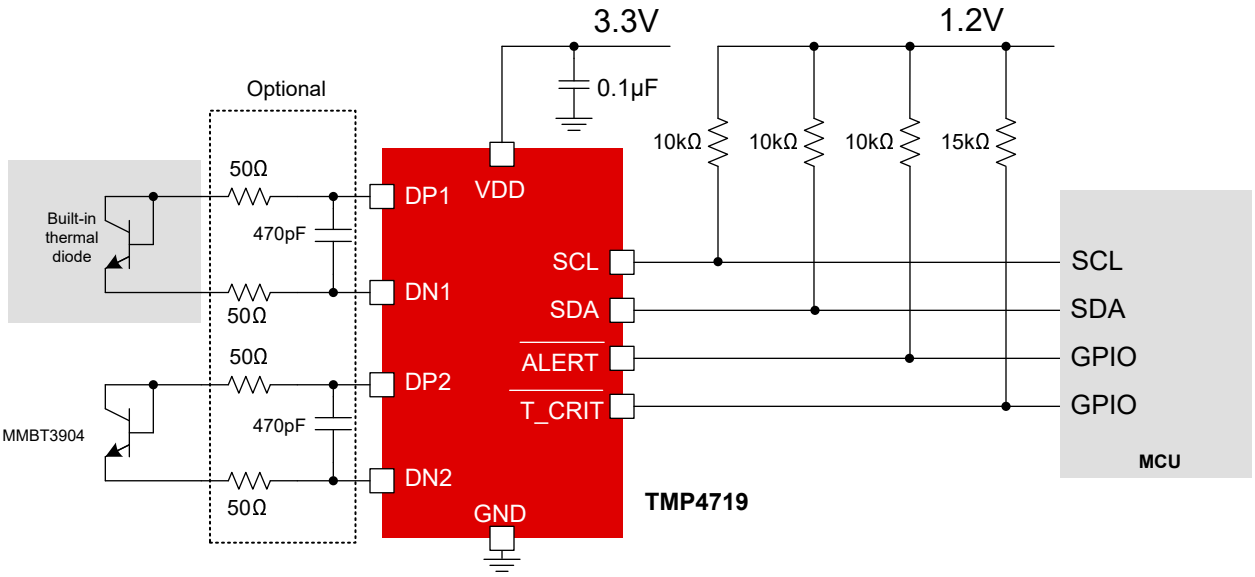


Figure 9-1. Design Example

9.2.1 Design Requirements

In this design example, the requirement is to design a temperature monitoring system using the TMP4719-Q1 with the MMBT3904 as the bipolar sensing transistor. The high temperature limit requirement for this example is 88°C. Table 9-1 lists the design parameters for this application.

Table 9-1. Design Parameters

PARAMETER	VALUE
Supply	3.3V
I/O Pullup Voltage	1.2V
Temperature High Limit Requirement	88°C
Bipolar Transistor	MMBT3904 (NTE Electronics, Inc)

9.2.2 Detailed Design Procedure

The ideality factor (η) is a measured characteristic of a remote temperature sensor diode as compared to an ideal diode. Compensating for ideality factor differences is simple if the diode manufacturer specifies the n-factor in the respective data sheet. If the ideality factor of the transistor is not specified, the manufacturer can be able to provide the n-factor value by a special request.

Typical ideality factor specification differences cause a gain variation of the transfer function. The TMP4719-Q1 is calibrated for the ideality factor of 1.004, so use η-Factor Lookup Table to compensate for a target ideality factor that differs from 1.004.

For example, if MMBT3906FZ-7B bipolar transistor, which has an ideality factor of approximately 1.008, is selected for this design example, 15h with a ideality factor (η) of 1.0079 is the closest value that can be programmed to compensate for the differing typical ideality factors. Referring to *I²C and Register Map*, the controller then sends a write command to the address of the target (4Dh) followed by the register pointer (27h) and finally the data (15h) to η-Factor_Ch1 Register.

The design calls for the high temperature limit of 88°C at device power up, which is programmed using I²C. Referring to *I²C and Register Map*, the controller sends a write command to the address of the target (4Dh) followed by the register pointer (07h) and finally the data (51h) to THigh_Limit_Remote_Ch1_High Register.

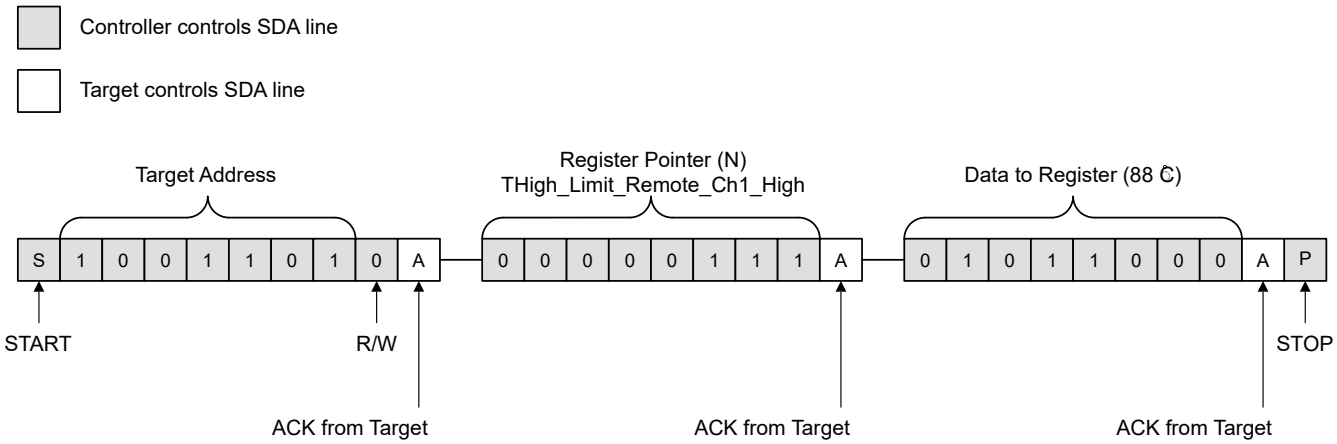


Figure 9-2. Application Example: Program Using I²C to Set Temperature High Limit

Remote junction temperature sensors are typically implemented in a noisy environment. Noise is most often created by fast digital signals, and noise can corrupt measurements. The TMP4719-Q1 device has a built-in, 65kHz low-pass filter on the inputs of D+ and D– to minimize the effects of noise. However, a bypass capacitor placed differentially across the inputs of the remote temperature sensor is recommended to make the application more robust against unwanted coupled signals. For this capacitor, select a value between 100pF and 1.5nF. Some applications attain better overall accuracy with additional series resistance; however, this increased accuracy is application-specific. When series resistance is added, the total value must not be greater than 1kΩ. If filtering is required, suggested component values are 470pF and 50Ω on each input; exact values are application-specific.

9.2.3 Application Curve

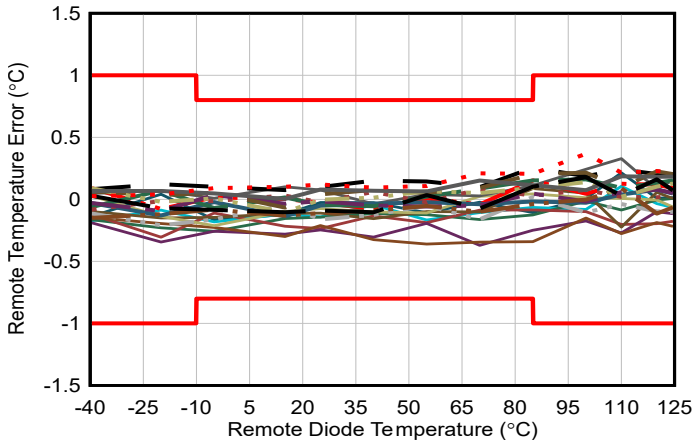


Figure 9-3. Remote Temperature Accuracy vs Temperature

9.3 Power Supply Recommendations

The TMP4719-Q1 device operates with a power-supply range of 1.62V to 5.5V. The device is optimized for operation at a 3.3V supply but can measure temperature accurately in the full supply range. A power-supply bypass capacitor is highly recommended. Place this capacitor as close as possible to the supply and ground pins of the device. A typical value for this supply bypass capacitor is 0.1µF. Applications with noisy or high-impedance power supplies can require additional decoupling capacitors to reject power-supply noise.

9.4 Layout

9.4.1 Layout Guidelines

Remote temperature sensing on the TMP4719-Q1 device measures small voltages using very low currents; therefore, noise at the device inputs must be minimized. Most applications using the TMP4719-Q1 have high digital content, with several clocks and logic-level transitions that create a noisy environment. The layout must adhere to the following guidelines:

1. Place the TMP4719-Q1 device as close to the remote junction sensor as possible.
2. Route the DP and DN traces next to each other and shield them from adjacent signals through the use of ground guard traces. If a multilayer PCB is used, bury these traces between the ground or V+ planes to shield them from extrinsic noise sources. 5mil (0.127mm) PCB traces are recommended.
3. Minimize additional thermocouple junction-induced offset voltage caused by copper-to-solder connections. If these junctions are used, make the same number and approximate locations of copper-to-solder connections in both the DP and DN connections to cancel any thermocouple effects.
4. Use a 0.1µF local bypass capacitor directly between the VDD and GND of the TMP4719-Q1 device. For optimum measurement performance, minimize filter capacitance between DP and DN to 1.5nF or less. This capacitance includes any cable capacitance between the remote temperature sensor and the TMP4719-Q1 device. The external capacitor shall be placed as close to the DP and DN pin as possible.
5. If the connection between the remote temperature sensor and the TMP4719-Q1 device is less than 8in (20.32cm) long, use a twisted-wire pair connection. For lengths greater than 8 inches, use a twisted, shielded pair with the shield grounded as close to the TMP4719-Q1 device as possible. Leave the remote sensor connection end of the shield wire open to avoid ground loops and 60Hz pickup.
6. Thoroughly clean and remove all flux residue in and around the pins of the TMP4719-Q1 device to avoid any leakage-induced temperature measurement error.
7. If series resistors are added, equal value shall be used for the DP and DN connections, and the total value shall not be greater than 1kΩ. Place the resistors as close to the DP and DN pins as possible.

9.4.2 Layout Example

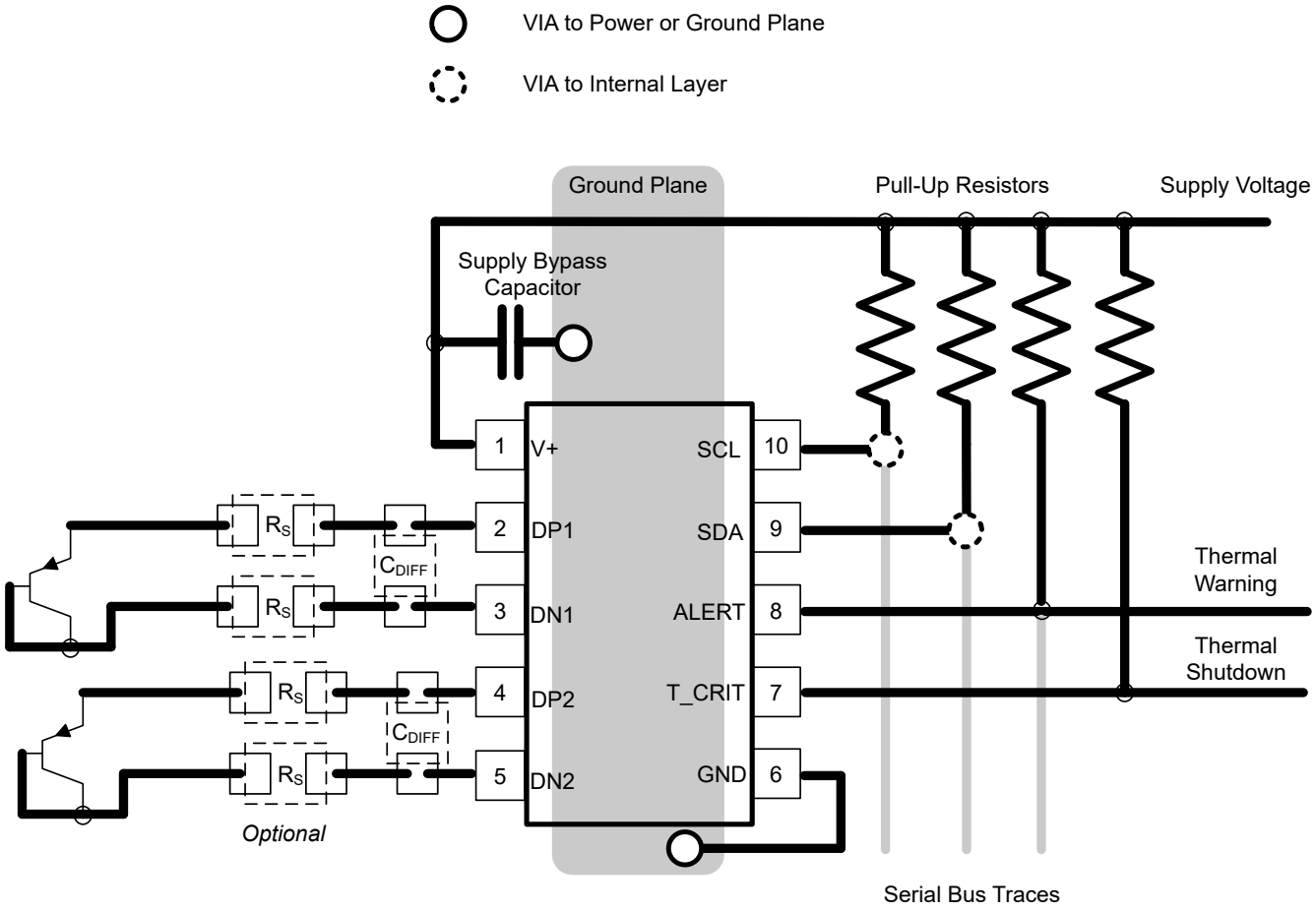


Figure 9-4. Layout Example

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *I2C Bus Pullup Resistor Calculation* Application Note
- Texas Instruments, *TMP4719EVM User's Guide*

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2025	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMP4719QDGSRQ1	Active	Production	VSSOP (DGS) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3QLS

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TMP4719-Q1 :

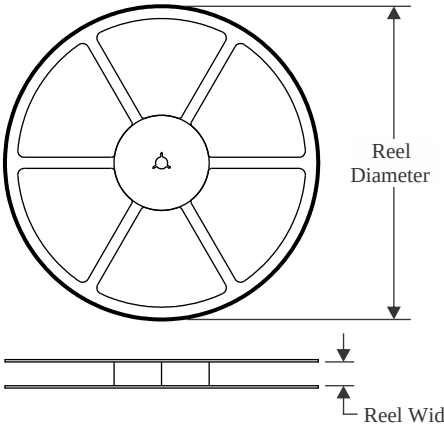
- Catalog : TMP4719

NOTE: Qualified Version Definitions:

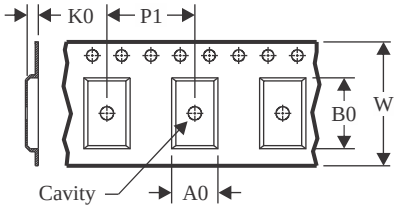
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

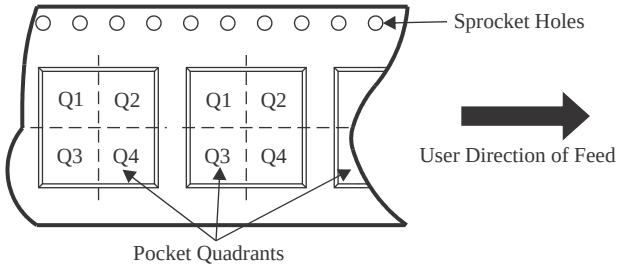


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

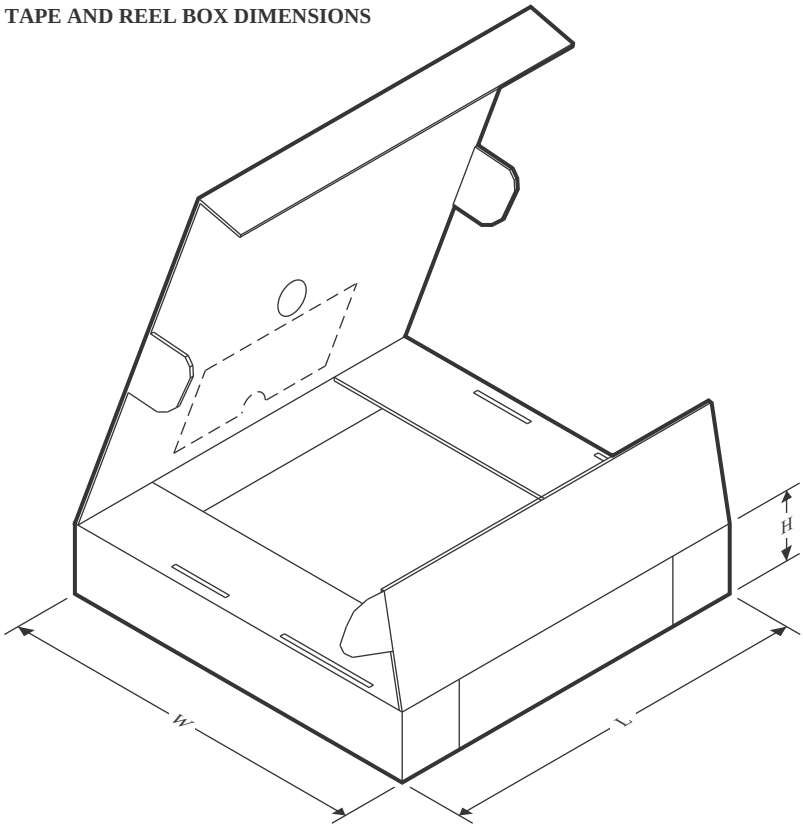
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP4719QDGSRQ1	VSSOP	DGS	10	3000	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

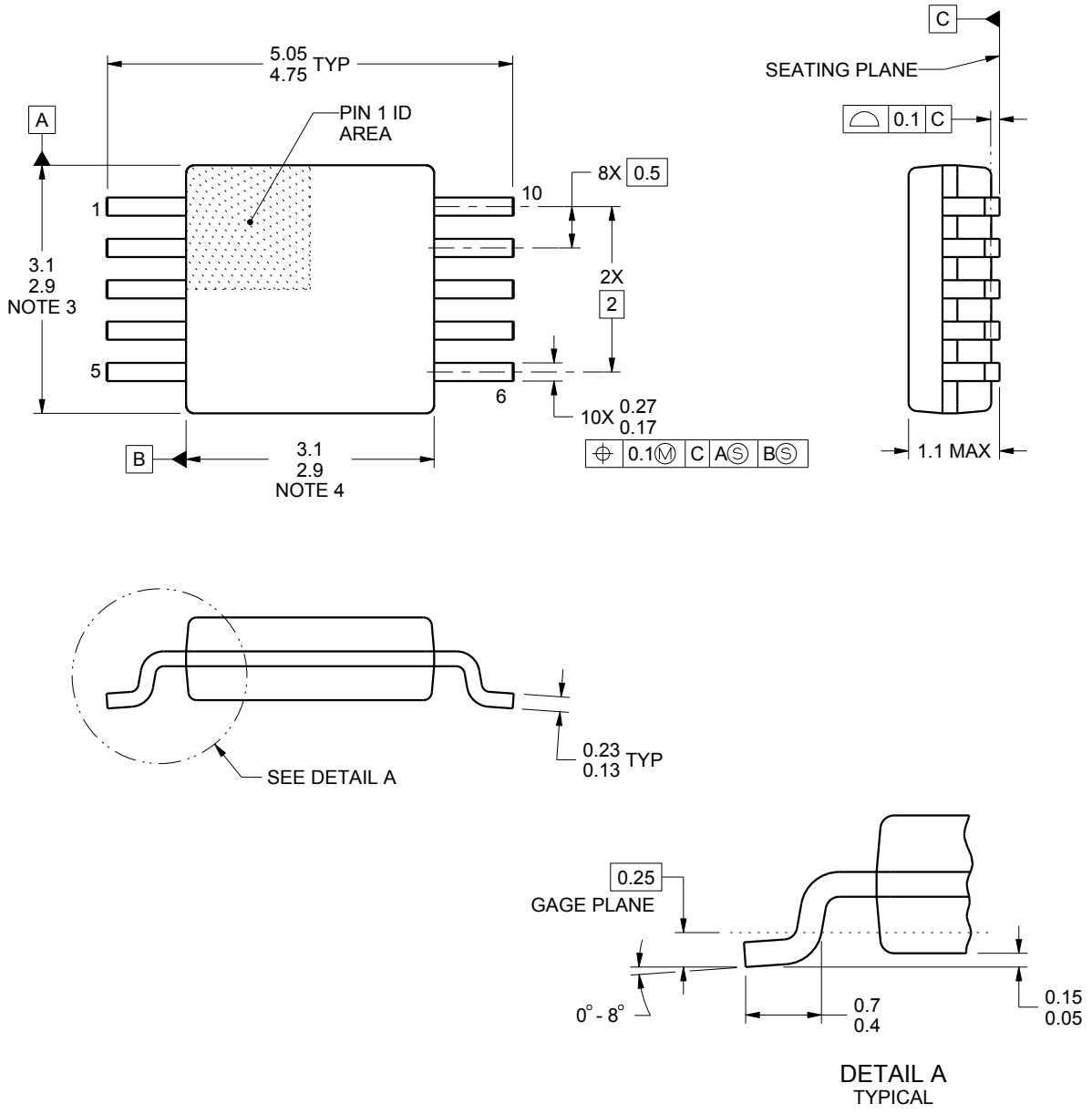
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP4719QDGSRQ1	VSSOP	DGS	10	3000	353.0	353.0	32.0

PACKAGE OUTLINE

DGS0010A

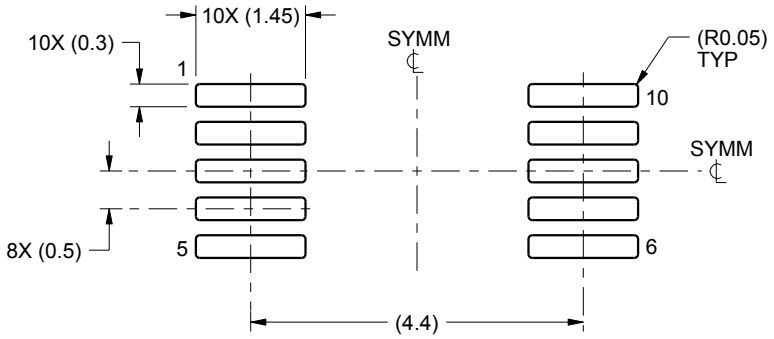
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

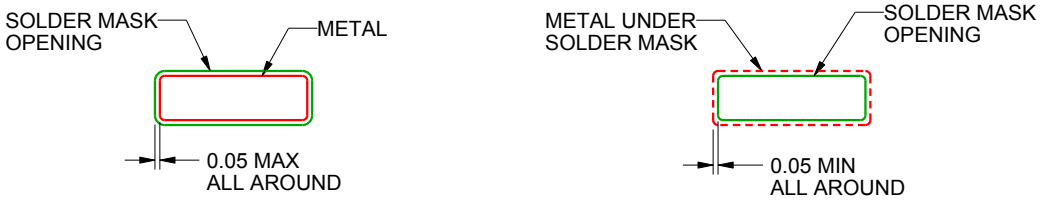


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

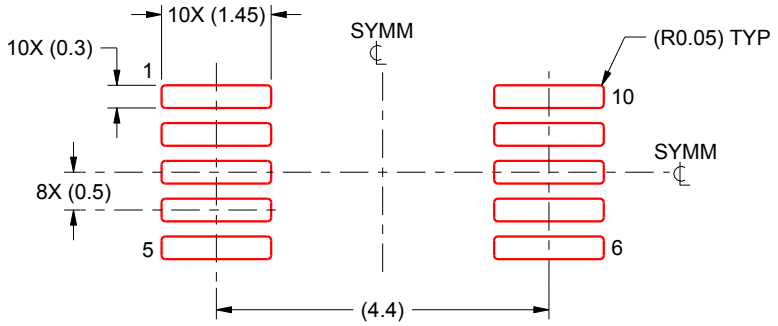


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025