TMUX620x 36 V, Low-Ron, 8:1 1-Channel and 4:1, 2-Channel Precision Multiplexers with 1.8 V Logic

1 Features

- Single supply range: 4.5 V to 36 V
- Dual supply range: ±4.5 V to ±18 V
- Low on-resistance: 4 Ω
- Low charge injection: 3 pC
- High current support: 400 mA (maximum) (WQFN)
- High current support: 300 mA (maximum) (TSSOP)
- –40°C to +125°C operating temperature
- 1.8 V logic compatible inputs
- Integrated pull-down resistor on logic pins
- Fail-safe logic
- Rail-to-rail operation
- Bidirectional signal path
- Break-before-make switching

2 Applications

- Factory automation and control
- Programmable logic controllers (PLC)
- Analog input modules
- Semiconductor test equipment
- Battery test equipment
- Ultrasound scanners
- Patient monitoring and diagnostics
- Optical networking
- Optical test equipment
- Wired networking
- Data acquisition systems (DAQ)

3 Description

The TMUX6208 is a precision 8:1, single channel multiplexer while the TMUX6209 is a 4:1, 2 channel multiplexer featuring low on resistance and charge injection. The devices work with a single supply (4.5V to 36V), dual supply (±4.5V to ±18V), or asymmetric supply (such as VDD = 12V, VSS = –5V). The TMUX620x supports bidirectional analog and digital signals onthe source (Sx) and drain (D) pins ranging from V_{SS} to V_{DD}.

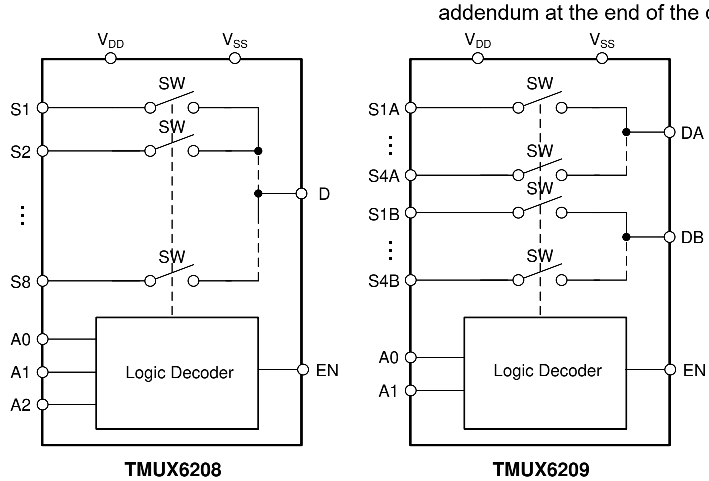
All logic control inputs support logic high levels from 1.8 V to V_{DD}, ensuring both TTL and CMOS logic compatibility when operating in the valid supply voltage range. Fail-Safe Logic circuitry allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage.

The TMUX620x are part of the precision switches and multiplexers family of devices. These devices have very low on and off leakage currents and low charge injection, allowing them to be used in high precision measurement applications.

Table 3-1. Device Information

PART NUMBER	CONFIGURATION	PACKAGE (1)
TMUX6208	1 Channel 8:1 Multiplexer	TSSOP (16) (PW) WQFN (16) (RUM)
TMUX6209	2 Channel 4:1 Multiplexer	

(1) For all available packages, see the package option addendum at the end of the data sheet.



TMUX6208 and TMUX6209 Block Diagram

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4 Device Comparison Table

PRODUCT	DESCRIPTION
TMUX6208	Low-Leakage-Current, Precision, 8:1, 1-Ch. multiplexer
TMUX6209	Low-Leakage-Current, Precision, 4:1, 2-Ch. multiplexer

5 Pin Configuration and Functions

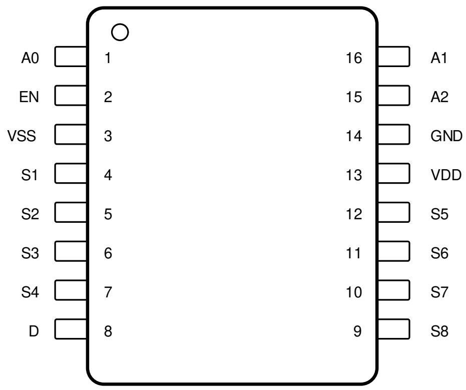


Figure 5-1. TMUX6208: PW Package 16-Pin TSSOP Top View

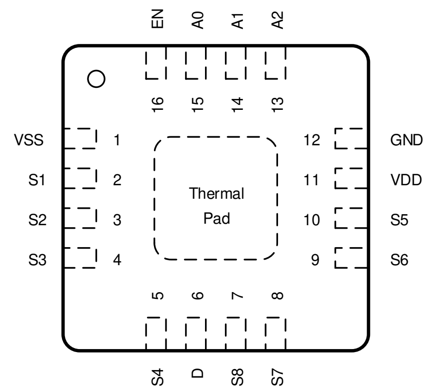


Figure 5-2. TMUX6208: RUM Package 16-Pin WQFN Top View

Table 5-1. TMUX6208 Pin Functions

NAME	PW NO.	RUM NO.	TYPE[1]	DESCRIPTION[2]
A0	1	15	I	Logic control input, has internal 4 MΩ pull-down resistor. Controls the switch configuration as shown in Section 8.5.
A1	16	14	I	Logic control input, has internal 4 MΩ pull-down resistor. Controls the switch configuration as shown in Section 8.5.
A2	15	13	I	Logic control input, has internal 4 MΩ pull-down resistor. Controls the switch configuration as shown in Section 8.5.
D	8	6	I/O	Drain pin. Can be an input or output.
EN	2	16	I	Active high logic enable, has internal 4 MΩ pull-down resistor. When this pin is low, all switches are turned off. When this pin is high, the Ax logic input determines which switch is turned on.
GND	14	12	P	Ground (0 V) reference.
S1	4	2	I/O	Source pin 1. Can be an input or output.
S2	5	3	I/O	Source pin 2. Can be an input or output.
S3	6	4	I/O	Source pin 3. Can be an input or output.
S4	7	5	I/O	Source pin 4. Can be an input or output.
S5	12	10	I/O	Source pin 5. Can be an input or output.
S6	11	9	I/O	Source pin 6. Can be an input or output.
S7	10	8	I/O	Source pin 7. Can be an input or output.
S8	9	7	I/O	Source pin 8. Can be an input or output.
VDD	13	11	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and GND.
VSS	3	1	P	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{SS} and GND.
Thermal Pad			—	The thermal pad is not connected internally. It is recommended that the pad be tied to GND or VSS for best performance.

(1) I = input, O = output, I/O = input and output, P = power.
(2) Refer to Section 8.4 for what to do with unused pins.

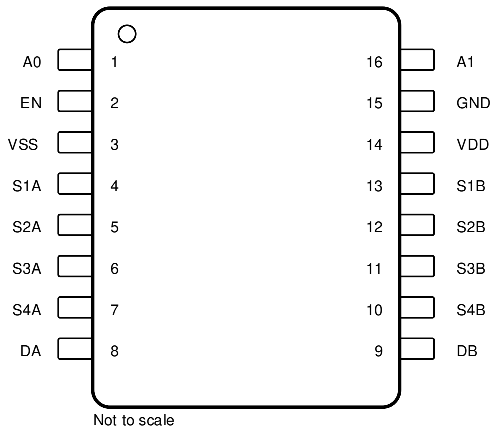


Figure 5-3. TMUX6209: PW Package 16-Pin TSSOP Top View

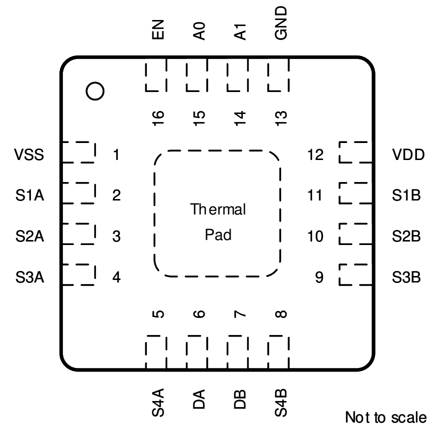


Figure 5-4. TMUX6209: RUM Package 16-Pin WQFN Top View

Table 5-2. TMUX6209 Pin Functions

NAME	PW NO.	RUM NO.	TYPE(1)	DESCRIPTION(2)
A0	1	15	I	Logic control input, has internal pull-down resistor. Controls the switch configuration as shown in Section 8.5.
A1	16	14	I	Logic control input, has internal pull-down resistor. Controls the switch configuration as shown in Section 8.5.
DA	8	6	I/O	Drain Terminal A. Can be an input or an output.
DB	9	7	I/O	Drain Terminal B. Can be an input or an output.
EN	2	16	I	Active high logic enable, has internal pull-up resistor. When this pin is low, all switches are turned off. When this pin is high, the Ax logic input determines which switch is turned on.
GND	15	13	P	Ground (0 V) reference.
S1A	4	2	I/O	Source pin 1A. Can be an input or output.
S1B	13	11	I/O	Source pin 1B. Can be an input or output.
S2A	5	3	I/O	Source pin 2A. Can be an input or output.
S2B	12	10	I/O	Source pin 2B. Can be an input or output.
S3A	6	4	I/O	Source pin 3A. Can be an input or output.
S3B	11	9	I/O	Source pin 3B. Can be an input or output.
S4A	7	5	I/O	Source pin 4A. Can be an input or output.
S4B	10	8	I/O	Source pin 4B. Can be an input or output.
VDD	14	12	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and GND.
VSS	3	1	P	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{SS} and GND.
Thermal Pad			—	The thermal pad is not connected internally. It is recommended that the pad be tied to GND or VSS for best performance.

(1) I = input, O = output, I/O = input and output, P = power.
(2) Refer to Section 8.4 for what to do with unused pins.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
$V_{DD} – V_{SS}$	Supply voltage		38	V
V_{DD}		–0.5	38	V
V_{SS}		–38	0.5	V
$V_{ADDRESS}$ or V_{EN}	Logic control input pin voltage (EN, A0, A1, A2)	–0.5	38	V
$I_{ADDRESS}$ or I_{EN}	Logic control input pin current (EN, A0, A1, A2)	–30	30	mA
V_S or V_D	Source or drain voltage (Sx, D)	V_{SS}–0.5	V_{DD}+0.5	V
I_{IK}	Diode clamp current(3)	–30	30	mA
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, D)		I_{DC} + 10 %(4)	mA
T_A	Ambient temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C
T_J	Junction temperature		150	°C
P_{tot}	Total power dissipation (QFN package)(5)		1650	mW
	Total power dissipation (TSSOP package)(5)		700	mW

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
(4) Refer to *Source or Drain Continuous Current* table for I_{DC} specifications.
(5) For QFN package: P_{tot} derates linearly above T_A = 70°C by 24.4mW/°C.
For TSSOP package: P_{tot} derates linearly above T_A = 70°C by 10.8mW/°C.

6.2 ESD Ratings

			VALUE	UNIT
TMUX620x				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Thermal Information

THERMAL METRIC[1]		TMUX620x		UNIT
		PW (TSSOP)	RUM (WQFN)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	93.5	41.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.9	24.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.0	16.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.0	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	39.4	16.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	2.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{DD} – V_{SS}$ [1]	Power supply voltage differential	4.5		36	V
V_{DD}	Positive power supply voltage	4.5		36	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (Sx, D)	V_{SS}		V_{DD}	V
$V_{ADDRESS}$ or V_{EN}	Address or enable pin voltage	0		36	V
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, D)			I_{DC} [2]	mA
T_A	Ambient temperature	–40		125	°C

(1) V_{DD} and V_{SS} can be any value as long as 4.5 V ≤ (V_{DD} – V_{SS}) ≤ 36 V, and the minimum V_{DD} is met.
(2) Refer to *Source or Drain Continuous Current* table for I_{DC} specifications.

6.5 Source or Drain Continuous Current

at supply voltage of V_{DD} ± 10%, V_{SS} ± 10 % (unless otherwise noted)

CONTINUOUS CURRENT PER CHANNEL (I_{DC})		T_A = 25°C	T_A = 85°C	T_A = 125°C	UNIT
PACKAGE	TEST CONDITIONS				
PW (TSSOP)	±15 V Dual Supply	300	190	110	mA
	+36 V Single Supply[1]	280	170	100	mA
	+12 V Single Supply	220	150	90	mA
	±5 V Dual Supply	210	140	90	mA
	+5 V Single Supply	170	110	70	mA
RUM (WQFN)	±15 V Dual Supply	400	230	120	mA
	+36 V Single Supply[1]	380	220	110	mA
	+12 V Single Supply	310	190	100	mA
	±5 V Dual Supply	300	190	100	mA
	+5 V Single Supply	230	150	90	mA

(1) Specified for nominal supply voltage only.

6.6 ±15 V Dual Supply: Electrical Characteristics

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –10 V to +10 V I_D = –10 mA Refer to On-Resistance	25°C		4	5.9	Ω
			–40°C to +85°C			7.4	Ω
			–40°C to +125°C			8.7	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = –10 V to +10 V I_D = –10 mA Refer to On-Resistance	25°C		0.2	0.7	Ω
			–40°C to +85°C			0.8	Ω
			–40°C to +125°C			0.9	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = –10 V to +10 V I_S = –10 mA Refer to On-Resistance	25°C		0.4	1.5	Ω
			–40°C to +85°C			1.7	Ω
			–40°C to +125°C			1.8	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = –10 mA Refer to On-Resistance	–40°C to +125°C		0.02		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is off V_S = +10 V / –10 V V_D = –10 V / + 10 V Refer to Section 7.2	25°C	–0.4	0.04	0.4	nA
			–40°C to +85°C	–1		1	nA
			–40°C to +125°C	–5		5	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is off V_S = +10 V / –10 V V_D = –10 V / + 10 V Refer to Section 7.2	25°C	–0.4	0.04	0.4	nA
			–40°C to +85°C	–6		6	nA
			–40°C to +125°C	–42		42	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is on V_S = V_D = ±10 V Refer to Section 7.3	25°C	–0.4	0.04	0.4	nA
			–40°C to +85°C	–5		5	nA
			–40°C to +125°C	–40		40	nA
LOGIC INPUTS (EN, A0, A1, A2)							
V_{IH}	Logic voltage high		–40°C to +125°C	1.3		36	V
V_{IL}	Logic voltage low		–40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–40°C to +125°C		0.4	2	µA
I_{IL}	Input leakage current		–40°C to +125°C	–0.1	–0.005		µA
C_{IN}	Logic input capacitance		–40°C to +125°C		3.5		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 16.5 V, V_{SS} = –16.5 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		35	57	µA
			–40°C to +85°C			60	µA
			–40°C to +125°C			75	µA
I_{SS}	V_{SS} supply current	V_{DD} = 16.5 V, V_{SS} = –16.5 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		3	14	µA
			–40°C to +85°C			15	µA
			–40°C to +125°C			22	µA

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

6.7 ±15 V Dual Supply: Switching Characteristics

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ± 10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF Refer to Transition Time	25°C		140	195	ns
			–40°C to +85°C			220	ns
			–40°C to +125°C			240	ns
$t_{ON\ (EN)}$	Turn-on time from enable	V_S = 10 V R_L = 300 Ω, C_L = 35 pF Refer to Section 7.5	25°C		140	195	ns
			–40°C to +85°C			220	ns
			–40°C to +125°C			240	ns
$t_{OFF\ (EN)}$	Turn-off time from enable	V_S = 10 V R_L = 300 Ω, C_L = 35 pF Refer to Section 7.5	25°C		200	268	ns
			–40°C to +85°C			285	ns
			–40°C to +125°C			298	ns
t_{BBM}	Break-before-make time delay	V_S = 10 V, R_L = 300 Ω, C_L = 35 pF Refer to Break-Before-Make	25°C		60		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$T_{ON\ (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1 µs R_L = 300 Ω, C_L = 35 pF Refer to Turn-on (VDD) Time	25°C		0.16		ms
			–40°C to +85°C		0.17		ms
			–40°C to +125°C		0.17		ms
t_{PD}	Propagation delay	R_L = 50 Ω , C_L = 5 pF Refer to Section 7.8	25°C		1.8		ns
Q_{INJ}	Charge injection	V_S = 0 V, C_L = 100 pF Refer to Section 7.9	25°C		3		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 100 kHz Refer to Off Isolation	25°C		–82		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1 MHz Refer to Off Isolation	25°C		–62		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 100 kHz Refer to Crosstalk	25°C		–85		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1MHz Refer to Crosstalk	25°C		–65		dB
BW	–3dB Bandwidth (TMUX6208)	R_L = 50 Ω , C_L = 5 pF V_S = 0 V Refer to Bandwidth	25°C		30		MHz
BW	–3dB Bandwidth (TMUX6209)	R_L = 50 Ω , C_L = 5 pF V_S = 0 V Refer to Bandwidth	25°C		52		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1 MHz	25°C		–0.35		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz Refer to ACPSRR	25°C		–74		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 15 V, V_{BIAS} = 0 V R_L = 10 kΩ , C_L = 5 pF, f = 20 Hz to 20 kHz Refer to THD + Noise	25°C		0.0003		%
$C_{S(OFF)}$	Source off capacitance	V_S = 0 V, f = 1 MHz	25°C		15		pF
$C_{D(OFF)}$	Drain off capacitance (TMUX6208)	V_S = 0 V, f = 1 MHz	25°C		135		pF
$C_{D(OFF)}$	Drain off capacitance (TMUX6209)	V_S = 0 V, f = 1 MHz	25°C		68		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance (TMUX6208)	V_S = 0 V, f = 1 MHz	25°C		185		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance (TMUX6209)	V_S = 0 V, f = 1 MHz	25°C		115		pF

6.8 36 V Single Supply: Electrical Characteristics

V_{DD} = +36 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +36 V, V_{SS} = 0 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to 30 V I_D = –10 mA Refer to On-Resistance	25°C		4	6.2	Ω
			–40°C to +85°C			7.9	Ω
			–40°C to +125°C			9.4	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = 0 V to 30 V I_D = –10 mA Refer to On-Resistance	25°C		0.2	0.7	Ω
			–40°C to +85°C			0.8	Ω
			–40°C to +125°C			0.9	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0 V to 30 V I_S = –10 mA Refer to On-Resistance	25°C		0.4	1.8	Ω
			–40°C to +85°C			2.5	Ω
			–40°C to +125°C			3.1	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 18 V, I_S = –10 mA Refer to On-Resistance	–40°C to +125°C		0.015		Ω/°C
$I_{S(OFF)}$	Source off leakage current[1]	V_{DD} = 39.6 V, V_{SS} = 0 V Switch state is off V_S = 30 V / 1 V V_D = 1 V / 30 V Refer to Section 7.2	25°C	–0.4	0.04	0.4	nA
			–40°C to +85°C	–2		2	nA
			–40°C to +125°C	–10		10	nA
$I_{D(OFF)}$	Drain off leakage current[1]	V_{DD} = 39.6 V, V_{SS} = 0 V Switch state is off V_S = 30 V / 1 V V_D = 1 V / 30 V Refer to Section 7.2	25°C	–0.5	0.05	0.5	nA
			–40°C to +85°C	–12		12	nA
			–40°C to +125°C	–85		85	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current[2]	V_{DD} = 39.6 V, V_{SS} = 0 V Switch state is on V_S = V_D = 30 V or 1 V Refer to Section 7.3	25°C	–0.5	0.05	0.5	nA
			–40°C to +85°C	–11		11	nA
			–40°C to +125°C	–78		78	nA
LOGIC INPUTS (EN, A0, A1, A2)							
V_{IH}	Logic voltage high		–40°C to +125°C	1.3		36	V
V_{IL}	Logic voltage low		–40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–40°C to +125°C		0.4	2	µA
I_{IL}	Input leakage current		–40°C to +125°C	–0.1	–0.005		µA
C_{IN}	Logic input capacitance		–40°C to +125°C		3.5		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 39.6 V, V_{SS} = 0 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		55	86	µA
			–40°C to +85°C			90	µA
			–40°C to +125°C			105	µA

(1) When V_S is positive, V_D is negative, and vice versa.
(2) When V_S is at a voltage potential, V_D is floating, and vice versa.

6.9 36 V Single Supply: Switching Characteristics

V_{DD} = +36 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +36 V, V_{SS} = 0 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input	V_S = 18 V R_L = 300 Ω, C_L = 35 pF Refer to Transition Time	25°C		105	200	ns
			–40°C to +85°C			225	ns
			–40°C to +125°C			240	ns
$t_{ON\ (EN)}$	Turn-on time from enable	V_S = 18 V R_L = 300 Ω, C_L = 35 pF Refer to Section 7.5	25°C		115	200	ns
			–40°C to +85°C			220	ns
			–40°C to +125°C			240	ns
$t_{OFF\ (EN)}$	Turn-off time from enable	V_S = 18 V R_L = 300 Ω, C_L = 35 pF Refer to Section 7.5	25°C		90	290	ns
			–40°C to +85°C			305	ns
			–40°C to +125°C			315	ns
t_{BBM}	Break-before-make time delay	V_S = 18 V, R_L = 300 Ω, C_L = 35 pF Refer to Break-Before-Make	25°C		40		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$T_{ON\ (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1 µs R_L = 300 Ω, C_L = 35 pF Refer to Turn-on (VDD) Time	25°C		0.14		ms
			–40°C to +85°C		0.15		ms
			–40°C to +125°C		0.15		ms
t_{PD}	Propagation delay	R_L = 50 Ω , C_L = 5 pF Refer to Section 7.8	25°C		2.5		ns
Q_{INJ}	Charge injection	V_S = 18 V, C_L = 100 pF Refer to Section 7.9	25°C		2		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1 MHz Refer to Off Isolation	25°C		–62		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 100 kHz Refer to Crosstalk	25°C		–85		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1MHz Refer to Crosstalk	25°C		–65		dB
BW	–3dB Bandwidth (TMUX6208)	R_L = 50 Ω , C_L = 5 pF V_S = 6 V Refer to Bandwidth	25°C		30		MHz
BW	–3dB Bandwidth (TMUX6209)	R_L = 50 Ω , C_L = 5 pF V_S = 6 V	25°C		50		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1 MHz	25°C		–0.35		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz Refer to ACPSRR	25°C		–70		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} =18 V, V_{BIAS} = 18 V R_L = 10 kΩ , C_L = 5 pF, f = 20 Hz to 20 kHz Refer to THD + Noise	25°C		0.0003		%
$C_{S(OFF)}$	Source off capacitance	V_S = 18 V, f = 1 MHz	25°C		15		pF
$C_{D(OFF)}$	Drain off capacitance (TMUX6208)	V_S = 18 V, f = 1 MHz	25°C		138		pF
$C_{D(OFF)}$	Drain off capacitance (TMUX6209)	V_S = 18 V, f = 1 MHz	25°C		68		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance (TMUX6208)	V_S = 18 V, f = 1 MHz	25°C		185		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance (TMUX6209)	V_S = 18 V, f = 1 MHz	25°C		115		pF

6.10 12 V Single Supply: Electrical Characteristics

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to 10 V I_D = –10 mA Refer to On-Resistance	25°C		7	11.8	Ω
			–40°C to +85°C			14.2	Ω
			–40°C to +125°C			16.5	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = 0 V to 10 V I_D = –10 mA Refer to On-Resistance	25°C		0.2	0.7	Ω
			–40°C to +85°C			0.8	Ω
			–40°C to +125°C			0.9	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0 V to 10 V I_S = –10 mA Refer to On-Resistance	25°C		1.7	3.4	Ω
			–40°C to +85°C			3.8	Ω
			–40°C to +125°C			4.6	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 6 V, I_S = –10 mA Refer to On-Resistance	–40°C to +125°C		0.03		Ω/°C
$I_{S(OFF)}$	Source off leakage current[(1)]	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is off V_S = 10 V / 1 V V_D = 1 V / 10 V Refer to Section 7.2	25°C	–0.4	0.04	0.4	nA
			–40°C to +85°C	–1		1	nA
			–40°C to +125°C	–8		8	nA
$I_{D(OFF)}$	Drain off leakage current[(1)]	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is off V_S = 10 V / 1 V V_D = 1 V / 10 V Refer to Section 7.2	25°C	–0.4	0.05	0.4	nA
			–40°C to +85°C	–5		5	nA
			–40°C to +125°C	–30		30	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current[(2)]	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is on V_S = V_D = 10 V or 1 V Refer to Section 7.3	25°C	–0.4	0.05	0.4	nA
			–40°C to +85°C	–4		4	nA
			–40°C to +125°C	–28		28	nA
LOGIC INPUTS (EN, A0, A1, A2)							
V_{IH}	Logic voltage high		–40°C to +125°C	1.3		36	V
V_{IL}	Logic voltage low		–40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–40°C to +125°C		0.4	2	µA
I_{IL}	Input leakage current		–40°C to +125°C	–0.1	–0.005		µA
C_{IN}	Logic input capacitance		–40°C to +125°C		3.5		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 13.2 V, V_{SS} = 0 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		30	48	µA
			–40°C to +85°C			54	µA
			–40°C to +125°C			65	µA

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

6.11 12 V Single Supply: Switching Characteristics

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input	V_S = 8 V R_L = 300 Ω, C_L = 35 pF Refer to Transition Time	25°C		180	210	ns
			–40°C to +85°C			245	ns
			–40°C to +125°C			276	ns
$t_{ON\ (EN)}$	Turn-on time from enable	V_S = 8 V R_L = 300 Ω, C_L = 35 pF Refer to Section 7.5	25°C		115	202	ns
			–40°C to +85°C			235	ns
			–40°C to +125°C			265	ns
$t_{OFF\ (EN)}$	Turn-off time from enable	V_S = 8 V R_L = 300 Ω, C_L = 35 pF Refer to Section 7.5	25°C		290	318	ns
			–40°C to +85°C			350	ns
			–40°C to +125°C			370	ns
t_{BBM}	Break-before-make time delay	V_S = 8 V, R_L = 300 Ω, C_L = 35 pF Refer to Break-Before-Make	25°C		50		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$T_{ON\ (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1 µs R_L = 300 Ω, C_L = 35 pF Refer to Turn-on (VDD) Time	25°C		0.16		ms
			–40°C to +85°C		0.17	1	ms
			–40°C to +125°C		0.17	1	ms
t_{PD}	Propagation delay	R_L = 50 Ω , C_L = 5 pF Refer to Section 7.8	25°C		2.5		ns
Q_{INJ}	Charge injection	V_S = 6 V, C_L = 100 pF Refer to Section 7.9	25°C		2		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 100 kHz	25°C		–82		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1 MHz Refer to Off Isolation	25°C		–62		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 100 kHz Refer to Crosstalk	25°C		–85		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1MHz Refer to Crosstalk	25°C		–65		dB
BW	–3dB Bandwidth (TMUX6208)	R_L = 50 Ω , C_L = 5 pF V_S = 6 V Refer to Bandwidth	25°C		28		MHz
BW	–3dB Bandwidth (TMUX6209)	R_L = 50 Ω , C_L = 5 pF V_S = 6 V	25°C		55		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1 MHz	25°C		–0.6		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz Refer to ACPSRR	25°C		–74		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 6 V, V_{BIAS} = 6 V R_L = 10 kΩ , C_L = 5 pF, f = 20 Hz to 20 kHz Refer to THD + Noise	25°C		0.0007		%
$C_{S(OFF)}$	Source off capacitance	V_S = 6 V, f = 1 MHz	25°C		17		pF
$C_{D(OFF)}$	Drain off capacitance (TMUX6208)	V_S = 6 V, f = 1 MHz	25°C		155		pF
$C_{D(OFF)}$	Drain off capacitance (TMUX6209)	V_S = 6 V, f = 1 MHz	25°C		78		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance (TMUX6208)	V_S = 6 V, f = 1 MHz	25°C		200		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance (TMUX6209)	V_S = 6 V, f = 1 MHz	25°C		122		pF

6.12 ±5 V Dual Supply: Electrical Characteristics

V_{DD} = +5 V ± 10%, V_{SS} = –5 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +5 V, V_{SS} = –5 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_{DD} = +4.5 V, V_{SS} = –4.5 V V_S = –4.5 V to +4.5 V I_D = –10 mA	25°C		7	13.5	Ω
			–40°C to +85°C			16.2	Ω
			–40°C to +125°C			18.5	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = –4.5 V to +4.5 V I_D = –10 mA	25°C		0.2	0.7	Ω
			–40°C to +85°C			0.8	Ω
			–40°C to +125°C			0.9	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = –4.5 V to +4.5 V I_D = –10 mA	25°C		2	3.8	Ω
			–40°C to +85°C			4.2	Ω
			–40°C to +125°C			4.9	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = –10 mA	–40°C to +125°C		0.03		Ω/°C
$I_{S(OFF)}$	Source off leakage current[(1)]	V_{DD} = +5.5 V, V_{SS} = –5.5 V Switch state is off V_S = +4.5 V / –4.5 V V_D = –4.5 V / + 4.5 V	25°C	–0.5	0.02	0.5	nA
			–40°C to +85°C	–1.5		1.5	nA
			–40°C to +125°C	–8		8	nA
$I_{D(OFF)}$	Drain off leakage current[(1)]	V_{DD} = +5.5 V, V_{SS} = –5.5 V Switch state is off V_S = +4.5 V / –4.5 V V_D = –4.5 V / + 4.5 V	25°C	–0.5	0.04	0.5	nA
			–40°C to +85°C	–3.5		3.5	nA
			–40°C to +125°C	–28		28	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current[(2)]	V_{DD} = +5.5 V, V_{SS} = –5.5 V Switch state is on V_S = V_D = ±4.5 V	25°C	–0.5	0.04	0.5	nA
			–40°C to +85°C	–3		3	nA
			–40°C to +125°C	–26		26	nA
LOGIC INPUTS (EN, A0, A1, A2)							
V_{IH}	Logic voltage high		–40°C to +125°C	1.3		36	V
V_{IL}	Logic voltage low		–40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–40°C to +125°C		0.4	2	µA
I_{IL}	Input leakage current		–40°C to +125°C	–0.1	–0.005		µA
C_{IN}	Logic input capacitance		–40°C to +125°C		3.5		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = +5.5 V, V_{SS} = –5.5 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		25	38	µA
			–40°C to +85°C			44	µA
			–40°C to +125°C			55	µA
I_{SS}	V_{SS} supply current	V_{DD} = +5.5 V, V_{SS} = –5.5 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		2	6.2	µA
			–40°C to +85°C			7	µA
			–40°C to +125°C			15	µA

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

6.13 ±5 V Dual Supply: Switching Characteristics

V_{DD} = +5 V ± 10%, V_{SS} = –5 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +5 V, V_{SS} = –5 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input	V_S = 3 V R_L = 300 Ω, C_L = 35 pF Refer to Transition Time	25°C		125	250	ns
			–40°C to +85°C			280	ns
			–40°C to +125°C			305	ns
$t_{ON\ (EN)}$	Turn-on time from enable	V_S = 3 V R_L = 300 Ω, C_L = 35 pF Refer to Section 7.5	25°C		128	245	ns
			–40°C to +85°C			278	ns
			–40°C to +125°C			305	ns
$t_{OFF\ (EN)}$	Turn-off time from enable	V_S = 3 V R_L = 300 Ω, C_L = 35 pF Refer to Section 7.5	25°C		300	372	ns
			–40°C to +85°C			400	ns
			–40°C to +125°C			420	ns
t_{BBM}	Break-before-make time delay	V_S = 3 V, R_L = 300 Ω, C_L = 35 pF Refer to Break-Before-Make	25°C		50		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$T_{ON\ (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1 µs R_L = 300 Ω, C_L = 35 pF Refer to Turn-on (VDD) Time	25°C		0.16		ms
			–40°C to +85°C		0.17	1	ms
			–40°C to +125°C		0.17	1	ms
t_{PD}	Propagation delay	R_L = 50 Ω , C_L = 5 pF Refer to Section 7.8	25°C		2		ns
Q_{INJ}	Charge injection	V_S = 0 V, C_L = 100 pF Refer to Section 7.9	25°C		1.2		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 100 kHz Refer to Off Isolation	25°C		–82		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1 MHz Refer to Off Isolation	25°C		–62		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 100 kHz Refer to Crosstalk	25°C		–85		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1MHz Refer to Crosstalk	25°C		–65		dB
BW	–3dB Bandwidth (TMUX6208)	R_L = 50 Ω , C_L = 5 pF V_S = 0 V Refer to Bandwidth	25°C		28		MHz
BW	–3dB Bandwidth (TMUX6209)	R_L = 50 Ω , C_L = 5 pF V_S = 0 V	25°C		54		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1 MHz	25°C		–0.7		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz Refer to ACPSRR	25°C		–76		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 5 V, V_{BIAS} = 0 V R_L = 10 kΩ , C_L = 5 pF, f = 20 Hz to 20 kHz Refer to THD + Noise	25°C		0.0017		%
$C_{S(OFF)}$	Source off capacitance	V_S = 0 V, f = 1 MHz	25°C		18		pF
$C_{D(OFF)}$	Drain off capacitance (TMUX6208)	V_S = 0 V, f = 1 MHz	25°C		160		pF
$C_{D(OFF)}$	Drain off capacitance (TMUX6209)	V_S = 0 V, f = 1 MHz	25°C		80		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance (TMUX6208)	V_S = 0 V, f = 1 MHz	25°C		205		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance (TMUX6209)	V_S = 0 V, f = 1 MHz	25°C		124		pF

6.14 Typical Characteristics

at T_A = 25°C (unless otherwise noted)

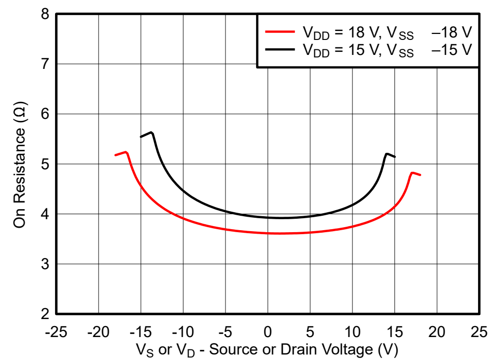


Figure 6-1. On-Resistance vs Source or Drain Voltage – Dual Supply

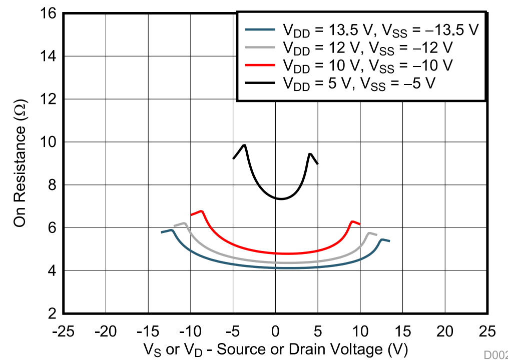


Figure 6-2. On-Resistance vs Source or Drain Voltage – Dual Supply

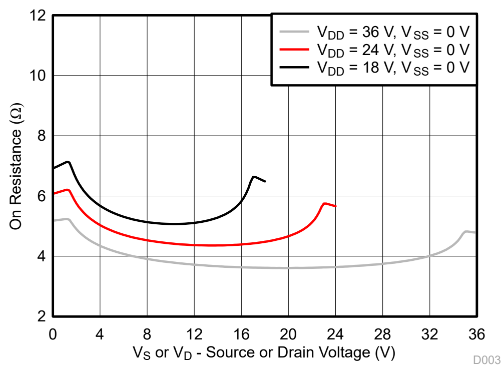


Figure 6-3. On-Resistance vs Source or Drain Voltage – Single Supply

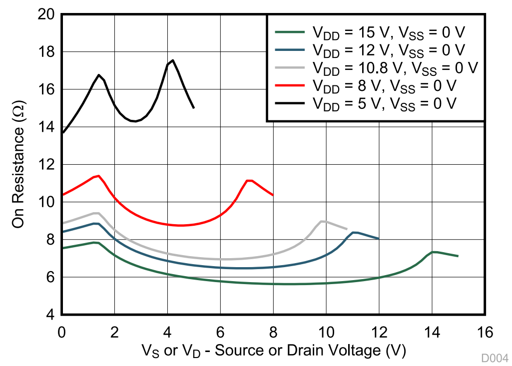
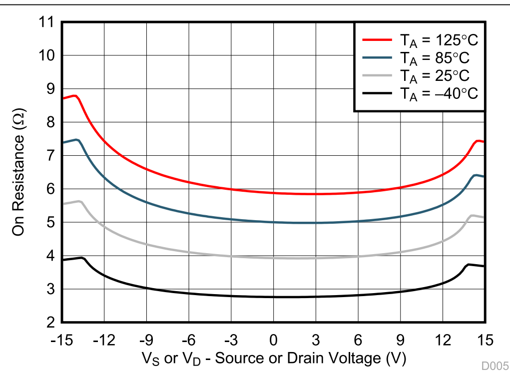
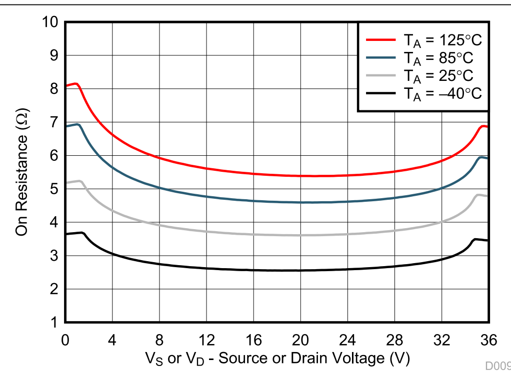


Figure 6-4. On-Resistance vs Source or Drain Voltage – Single Supply



V_{DD} = 15 V, V_{SS} = -15 V

Figure 6-5. On-Resistance vs Temperature

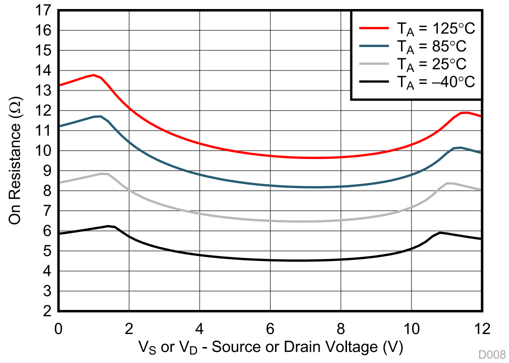


V_{DD} = 36 V, V_{SS} = 0 V

Figure 6-6. On-Resistance vs Temperature

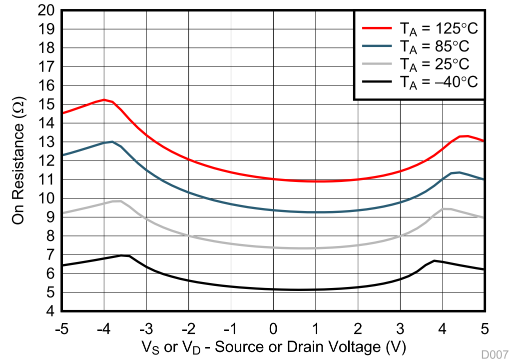
6.14 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



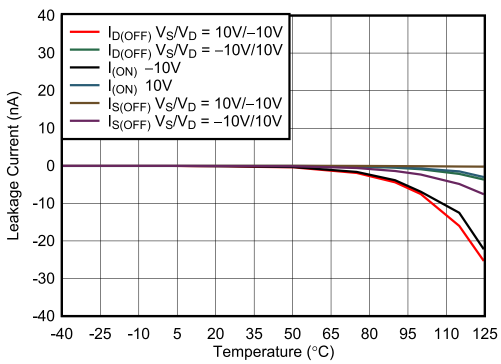
V_{DD} = 12 V, V_{SS} = 0 V

Figure 6-7. On-Resistance vs Temperature



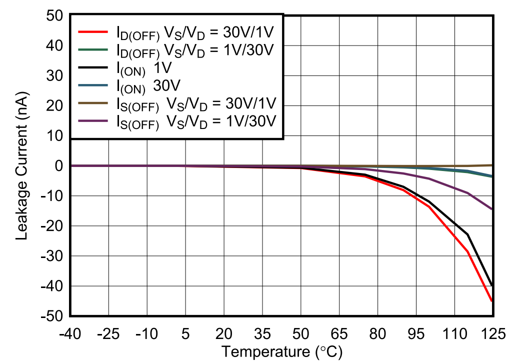
V_{DD} = 5 V, V_{SS} = -5 V

Figure 6-8. On-Resistance vs Temperature



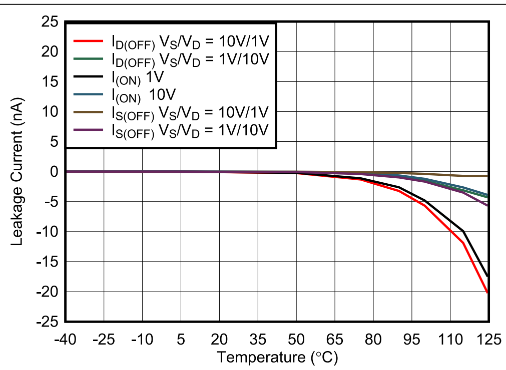
V_{DD} = 15 V, V_{SS} = -15 V

Figure 6-9. Leakage Current vs Temperature



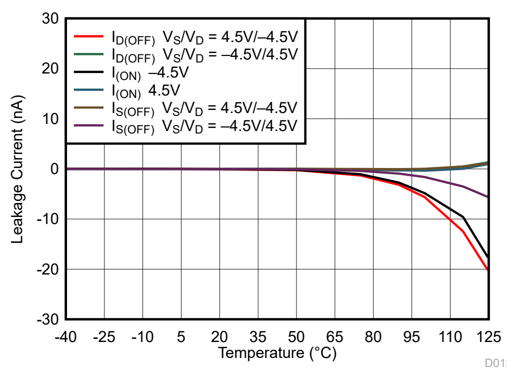
V_{DD} = 36 V, V_{SS} = 0 V

Figure 6-10. Leakage Current vs Temperature



V_{DD} = 12 V, V_{SS} = 0 V

Figure 6-11. Leakage Current vs Temperature



V_{DD} = 5 V, V_{SS} = -5 V

Figure 6-12. Leakage Current vs Temperature

6.14 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)

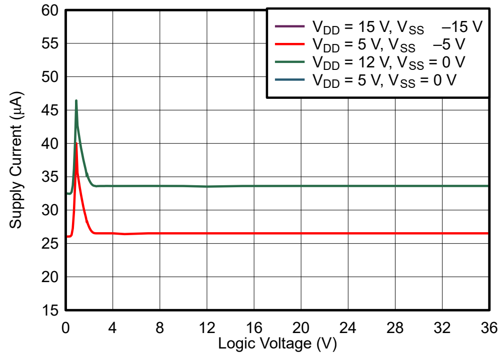


Figure 6-13. Supply Current vs Logic Voltage

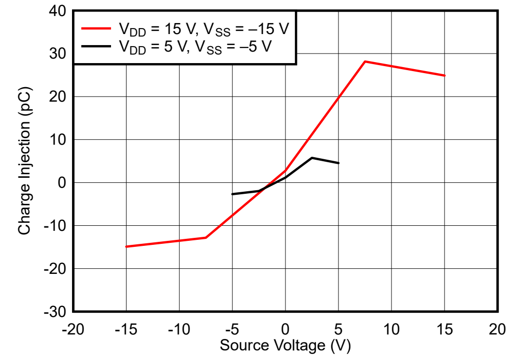


Figure 6-14. Charge Injection vs Source Voltage – Dual Supply

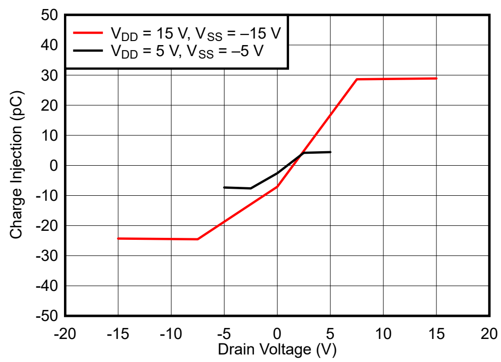


Figure 6-15. Charge Injection vs Drain Voltage – Dual Supply

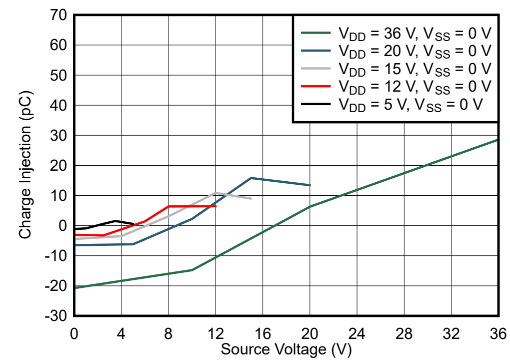


Figure 6-16. Charge Injection vs Source Voltage – Single Supply

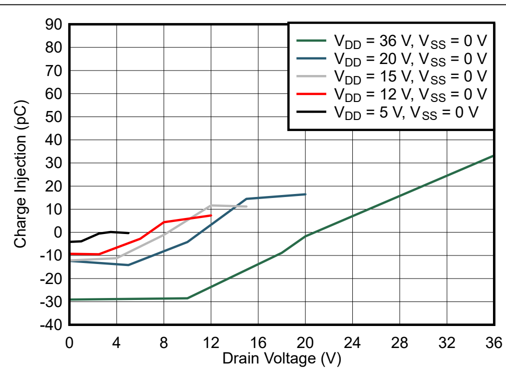


Figure 6-17. Charge Injection vs Drain Voltage – Single Supply

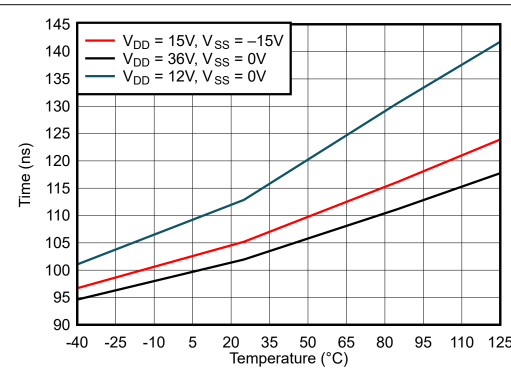
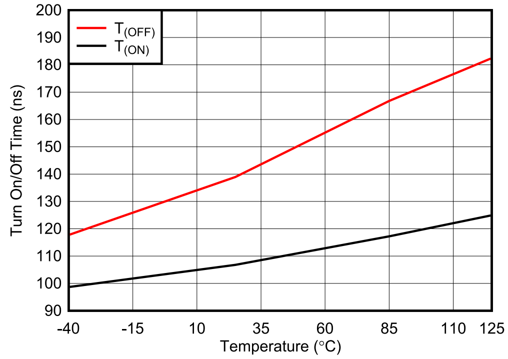


Figure 6-18. $T_{TRANSITION}$ vs Temperature

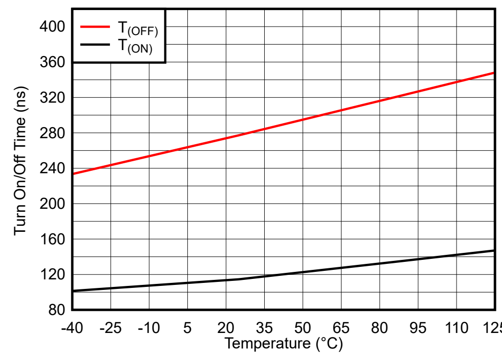
6.14 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



V_{DD} = 15 V, V_{SS} = -15 V

Figure 6-19. T_{ON} and T_{OFF} vs Temperature



V_{DD} = 36 V, V_{SS} = 0 V

Figure 6-20. T_{ON} and T_{OFF} vs Temperature

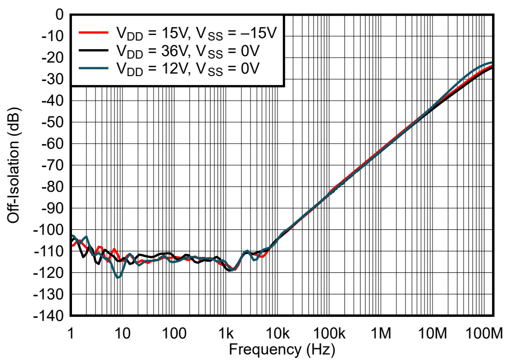
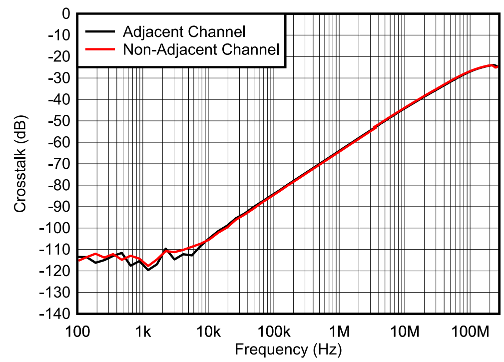


Figure 6-21. Off-Isolation vs Frequency



V_{DD} = 15 V, V_{SS} = -15 V

Figure 6-22. Crosstalk vs Frequency

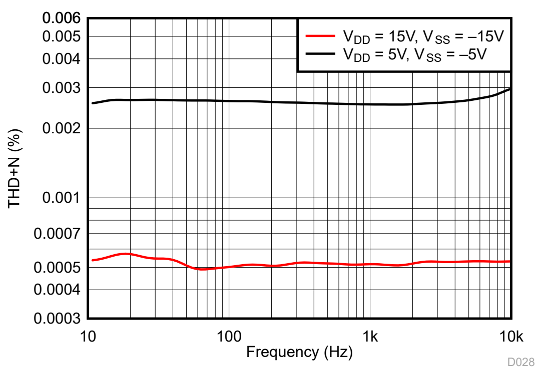


Figure 6-23. THD+N vs Frequency (Dual Supply)

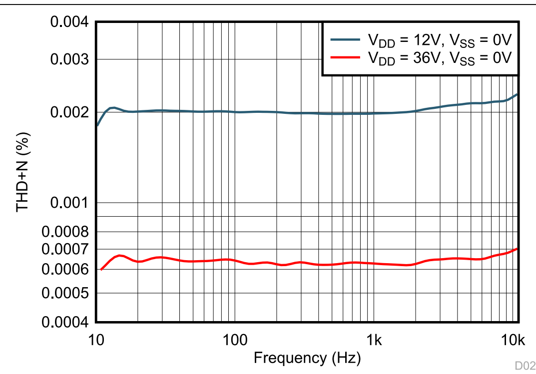
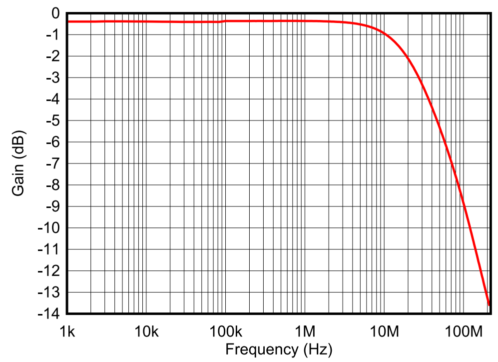


Figure 6-24. THD+N vs Frequency (Single Supply)

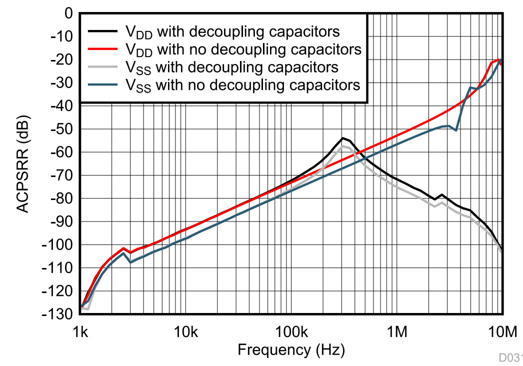
6.14 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



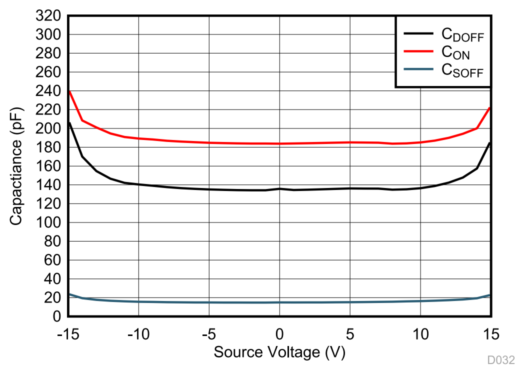
V_{DD} = +15 V, V_{SS} = -15 V

Figure 6-25. On Response vs Frequency



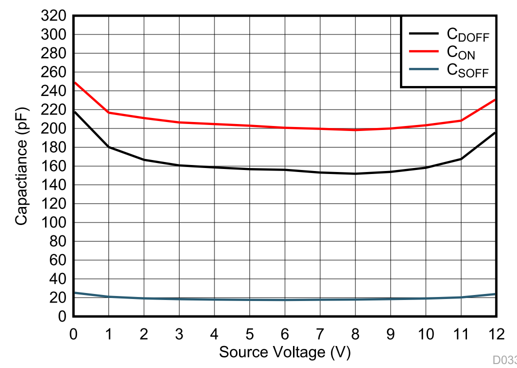
V_{DD} = +15 V, V_{SS} = -15 V

Figure 6-26. ACPSRR vs Frequency



V_{DD} = +15 V, V_{SS} = -15 V

Figure 6-27. Capacitance vs Source Voltage or Drain Voltage



V_{DD} = 12 V, V_{SS} = 0 V

Figure 6-28. Capacitance vs Source Voltage or Drain Voltage

7 Parameter Measurement Information

7.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. Figure 7-1 shows the measurement setup used to measure R_{ON}. Voltage (V) and current (I_{SD}) are measured using this setup, and R_{ON} is computed with $R_{ON} = V / I_{SD}$.

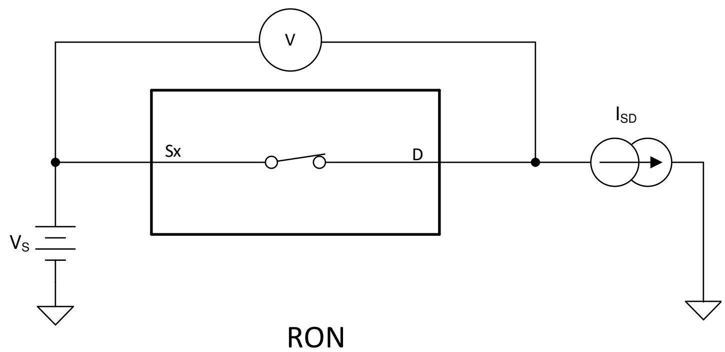


Figure 7-1. On-Resistance Measurement Setup

7.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

- Source off-leakage current
- Drain off-leakage current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

Figure 7-2 shows the setup used to measure both off-leakage currents.

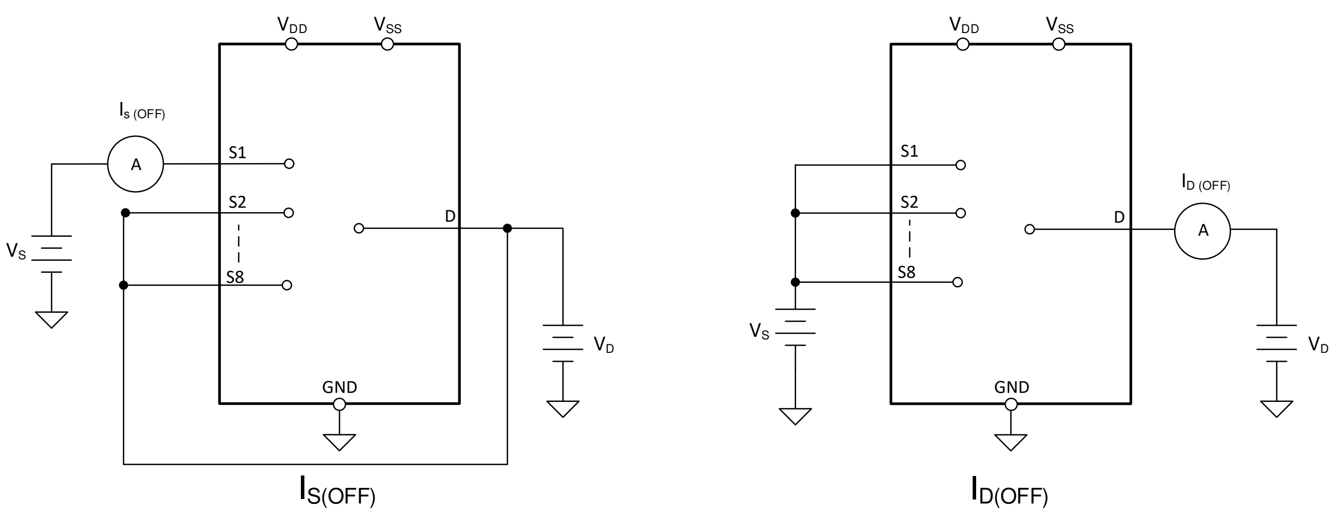


Figure 7-2. Off-Leakage Measurement Setup

7.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. Figure 7-3 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

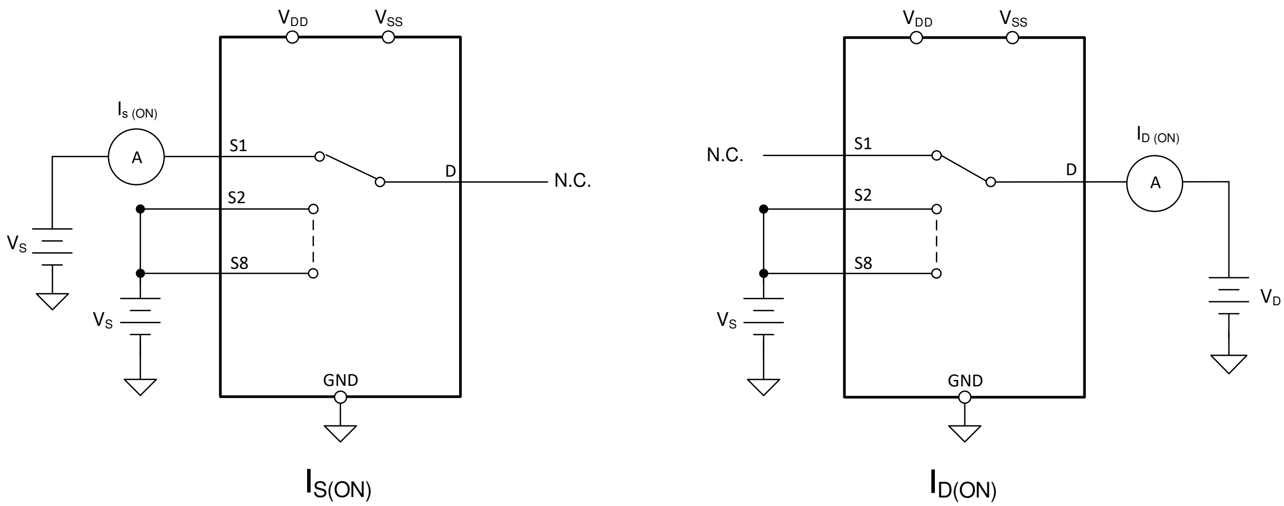


Figure 7-3. On-Leakage Measurement Setup

7.4 Transition Time

Transition time is defined as the time taken by the output of the device to rise or fall 90% after the address signal has risen or fallen past the logic threshold. The 90% transition measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 7-4 shows the setup used to measure transition time, denoted by the symbol $t_{TRANSITION}$.

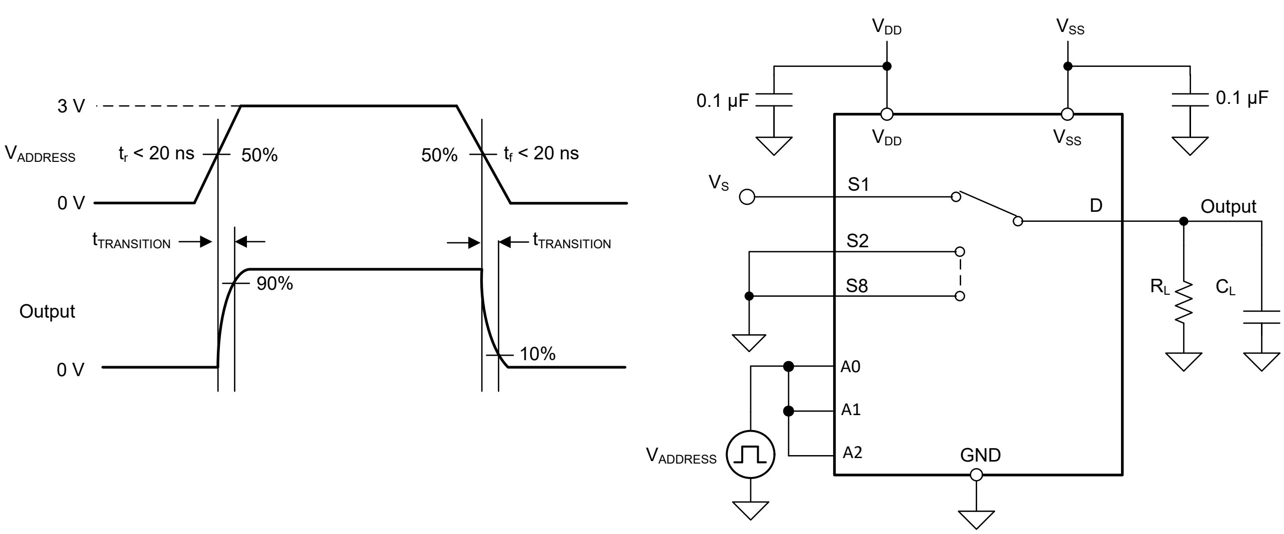


Figure 7-4. Transition-Time Measurement Setup

7.5 $t_{ON(EN)}$ and $t_{OFF(EN)}$

Turn-on time is defined as the time taken by the output of the device to rise to 90% after the enable has risen past the logic threshold. The 90% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 7-5 shows the setup used to measure turn-on time, denoted by the symbol $t_{ON(EN)}$.

Turn-off time is defined as the time taken by the output of the device to fall to 10% after the enable has fallen past the logic threshold. The 10% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 7-5 shows the setup used to measure turn-off time, denoted by the symbol $t_{OFF(EN)}$.

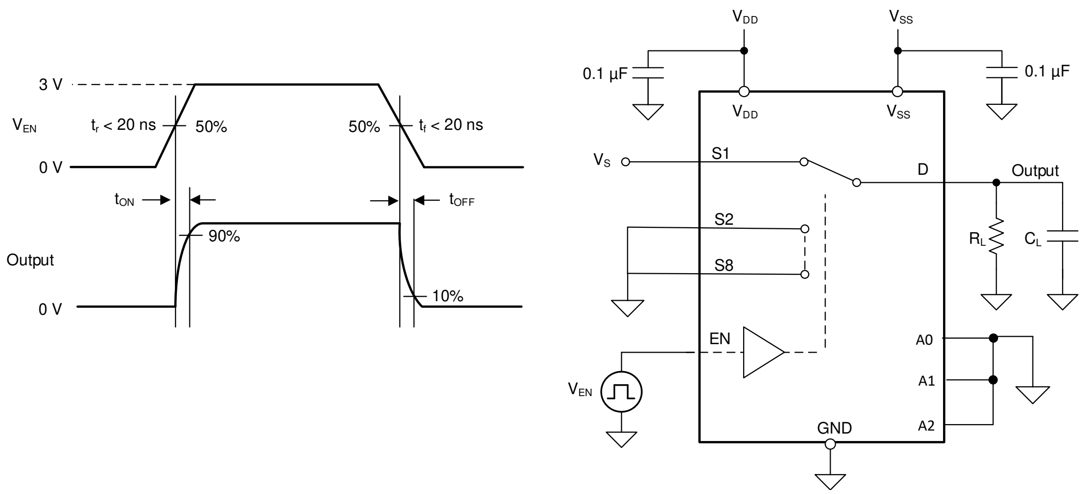


Figure 7-5. Turn-On and Turn-Off Time Measurement Setup

7.6 Break-Before-Make

Break-before-make delay is a safety feature that prevents two inputs from connecting when the device is switching. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. Figure 7-6 shows the setup used to measure break-before-make delay, denoted by the symbol $t_{OPEN(BBM)}$.

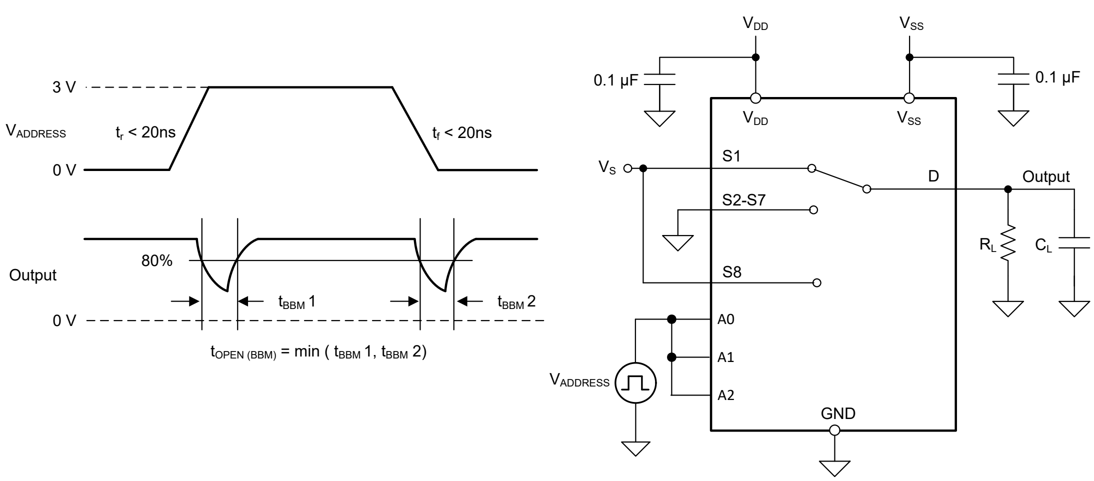


Figure 7-6. Break-Before-Make Delay Measurement Setup

7.7 $t_{ON\ (VDD)}$ Time

The $t_{ON\ (VDD)}$ time is defined as the time taken by the output of the device to rise to 90% after the supply has risen past the supply threshold. The 90% measurement is used to provide the timing of the device turning on in the system. Figure 7-7 shows the setup used to measure turn on time, denoted by the symbol $t_{ON\ (VDD)}$.

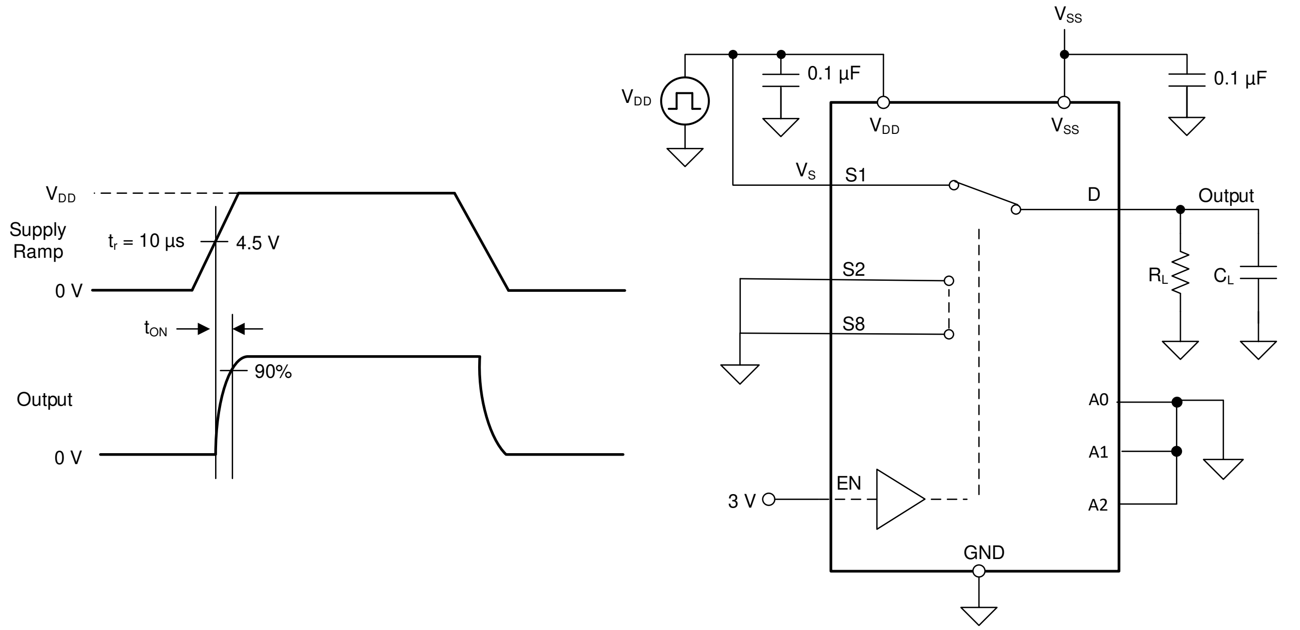


Figure 7-7. $t_{ON\ (VDD)}$ Time Measurement Setup

7.8 Propagation Delay

Propagation delay is defined as the time taken by the output of the device to rise or fall 50% after the input signal has risen or fallen past the 50% threshold. Figure 7-8 shows the setup used to measure propagation delay, denoted by the symbol t_{PD}.

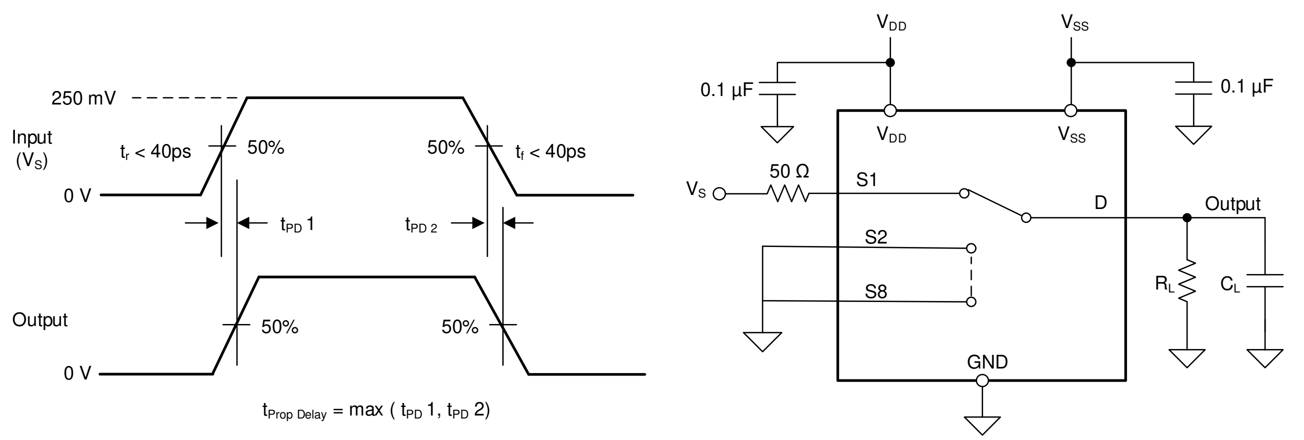


Figure 7-8. Propagation Delay Measurement Setup

7.9 Charge Injection

The TMUX6208 has a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_{INJ}. Figure 7-9 shows the setup used to measure charge injection from source (Sx) to drain (D).

The TMUX6208 and have a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_{INJ}. Figure 7-9 shows the setup used to measure charge injection from source (Sx) to drain (D).

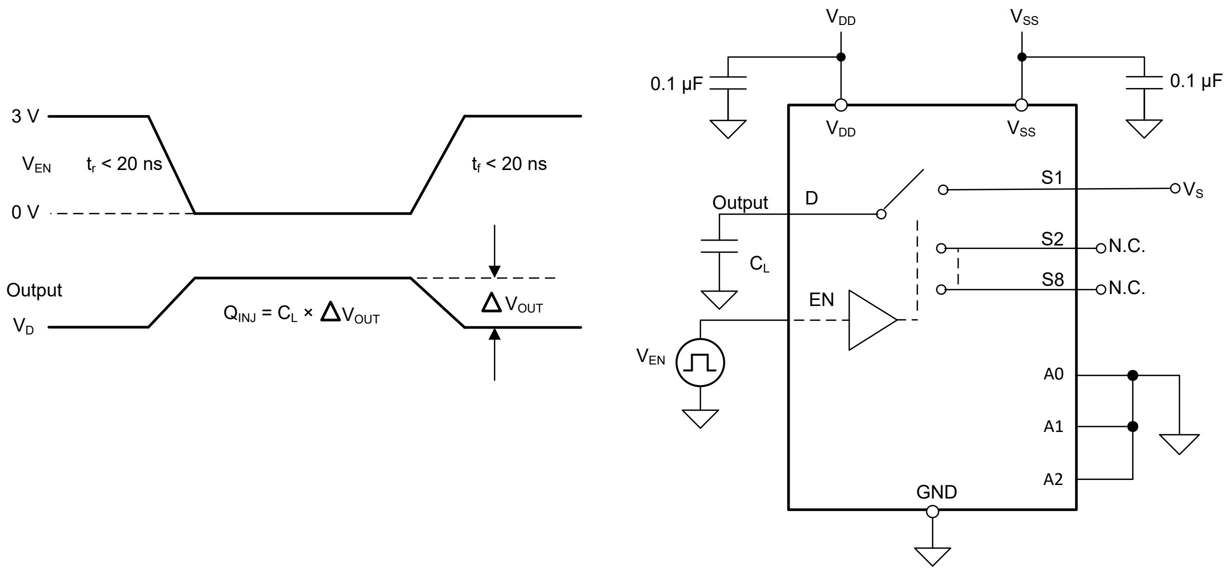
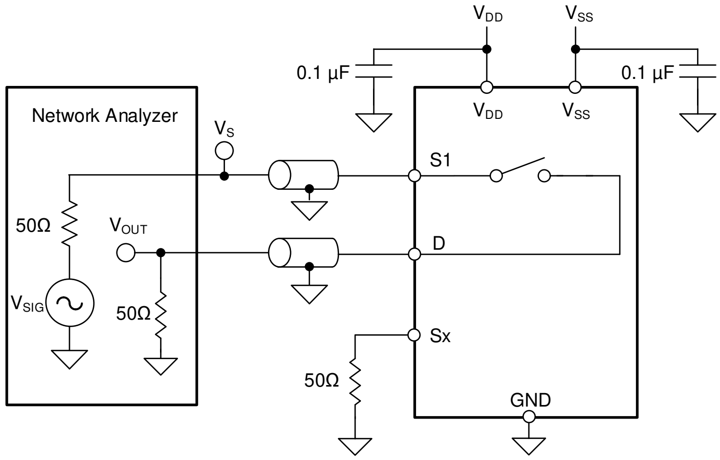


Figure 7-9. Charge-Injection Measurement Setup

7.10 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (D) of the device when a signal is applied to the source pin (Sx) of an off-channel. Figure 7-10 shows the setup used to measure, and the equation used to calculate off isolation.

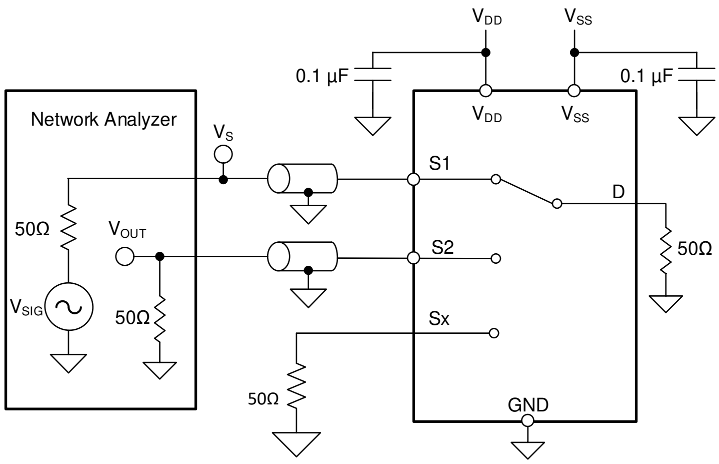


$$Off\ Isolation = 20 \times Log \frac{V_{OUT}}{V_S}$$

Figure 7-10. Off Isolation Measurement Setup

7.11 Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (D) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. Figure 7-11 shows the setup used to measure and the equation used to calculate crosstalk.

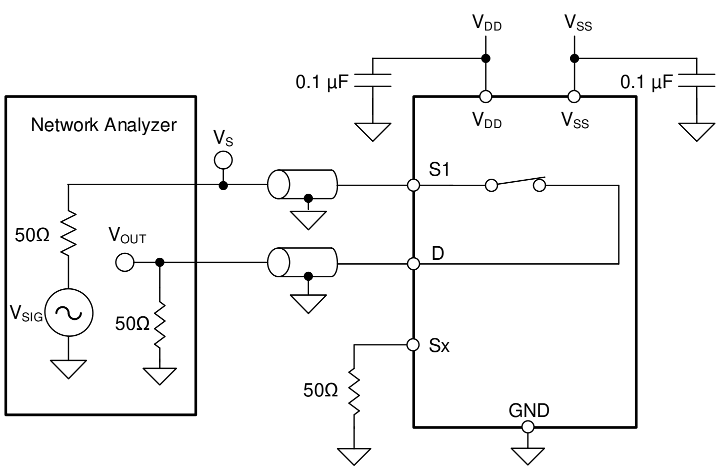


$$Crosstalk = 20 \times Log\frac{V_{OUT}}{V_S}$$

Figure 7-11. Crosstalk Measurement Setup

7.12 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D) of the device. Figure 7-12 shows the setup used to measure bandwidth.



$$Bandwidth = 20 \times Log\frac{V_{OUT}}{V_S}$$

Figure 7-12. Bandwidth Measurement Setup

7.13 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output. The on-resistance of the device varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD.

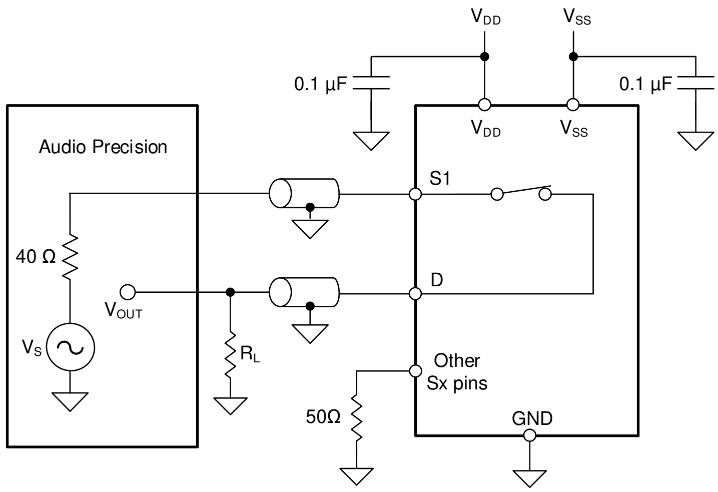
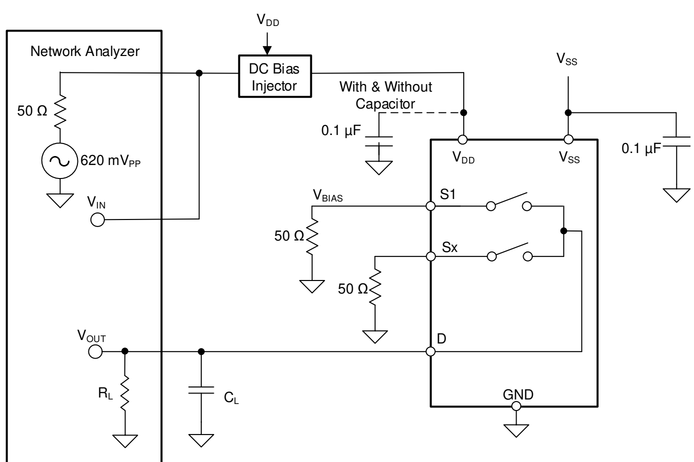


Figure 7-13. THD Measurement Setup

7.14 Power Supply Rejection Ratio (PSRR)

PSRR measures the ability of a device to prevent noise and spurious signals that appear on the supply voltage pin from coupling to the output of the switch. The DC voltage on the device supply is modulated by a sine wave of 620mVPP. The ratio of the amplitude of signal on the output to the amplitude of the modulated signal is the ACPSRR. A high ratio represents a high degree of tolerance to supply rail variation.

The below shows how the decoupling capacitors reduce high frequency noise on the supply pins. This helps stabilize the supply and immediately filter as much of the supply noise as possible.



$$PSRR = 20 \times Log \frac{V_{OUT}}{V_{IN}}$$

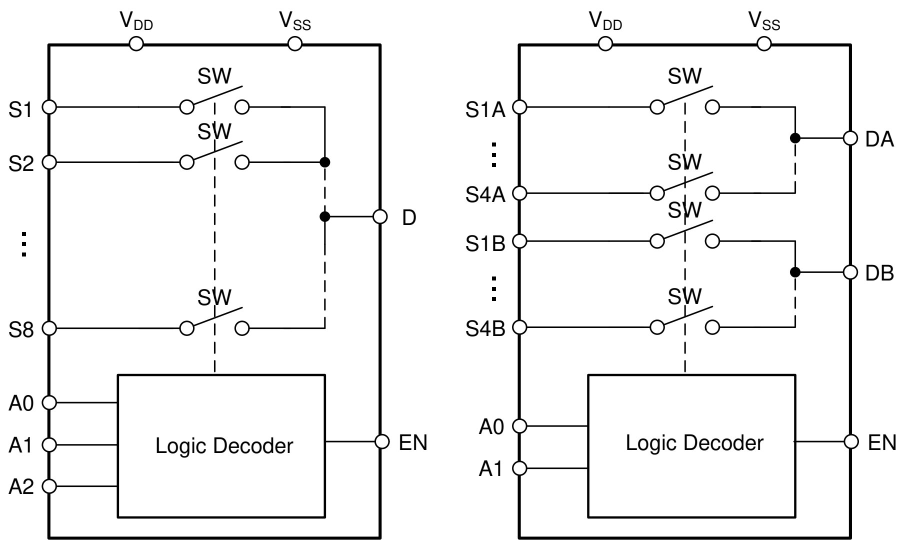
Figure 7-14. ACPSRR Measurement Setup

8 Detailed Description

8.1 Overview

The TMUX6208 is an 8:1, 1-channel multiplexer and the TMUX6209 is a 4:1, 2 channel multiplexer. Each input is turned on or turned off based on the state of the address lines and enable pin.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Bidirectional Operation

The TMUX6208 and TMUX6209 conduct equally well from source (Sx) to drain (D) or from drain (D) to source (Sx). Each channel has very similar characteristics in both directions and supports both analog and digital signals.

8.3.2 Rail-to-Rail Operation

The valid signal path input or output voltage for TMUX6208 and TMUX6209 ranges from V_{SS} to V_{DD}.

8.3.3 1.8 V Logic Compatible Inputs

TMUX6208 and TMUX6209 support 1.8-V logic compatible control for all logic control inputs. 1.8-V logic level inputs allows the to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. For more information on 1.8 V logic implementations refer to *Simplifying Design with 1.8 V logic Muxes and Switches*.

8.3.4 Integrated Pull-Down Resistor on Logic Pins

The TMUX620x has internal weak pull-down resistors to GND to ensure the logic pins are not left floating. The value of this pull-down resistor is approximatly 4 MΩ, but is clamped to about 1 µA at higher voltages. This feature integrates up to four external components and reduces system size and cost.

8.3.5 Fail-Safe Logic

TMUX6208 and TMUX6209 support Fail-Safe Logic on the control input pins (EN and Ax) allowing it to operate up to 36 V, regardless of the state of the supply pins. This feature allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the TMUX6208 and TMUX6209 logic input pins to ramp up to +36 V while V_{DD}

and V_{SS} = 0 V. The logic control inputs are protected against positive faults of up to +36 V in powered-off condition, but do not offer protection against negative overvoltage conditions.

8.3.6 Latch-Up Immune

Latch-Up is a condition where a low impedance path is created between a supply pin and ground. This condition is caused by a trigger (current injection or overvoltage), but once activated, the low impedance path remains even after the trigger is no longer present. This low impedance path may cause system upset or catastrophic damage due to excessive current levels. The Latch-Up condition typically requires a power cycle to eliminate the low impedance path.

The TMUX62xx family of devices are constructed on Silicon on Insulator (SOI) based process where an oxide layer is added between the PMOS and NMOS transistor of each CMOS switch to prevent parasitic structures from forming. The oxide layer is also known as an insulating trench and prevents triggering of latch up events due to overvoltage or current injections. The latch-up immunity feature allows the TMUX62xx family of switches and multiplexers to be used in harsh environments. For more information on latch-up immunity refer to *Using Latch Up Immune Multiplexers to Help Improve System Reliability*.

8.3.7 Ultra-Low Charge Injection

Figure 8-1 shows that the TMUX620x have a transmission gate topology. Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed.

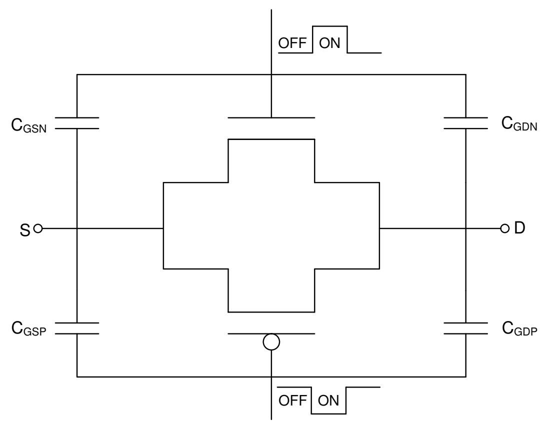


Figure 8-1. Transmission Gate Topology

The TMUX620x contain specialized architecture to reduce charge injection on the Drain (D). To further reduce charge injection in a sensitive application, a compensation capacitor (Cp) can be added on the Source (Sx). This will ensure that excess charge from the switch transition will be pushed into the compensation capacitor on the Source (Sx) instead of the Drain (D). As a general rule of thumb, Cp should be 20x larger than the equivalent load capacitance on the Drain (D). Figure 8-2 shows charge injection variation with different compensation capacitors on the Source side. This plot was captured on the TMUX6219 as part of the TMUX62xx family with a 100pF load capacitance.

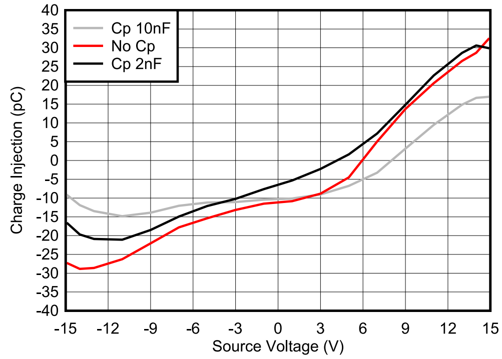


Figure 8-2. Charge Injection Compesation

8.4 Device Functional Modes

When the EN pin of the TMUX6208 is pulled high, one of the switches is closed based on the state of the Ax pin. Similarly, when the EN pin of the TMUX6209 is pulled high, two of the switches are closed based on the state of the address lines. When the EN pin is pulled low, all of the switches are in an open state regardless of the state of the Ax pin. The control pins can be as high as 36V.

The TMUX6208 and TMUX6209 can be operated without any external components except for the supply decoupling capacitors. The EN and Ax pins have internal pull-down resistors of 4 MΩ. If unused, Ax and EN pins must be tied to GND in order to ensure the device does not consume additional current as highlighted in Implications of Slow or Floating CMOS Inputs. Unused signal path inputs (Sx or D) should be connected to GND.

8.5 Truth Tables

Table 8-1 shows the truth tables for the TMUX6208.

Table 8-1. TMUX6208 Truth Table

EN	A2	A1	A0	Selected Source Connected To Drain (D) Pin
0	X[(1)]	X	X	All sources are off (HI-Z)
1	0	0	0	S1
1	0	0	1	S2
1	0	1	0	S3
1	0	1	1	S4
1	1	0	0	S5
1	1	0	1	S6
1	1	1	0	S7
1	1	1	1	S8

(1) X denotes *do not care*.

Table 8-2 show the truth tables for the TMUX6209.

Table 8-2. TMUX6209 Truth Table

EN	A1	A0	Selected Source Connected To Drain (D) Pin
0	X[(1)]	X	All sources are off (HI-Z)
1	0	0	S1x
1	0	1	S2x
1	1	0	S3x
1	1	1	S4x

(1) X denotes *do not care*.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TMUX6208 and TMUX6209 are part of the precision switches and multiplexers family of devices. These devices operate with dual supplies (±4.5 V to ±18 V), a single supply (4.5 V to 36 V), or asymmetric supplies (such as VDD = 12 V, VSS = –5 V), and offer true rail-to-rail input and output. The TMUX6208 and TMUX6209 offer low RON, low on and off leakage currents and ultra-low charge injection performance. These features make the TMUX62xx a family of precision, robust, high-performance analog multiplexers for high-voltage, industrial applications.

9.2 Typical Application

One example to take advantage of TMUX6208 performance is the implementation of multiplexed data aquisition front end for multiple input sensors. Applications such as analog input modules for programmable logic controllers (PLCs), data aquisition (DAQ), and seminconducter test systems commonly need to monitor multiple signals into a single ADC channel. The multiple inputs can come from different system voltages being montitored, or environemental sensors such as temperature or humidity. Figure 9-1 shows a simplified example of monitoring multiple inputs into a single ADC using a multiplexer.

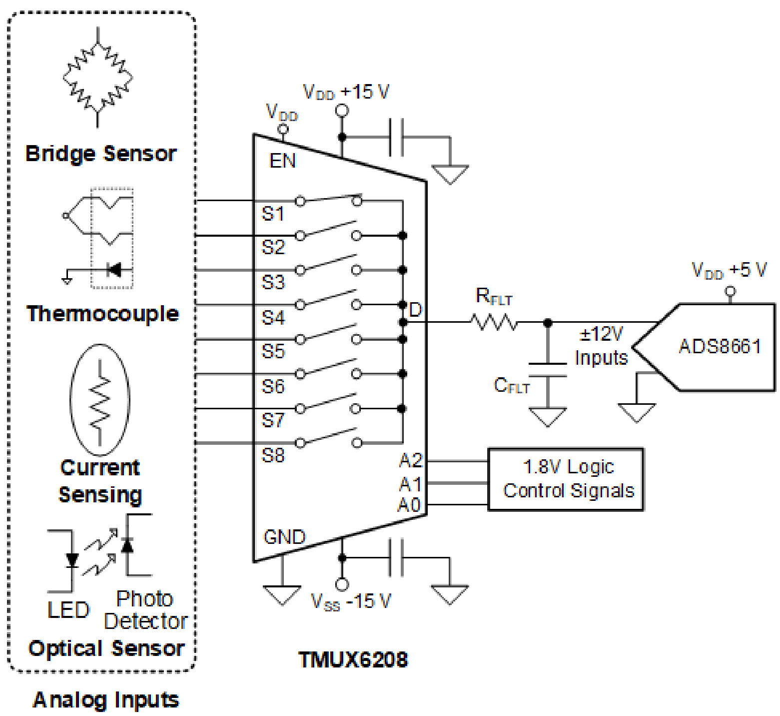


Figure 9-1. Multiplexed Data Aqcuisition Front End

9.2.1 Design Requirements

Table 9-1. Design Parameters

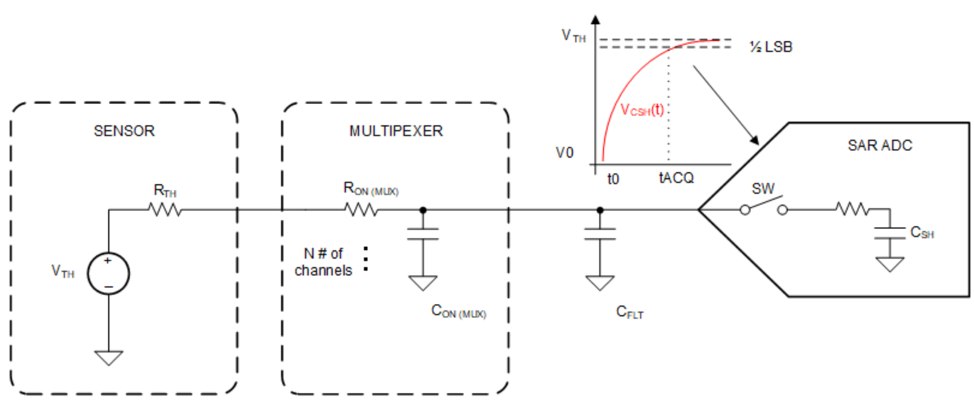
PARAMETER	VALUE
Positive supply (VDD)	+15 V
Negative supply (V_{SS})	-15 V
Input / output signal range	-12 V to 12 V (limit of ADC)
Control logic thresholds	1.8 V compatible
Temperature range	-40°C to +125°C

9.2.2 Detailed Design Procedure

The application shown in Figure 9-1 demonstrates how a multiplexer can be used to simplfy the signal chain and monitor multiple input signals to a single ADC channel. In this example the ADC (ADS8661) has software programmable input ranges up to ±12.288 V. The ADC also has overvotlage protection up to ±20 V which allows for the multiplexer to be powered with wider supply voltages than the input signal range to maximize on-resistance performance of the multiplxer, while still maintaining system level overvotlage protection beyond the usuable signal range. Both the multiplexer and the ADC are capable of operation in extended industrial temperature range of -40°C to +125°C allowing for use in a wider array of industrial systems.

Many SAR ADCs have an analog input structure that consists of a sampling switch and a sampling capacitor. Many signal chains will have a driver amplifier to help charge the input of the ADC to meet a fast system aquisition time. However a driver amplifier is not always needed to drive SAR ADCs. Figure 9-2 shows a typical diagram of a sensor driving the SAR ADC input directly after being passed through the multiplxer. A filter capacitor (C_{FLT}) is connected to the input of the ADC to reduce the sampling charge injection and provides a charge bucket to quickly charge the internal sample-and-hold capacitor of the ADC.

The sensor block simplifies the device into a Thevenin equivalant voltage source (V_{TH}) and resistance (R_{TH}) which can be extracted from the device datasheets. Similarly the multixplexer can be thought of as a series resistance ($R_{ON(MUX)}$) and capacitance ($C_{ON(MUX)}$). To ensure maximum precison of the signal chain the system should be able to settle within 1/2 of an LSB within the acquisition time of the ADC. Figure 9-2 shows the time constant can be calculated. This equation highlights the importance of selecting a multiplexer with low on-resistance to further reduce the system time constant. Additionaly low charge injection performance of the multiplexer is helpful to reduce conversion errors and improve accuracy of the measurements.



$t_{ACQ} > k \times \tau_{FLT}$

- $\tau_{FLT} = (R_{TH} + R_{ON\,(MUX)}) \times (C_{FLT} + C_{ON\,(MUX)})$
- k is single pole time constant for N bit ADC

Figure 9-2. Driving SAR ADC

9.2.3 Application Curve

The low on and off leakage currents of TMUX620x and ultra-low charge injection performance make this device ideal for implementing high precision industrial systems. Figure 9-3 shows the plot for the charge injection versus source voltage for the TMUX6208.

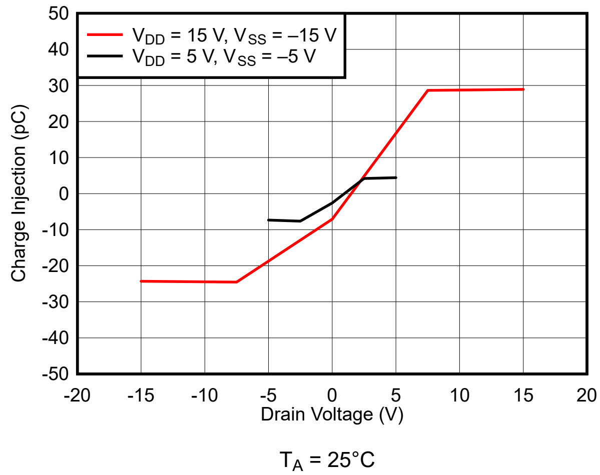


Figure 9-3. Charge Injection vs Drain Voltage

9.3 Power Supply Recommendations

The TMUX6208 and TMUX6209 operate across a wide supply range of of ±4.5 V to ±18 V (4.5 V to 36 V in single-supply mode). The device also perform well with asymmetrical supplies such as V_{DD} = 12 V and V_{SS} = –5 V.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the supply rails to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 µF to 10 µF at both the V_{DD} and V_{SS} pins to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground and power planes. Always ensure the ground (GND) connection is established before supplies are ramped.

9.4 Layout

9.4.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 9-4 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

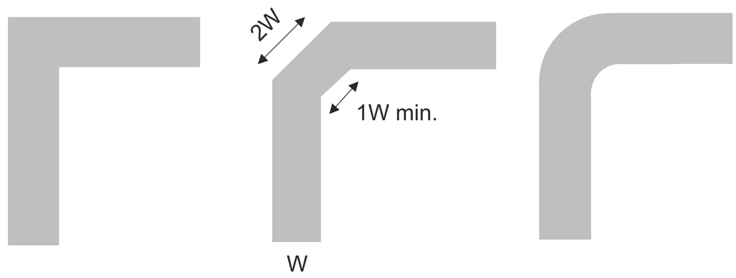


Figure 9-4. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Figure 9-5 and Figure 9-6 illustrate an example of a PCB layout with the TMUX6208. Some key considerations are:

- For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between VDD/VSS and GND. We recommend a 0.1 µF and 1 µF capacitor, placing the lowest value capacitor as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the supply voltage.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.
- Using multiple vias in parallel will lower the overall inductance and is beneficial for connection to ground planes.

9.4.2 Layout Example

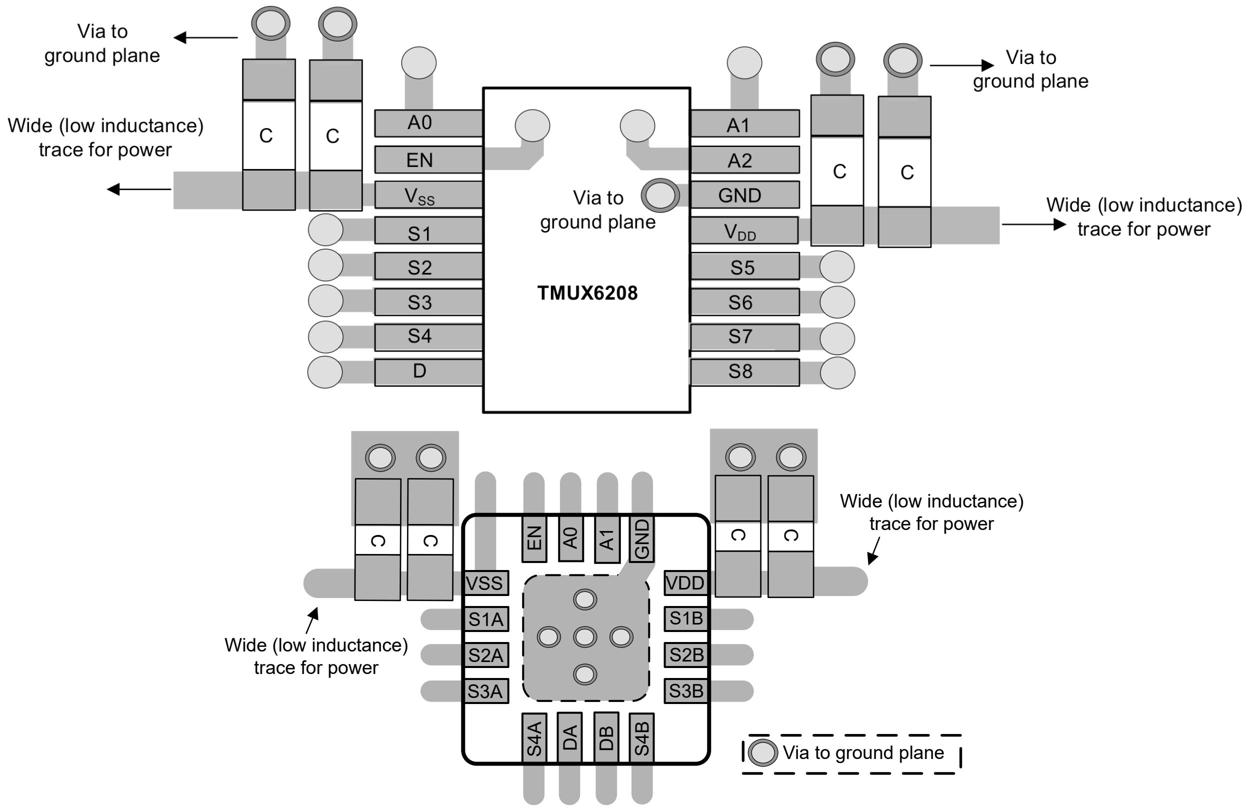


Figure 9-5. TMUX6208 Layout Example

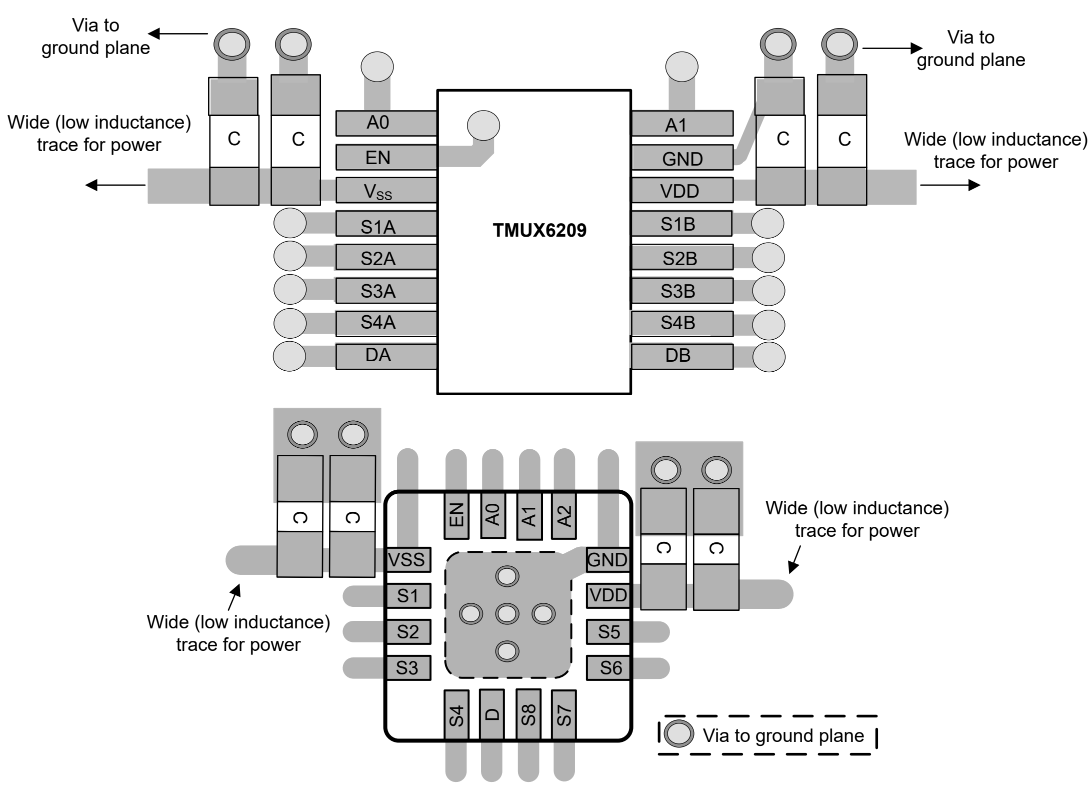


Figure 9-6. TMUX6209 Layout Example

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

- Texas Instruments, *Improve Stability Issues with Low CON Multiplexers* application brief.
- Texas Instruments, *Improving Signal Measurement Accuracy in Automated Test Equipment* application brief
- Texas Instruments, *Sample & Hold Glitch Reduction for Precision Outputs Reference Design* reference guide.
- Texas Instruments, *Simplifying Design with 1.8 V logic Muxes and Switches* application brief.
- Texas Instruments, *System-Level Protection for High-Voltage Analog Multiplexers* application reports.
- Texas Instruments, *True Differential, 4 x 2 MUX, Analog Front End, Simultaneous-Sampling ADC Circuit* application reports.
- Texas Instruments, *QFN/SON PCB Attachment* application reports.
- Texas Instruments, *Quad Flatpack No-Lead Logic Packages* application reports.
- Texas Instruments, *Using Latch Up Immune Multiplexers to Help Improve System Reliability* application reports.

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (January 2022) to Revision E (July 2024)	Page
• Updated HBM ESD for all packages	5
• Updated IIH max specification	7

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMUX6208PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	X208
TMUX6208PWR.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	X208
TMUX6208RUMR	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMUX X208
TMUX6208RUMR.B	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMUX X208
TMUX6209PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	X209
TMUX6209PWR.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	X209
TMUX6209RUMR	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMUX X209
TMUX6209RUMR.B	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMUX X209
TMUX6209RUMRG4	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMUX X209
TMUX6209RUMRG4.B	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMUX X209

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

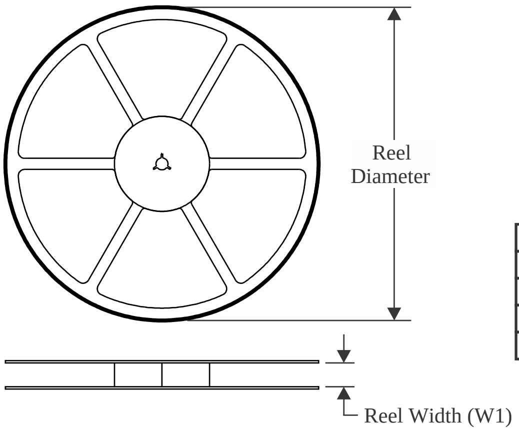
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

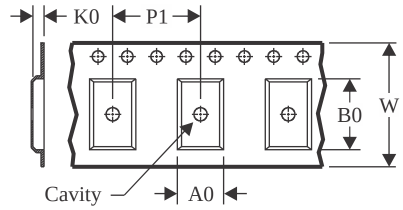
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

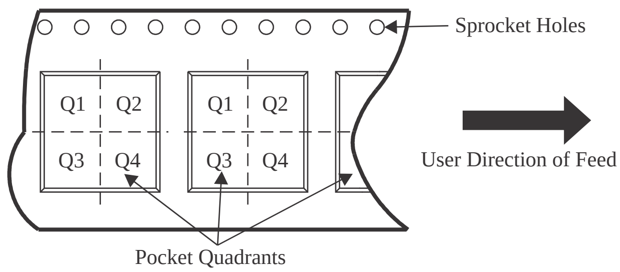


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

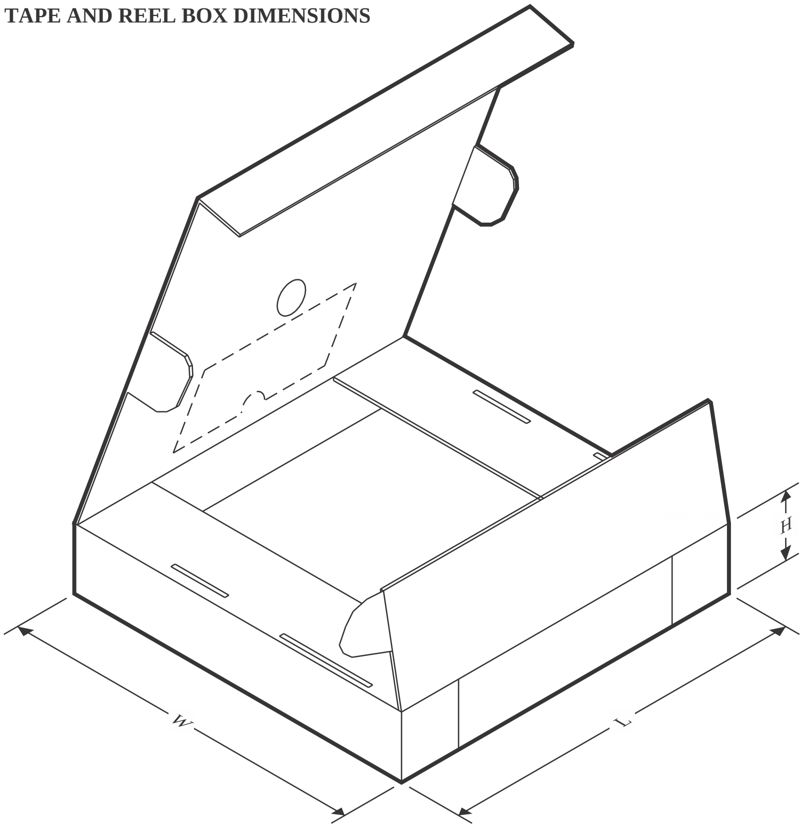
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX6208PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TMUX6208RUMR	WQFN	RUM	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TMUX6209PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TMUX6209RUMR	WQFN	RUM	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TMUX6209RUMRG4	WQFN	RUM	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX6208PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
TMUX6208RUMR	WQFN	RUM	16	3000	367.0	367.0	35.0
TMUX6209PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
TMUX6209RUMR	WQFN	RUM	16	3000	367.0	367.0	35.0
TMUX6209RUMRG4	WQFN	RUM	16	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

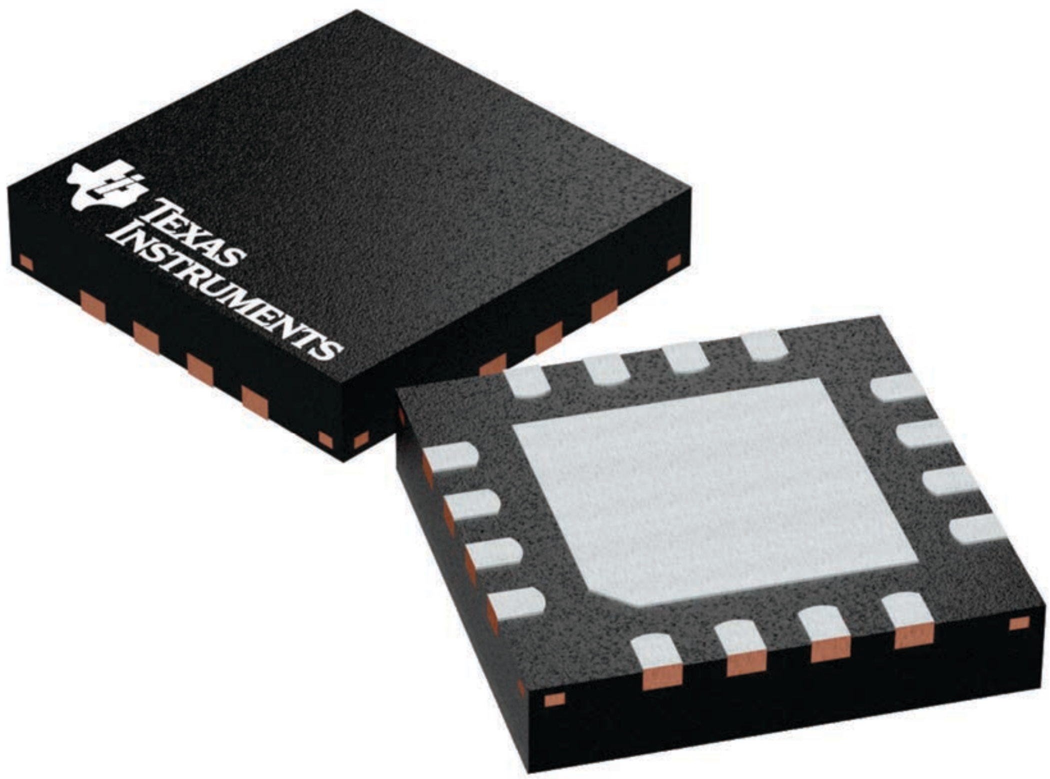
RUM 16

WQFN - 0.8 mm max height

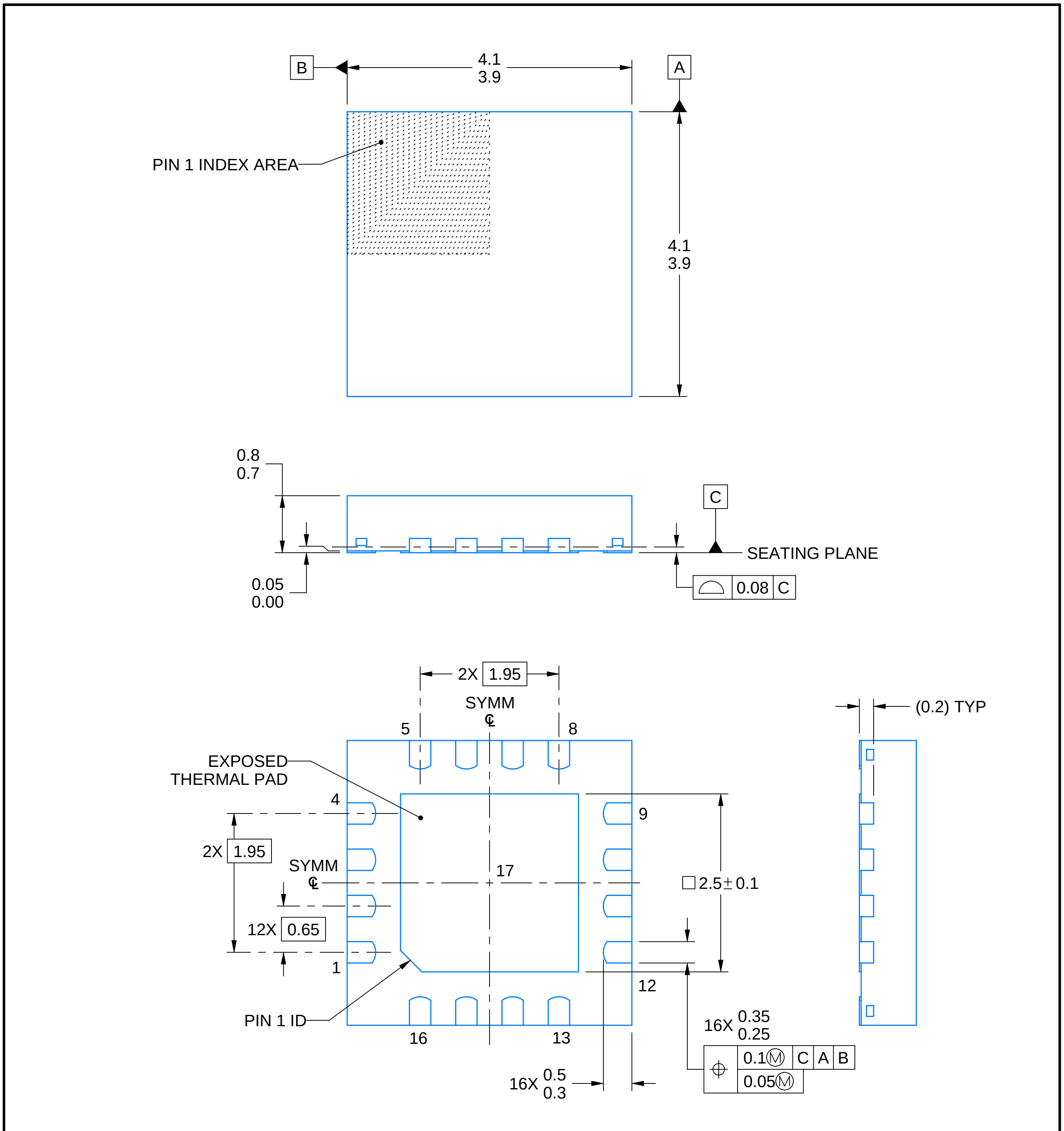
4 x 4, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



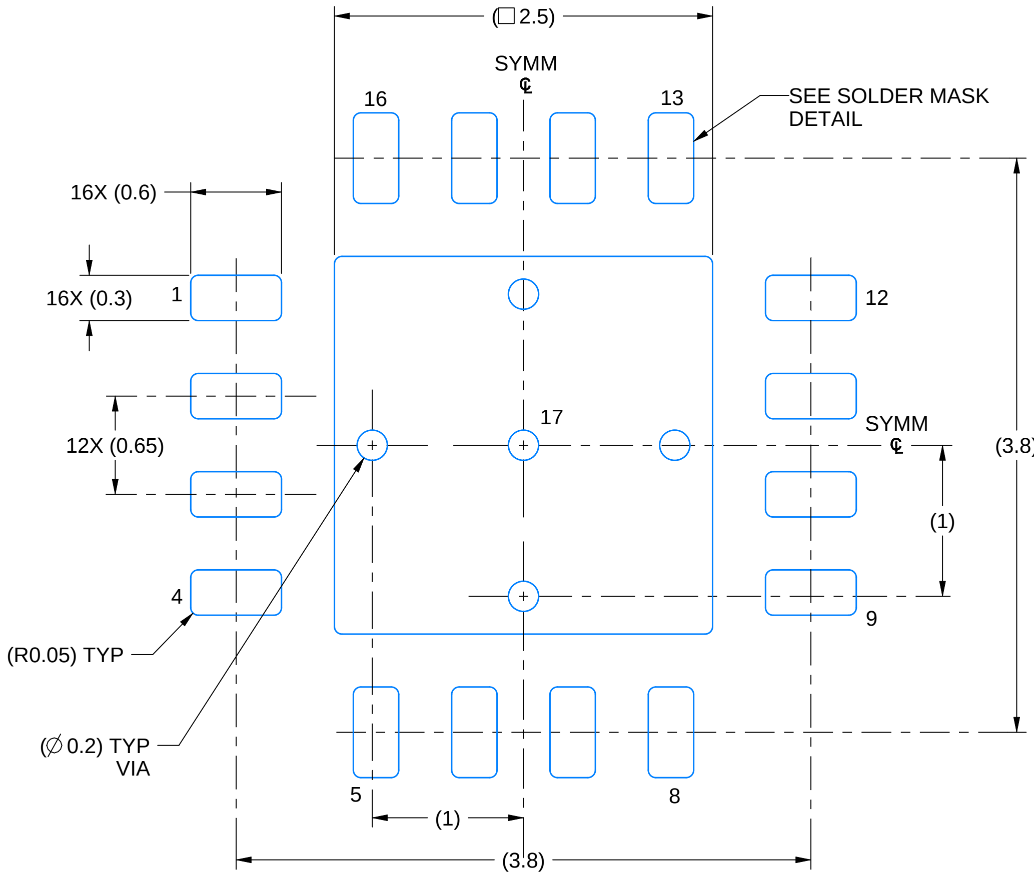
4224843/A



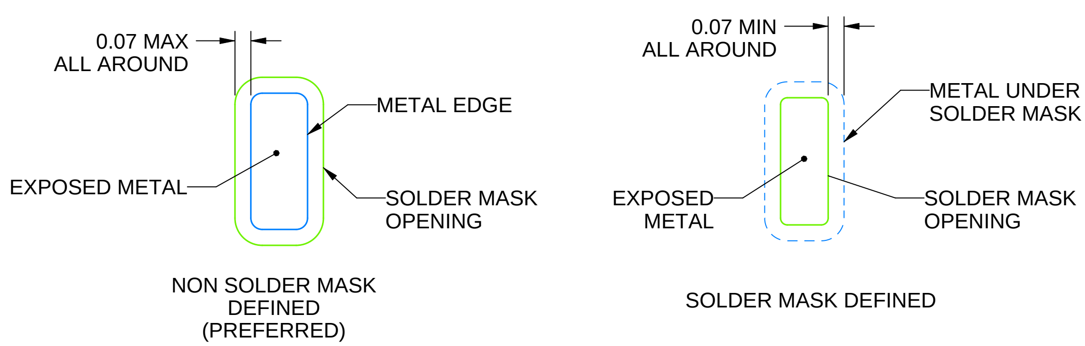
4224815/A 02/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

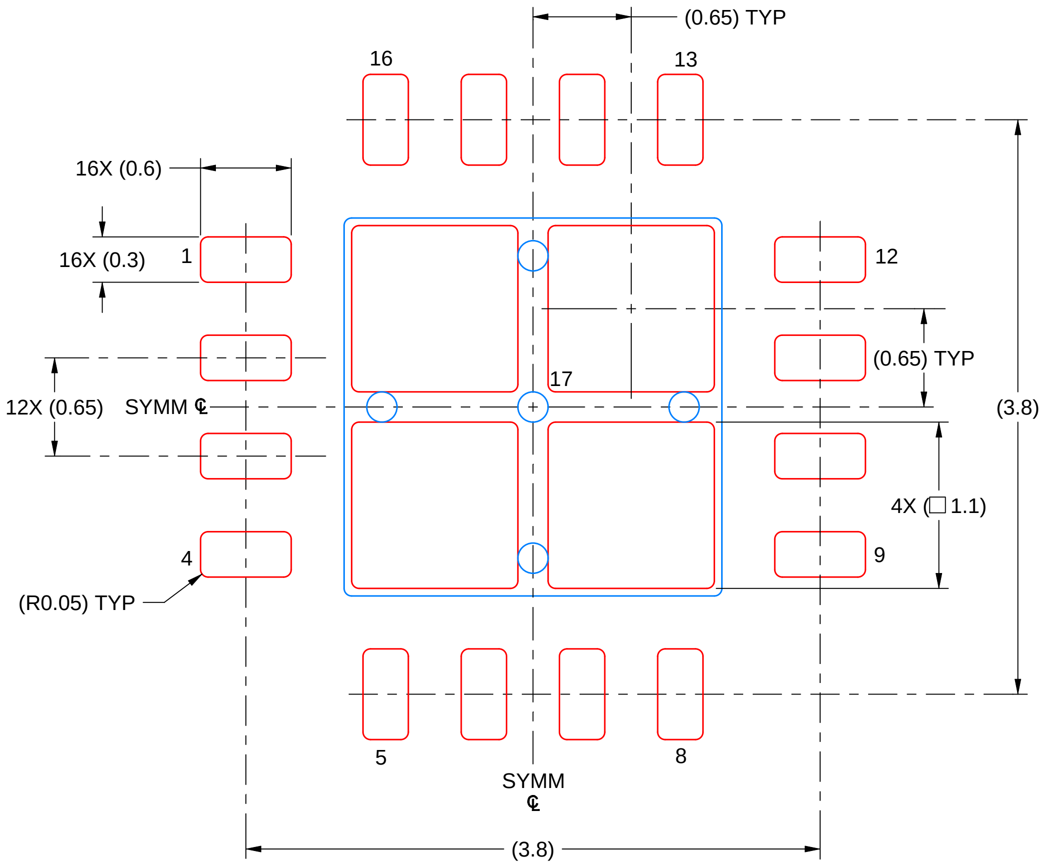


SOLDER MASK DETAILS

4224815/A 02/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



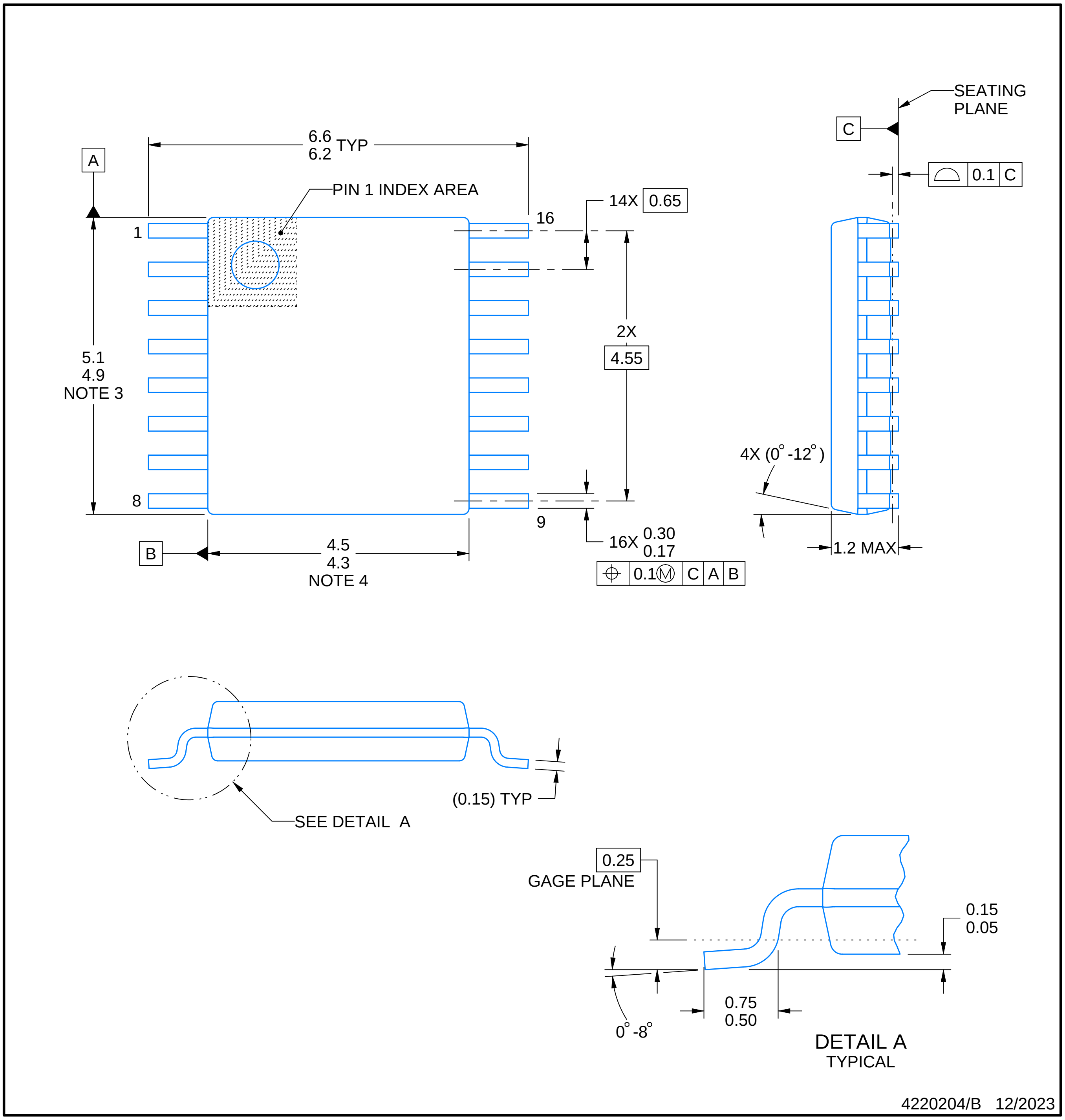
SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4224815/A 02/2019

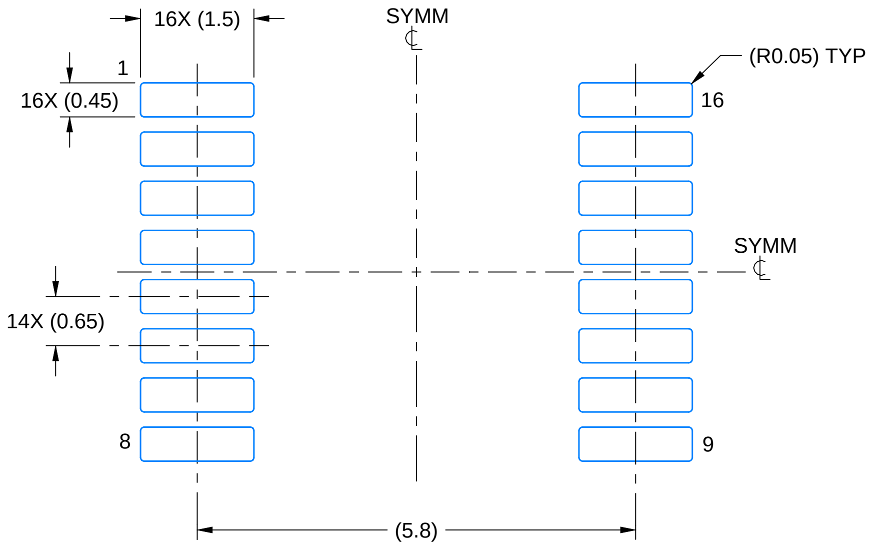
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

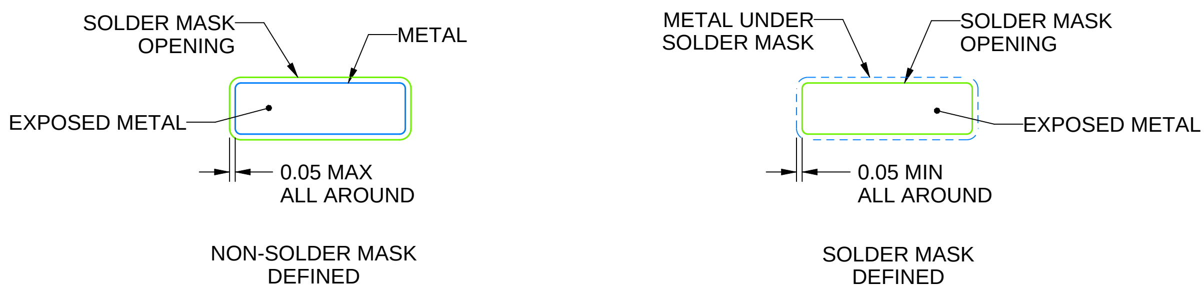


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

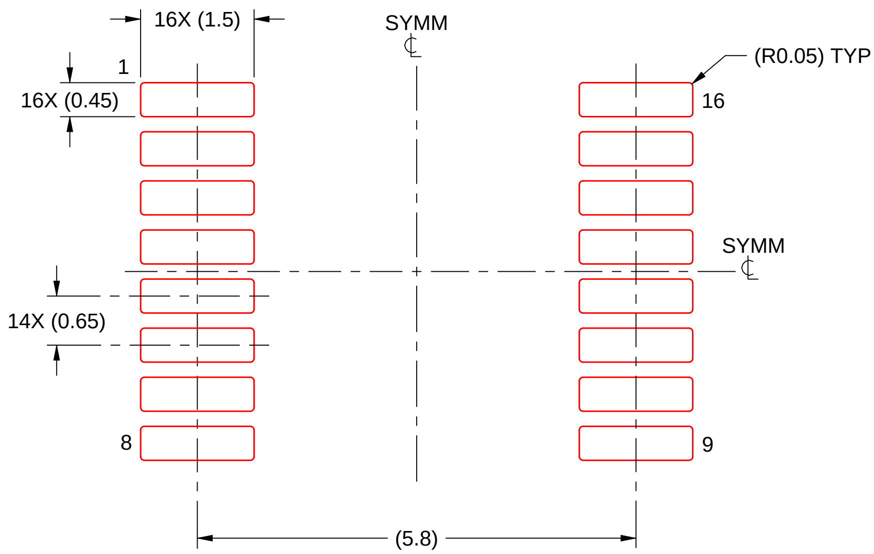


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.