TPL5010 Nano-Power System Timer With Watchdog Function

1 Features

- Supply Voltage From 1.8 V to 5.5 V
- Current Consumption at 2.5 V and 35 nA (Typical)
- Selectable Time Intervals: 100 ms to 7200 s
- Timer Accuracy: 1% (Typical)
- Resistor Selectable Time Interval
- Watchdog Functionality
- Manual Reset

2 Applications

- Battery-Powered Systems
- Internet of Things (IoT)
- Intruder Detection
- Tamper Detection
- Home Automation Sensors
- Thermostats
- Consumer Electronics
- Remote Sensors
- White Goods

3 Description

The TPL5010 Nano Timer is an ultra-low power timer with a watchdog feature designed for system wake up in duty-cycled, battery-powered applications such as those in IoT. Many of these applications require the use of a μC, so it is desirable to keep the μC in a low power mode to maximize current savings, waking up only during certain time intervals to collect data or service an interrupt. Although the internal timer of the μC can be used for system wake-up, it can single-handedly consume microamps of total system current.

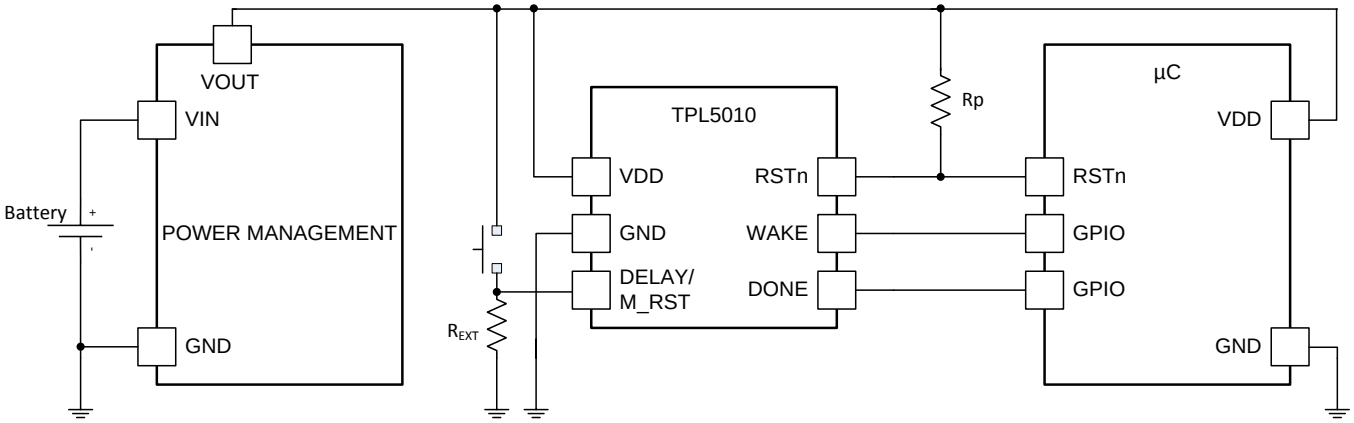
Consuming only 35 nA, the TPL5010 can replace the functionality of the integrated μC timer. This allows the μC to be placed in a much lower power mode, with the internal timer off, returning only to active mode upon an interrupt by the TPL5010. By offering power savings of almost two orders of magnitude, the TPL5010 enables the use of significantly smaller batteries for energy harvesting or wireless sensor applications. The TPL5010 provides selectable timing intervals from 100 ms to 7200 s and is designed for interrupt-driven applications. Some standards (such as EN50271) require implementation of a watchdog for safety and the TPL5010 realizes this watchdog function at almost no additional power consumption. The TPL5010 is available in a 6-pin SOT23 package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPL5010	SOT23 (6)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application Schematic



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4 Revision History

Changes from Original (January 2015) to Revision A **Page**

- Added *TPL5x1x Family of Nano Timers* table ... 3
- Changed T_{ADC} and R_D equations in the *Quantization Error* section ... 14
- Added *Receiving Notification of Documentation Updates* section ... 19

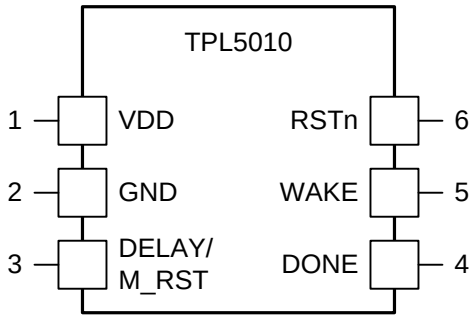
5 Device Comparison Table

TPL5x1x Family of Nano Timers

PART NUMBER	Special Features	Output	Rating
TPL5010	Low Power Timer, Watchdog Functionality	Active High	Catalog
TPL5010Q	Low Power Timer, Watchdog Functionality	Active High	Automotive
TPL5111	Low Power Timer, Power Gating MOS-Driver	Active High	Catalog
TPL5110	Low Power Timer, Power Gating MOS-Driver	Active Low	Catalog

6 Pin Configuration and Functions

DDC Package
6-Lead SOT-23
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION	APPLICATION INFORMATION
NO.	NAME			
1	VDD	P	Supply voltage	
2	GND	G	Ground	
3	DELAY/ M_RST	I	Time Interval set and Manual Reset	Resistance between this pin and GND is used to select the time interval. The reset switch is also connected to this pin.
4	DONE	I	Logic Input for watchdog functionality	Digital signal driven by the µC to indicate successful processing of the WAKE signal.
5	WAKE	O	Timer output signal generated every t_{IP} period.	Digital pulsed signal to wake up the µC at the end of the programmed time interval.
6	RSTn	O	Reset Output (open drain output)	Digital signal to RESET the µC, pullup resistance is required

(1) G= Ground, P= Power, O= Output, I= Input.

7 Specifications

7.1 Absolute Maximum Ratings(1)

	MIN	MAX	UNIT
Supply Voltage (VDD-GND)	–0.3	6	V
Input Voltage at any pin(2)	–0.3	VDD + 0.3	V
Input Current on any pin	–5	+5	mA
Junction Temperature, TJ(3)		150	°C
Storage Temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The voltage between any two pins should not exceed 6V.
(3) The maximum power dissipation is a function of T_J(MAX), θJA, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is PDMAX = (T_J(MAX) - T_A)/ θJA. All numbers apply for packages soldered directly onto a printed-circuit board (PCB).

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human Body Model, per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
	Charged-device model (CDM), per JEDEC specification JESD22-101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Ratings

	MIN	MAX	UNIT
Supply Voltage (VDD-GND)	1.8	5.5	V
Temperature	–40	105	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPL5010 DDC (SOT-23) 6 PINS	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	163	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	26	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	57	°C/W
$ψ_{JT}$	Junction-to-top characterization parameter	7.5	°C/W
$ψ_{JB}$	Junction-to-board characterization parameter	57	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

7.5 Electrical Characteristics(1)

Specifications are for T_A= 25°C, VDD-GND = 2.5 V, unless otherwise stated.

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
POWER SUPPLY							
IDD	Supply current(4)	Operation mode			35	50	nA
		Digital conversion of external resistance (Rext)			200	400	µA
TIMER							
t_{IP}	Time Interval Period	1650 selectable Time Intervals	Minimum time interval		100		ms
			Maximum time interval		7200		s
	Time Interval Setting Accuracy(5)	Excluding the precision of Rext			±0.6%		
	Timer Interval Setting Accuracy over supply voltage	1.8 V ≤ VDD ≤ 5.5 V			±25		ppm/V
t_{OSC}	Oscillator Accuracy			–0.5%		0.5%	
	Oscillator Accuracy over temperature(6)	–40°C ≤ T_A ≤ 105°C			±100	±400	ppm/°C
	Oscillator Accuracy over supply voltage	1.8 V ≤ VDD ≤ 5.5 V			±0.4		%/V
	Oscillator Accuracy over life time(7)				0.24%		
t_{DONE}	DONE Pulse width (6)			100			ns
t_{RSTn}	RSTn Pulse width				320		ms
t_{WAKE}	WAKE Pulse width				20		ms
t_Rext	Time to convert Rext				100	120	ms
DIGITAL LOGIC LEVELS							
VIH	Logic High Threshold DONE pin			0.7 × VDD			V
VIL	Logic Low Threshold DONE pin					0.3 × VDD	V
VOH	Logic output High Level WAKE pin	Iout = 100 µA		VDD – 0.3			V
		Iout = 1 mA		VDD – 0.7			V
VOL	Logic output Low Level WAKE pin	Iout = -100 µA				0.3	V
		Iout = –1 mA				0.7	V
VOL_{RSTn}	RSTn Logic output Low Level	IOL = –1 mA				0.3	V
IOH_{RSTn}	RSTn High Level output current	VOH_{RSTn} = VDD			1		nA
VIH_{M_RST}	Logic High Threshold DELAY/M_RST pin			1.5			V

(1) *Electrical Characteristics* values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. *Absolute Maximum Ratings* indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) Limits are specified by testing, design, or statistical analysis at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(4) The supply current excludes load and pullup resistor current. Input pins are at GND or VDD.
(5) The accuracy for time interval settings below 1 second is ±100 ms.
(6) This parameter is specified by design and/or characterization and is not tested in production.
(7) Operational life time test procedure equivalent to 10 years.

7.6 Timing Requirements

			MIN(1)	NOM(2)	MAX(1)	UNIT
tr_{RSTn}	Rise Time RSTn (3)	Capacitive load 50 pF, Rpullup 100 kΩ		11		µs
tf_{RSTn}	Fall Time RSTn (3)	Capacitive load 50 pF, Rpullup 100 kΩ		50		ns
tr_{WAKE}	Rise Time WAKE (3)	Capacitive load 50 pF		50		ns
tf_{WAKE}	Fall Time WAKE (3)	Capacitive load 50 pF		50		ns
tD_{DONE}	DONE to RSTn or WAKE to DONE delay	Minimum delay(4)		100		ns
		Maximum delay (4)		t_{IP}-20ms		ms
t_{M_RST}	Valid Manual Reset	Observation time 30 ms	20			ms
t_{DB}	De-bounce Manual Reset			20		ms

(1) Limits are specified by testing, design, or statistical analysis at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(3) This parameter is specified by design and/or characterization and is not tested in production.
(4) In case of RSTn from its falling edge, or in case of WAKE from its rising edge.

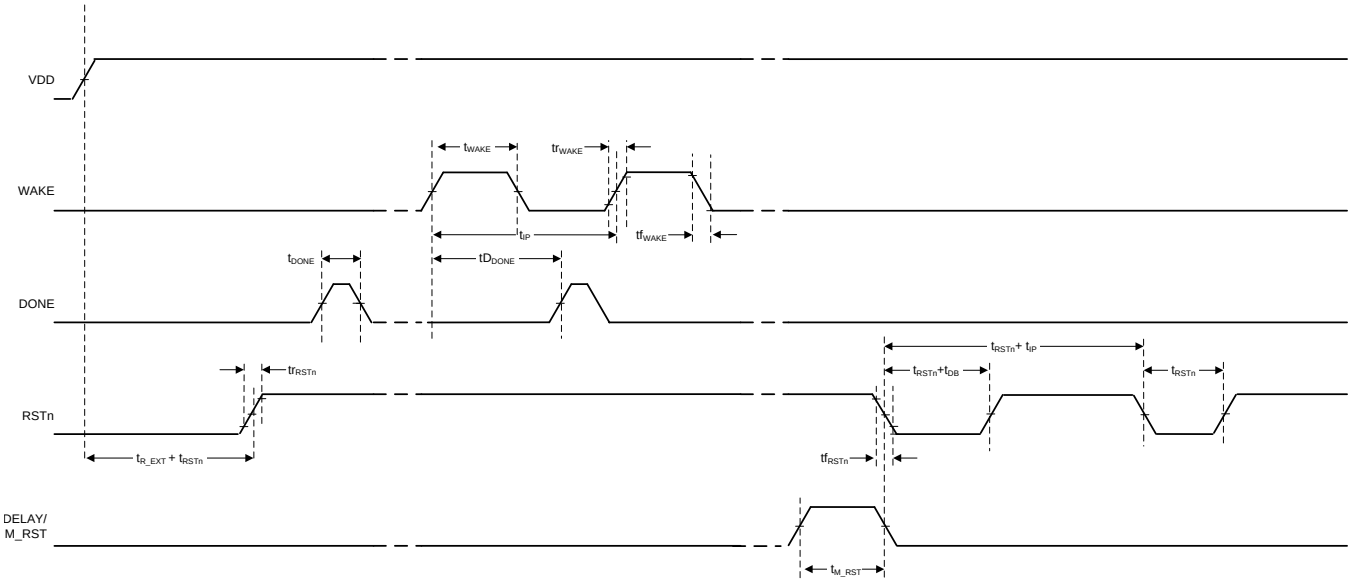


Figure 1. TPL5010 Timing

7.7 Typical Characteristics

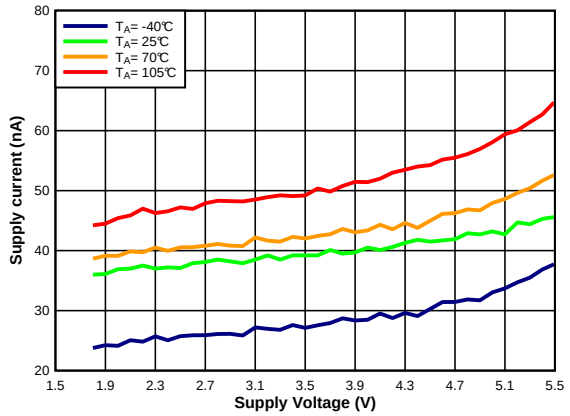


Figure 2. I_{DD} vs. V_{DD}

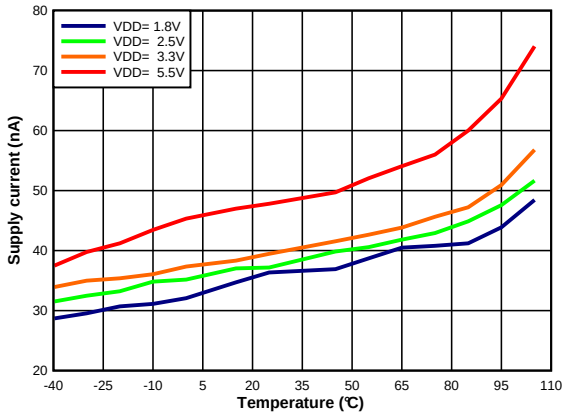


Figure 3. I_{DD} vs. Temperature

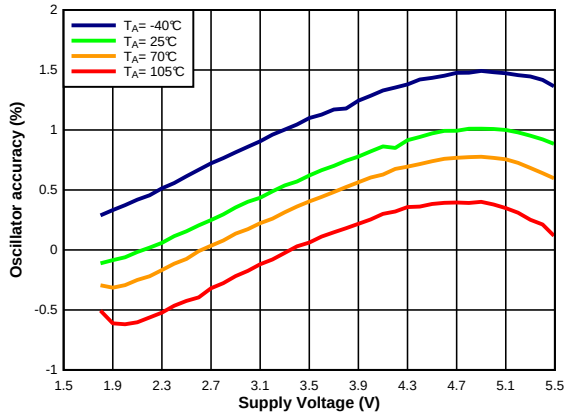


Figure 4. Oscillator Accuracy vs. V_{DD}

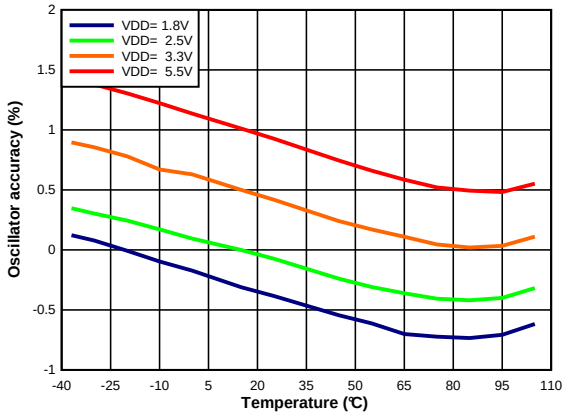


Figure 5. Oscillator Accuracy vs. Temperature

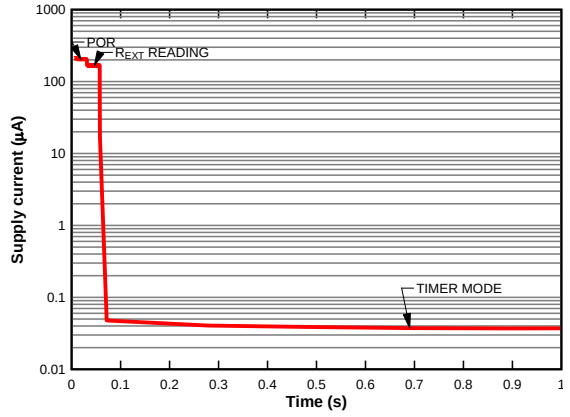
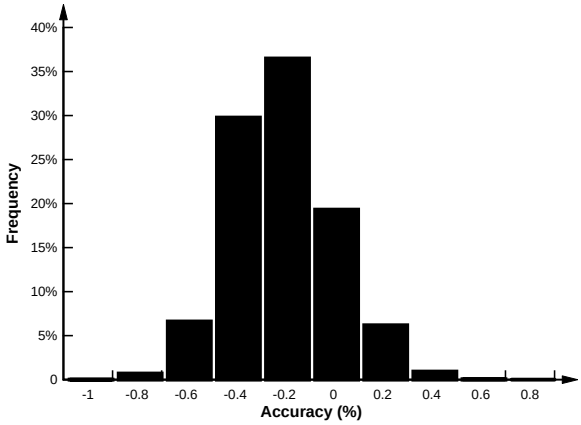


Figure 6. I_{DD} vs. Time



number of observations >20000

1s < t_{IP} ≤ 7200s

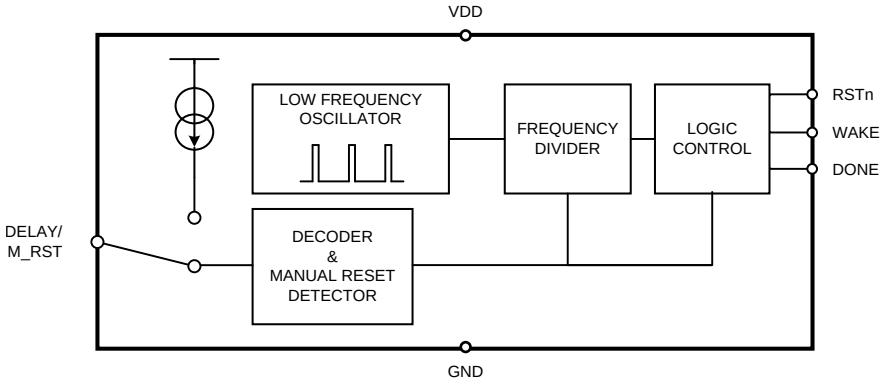
Figure 7. Time Interval Setting Accuracy

8 Detailed Description

8.1 Overview

The TPL5010 is a system wake-up timer with a watchdog feature designed for low-power applications. The TPL5010 can be used in interrupt-driven applications and provides selectable timing from 100 ms to 7200 s.

8.2 Functional Block Diagram



8.3 Feature Description

The DONE, WAKE and RSTn signals are used to implement the watchdog function. The TPL5010 is programmed to issue a periodic WAKE pulse to a µC which is in sleep or standby mode. After receiving the WAKE pulse, the µC must issue a DONE signal to the TPL5010 at least 20 ms before the rising edge of the next WAKE pulse. If the DONE signal is not asserted, the TPL5010 asserts the RSTn signal to reset the µC. A manual reset function is realized by momentarily pulling the DELAY/M_RST pin to VDD.

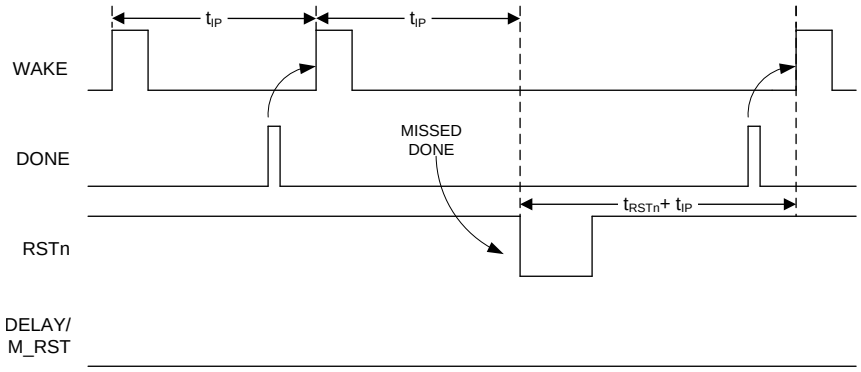


Figure 8. Watchdog

8.3.1 WAKE

The WAKE pulse is sent out from the TPL5010 when the programmed time interval starts (except at the beginning of the first cycle or if in the previous interval the DONE has not been received).

This signal is normally low.

8.3.2 DONE

The DONE pin is driven by a µC to signal successful processing of the WAKE signal. The TPL5010 recognizes a valid DONE signal as a low to high transition. If two or more DONE signals are received within the time interval, only the first DONE signal is processed.

The DONE signal resets the counter of the watchdog only. If the DONE signal is received when the WAKE is still high, the WAKE will go low as soon as the DONE is recognized.

Feature Description (continued)

8.3.3 RSTn

To implement the reset interface between the TPL5010 and the µC a pullup resistance is required. 100 KΩ is recommended to minimize current.

During the POR and the reading of the REXT, the RSTn signal is LOW.

RSTn is asserted (LOW) for either one of the following conditions:

1. If the DELAY/M_RST pin is high for at least two consecutive cycles of the internal oscillator (approximately 20 ms).
2. At the beginning of a new time interval if DONE is not received at least 20 ms before the next WAKE rising edge (see Figure 8).

8.4 Device Functional Modes

8.4.1 Start-Up

During start-up after POR, the TPL5010 executes a one-time measurement of the resistance attached to the DELAY/M_RST pin to determine the desired time interval for WAKE. This measurement interval is t_{R_EXT}. During this measurement, a constant current is temporarily flowing into R_{EXT}.

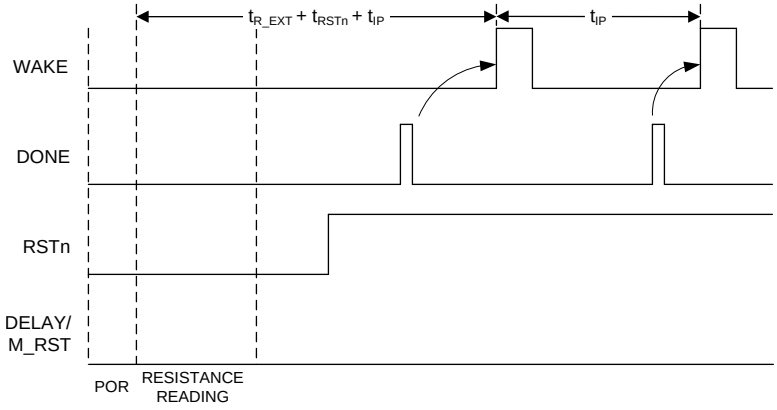


Figure 9. Start-Up

8.4.2 Normal Operating Mode

During normal operating mode, the TPL5010 asserts periodic WAKE pulses in response to valid DONE pulses from the µC. If either a manual reset is applied (logic HIGH on DELAY/M_RST pin), or the µC does not issue a DONE pulse within the required time, the TPL5010 asserts the RSTn signal to the µC and restarts its internal counters. See Figure 8 and Figure 10 .

8.5 Programming

8.5.1 Configuring the WAKE Interval With the DELAY/M_RST Pin

The time interval between two adjacent WAKE pulses (rising edges) is selectable through an external resistance (R_{EXT}) between the DELAY/M_RST pin and ground. The value of the resistance R_{EXT} is converted one time after POR. The allowable range of R_{EXT} is 500 Ω to 170 kΩ. At least a 1% precision resistance is recommended. See section *Timer Interval Selection Using External Resistance* on how to set the WAKE pulse interval using R_{EXT}.

The time between two adjacent RESET signals (falling edges), or between a RESET (falling edge) and a WAKE (rising edge), is given by the sum of the programmed time interval and the t_{RSTn} (reset pulse width).

Programming (continued)

8.5.2 Manual Reset

If VDD is connected to the DELAY/M_RST pin, the TPL5010 recognizes this as a manual reset condition. In this case, the time interval is not set. If the manual reset is asserted during the POR or during the reading procedure, the reading procedure is aborted and is restarted as soon as the manual reset switch is released. A pulse on the DELAY/M_RST pin is recognized as a valid manual reset only if it lasts at least 20 ms (observation time is 30 ms).

A valid manual reset resets all the counters inside the TPL5010. The counters restart only when the high digital voltage at DELAY/M_RST is removed and the next t_{RSTn} is elapsed.

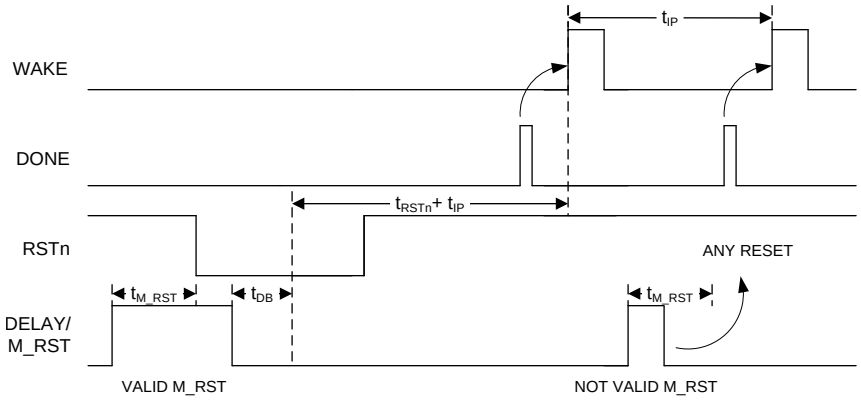


Figure 10. Manual Reset

8.5.2.1 DELAY/M_RST

A resistance in the range between 500 Ω and 170 kΩ needs to be connected to select a valid time interval. At the POR and during the reading of the resistance the DELAY/M_RST is connected to an analog signal chain though a mux. After the reading of the resistance the analog circuit is switched off and the DELAY/RST is connected to a digital circuit.

The manual reset detection is supported with a de-bounce feature which makes the TPL5010 insensitive to the glitches on the DELAY/M_RST pin. When a valid manual reset signal is asserted on the DELAY/M_RST pin, the RSTn signal is asserted LOW after a delay of t_{M_RST}. It remains LOW after a valid manual reset is asserted + t_{DB} + t_{RSTn}. Due to the asynchronous nature of the manual reset signal and its arbitrary duration, the LOW status of the RSTn signal maybe affected by an uncertainty of about ±5 ms.

A valid manual reset puts all the digital output signals at their default values:

- WAKE = LOW
- RSTn = asserted LOW

8.5.2.2 Circuitry

The manual reset may be implemented using a switch (momentary mechanical action). The TPL5010 offers two possible approaches according to the power consumption constraints of the application.

Programming (continued)

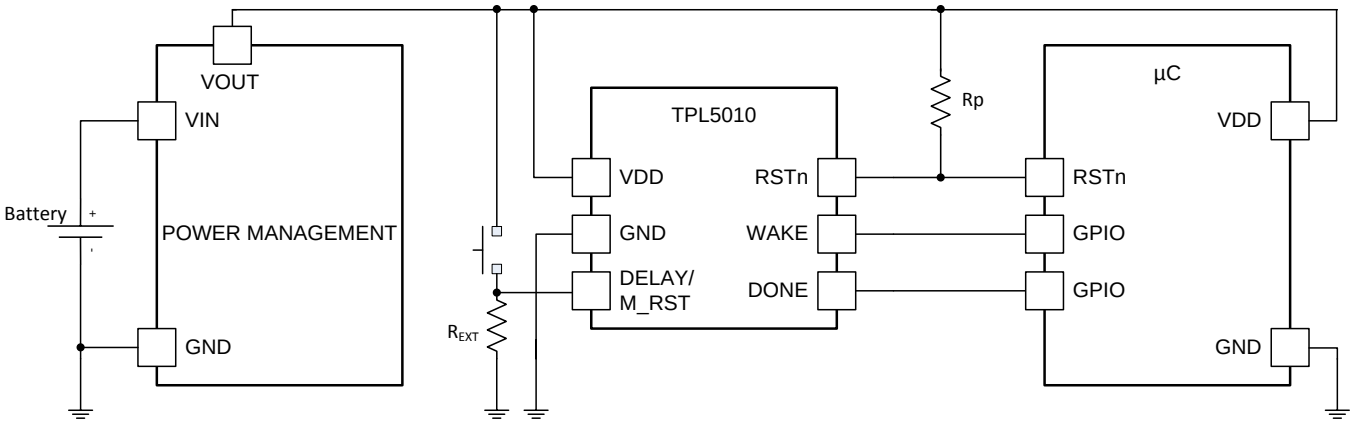


Figure 11. Manual Reset With SPST Switch

For use cases that do not require the lowest power consumption, using a single-pole single-throw switch may offer a lower-cost solution. The DELAY/M_RST pin may be directly connected to VDD with R_{EXT} in the circuit. The current drawn from the supply voltage during the reset is given by VDD/R_{EXT}.

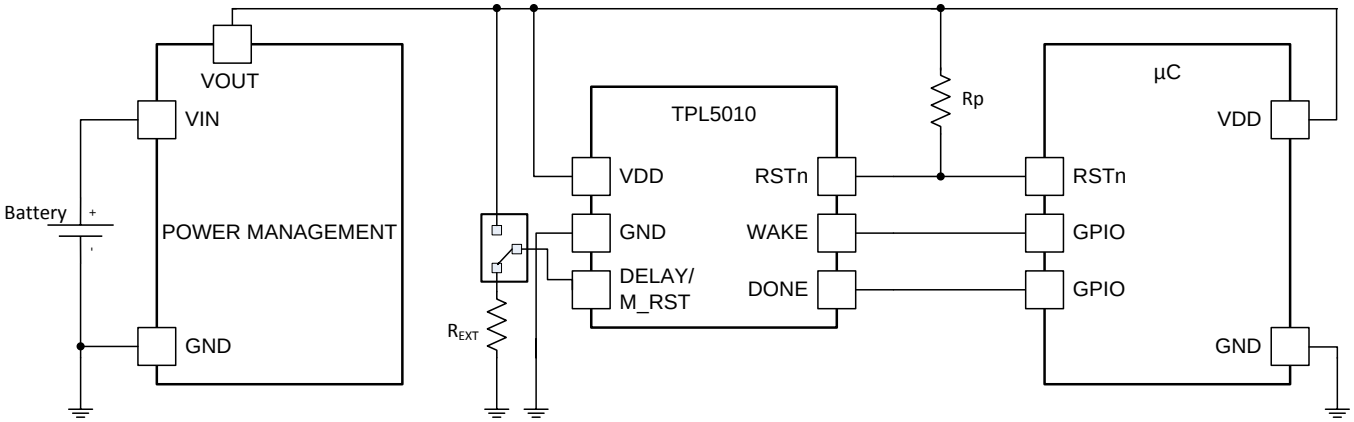


Figure 12. Manual Reset With SPDT Switch

The reset function may also be asserted by switching DELAY/M_RST from R_{EXT} to VDD using a single-pole double-throw switch, which will provide a lower power solution for the manual reset, because no current flows.

8.5.3 Timer Interval Selection Using External Resistance

To set the time interval, the external resistance R_{EXT} is selected according to Equation 1:

$$R_{EXT} = 100 \left(\frac{-b + \sqrt{b^2 - 4a(c - 100\,T)}}{2a} \right) \quad (1)$$

where

- T is the desired time interval in seconds.
- R_{EXT} is the resistance value to use in Ω.
- a, b, and c are coefficients depending on the range of the time interval.

Programming (continued)

Table 1. Coefficients for Equation 1

SET	Time interval Range (s)	a	b	c
1	1 < T ≤ 5	0.2253	–20.7654	570.5679
2	5 < T ≤ 10	–0.1284	46.9861	–2651.8889
3	10 < T ≤ 100	0.1972	–19.3450	692.1201
4	100 < T ≤ 1000	0.2617	–56.2407	5957.7934
5	T > 1000	0.3177	–136.2571	34522.4680

EXAMPLE

Required time interval: 8 s

The coefficient set to be selected is the number 2. The formula becomes Equation 2.

$$R_{EXT}=100\left(\frac{46.9861-\sqrt{46.9861^2+4*0.1284\left(-2561.8889-100*8\right)}}{2*0.1284}\right) \quad (2)$$

The resistance value is 10.18 kΩ.

Table 2 and Table 3 contain example values of t_{IP} and their corresponding value of R_{EXT}.

Table 2. First 9 Time Intervals

t_{IP} (ms)	Resistance (Ω)	Closest Real Value (Ω)	Parallel of Two 1% Tolerance Resistors, (kΩ)
100	500	500	1.0 // 1.0
200	1000	1000	-
300	1500	1500	2.43 // 3.92
400	2000	2000	-
500	2500	2500	4.42 // 5.76
600	3000	3000	5.36 // 6.81
700	3500	3500	4.75 // 13.5
800	4000	4000	6.19 // 11.3
900	4500	4501	6.19 // 16.5

Table 3. Most Common Time Intervals Between 1s to 2h

t_{IP}	Calculated Resistance (kΩ)	Closest Real Value (kΩ)	Parallel of Two 1% Tolerance Resistors, (kΩ)
1s	5.20	5.202	7.15 // 19.1
2s	6.79	6.788	12.4 // 15.0
3s	7.64	7.628	12.7// 19.1
4s	8.30	8.306	14.7 // 19.1
5s	8.85	8.852	16.5 // 19.1
6s	9.27	9.223	18.2 // 18.7
7s	9.71	9.673	19.1 // 19.6
8s	10.18	10.180	11.5 // 8.87
9s	10.68	10.68	17.8 // 26.7
10s	11.20	11.199	15.0 // 44.2
20s	14.41	14.405	16.9 // 97.6
30s	16.78	16.778	32.4 // 34.8
40s	18.75	18.748	22.6 // 110.0
50s	20.047	20.047	28.7 // 66.5

Table 3. Most Common Time Intervals Between 1s to 2h (continued)

t_{IP}	Calculated Resistance (kΩ)	Closest Real Value (kΩ)	Parallel of Two 1% Tolerance Resistors, (kΩ)
1min	22.02	22.021	40.2 // 48.7
2min	29.35	29.349	35.7 // 165.0
3min	34.73	34.729	63.4 // 76.8
4min	39.11	39.097	63.4 // 102.0
5min	42.90	42.887	54.9 // 196.0
6min	46.29	46.301	75.0 // 121.0
7min	49.38	49.392	97.6 // 100.0
8min	52.24	52.224	88.7 // 127.0
9min	54.92	54.902	86.6 // 150.0
10min	57.44	57.437	107.0 // 124.0
20min	77.57	77.579	140.0 // 174.0
30min	92.43	92.233	182.0 // 187.0
40min	104.67	104.625	130.0 // 536.00
50min	115.33	115.331	150.0 // 499.00
1h	124.91	124.856	221.0 // 287.00
1h30min	149.39	149.398	165.0 // 1580.0
2h	170.00	170.00	340.0 // 340.0

8.5.4 Quantization Error

The TPL5010 can generate 1650 discrete timer intervals in the range of 100 ms to 7200 s. The first 9 intervals are multiples of 100 ms. The remaining 1641 intervals cover the range between 1 s to 7200 s. Because they are discrete intervals, there is a quantization error associated with each value.

The quantization error can be evaluated according to Equation 3:

$$Err = 100\frac{\left(T_{DESIRED} - T_{ADC}\right)}{T_{DESIRED}}$$

where

- $T_{ADC} = INT\left[\frac{1}{100}\left(aR_D^2 + bR_D + c\right)\right]$
- $R_D = \frac{R_{EXT}}{100}$ (3)

R_{EXT} is the resistance calculated with Equation 1 and a, b, c are the coefficients of the equation listed in Table 1.

8.5.5 Error Due to Real External Resistance

R_{EXT} is a theoretical value and may not be available in standard commercial resistor values. It is possible to closely approach the theoretical R_{EXT} using two or more standard values in parallel. However, standard values are characterized by a certain tolerance. This tolerance will affect the accuracy of the time interval.

The accuracy can be evaluated using the following procedure:

1. Evaluate the min and max values of R_{EXT} (R_{EXT_MIN}, R_{EXT_MAX} with Equation 1 using the selected commercial resistance values and their tolerances.
2. Evaluate the time intervals ($T_{ADC\_MIN}[R_{EXT\_MIN}]$, $T_{ADC\_MAX}[R_{EXT\_MAX}]$) with the T_{ADC} equation mentioned in Equation 3.
3. Find the errors using Equation 3 with T_{ADC_MIN}, T_{ADC_MAX}.

The results of the formula indicate the accuracy of the time interval.

The example below illustrates the procedure.

- Desired time interval, T_desired = 600 s,
- Required R_{EXT} from Equation 1, R_{EXT}= 57.44 kΩ.

From Table 3 R_{EXT} can be built with a parallel combination of two commercial values with 1% tolerance: R1 = 107 kΩ, R2 = 124 kΩ. The uncertainty of the equivalent parallel resistance can be found using Equation 4:

$$uR_{//} = R_{//}\sqrt{\left(\frac{u_{R1}}{R1}\right)^2 + \left(\frac{u_{R2}}{R2}\right)^2} \quad (4)$$

where

- uRn (n=1,2) represent the uncertainty of a resistance (see Equation 5)

$$u_{Rn} = Rn\frac{Tolerance}{\sqrt{3}} \quad (5)$$

The uncertainty of the parallel resistance is 0.82%, which means the value of R_{EXT} may range between R_{EXT_MIN} = 56.96 kΩ and R_{EXT_MAX} = 57.90 kΩ.

Using these value of R_{EXT}, the digitized timer intervals calculated by T_{ADC} equation mentioned in Equation 3 are respectively T_{ADC_MIN} = 586.85 s and T_{ADC_MAX} = 611.3 s, giving an error range of –1.88% / +2.19%. The asymmetry of the error range is due to the quadratic transfer function of the resistance digitizer.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

In battery-powered applications, one design constraint is the need for low current consumption. The TPL5010 is designed for applications where there is a need to monitor environmental conditions at a fixed time interval. Often in these applications a watchdog or other internal timer in a µC is used to implement a wake-up function. Using the TPL5010 to implement the watchdog function will consume only tens of nA, significantly improving the power consumption of the system.

9.2 Typical Application

The TPL5010 can be used in conjunction with environment sensors to build a low-power environment data-logger, such as an air quality data-logger. In this application, due to the monitored phenomena, the µC and the front end of the sensor spend most of the time in the idle state, waiting for the next logging interval, usually a few hundred of milliseconds. Figure 13 shows a data logging application based on a µC and a front end for a gas sensor based on the LMP91000.

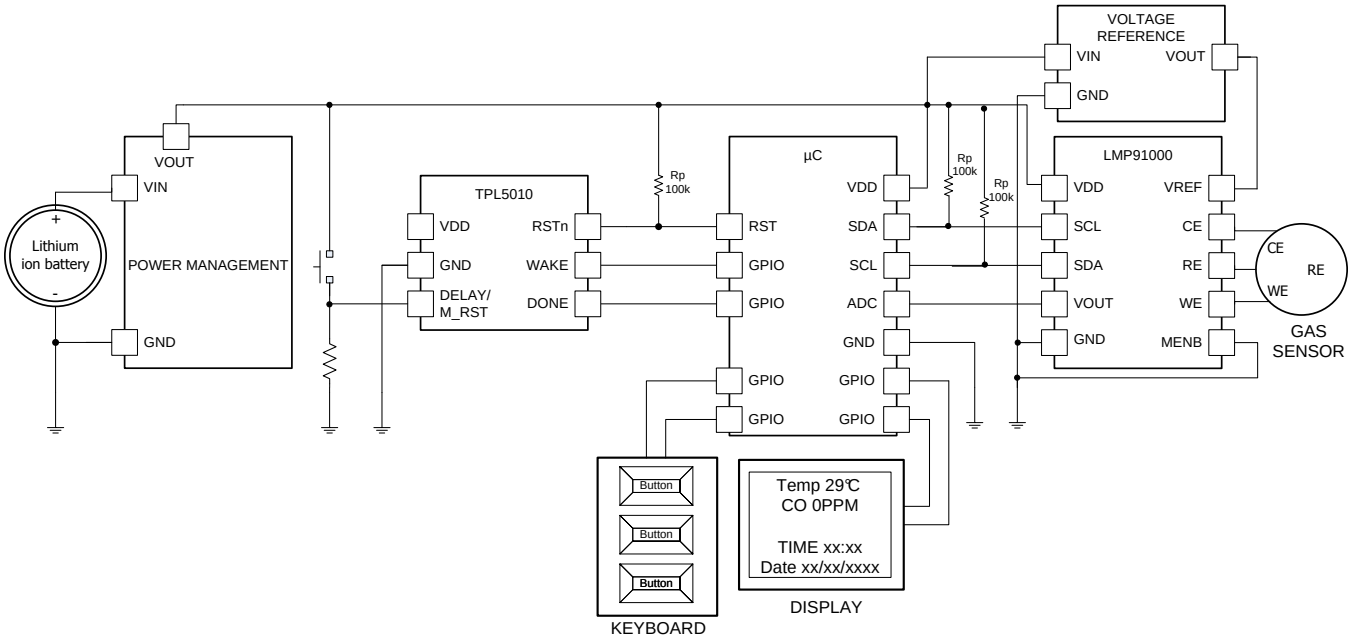


Figure 13. Data-Logger

9.2.1 Design Requirements

The design is driven by the low-current consumption constraint. The data are usually acquired on a rate that ranges between 1 s and 10 s. The highest necessity is the maximization of the battery life. The TPL5010 helps achieve that goal because it allows putting the µC in its lowest power mode. The TPL5010 will take care of the watchdog and the timing.

Typical Application (continued)

9.2.2 Detailed Design Procedure

When the main constraint is the battery life, the selection of a low power voltage reference, the µC, and the display is mandatory. The first step in the design is the calculation of the power consumption of the devices in their different mode of operations. For instance, the LMP91000 burns most of the power when in gas measurement mode, then, according to the connected gas sensor, it has two idle states (standby and deep sleep). The same is true for the µC, such as one of the MSP430 family, which can be placed in one of its lower power modes, such as LMP3.5 or LMP4.5. In this case, the TPL5010 can be used to implement the watchdog and wake-up timing functions.

After the power budget calculation, it is possible to select the appropriate time interval which satisfies the application constraints and maximize the life of the battery.

9.2.3 Application Curve

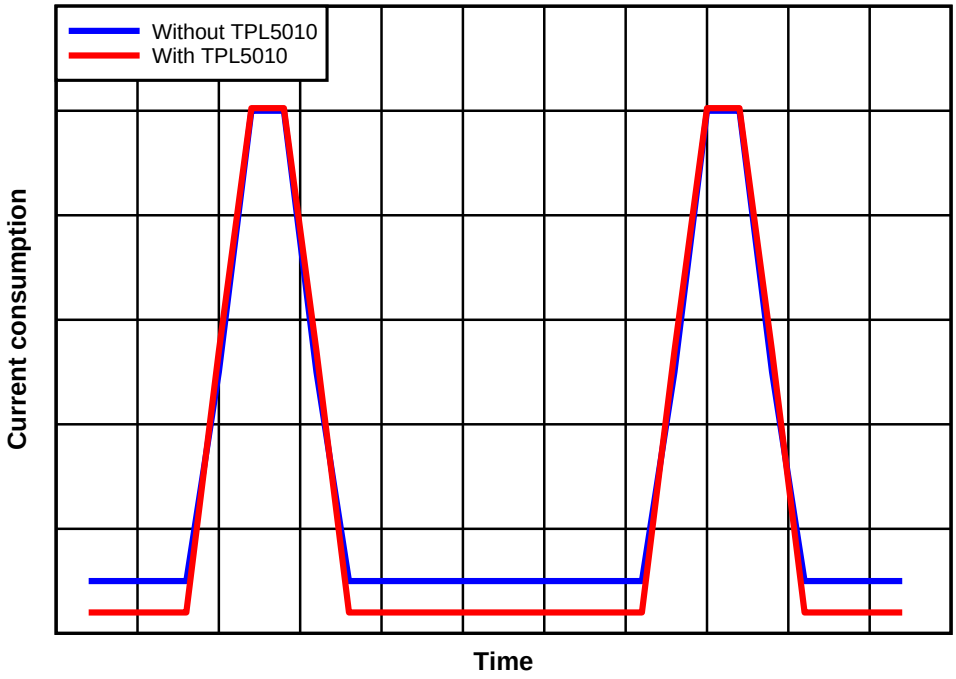


Figure 14. Effect of TPL5010 on Current Consumption

10 Power Supply Recommendations

The TPL5010 requires a voltage supply within 1.8 V and 5.5 V. A multilayer ceramic bypass X7R capacitor of 0.1 µF between VDD and GND pin is recommended.

11 Layout

11.1 Layout Guidelines

The DELAY/M_RST pin is sensitive to parasitic capacitance. TI suggests that the traces connecting the resistance on this pin to GROUND be kept as short as possible to minimize parasitic capacitance. This capacitance can affect the initial set up of the time interval. Signal integrity on the WAKE and RSTn pins is also improved by keeping the trace length between the TPL5010 and the µC short to reduce the parasitic capacitance.

11.2 Layout Example

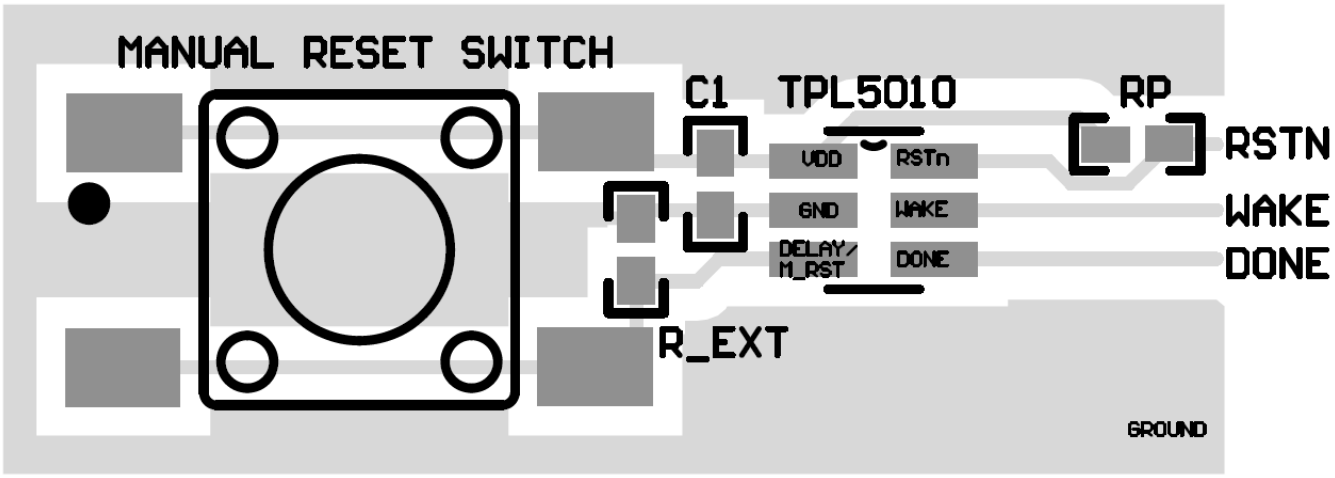


Figure 15. Layout

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

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12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPL5010DDCR	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ZAKX
TPL5010DDCR.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ZAKX
TPL5010DDCR.B	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ZAKX
TPL5010DDCT	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ZAKX
TPL5010DDCT.A	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ZAKX
TPL5010DDCT.B	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ZAKX
TPL5010DDCTG4	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ZAKX
TPL5010DDCTG4.A	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ZAKX
TPL5010DDCTG4.B	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ZAKX

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TPL5010 :

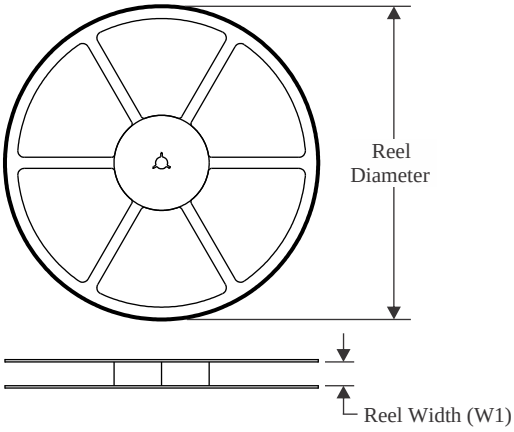
- Automotive : TPL5010-Q1

NOTE: Qualified Version Definitions:

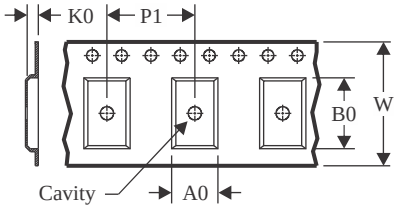
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

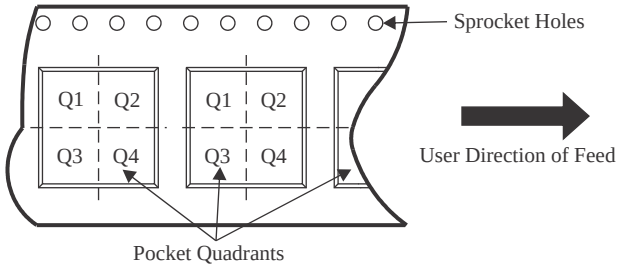


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

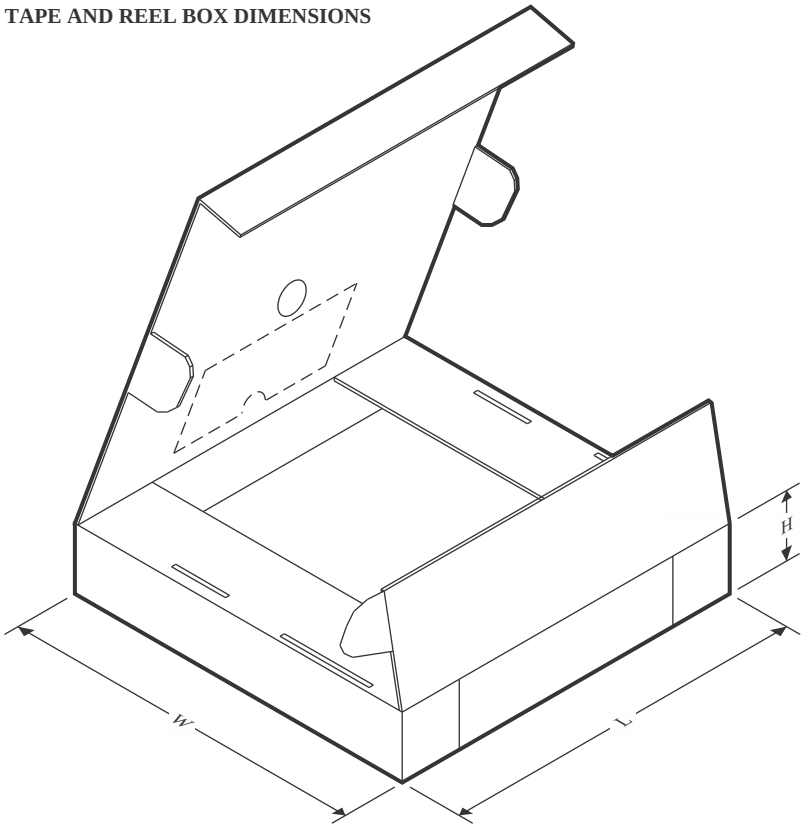
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPL5010DDCR	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPL5010DDCT	SOT-23-THIN	DDC	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPL5010DDCTG4	SOT-23-THIN	DDC	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

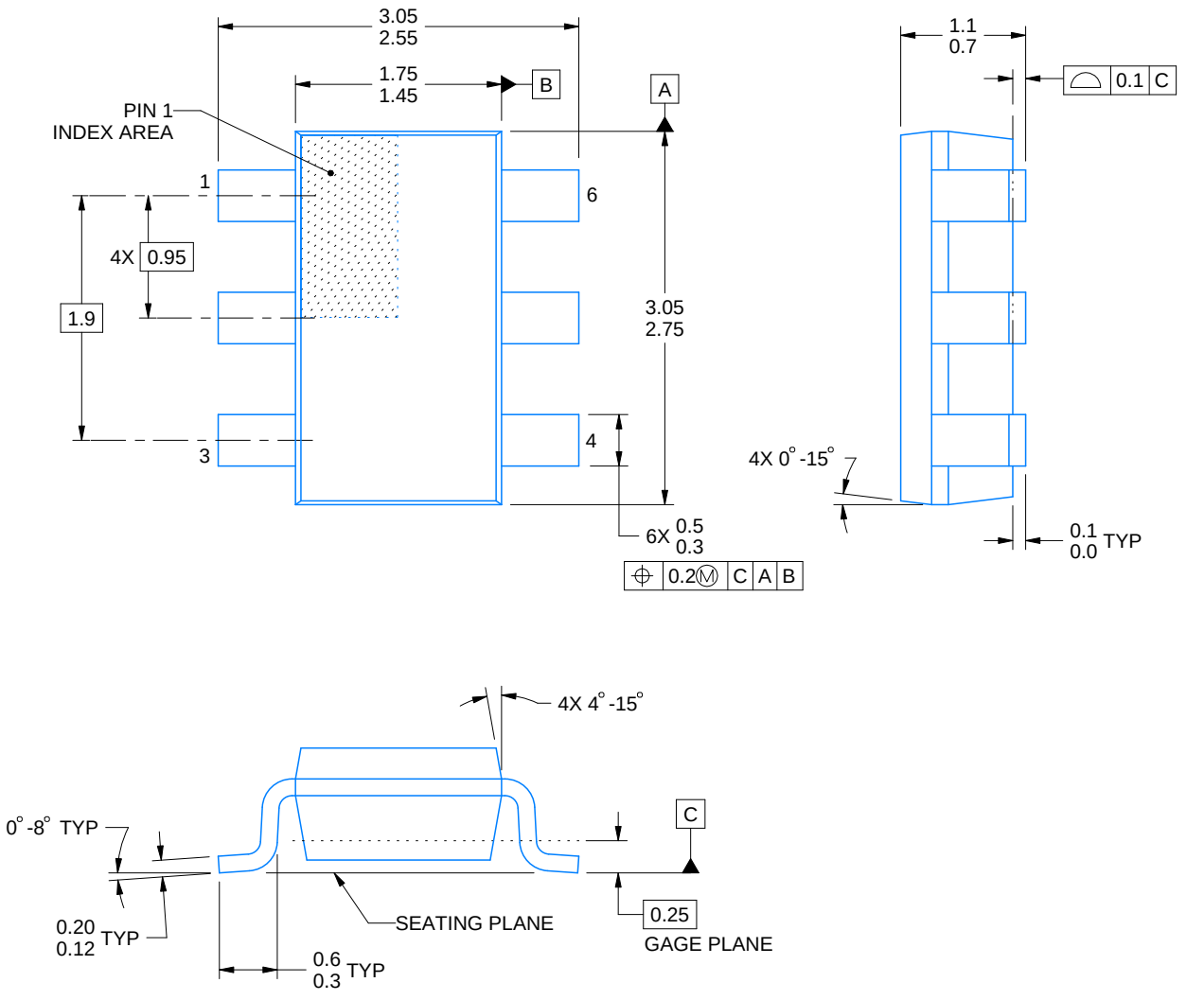
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPL5010DDCR	SOT-23-THIN	DDC	6	3000	208.0	191.0	35.0
TPL5010DDCT	SOT-23-THIN	DDC	6	250	208.0	191.0	35.0
TPL5010DDCTG4	SOT-23-THIN	DDC	6	250	208.0	191.0	35.0

PACKAGE OUTLINE

DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



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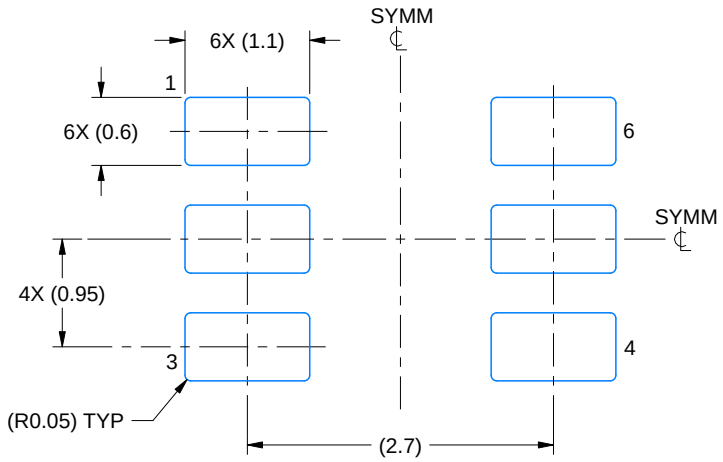
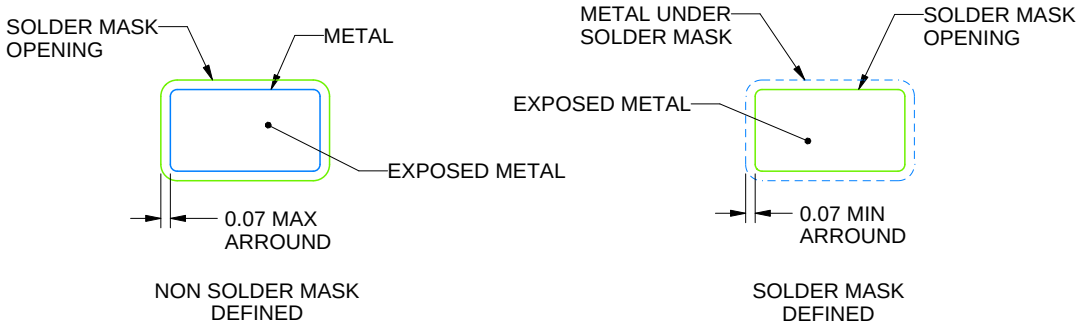
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X



SOLDERMASK DETAILS

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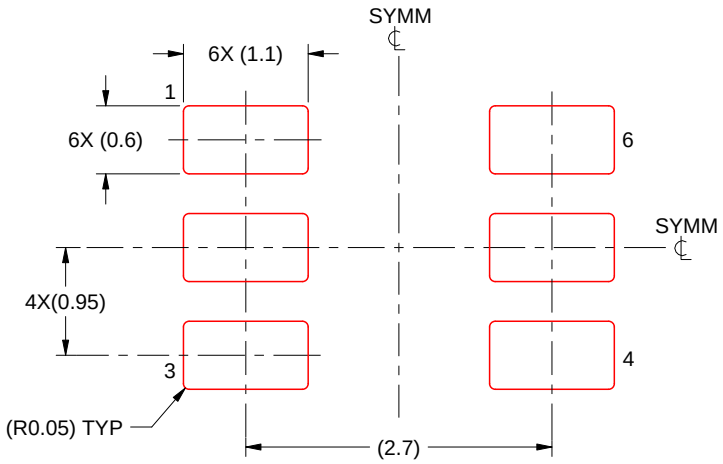
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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