

## TPS22969 5.5-V, 6-A, 4.4-mΩ On-Resistance Load Switch

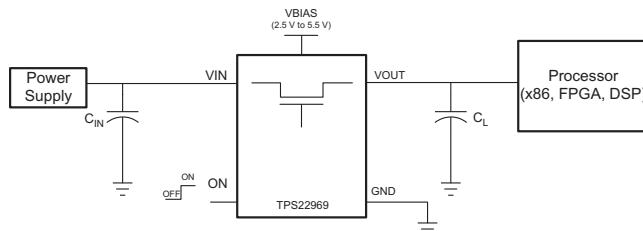
### 1 Features

- Integrated Single Channel Load Switch
- V<sub>BIAS</sub> Voltage Range: 2.5 V to 5.5 V
- V<sub>IN</sub> Voltage Range: 0.8 V to 5.5 V
- Ultra Low R<sub>ON</sub> Resistance
  - R<sub>ON</sub> = 4.4 mΩ at V<sub>IN</sub> = 1.05 V (V<sub>BIAS</sub> = 5 V)
- 6 A Maximum Continuous Switch Current
- Low Quiescent Current
  - (20 μA (Typ) for V<sub>BIAS</sub> = 5 V)
- Low Shutdown Current
  - (1 μA (Typ) for V<sub>BIAS</sub> = 5 V)
- Low Control Input Threshold Enables Use of 1.2 V or Higher GPIO
- Controlled and Fixed Slew Rate Across V<sub>BIAS</sub> and V<sub>IN</sub>
  - t<sub>R</sub> = 599 μs at V<sub>IN</sub> = 1.05 V (V<sub>BIAS</sub> = 5 V)
- Quick Output Discharge (QOD)
- SON 8-Pin Package with Thermal Pad
- ESD Performance Tested per JESD 22
  - 2-kV Human-Body Model (HBM)
  - 1-kV Charged-Device Model (CDM)

### 2 Applications

- Ultrabook™/Notebooks
- Desktop PC
- Industrial PC
- Chromebook
- Servers
- Set-top Boxes
- Telecom Systems
- Tablet PC

### Driving High Current Core Rails For a Processor



### 3 Description

The TPS22969 is a small, ultra-low R<sub>ON</sub> single channel load switch with controlled turn on. The device contains an N-channel MOSFET that can operate over an input voltage range of 0.8 V to 5.5 V and can support a maximum continuous current of 6 A.

The combination of ultra-low R<sub>ON</sub> and high current capability of the device makes it ideal for driving processor rails with very tight voltage dropout tolerances. The controlled rise time of the device greatly reduces inrush current caused by large bulk load capacitances, thereby reducing or eliminating voltage droop on the power supply. The switch can be independently controlled via the ON pin, which is capable of interfacing directly with low-voltage control signals originating from microcontrollers or low voltage discrete logic. The device further reduces the total solution size by integrating a 224-Ω pull-down resistor for quick output discharge (QOD) when the switch is turned off.

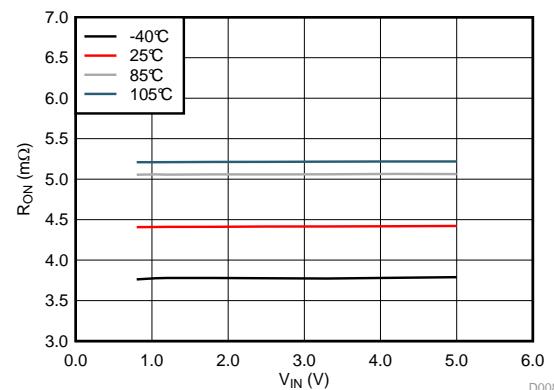
The TPS22969 is available in a small 3.00 mm x 3.00 mm SON-8 package (DNY). The DNY package integrates a thermal pad which allows for high power dissipation in high current and high temperature applications. The device is characterized for operation over the free-air temperature range of -40°C to 105°C.

### Device Information<sup>(1)</sup>

ORDER NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22969	WSON (8)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

### R<sub>ON</sub> vs V<sub>IN</sub> (V<sub>BIAS</sub> = 5 V, I<sub>OUT</sub> = -200 mA)



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

## Table of Contents

<b>1</b>	<b>Features</b> .....	<b>1</b>	7.2	Functional Block Diagram .....	<b>14</b>
<b>2</b>	<b>Applications</b> .....	<b>1</b>	7.3	Feature Description .....	<b>15</b>
<b>3</b>	<b>Description</b> .....	<b>1</b>	<b>8</b>	<b>Applications and Implementation</b> .....	<b>16</b>
<b>4</b>	<b>Revision History</b> .....	<b>2</b>	8.1	Application Information .....	<b>16</b>
<b>5</b>	<b>Pin Configuration and Functions</b> .....	<b>3</b>	8.2	Typical Application .....	<b>16</b>
<b>6</b>	<b>Specifications</b> .....	<b>3</b>	<b>9</b>	<b>Power Supply Recommendations</b> .....	<b>19</b>
6.1	Absolute Maximum Ratings .....	3	<b>10</b>	<b>Layout</b> .....	<b>19</b>
6.2	ESD Ratings .....	4	10.1	Layout Guidelines .....	<b>19</b>
6.3	Recommended Operating Conditions .....	4	10.2	Layout Example .....	<b>20</b>
6.4	Thermal Information .....	4	<b>11</b>	<b>Device and Documentation Support</b> .....	<b>21</b>
6.5	Electrical Characteristics, $V_{BIAS} = 5.0$ V .....	5	11.1	Community Resources .....	<b>21</b>
6.6	Electrical Characteristics, $V_{BIAS} = 2.5$ V .....	6	11.2	Trademarks .....	<b>21</b>
6.7	Switching Characteristics .....	7	11.3	Electrostatic Discharge Caution .....	<b>21</b>
6.8	Typical Characteristics .....	9	11.4	Glossary .....	<b>21</b>
<b>7</b>	<b>Detailed Description</b> .....	<b>14</b>	<b>12</b>	<b>Mechanical, Packaging, and Orderable</b> <b>Information</b> .....	<b>21</b>
7.1	Overview .....	14			

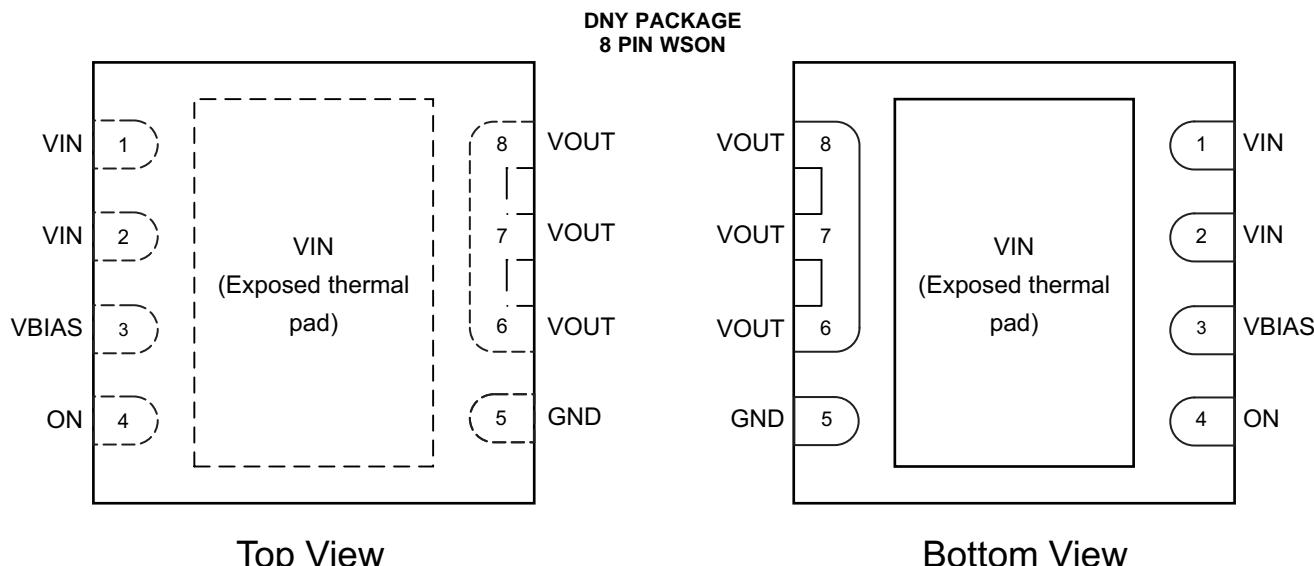
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2014) to Revision B	Page
• Updated $T_A$ ratings in datasheet from 85°C to 105°C. ....	<b>1</b>

Changes from Original (February 2014) to Revision A	Page
• Initial release of full version. ....	<b>1</b>

## 5 Pin Configuration and Functions



### Pin Functions

Pin		I/O	DESCRIPTION
NAME	NO.		
VIN	1, 2	I	Switch input. Place ceramic bypass capacitor(s) between this pin and GND. See the <a href="#">Detailed Description</a> section for more information.
VIN	Exposed thermal Pad	I	Switch input. Place ceramic bypass capacitor(s) between this pin and GND. See the <a href="#">Detailed Description</a> section for more information.
VBIAS	3	I	Bias voltage. Power supply to the device.
ON	4	I	Active high switch control input. Do not leave floating.
GND	5	–	Ground.
VOUT	6, 7, 8	O	Switch output. Place ceramic bypass capacitor(s) between this pin and GND. See the <a href="#">Detailed Description</a> section for more information.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>IN</sub>	Input voltage range	–0.3	6	V
V <sub>BIAS</sub>	Bias voltage range	–0.3	6	V
V <sub>OUT</sub>	Output voltage range	–0.3	6	V
V <sub>ON</sub>	ON pin voltage range	–0.3	6	V
I <sub>MAX</sub>	Maximum Continuous Switch Current		6	A
I <sub>PLS</sub>	Maximum Pulsed Switch Current, pulse < 300-μs, 2% duty cycle		8	A
T <sub>A</sub>	Operating free-air temperature range	–40	105	°C
T <sub>J</sub>	Maximum junction temperature		125	°C
T <sub>STG</sub>	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#). Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

## 6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
V <sub>IN</sub>	Input voltage range	0.8	V <sub>BIAS</sub>	V	
V <sub>BIAS</sub>	Bias voltage range	2.5	5.5	V	
V <sub>ON</sub>	ON voltage range	0	5.5	V	
V <sub>OUT</sub>	Output voltage range		V <sub>IN</sub>	V	
V <sub>IH, ON</sub>	High-level voltage, ON	V <sub>BIAS</sub> = 2.5V to 5.5V	1.2	5.5	V
V <sub>IL, ON</sub>	Low-level voltage, ON	V <sub>BIAS</sub> = 2.5V to 5.5V	0	0.5	V
C <sub>IN</sub>	Input Capacitor	1 <sup>(1)</sup>		µF	

(1) Refer to [Detailed Description](#) section.

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	TPS22969	UNIT
	DNY (WSON)	
	8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	44.6
R <sub>θJCtop</sub>	Junction-to-case (top) thermal resistance	44.4
R <sub>θJB</sub>	Junction-to-board thermal resistance	17.6
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.4
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	17.4
R <sub>θJCbot</sub>	Junction-to-case (bottom) thermal resistance	1.1

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics, $V_{BIAS} = 5.0$ V

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature  $-40^\circ\text{C} \leq T_A \leq 105^\circ\text{C}$ . Typical values are for  $T_A = 25^\circ\text{C}$  (unless otherwise noted).

PARAMETER	TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
<b>CURRENTS AND THRESHOLDS</b>						
$I_Q, V_{BIAS}$ V <sub>BIAS</sub> quiescent current	$I_{OUT} = 0, V_{IN} = V_{BIAS}, V_{ON} = 5.0$ V	-40°C to 85°C	20.4	26.0		$\mu\text{A}$
		-40°C to 105°C		27.0		
$I_{SD, V_{BIAS}}$ V <sub>BIAS</sub> shutdown current	$V_{ON} = 0$ V, $V_{OUT} = 0$ V	-40°C to 85°C	1.1	1.5		$\mu\text{A}$
		-40°C to 105°C		1.6		
$I_{SD, V_{IN}}$ V <sub>IN</sub> shutdown current	$V_{ON} = 0$ V, $V_{OUT} = 0$ V	$V_{IN} = 5.0$ V	-40°C to 85°C	0.1		$\mu\text{A}$
			-40°C to 105°C	0.5		
		$V_{IN} = 3.3$ V	-40°C to 85°C	0.1		
			-40°C to 105°C	0.5		
		$V_{IN} = 1.8$ V	-40°C to 85°C	0.1		
			-40°C to 105°C	0.5		
		$V_{IN} = 1.05$ V	-40°C to 85°C	0.1		
			-40°C to 105°C	0.5		
		$V_{IN} = 0.8$ V	-40°C to 85°C	0.1		
			-40°C to 105°C	0.5		
$I_{ON}$	ON pin leakage current	$V_{ON} = 5.5$ V	-40°C to 105°C		0.1	$\mu\text{A}$
$V_{HYS, ON}$	ON pin hysteresis	$V_{BIAS} = V_{IN}$	25°C	113		mV
<b>RESISTANCE CHARACTERISTICS</b>						
$R_{ON}$ On-state resistance	$I_{OUT} = -200$ mA, $V_{BIAS} = 5.0$ V	$V_{IN} = 5.0$ V	25°C	4.4	5.0	$\text{m}\Omega$
			-40°C to 85°C		5.6	
			-40°C to 105°C		5.8	
		$V_{IN} = 3.3$ V	25°C	4.4	5.0	$\text{m}\Omega$
			-40°C to 85°C		5.6	
			-40°C to 105°C		5.8	
		$V_{IN} = 2.5$ V	25°C	4.4	5.0	$\text{m}\Omega$
			-40°C to 85°C		5.6	
			-40°C to 105°C		5.8	
		$V_{IN} = 1.8$ V	25°C	4.4	5.0	$\text{m}\Omega$
			-40°C to 85°C		5.6	
			-40°C to 105°C		5.8	
$R_{PD}$	Output pulldown resistance	$V_{IN} = 5.0$ V, $V_{ON} = 0$ V, $V_{OUT} = 1$ V	25°C	4.4	5.0	$\text{m}\Omega$
			-40°C to 85°C		5.6	
		$V_{IN} = 1.05$ V	-40°C to 105°C		5.8	$\text{m}\Omega$
			-40°C to 85°C	4.6	5.8 <sup>(1)</sup>	
			-40°C to 105°C		6.0 <sup>(1)</sup>	

(1) Parameter verified by design and characterization, but not tested in production.

## 6.6 Electrical Characteristics, $V_{BIAS} = 2.5\text{ V}$

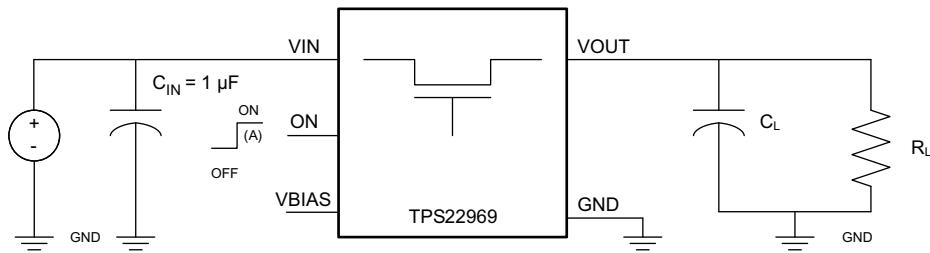
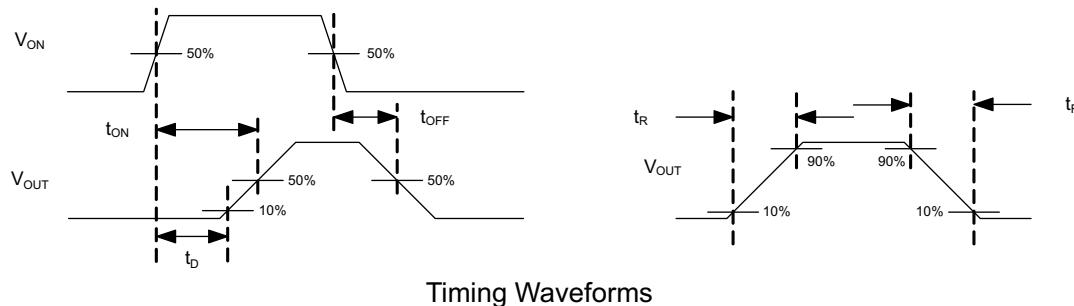
Unless otherwise noted, the specification in the following table applies over the operating ambient temperature  $-40^\circ\text{C} \leq T_A \leq 105^\circ\text{C}$ . Typical values are for  $T_A = 25^\circ\text{C}$  unless otherwise noted.

PARAMETER	TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT	
<b>CURRENTS AND THRESHOLDS</b>							
$I_Q, V_{BIAS}$	$V_{BIAS}$ quiescent current	$I_{OUT} = 0, V_{IN} = V_{BIAS}, V_{ON} = 5.0\text{ V}$	-40°C to 85°C	9.9	12.5	$\mu\text{A}$	
			-40°C to 105°C		12.7		
$I_{SD, V_{BIAS}}$	$V_{BIAS}$ shutdown current	$V_{ON} = 0\text{ V}, V_{OUT} = 0\text{ V}$	-40°C to 85°C	0.5	0.65	$\mu\text{A}$	
			-40°C to 105°C		0.7		
$I_{SD, V_{IN}}$	$V_{IN}$ shutdown current	$V_{ON} = 0\text{ V}, V_{OUT} = 0\text{ V}$	$V_{IN} = 2.5\text{ V}$	-40°C to 85°C	0.1	$\mu\text{A}$	
				-40°C to 105°C	0.5		
			$V_{IN} = 1.8\text{ V}$	-40°C to 85°C	0.1		
				-40°C to 105°C	0.5		
			$V_{IN} = 1.05\text{ V}$	-40°C to 85°C	0.1		
				-40°C to 105°C	0.5		
			$V_{IN} = 0.8\text{ V}$	-40°C to 85°C	0.1		
				-40°C to 105°C	0.5		
$I_{ON}$	ON pin input leakage current	$V_{ON} = 5.5\text{ V}$	-40°C to 105°C		0.1	$\mu\text{A}$	
$V_{HYS, ON}$	ON pin hysteresis	$V_{BIAS} = V_{IN}$	25°C		83	$\text{mV}$	
<b>RESISTANCE CHARACTERISTICS</b>							
$R_{ON}$	On-state resistance	$I_{OUT} = -200\text{ mA}, V_{BIAS} = 2.5\text{ V}$	$V_{IN} = 2.5\text{ V}$	25°C	4.7	5.3	$\text{m}\Omega$
				-40°C to 85°C		6.0	
				-40°C to 105°C		6.2	
			$V_{IN} = 1.8\text{ V}$	25°C	4.6	5.2	$\text{m}\Omega$
				-40°C to 85°C		5.8	
				-40°C to 105°C		6.0	
			$V_{IN} = 1.05\text{ V}$	25°C	4.5	5.1	$\text{m}\Omega$
				-40°C to 85°C		5.7	
				-40°C to 105°C		5.9	
			$V_{IN} = 0.8\text{ V}$	25°C	4.5	5.1	$\text{m}\Omega$
				-40°C to 85°C		5.7	
				-40°C to 105°C		5.9	
$R_{PD}$	Output pulldown resistance	$V_{IN} = 2.5\text{ V}, V_{ON} = 0\text{ V}, V_{OUT} = 1\text{ V}$	-40°C to 105°C		224	233	$\Omega$

## 6.7 Switching Characteristics

Refer to the timing test circuit in [Figure 1](#) (unless otherwise noted) for references to external components used for the test condition in the switching characteristics table. Switching characteristics shown below are only valid for the power-up sequence where VIN and VBIAS are already in steady state condition before the ON pin is asserted high.

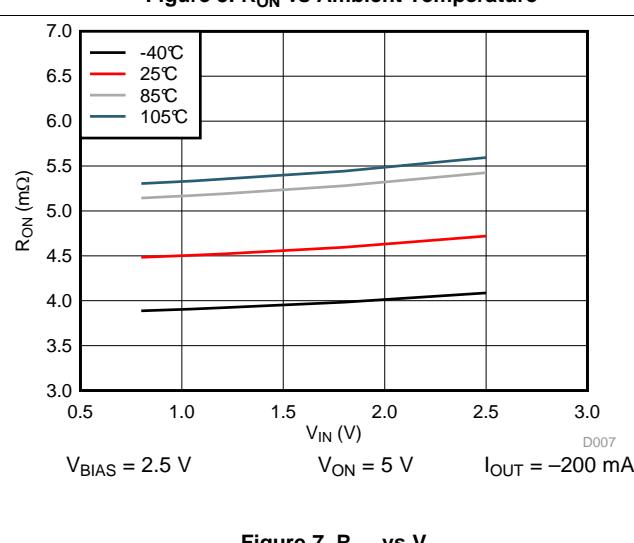
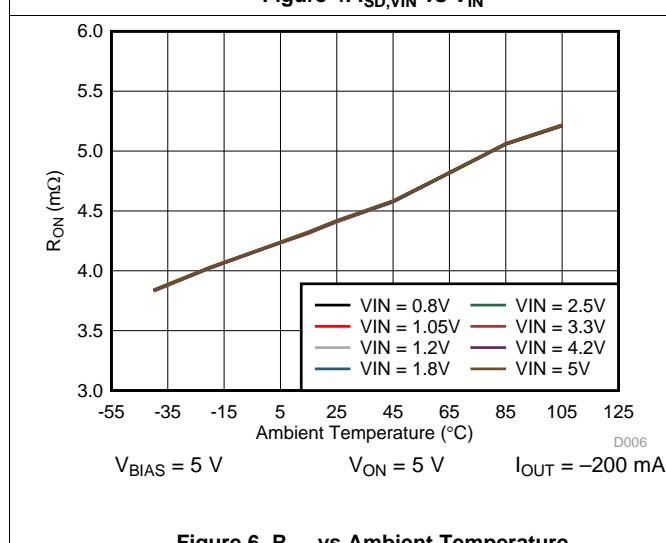
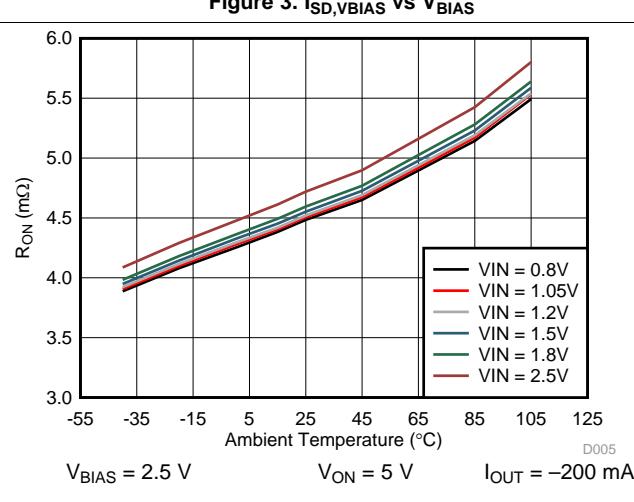
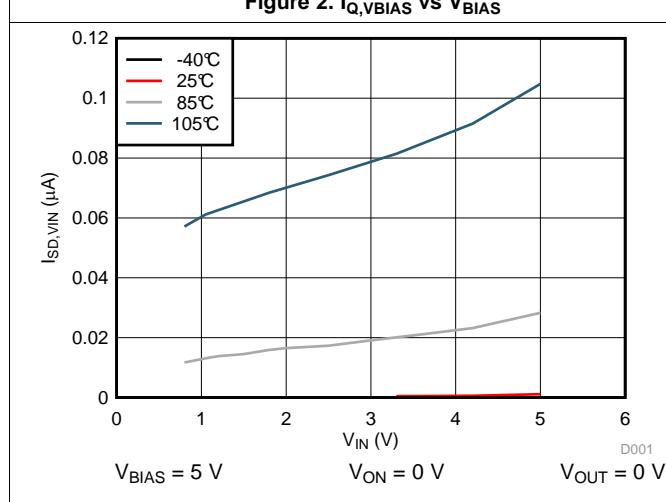
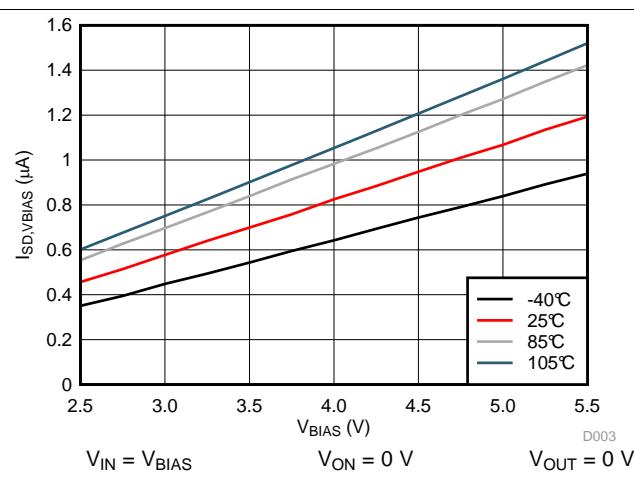
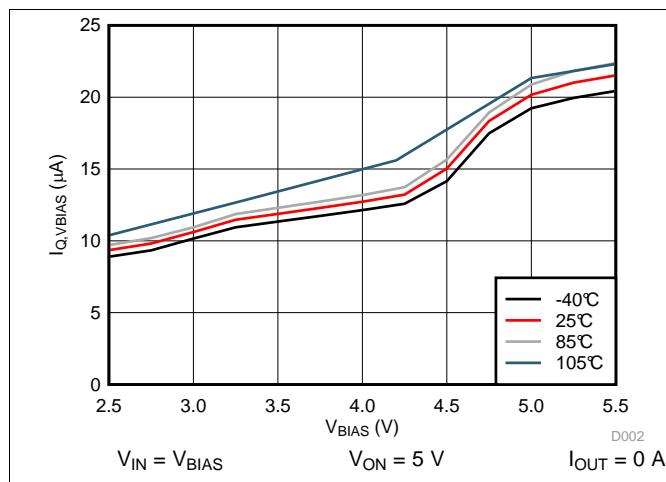
PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
<b><math>V_{IN} = 5 \text{ V}</math>, <math>V_{ON} = V_{BIAS} = 5 \text{ V}</math>, <math>T_A = 25^\circ\text{C}</math> (unless otherwise noted)</b>					
$t_{ON}$	$R_L = 10 \Omega$ , $C_L = 0.1 \mu\text{F}$	2397	$\mu\text{s}$		
$t_{OFF}$		4			
$t_R$		2663			
$t_F$		2			
$t_D$		1009			
<b><math>V_{IN} = 1.05 \text{ V}</math>, <math>V_{ON} = V_{BIAS} = 5 \text{ V}</math>, <math>T_A = 25^\circ\text{C}</math> (unless otherwise noted)</b>					
$t_{ON}$	$R_L = 10 \Omega$ , $C_L = 0.1 \mu\text{F}$	1064	$\mu\text{s}$		
$t_{OFF}$		4			
$t_R$		599			
$t_F$		2			
$t_D$		727			
<b><math>V_{IN} = 0.8 \text{ V}</math>, <math>V_{ON} = V_{BIAS} = 5 \text{ V}</math>, <math>T_A = 25^\circ\text{C}</math> (unless otherwise noted)</b>					
$t_{ON}$	$R_L = 10 \Omega$ , $C_L = 0.1 \mu\text{F}$	981	$\mu\text{s}$		
$t_{OFF}$		4			
$t_R$		500			
$t_F$		2			
$t_D$		714			
<b><math>V_{IN} = 2.5 \text{ V}</math>, <math>V_{ON} = 5 \text{ V}</math>, <math>V_{BIAS} = 2.5 \text{ V}</math>, <math>T_A = 25^\circ\text{C}</math> (unless otherwise noted)</b>					
$t_{ON}$	$R_L = 10 \Omega$ , $C_L = 0.1 \mu\text{F}$	1576	$\mu\text{s}$		
$t_{OFF}$		8			
$t_R$		1372			
$t_F$		2			
$t_D$		865			
<b><math>V_{IN} = 1.05 \text{ V}</math>, <math>V_{ON} = 5 \text{ V}</math>, <math>V_{BIAS} = 2.5 \text{ V}</math>, <math>T_A = 25^\circ\text{C}</math> (unless otherwise noted)</b>					
$t_{ON}$	$R_L = 10 \Omega$ , $C_L = 0.1 \mu\text{F}$	1080	$\mu\text{s}$		
$t_{OFF}$		8			
$t_R$		604			
$t_F$		2			
$t_D$		738			
<b><math>V_{IN} = 0.8 \text{ V}</math>, <math>V_{ON} = 5 \text{ V}</math>, <math>V_{BIAS} = 2.5 \text{ V}</math>, <math>T_A = 25^\circ\text{C}</math> (unless otherwise noted)</b>					
$t_{ON}$	$R_L = 10 \Omega$ , $C_L = 0.1 \mu\text{F}$	994	$\mu\text{s}$		
$t_{OFF}$		8			
$t_R$		502			
$t_F$		2			
$t_D$		723			


**Timing Test Circuit**


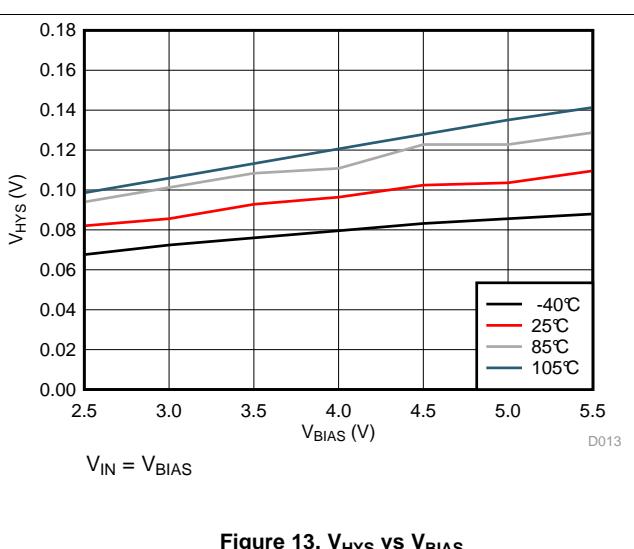
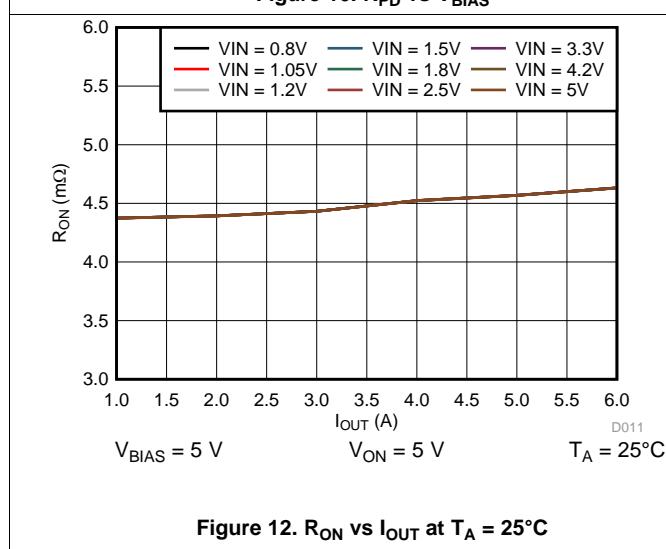
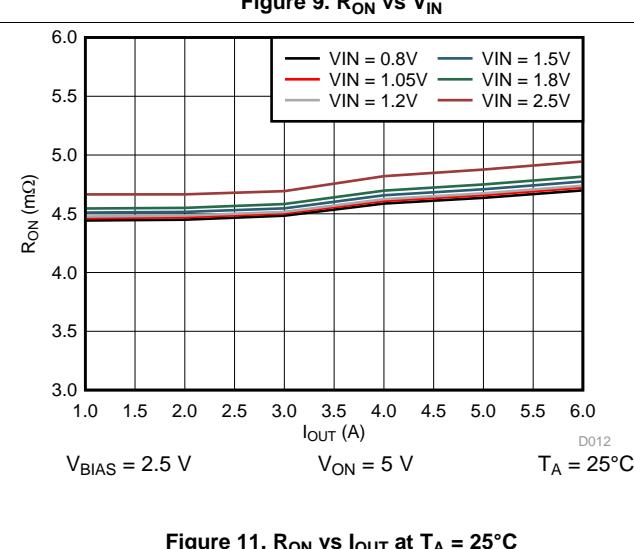
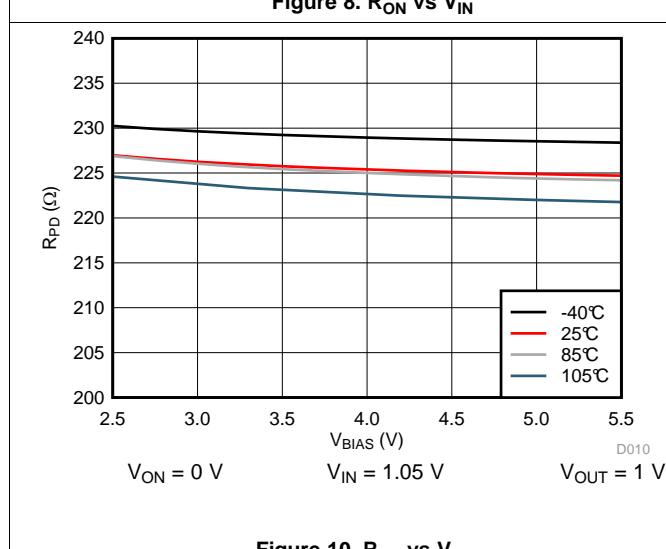
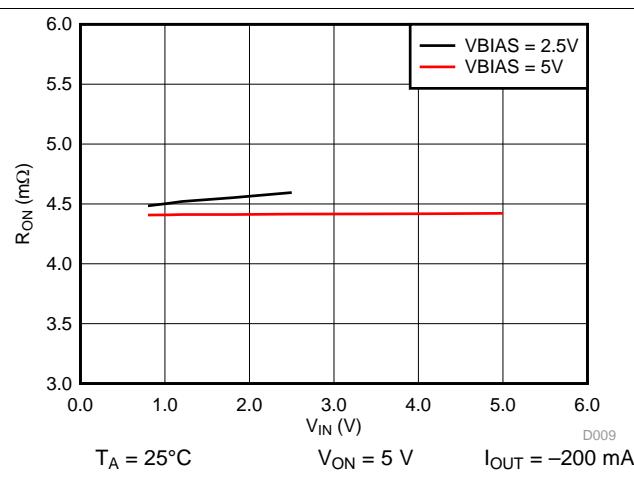
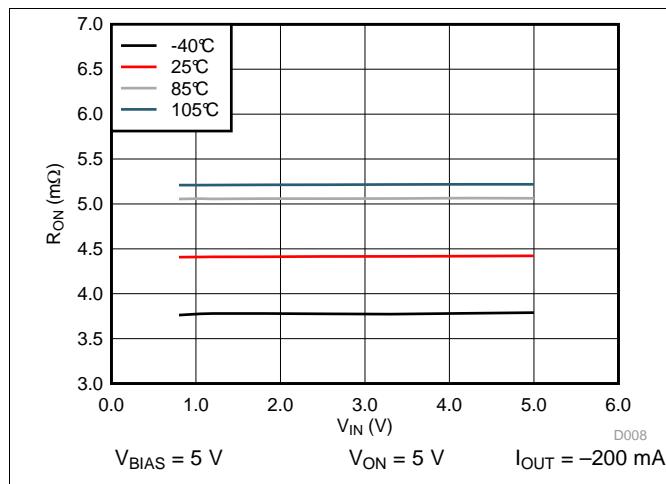
(A) Rise and fall times of the control signal is 100 ns.

**Figure 1. Switching Characteristics Measurement Setup and Definitions**

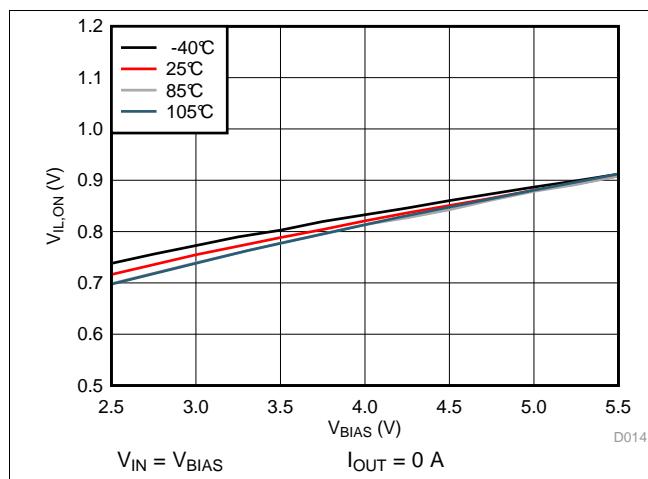
## 6.8 Typical Characteristics



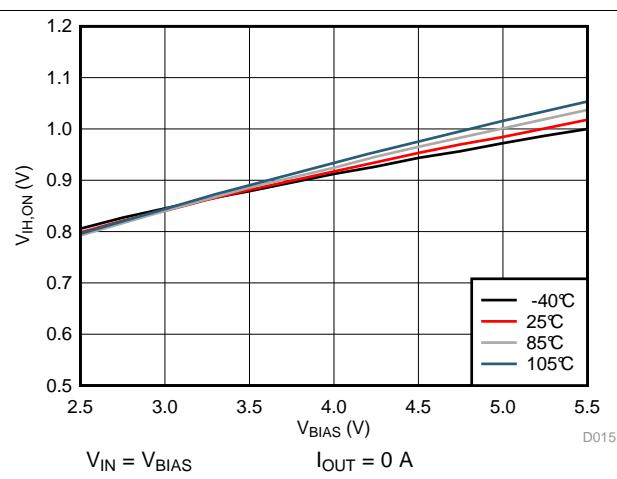
## Typical Characteristics (continued)



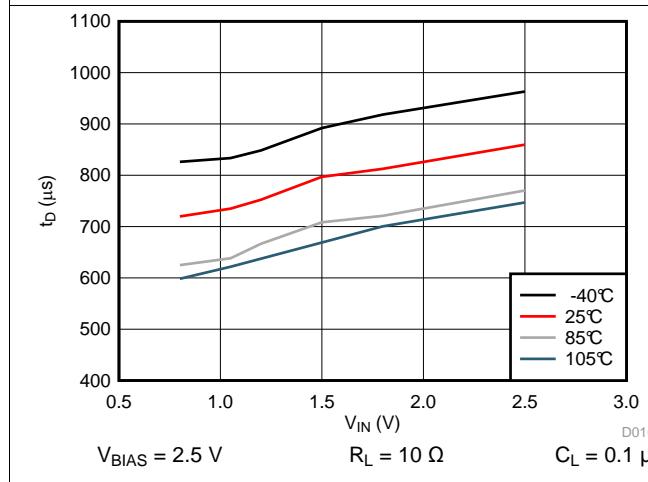
## Typical Characteristics (continued)



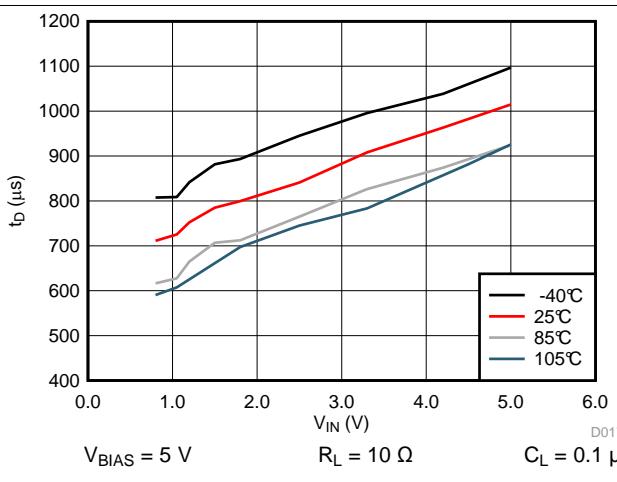
**Figure 14.  $V_{IL,ON}$  vs  $V_{BIAS}$**



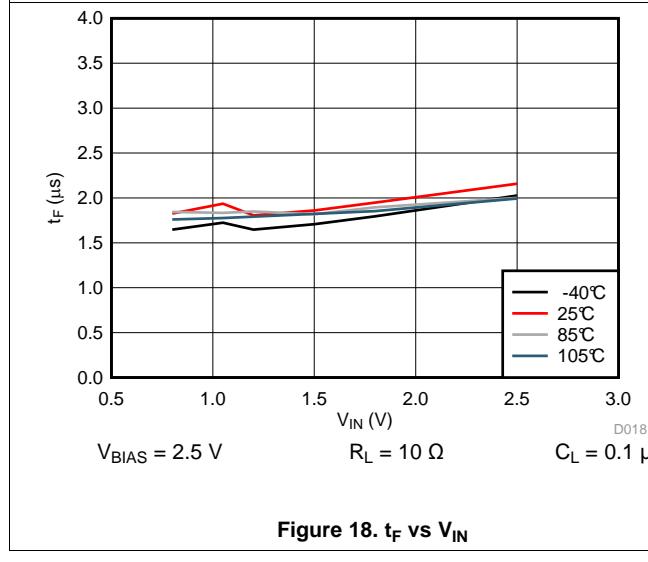
**Figure 15.  $V_{IH,ON}$  vs  $V_{BIAS}$**



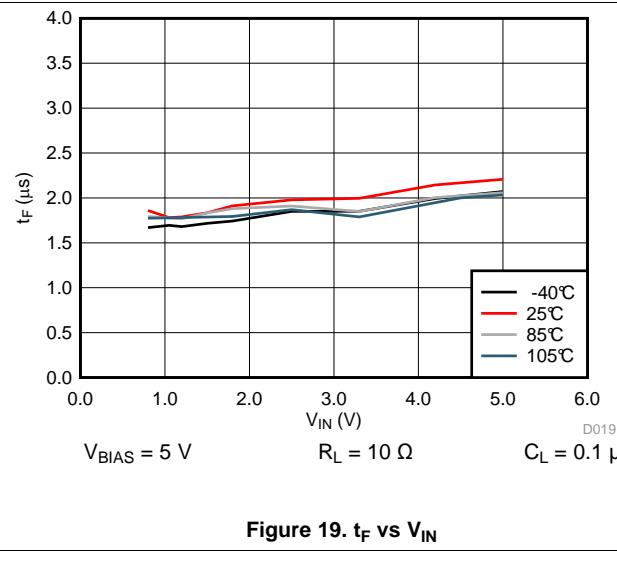
**Figure 16.  $t_D$  vs  $V_{IN}$**



**Figure 17.  $t_D$  vs  $V_{IN}$**

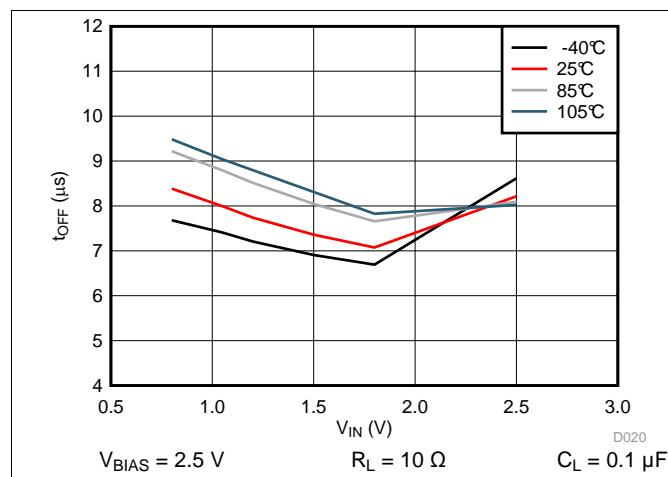


**Figure 18.  $t_F$  vs  $V_{IN}$**

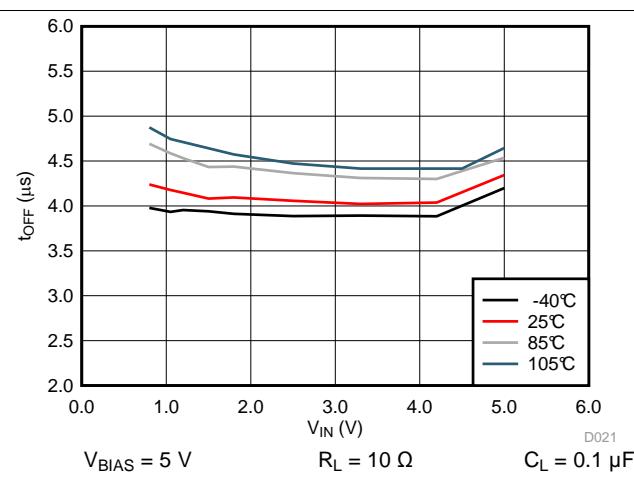


**Figure 19.  $t_F$  vs  $V_{IN}$**

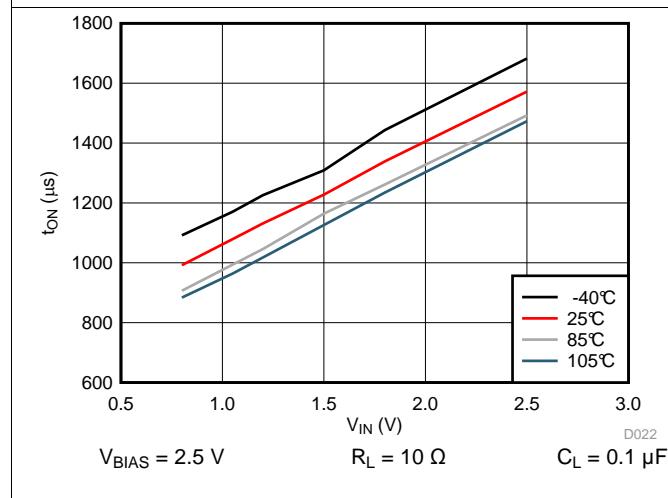
## Typical Characteristics (continued)



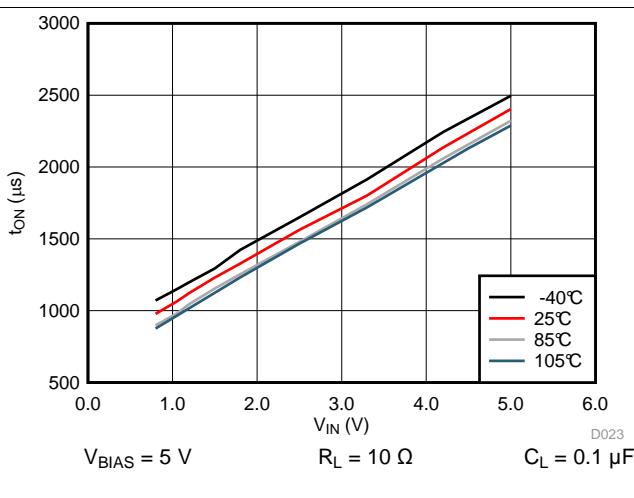
**Figure 20.  $t_{OFF}$  vs  $V_{IN}$**



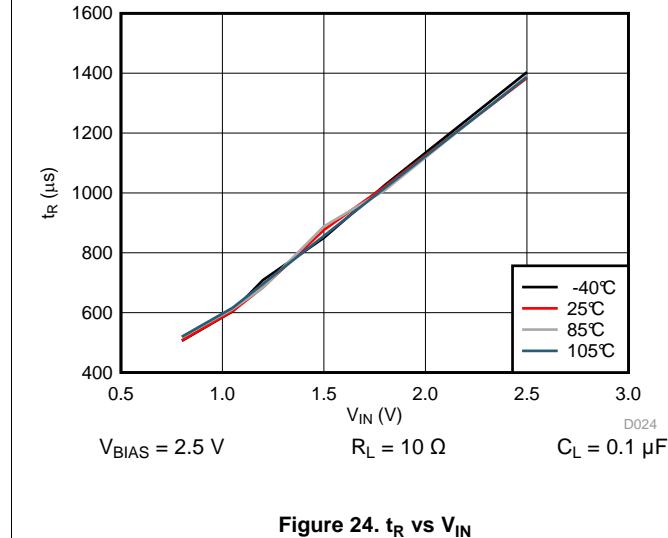
**Figure 21.  $t_{OFF}$  vs  $V_{IN}$**



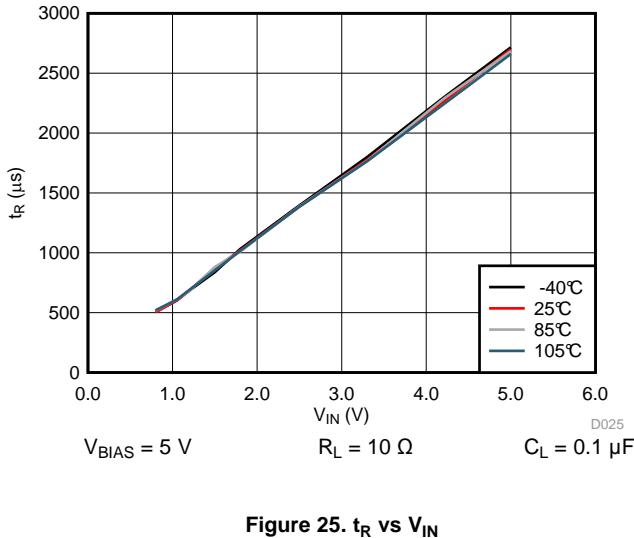
**Figure 22.  $t_{ON}$  vs  $V_{IN}$**



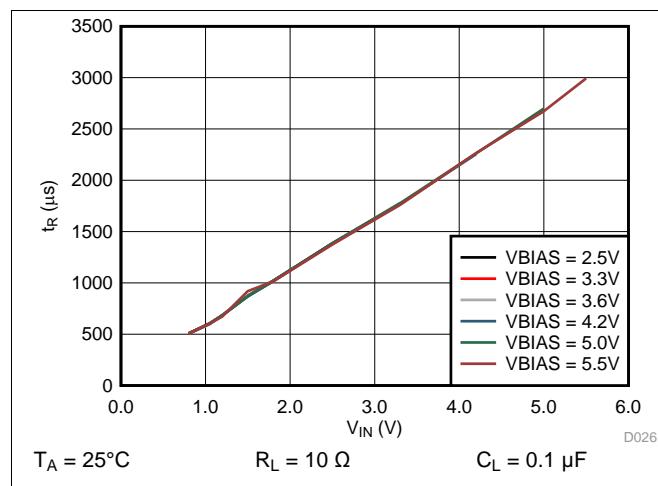
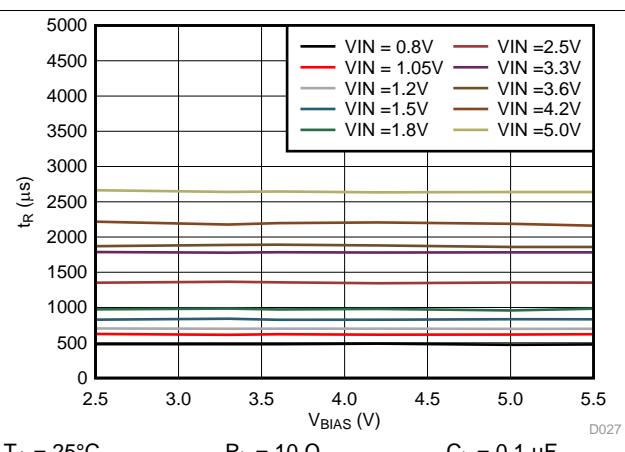
**Figure 23.  $t_{ON}$  vs  $V_{IN}$**



**Figure 24.  $t_R$  vs  $V_{IN}$**



**Figure 25.  $t_R$  vs  $V_{IN}$**

**Typical Characteristics (continued)**

**Figure 26.  $t_R$  vs  $V_{IN}$  for Various  $V_{BIAS}$** 

**Figure 27.  $t_R$  vs  $V_{BIAS}$  for Various  $V_{IN}$**

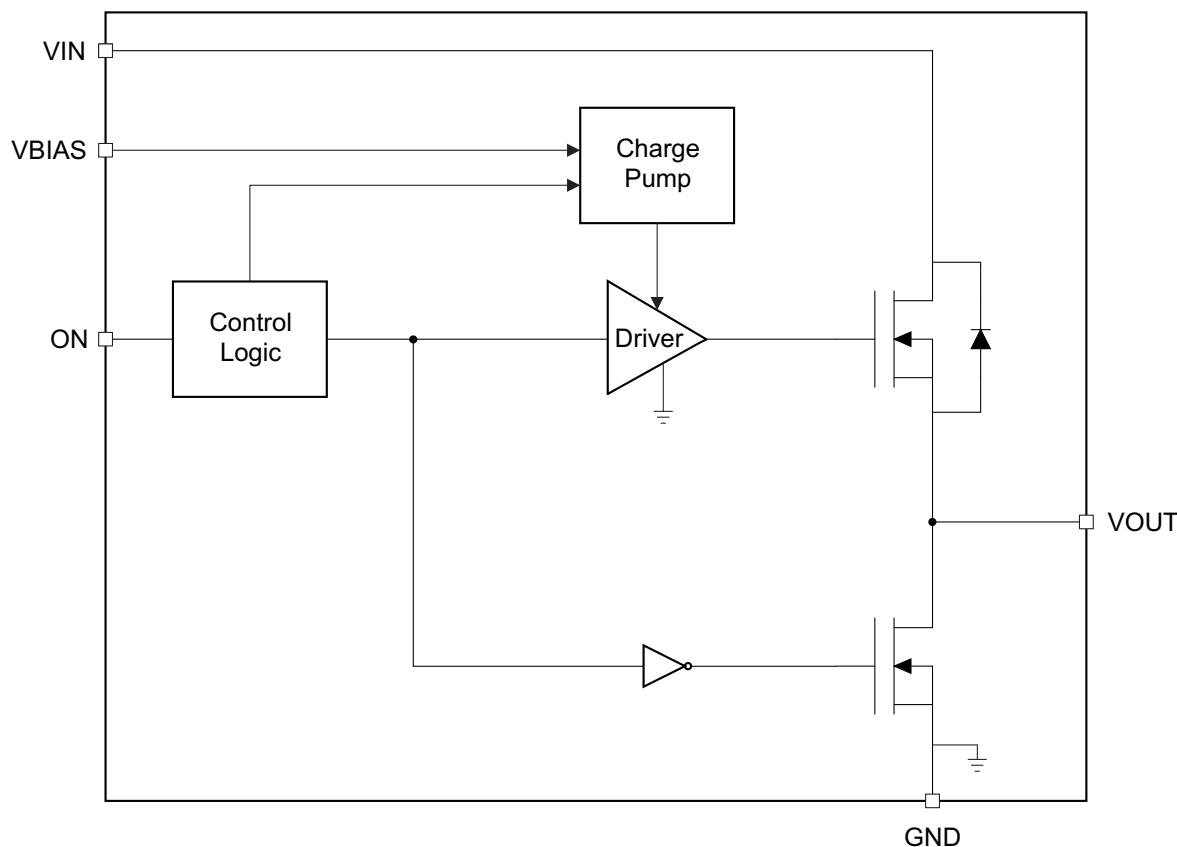
## 7 Detailed Description

### 7.1 Overview

The device is a 5.5 V, 6 A load switch in a 8-pin SON package. To reduce voltage drop for low voltage and high current rails, the device implements an ultra-low resistance N-channel MOSFET which reduces the drop out voltage through the device.

The device has a controlled and fixed slew rate which helps reduce or eliminate power supply droop due to large inrush currents. During shutdown, the device has very low leakage currents, thereby reducing unnecessary leakages for downstream modules during standby. Integrated control logic, driver, charge pump, and output discharge FET eliminates the need for any external components, which reduces solution size and BOM count.

### 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 On/off Control

The ON pin controls the state of the load switch, and asserting the pin high (active high) enables the switch. The ON pin is compatible with standard GPIO logic threshold and can be used with any microcontroller or discrete logic with 1.2-V or higher GPIO voltage. This pin cannot be left floating and must be tied either high or low for proper functionality.

### 7.3.2 Input Capacitor ( $C_{IN}$ )

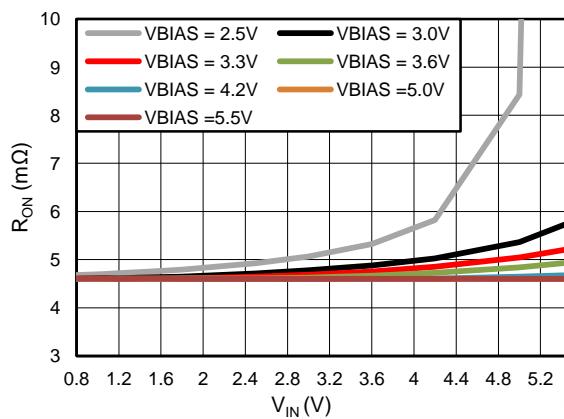
To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between  $V_{IN}$  and GND. A 1- $\mu$ F ceramic capacitor,  $C_{IN}$ , placed close to the pins, is usually sufficient. Higher values of  $C_{IN}$  can be used to further reduce the voltage drop in high-current application. When switching heavy loads, it is recommended to have an input capacitor 10 times higher than the output capacitor to avoid excessive voltage drop; however, a 10 to 1 ratio for capacitance is not required for proper functionality of the device, but a ratio smaller than 10 to 1 (such as 1 to 1) could cause a  $V_{IN}$  dip upon turn-on due to inrush currents based on external factor such as board parasitics and output bulk capacitance.

### 7.3.3 Output Capacitor ( $C_L$ )

Due to the integrated body diode in the N-channel MOSFET, a  $C_{IN}$  greater than  $C_L$  is highly recommended. A  $C_L$  greater than  $C_{IN}$  can cause  $V_{OUT}$  to exceed  $V_{IN}$  when the system supply is removed. This could result in current flow through the body diode from  $V_{OUT}$  to  $V_{IN}$ . A  $C_{IN}$  to  $C_L$  ratio of 10 to 1 is recommended for minimizing  $V_{IN}$  dip caused by inrush currents during startup, however a 10 to 1 ratio for capacitance is not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) could cause a  $V_{IN}$  dip upon turn-on due to inrush currents based on external factor such as board parasitics and output bulk capacitance.

### 7.3.4 $V_{IN}$ and $V_{BIAS}$ Voltage Range

For optimal  $R_{ON}$  performance, make sure  $V_{IN} \leq V_{BIAS}$ . The device may still be functional if  $V_{IN} > V_{BIAS}$  but it will exhibit  $R_{ON}$  greater than what is listed in the Electrical Characteristics table. See [Figure 28](#) for an example of a typical device. Notice the increasing  $R_{ON}$  as  $V_{IN}$  increases. Be sure to never exceed the maximum voltage rating for  $V_{IN}$  and  $V_{BIAS}$ . Performance of the device is not guaranteed for  $V_{IN} > V_{BIAS}$ .



**Figure 28.**  $R_{ON}$  vs  $V_{IN}$  ( $V_{IN} > V_{BIAS}$ )

## 8 Applications and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

This section will highlight some of the design considerations when implementing this device in various applications. A PSPICE model for this device is also available in the product page of this device.

### 8.2 Typical Application

This application demonstrates how the TPS22969 can be used to power downstream modules with large capacitances. The example below is powering a 100- $\mu$ F capacitive output load.

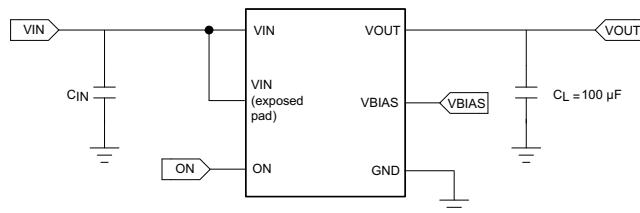


Figure 29. Typical Application Schematic for Powering a Downstream Module

#### 8.2.1 Design Requirements

For this design example, use [Table 1](#) as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
$V_{IN}$	1.05 V
$V_{BIAS}$	5.0 V
Load current	6 A

#### 8.2.2 Detailed Design Procedure

To begin the design process, the designer needs to know the following:

- $V_{IN}$  voltage
- $V_{BIAS}$  voltage
- Load current

##### 8.2.2.1 $V_{IN}$ to $V_{OUT}$ Voltage Drop

The  $V_{IN}$  to  $V_{OUT}$  voltage drop in the device is determined by the  $R_{ON}$  of the device and the load current. The  $R_{ON}$  of the device depends upon the  $V_{IN}$  and  $V_{BIAS}$  conditions of the device. Refer to the  $R_{ON}$  specification of the device in the [Electrical Characteristics,  \$V\_{BIAS} = 5.0\$  V](#) tables of this datasheet. Once the  $R_{ON}$  of the device is determined based upon the  $V_{IN}$  and  $V_{BIAS}$  conditions, use [Equation 1](#) to calculate the  $V_{IN}$  to  $V_{OUT}$  voltage drop:

$$\Delta V = I_{LOAD} \times R_{ON} \quad (1)$$

where

- $\Delta V$  = voltage drop from  $V_{IN}$  to  $V_{OUT}$
- $I_{LOAD}$  = load current
- $R_{ON}$  = on-resistance of the device for a specific  $V_{IN}$  and  $V_{BIAS}$  combination

An appropriate  $I_{LOAD}$  must be chosen such that the  $I_{MAX}$  specification of the device is not violated.

### 8.2.2.2 Inrush Current

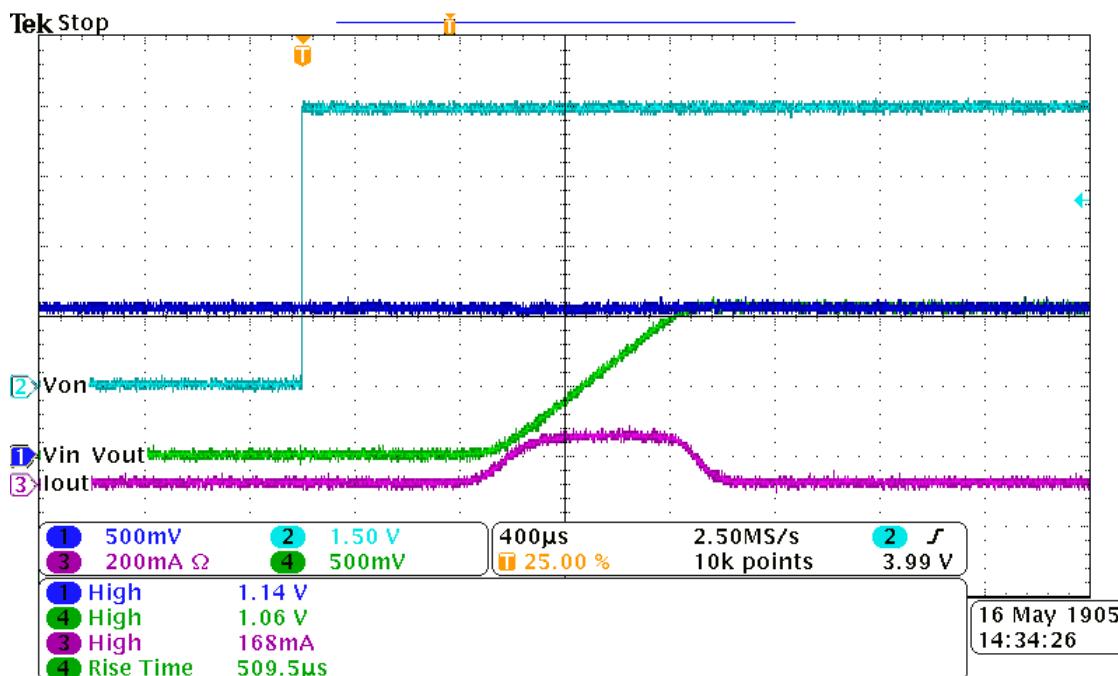
To determine how much inrush current will be caused by the  $C_L$  capacitor, use [Equation 2](#):

$$I_{\text{INRUSH}} = C_L \times \frac{dV_{\text{OUT}}}{dt} \quad (2)$$

where

- $I_{\text{INRUSH}}$  = amount of inrush caused by  $C_L$
- $C_L$  = capacitance on  $V_{\text{OUT}}$
- $dt$  = time it takes for change in  $V_{\text{OUT}}$  during the ramp up of  $V_{\text{OUT}}$  when the device is enabled
- $dV_{\text{OUT}}$  = change in  $V_{\text{OUT}}$  during the ramp up of  $V_{\text{OUT}}$  when the device is enabled

An appropriate  $C_L$  value should be placed on  $V_{\text{OUT}}$  such that the  $I_{\text{MAX}}$  and  $I_{\text{PLS}}$  specifications of the device are not violated.



**Figure 30. Inrush current ( $V_{\text{BIAS}} = 5 \text{ V}$ ,  $V_{\text{IN}} = 1.05 \text{ V}$ ,  $C_L = 100 \mu\text{F}$ )**

### 8.2.2.3 Thermal Considerations

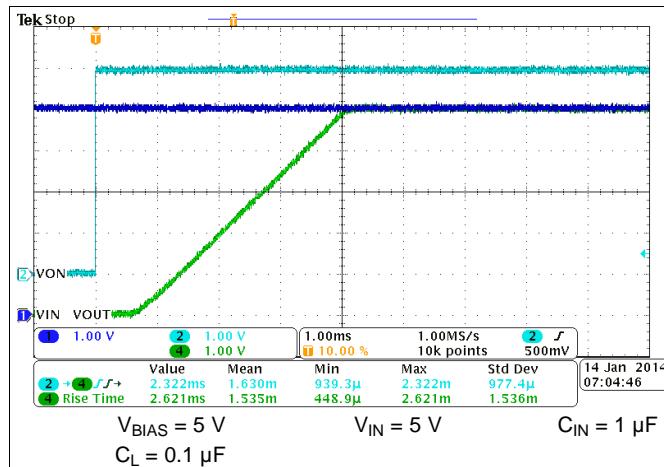
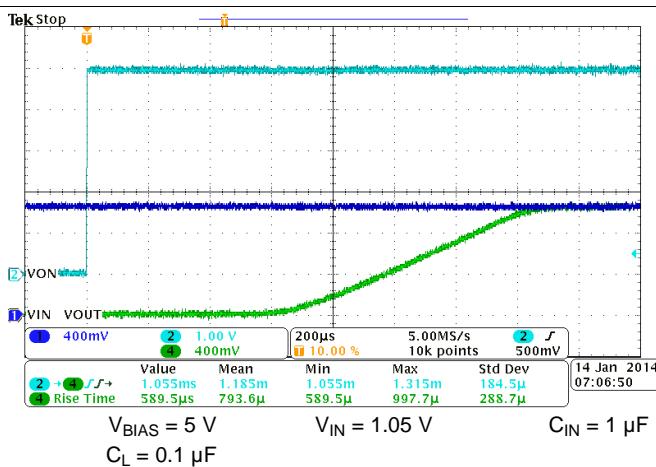
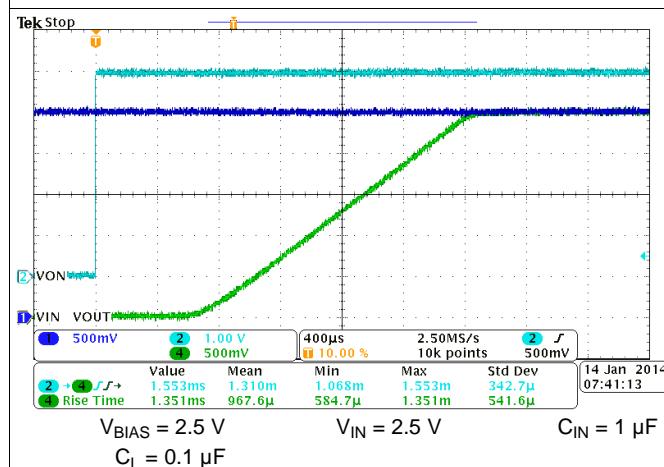
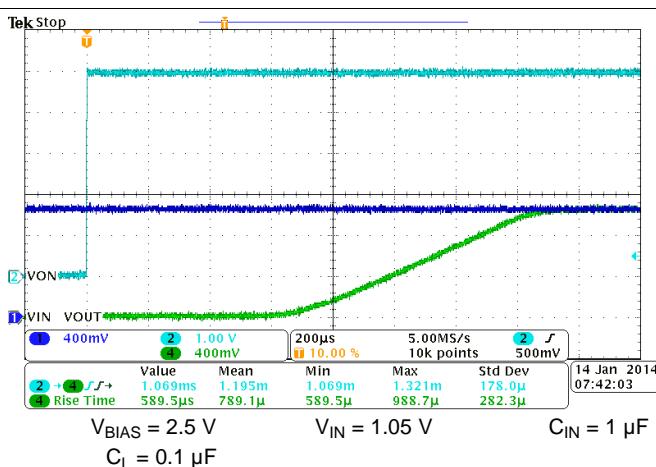
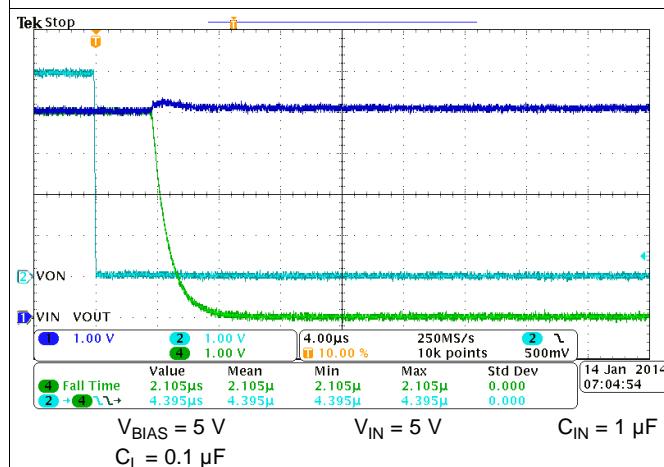
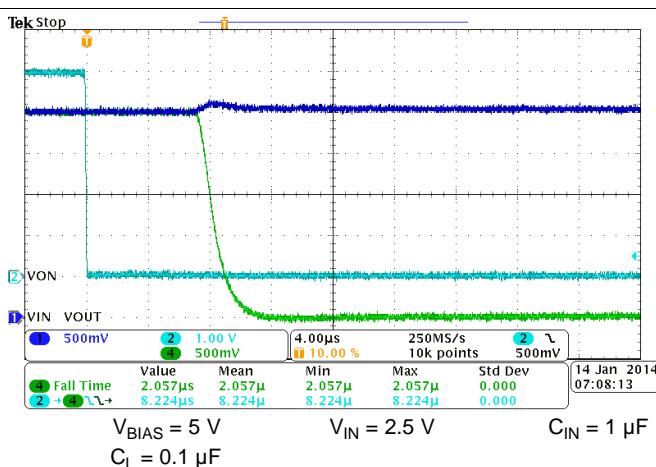
The maximum IC junction temperature should be restricted to  $125^{\circ}\text{C}$  under normal operating conditions. To calculate the maximum allowable dissipation,  $P_{\text{D}(\text{max})}$  for a given output current and ambient temperature, use [Equation 3](#).

$$P_{\text{D}(\text{MAX})} = \frac{T_{\text{J}(\text{MAX})} - T_{\text{A}}}{R_{\theta\text{JA}}} \quad (3)$$

where

- $P_{\text{D}(\text{max})}$  = maximum allowable power dissipation
- $T_{\text{J}(\text{max})}$  = maximum allowable junction temperature ( $125^{\circ}\text{C}$  for the TPS22969)
- $T_{\text{A}}$  = ambient temperature of the device
- $\Theta_{\text{JA}}$  = junction to air thermal impedance. See Thermal Information section. This parameter is highly dependent upon board layout.

### 8.2.3 Application Curves

Figure 31.  $t_R$  at  $V_{BIAS} = 5\text{ V}$ Figure 32.  $t_R$  at  $V_{BIAS} = 5\text{ V}$ Figure 33.  $t_R$  at  $V_{BIAS} = 2.5\text{ V}$ Figure 34.  $t_R$  at  $V_{BIAS} = 2.5\text{ V}$ Figure 35.  $t_F$  at  $V_{BIAS} = 5\text{ V}$ Figure 36.  $t_F$  at  $V_{BIAS} = 5\text{ V}$

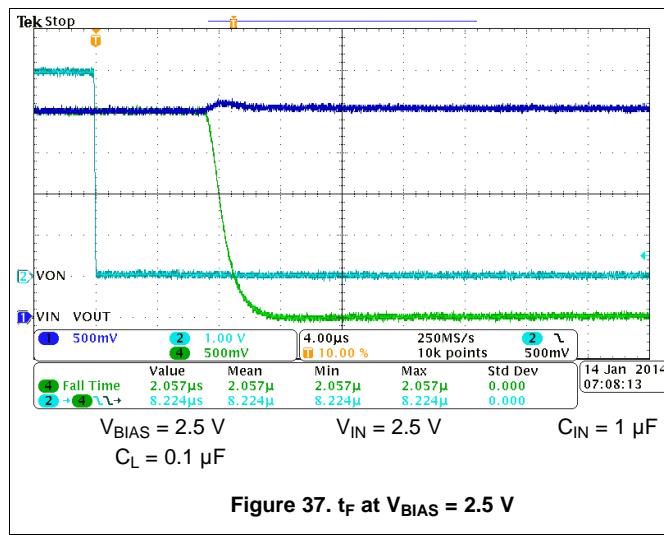


Figure 37.  $t_F$  at  $V_{BIAS} = 2.5 \text{ V}$

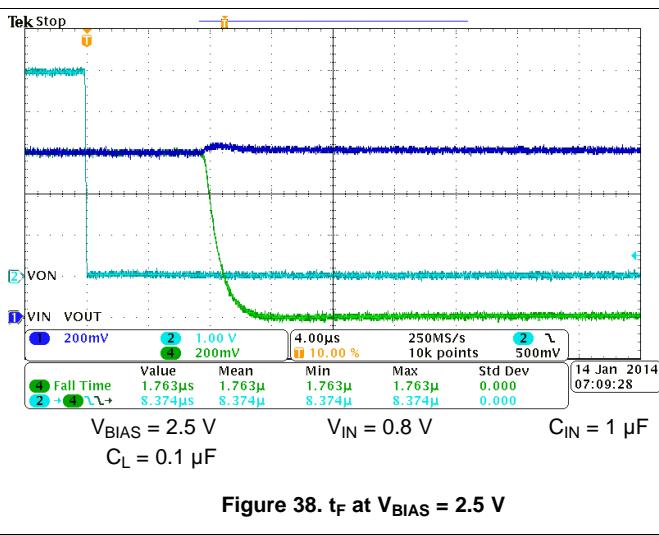


Figure 38.  $t_F$  at  $V_{BIAS} = 2.5 \text{ V}$

## 9 Power Supply Recommendations

The device is designed to operate from a  $V_{BIAS}$  range of 2.5 V to 5.5 V and  $V_{IN}$  range of 0.8 V to 5.5 V. This supply must be well regulated and placed as close to the device pin as possible with the recommended 1- $\mu\text{F}$  bypass capacitor. If the supply is located more than a few inches from the device pins, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 10  $\mu\text{F}$  may be sufficient.

## 10 Layout

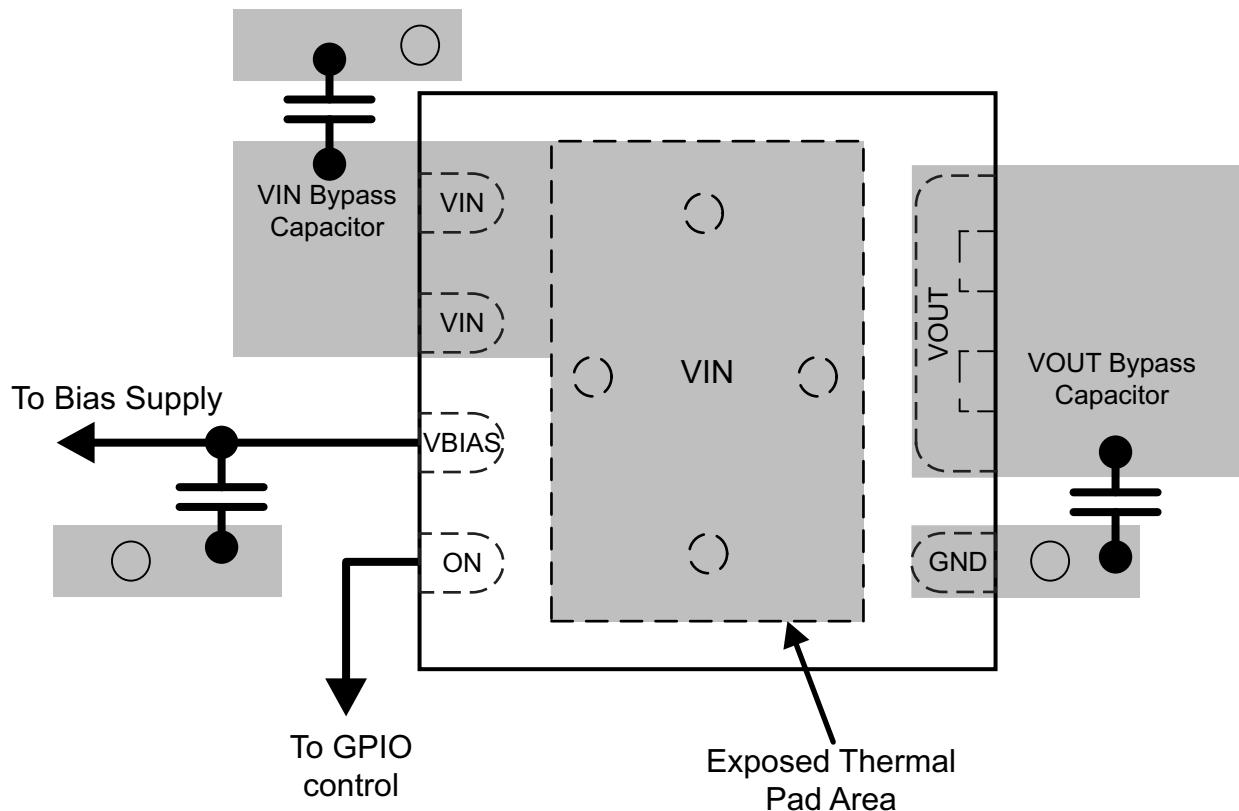
### 10.1 Layout Guidelines

- $V_{IN}$  and  $V_{OUT}$  traces should be as short and wide as possible to accommodate for high current.
- Use vias under the exposed thermal pad for thermal relief for high current operation.
- The  $V_{IN}$  pin should be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 1- $\mu\text{F}$  ceramic with X5R or X7R dielectric. This capacitor should be placed as close to the device pins as possible.
- The  $V_{OUT}$  pin should be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is one-tenth of the  $V_{IN}$  bypass capacitor of X5R or X7R dielectric rating. This capacitor should be placed as close to the device pins as possible.
- The  $V_{BIAS}$  pin should be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 0.1- $\mu\text{F}$  ceramic with X5R or X7R dielectric.

## 10.2 Layout Example

○ VIA to Power Ground Plane

○ VIA to VIN Plane



**Figure 39. Recommended Board Layout**

## 11 Device and Documentation Support

### 11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.2 Trademarks

E2E is a trademark of Texas Instruments.

Ultrabook is a trademark of Intel.

All other trademarks are the property of their respective owners.

### 11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.4 Glossary

[SLYZ022](#) — *TI Glossary.*

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS22969DNYR	Active	Production	WSON (DNY)   8	3000   LARGE T&R	Yes	Call TI   Nipdau	Level-2-260C-1 YEAR	-40 to 85	969A0
TPS22969DNYRG4	Active	Production	WSON (DNY)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	969A0
TPS22969DNYT	Active	Production	WSON (DNY)   8	250   SMALL T&R	Yes	Call TI   Nipdau	Level-2-260C-1 YEAR	-40 to 85	969A0

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

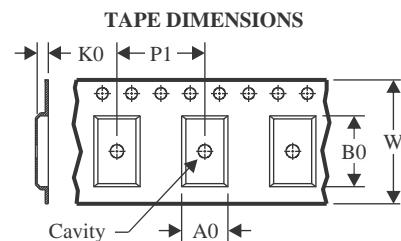
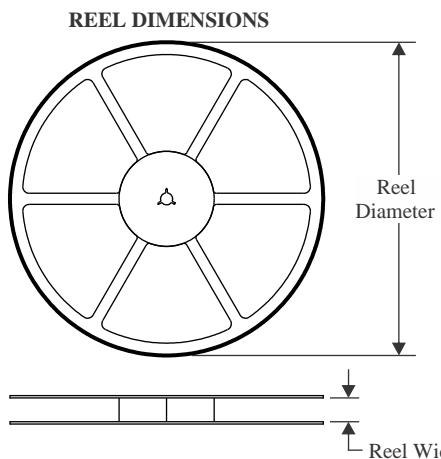
<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

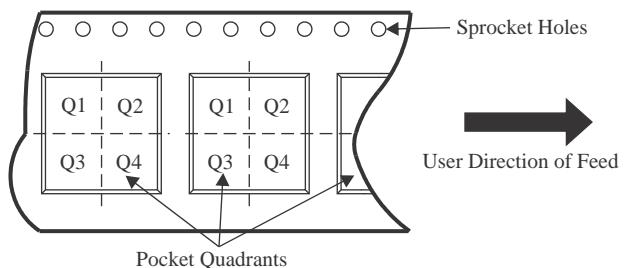
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

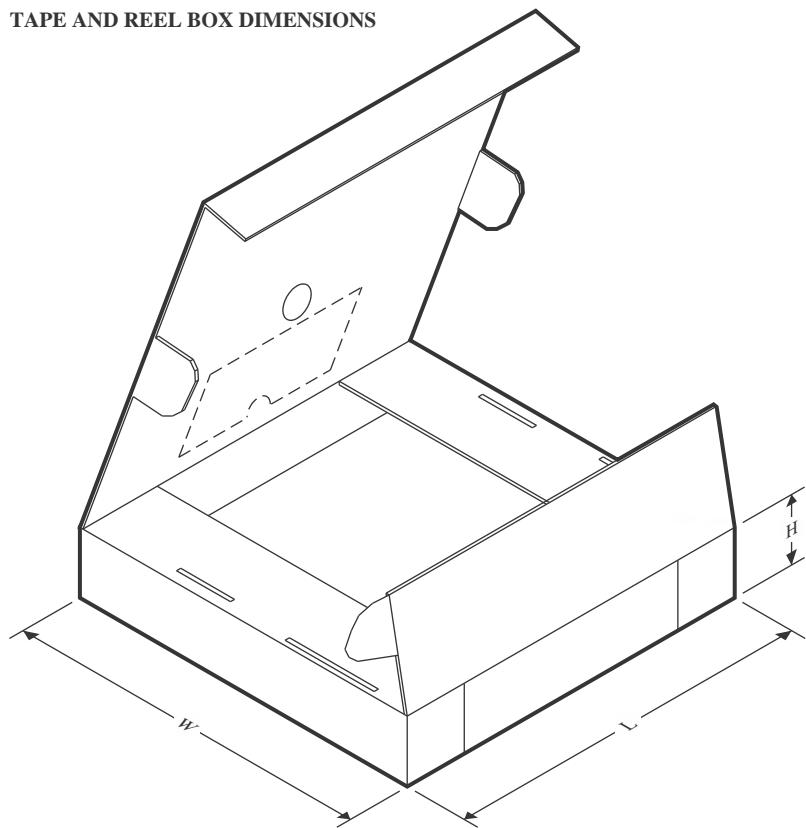
**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22969DNYRG4	WSON	DNY	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

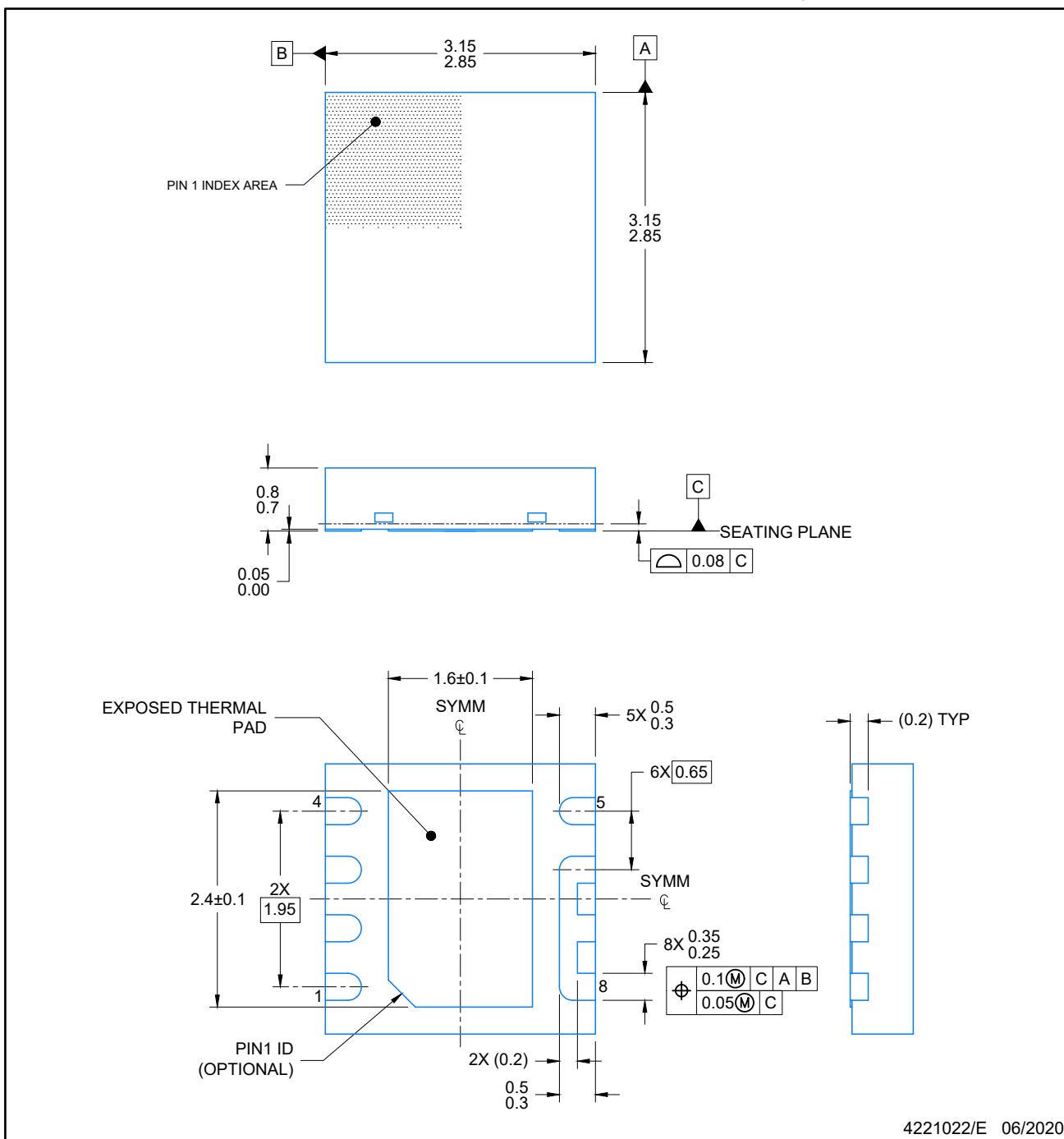
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22969DNYRG4	WSON	DNY	8	3000	367.0	367.0	38.0

# PACKAGE OUTLINE

## WSON - 0.8 mm max height

DNY0008A

PLASTIC QUAD FLATPACK- NO LEAD



4221022/E 06/2020

### NOTES:

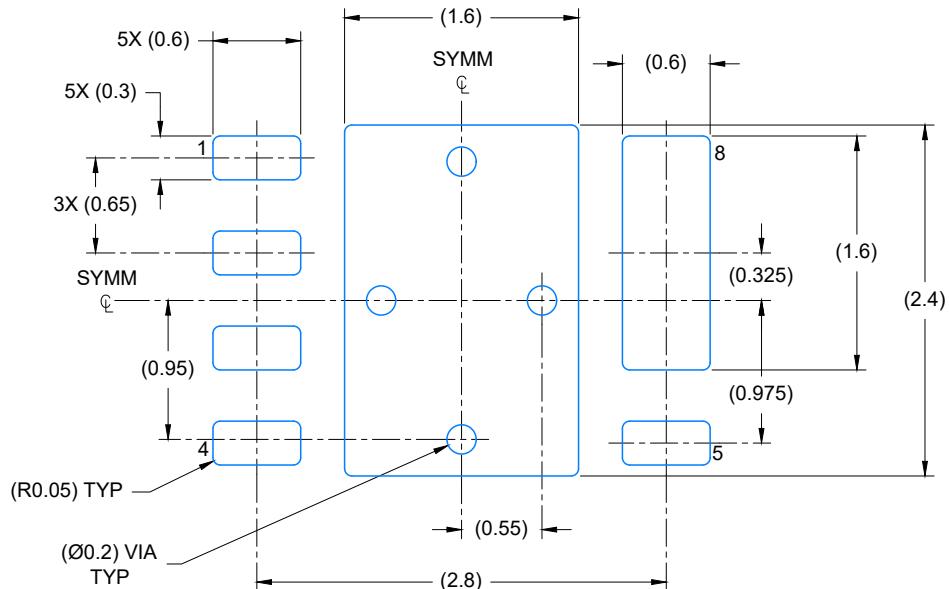
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

WSON - 0.8 mm max height

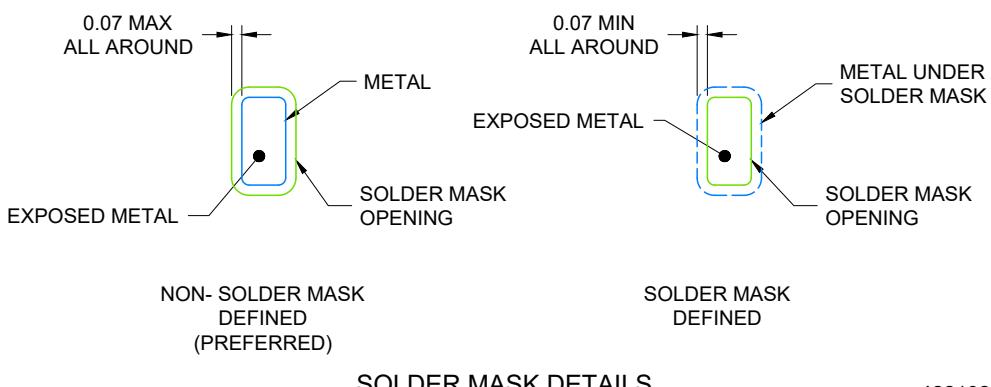
DNY0008A

PLASTIC QUAD FLATPACK- NO LEAD



LAND PATTERN EXAMPLE

SCALE: 20X



SOLDER MASK DETAILS

4221022/E 06/2020

NOTES: (continued)

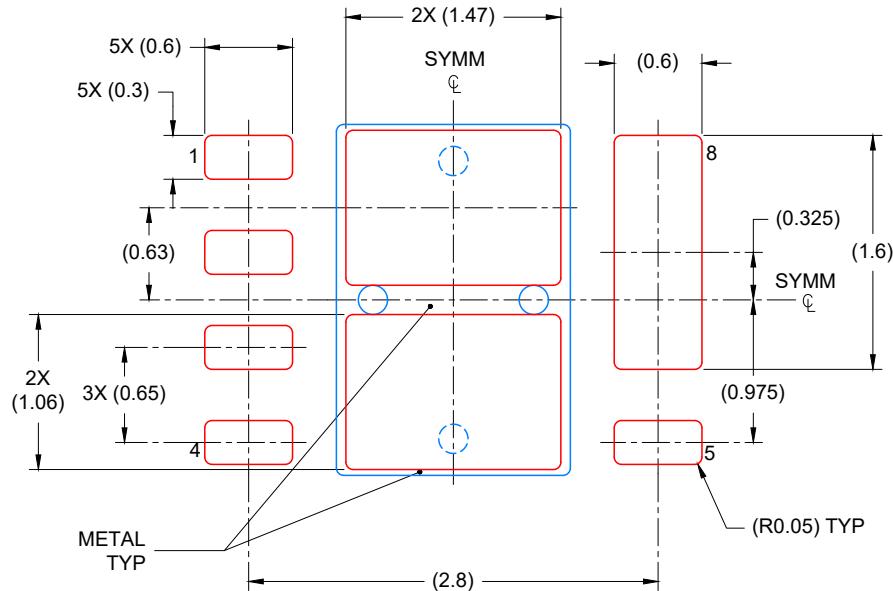
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DNY0008A

WSON - 0.8 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
81% PRINTED COVERAGE BY AREA  
SCALE: 20X

4221022/E 06/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025