TPS281C100x 60V, 100mΩ, Single-Channel Smart High-Side Switch

1 Features

- Wide operating voltage range: 6V to 60V
- Low R_{ON}: 83mΩ typ, 168mΩ max
- Improve system level reliability through adjustable current limiting
  - 1A to 5A (fixed 0.5A)
- Accurate current sensing
  - ±4% at 1A in standard sense mode
  - ±12.5% at 4mA in high accuracy sense mode
- Integrated inductive discharge clamp > 64V
- Low quiescent current (Iq) of < 1.5mA
- Operating junction temperature: –40 to 125°C
- Input control: 1.8V, 3.3V, and 5V logic compatible
- Integrated fault sense voltage scaling for ADC protection
- Open-load detection in off-state
- Thermal shutdown and swing detection
- Enhanced electrical fast transient (EFT) according to IEC61000-4-4
  - Device stays OFF with 22nF output capacitance, ±2kV EFT with DIAG_EN low
- 14-pin thermally-enhanced TSSOP package
- 12-pin thermally-enhanced WSON package

2 Applications

- Digital output module
- Safe torque off (STO)
- Holding brake
- General resistive, inductive, and capacitive loads

3 Description

TPS281C100 is a single channel smart high-side switch designed to meet the requirements of industrial control systems. The low R_{ON} minimizes device power dissipation, driving a wide range of output load current up to 60V DC operation range improves system robustness.

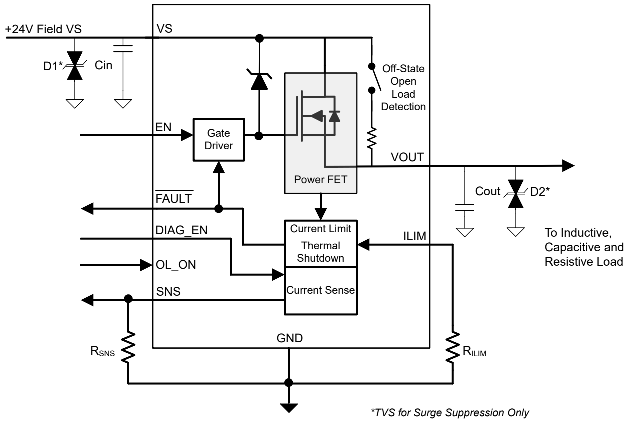
The device integrates protection features such as thermal shut down, output clamp, and current limit. These features improve system robustness during fault events such as short circuit. TPS281C100 implements an adjustable current limiting circuit that improves the reliability of the system by reducing inrush current when driving large capacitive loads and minimizing overload current. In order to drive high inrush current loads such as lamps or fast charging capacitive loads, TPS281C100A implements an inrush current time period with a higher level of allowed current. The device also provides an accurate load current sense that allows for improved load diagnostics such as overload and open-load detection enabling better predictive maintenance.

TPS281C100 is available in a small 14-pin, 4.4mm × 5mm HTSSOP leaded package with 0.65mm pin pitch and 12-pin, 4mm × 4mm WSON with 0.5mm pin pitch minimizing the PCB footprint.

Package Information

PART NUMBER	PACKAGE[1]	PACKAGE SIZE[2]
TPS281C100x	DNT (WSON, 12)	4mm × 4mm
	PWP (HTSSOP, 14)	5mm × 4.4mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Schematic

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4 Device Options

DEVICE VERSION	PART NUMBER	CURRENT LIMIT RANGE	INTEGRATED CLAMP FOR INDUCTIVE LOADS	INRUSH CURRENT PERIOD
A	TPS281C100A(1)	1 A to 5 A (fixed 0.5 A with ILIM short to GND)	Yes	Yes
B	TPS281C100B(1)	1 A to 5 A (fixed 0.5 A with ILIM short to GND)	Yes	No

(1) Devices available in DNT package now. PWP package in preview. Contact TI for additional information.

5 Pin Configuration and Functions

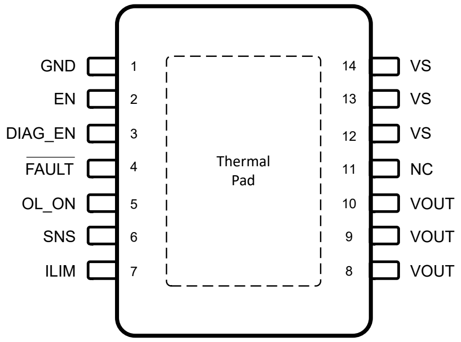


Figure 5-1. PWP Package, 14-Pin HTSSOP (Top View)

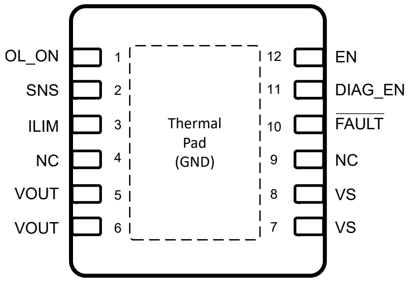


Figure 5-2. DNT Package, 12-Pin WSON (Top View)

Table 5-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	PWP	DNT		
GND	1	Pad	Power	Ground of device. Connect to resistor- diode ground network to have reverse polarity protection.
EN	2	12	I	Input control for channel activation. Internal pulldown.
DIAG_EN	3	11	I	Enable-disable pin for diagnostics and current sensing. Internal pulldown.
$\overline{\text{FAULT}}$	4	10	O	Open drain global fault output. Referred to $\overline{\text{FLT}}$, or fault pin. Active LOW signal.
OL_ON	5	1	I	Enable-disable pin for higher resolution current sense(Only available when $I_{OUT} < I_{Ksns2\_EN}$). Internal pulldown.
SNS	6	2	O	Analog current output corresponding to load current. Connect a resistor to GND to convert to voltage.
ILIM	7	3	O	Adjustable current limit. Connect a resistor to set the current limit. Optionally short to ground or leave pin floating to set the current limit to the default internal current limit. See the electrical characteristics for more information.
NC	11	4, 9	N/A	No internal connection.
VOUT	8, 9, 10	5, 6	Power	Output of high side switch, connect to load.
VS	12, 13, 14	7, 8	Power	Power supply input.
Pad	Thermal Pad	Pad	—	Thermal pad, internally shorted to ground.

Recommended Connection for Unused Pins

TPS281C100x is designed to provide an enhanced set of diagnostic and protection features. However, if the system design only allows for a limited number of I/O connections, some pins may be considered as optional.

Table 5-2. Connections for Optional Pins

PIN NAME	CONNECTION IF NOT USED	IMPACT IF NOT USED
SNS	Ground through 10-kΩ resistor	Analog sense is not available.
ILIM	Float	If the ILIM pin is left floating, the device will be set to the default internal current-limit threshold.
$\overline{\text{FAULT}}$	Float	If the $\overline{\text{FAULT}}$ pin is unused, the system cannot read faults from the output.
DIAG_EN	Float or ground through R_{PROT} resistor	With DIAG_EN unused, the analog sense, open-load, and short-to-supply diagnostics are not available.

Table 5-2. Connections for Optional Pins (continued)

PIN NAME	CONNECTION IF NOT USED	IMPACT IF NOT USED
OL_ON	Ground through R_{PROT} resistor	With OL_ON unused, the high accuracy sense mode is not available.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Continuous supply voltage, V_S with respect to IC GND: Version A, B		–0.7	64	V
Continuous supply voltage, V_{OUT} with respect to IC GND: Version A, B		–60	64	V
Transient (< 100µs) voltage at the supply pin, V_S with respect to IC GND: Version A, B		–0.7	81	V
Enable pin voltage, V_{EN}		–1	6	V
OL_ON pin voltage, V_{OL_ON}		–1	6	V
DIAG_EN pin voltage, V_{DIAG_EN}		–1	6	V
Sense pin voltage, V_{SNS}		–1	6	V
$\overline{\text{FAULT}}$ pin voltage, $V_{\overline{FAULT}}$		–1	6	V
Reverse ground current, I_{GND}	V_S < 0V		–50	mA
Maximum junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins except VS and VOUT	±2000	V
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	VS and VOUT with respect to GND	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	All pins	±750	V
$V_{(ESD4)}$	Electrostatic discharge	Contact discharge, per IEC 61000-4-2 (3)	VS and VOUT	±8000	V
$V_{(EFT)}$	Electrostatic discharge	Electrical fast transient, per IEC 61000-4-4 (3)	VS and VOUT	±2000	V
$V_{(surge)}$	Electrostatic discharge	Surge protection with 42Ω, per IEC 61000-4-5; 1.2/50µs (4)	VS and VOUT	±1000	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
(3) Tested with application circuit and supply voltage (VS) of 24V, ENx pins High (Output Enabled) and EN pins Low (Output Disabled).
(4) Tested with application circuit and supply voltage (VS) of 24V, ENx pins High (Output Enabled) and EN pins Low (Output Disabled). External TVS at VS and VOUT required. Please refer to the IEC 61000-4-5 Surge section.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
$V_{S\_OP\_NOM}$	Nominal supply voltage	6.0	60	V
V_{EN}	Enable voltage	–1	5.5	V
V_{OL_ON}	OL_ON pin voltage, V_{OL_ON}	–1	5.5	V
V_{DIAG_EN}	Diagnostic Enable voltage	–1	5.5	V
V_{FAULT}	$\overline{\text{FAULT}}$ pin voltage	–1	5.5	V
V_{SNS}	Sense voltage	–1	5.5	V

6.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
T_A	Operating free-air temperature	–40	125	°C

(1) All operating voltage conditions are measured with respect to device GND

6.4 Thermal Information

THERMAL METRIC(1) (2)		TPS281C100x		UNIT
		DNT (WSON)	PWP (HTSSOP)	
		12 PINS	14 PINS	
$R_{θJA}$	Junction-to-ambient thermal resistance	36.9	TBD	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	24.4	TBD	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	13.7	TBD	°C/W
$Ψ_{JT}$	Junction-to-top characterization parameter	0.4	TBD	°C/W
$Ψ_{JB}$	Junction-to-board characterization parameter	13.7	TBD	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	1.1	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the SPRA953 application report.
(2) The thermal parameters are based on a 4-layer PCB according to the JESD51-5 and JESD51-7 standards.

6.5 Electrical Characteristics

V_S = 6V to 60V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
VS SUPPLY VOLTAGE AND CURRENT							
IL_{NOM}	Continuous load current	V_{EN} = HI	T_{AMB} = 85°C		4		A
$I_{IDLE, VS}$	Total device idle state current (including MOSFET) with diagnostics disabled	VS ≤ 60V, V_{EN} = V_{DIAG_EN} = LO, V_{OUT} = 0V	T_J = –40°C to 85°C		1	1.3	mA
			T_J = 150°C			1.5	mA
I_{IDLE, VS_DIAG}	V_S standby idle state current with diagnostics enabled	VS ≤ 60V, V_{EN} = LO, V_{DIAG_EN} = HI, V_{OUT} = 0V			1.2	1.7	mA
$I_{Q, VS}$	V_S quiescent current with diagnostics disabled	V_{EN} = V_{DIAG_EN} = 0V	I_{OUT} = 0A		0.98	1.3	mA
I_{Q, VS_DIAG}	V_S quiescent current with diagnostics enabled	V_{ENx} = V_{DIAG_EN} = 0V	I_{OUT} = 0A		1.2	1.5	mA
$I_{OUT(OFF,SINK)}$	Output sink current	VS ≤ 60V, V_{EN} = 0V, V_{OUT} = 24V, V_{DIAG} = 0V	T_J = –40°C to 85°C		2.1	2.8	mA
			T_J = 150°C		2.3	2.6	mA
$V_{OUT(OFF)}$	Output floating voltage	VS ≤ 60V, V_{EN} = 0V, V_{OUT} floating, V_{DIAG} = 0V	T_J = –40°C to 85°C			0.9	V
			T_J = 150°C			0.9	V
VS UNDERVOLTAGE LOCKOUT (UVLO) INPUT							
$V_{S,UVLOR}$	V_S undervoltage lockout rising	Measured with respect to the GND pin of the device		5.0	5.4	5.75	V
$V_{S,UVLOF}$	V_S undervoltage lockout falling			4.1	4.5	4.85	V
VDS CLAMP							
$V_{DS,Clamp}$	V_{DS} clamp voltage	FET current = 10mA	V_S = 24V	64	75	81	V
			V_S = 6V	48	53	58	V
RON CHARACTERISTICS							

6.5 Electrical Characteristics (continued)

V_S = 6V to 60V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
R_{ON}	On-resistance	0.5A ≤ I_{OUT} ≤ 3A, V_S = 6V to 60V	T_J = 25°C		83		mΩ
			T_J = 125°C			168	mΩ
			T_J = 150°C			180	mΩ
$R_{ON(REV)}$	On-resistance during reverse polarity	0.5A ≤ I_{OUT} ≤ 3A, V_S = –24V	T_J = –40°C to 150°C			180	mΩ
R_{ON_AUX}	VS to VOUT On-resistance High Accuracy Sense Mode	V_S = 24V, I_{OUT} = 40 mA OL_ON=DIAG_EN=5V	T_J = –40°C to 150°C		4.7	12	Ω
CURRENT LIMIT CHARACTERISTICS							
K_{CL}	Current Limit Ratio		$I_{CL, typ}$ = 5.26A		52.6		A × kΩ
			$I_{CL, typ}$ = 4.15A		51.9		A × kΩ
			$I_{CL, typ}$ = 3.04A		50.8		A × kΩ
			$I_{CL, typ}$ = 1.98A		49.5		A × kΩ
			$I_{CL, typ}$ = 0.96A		48		A × kΩ
$I_{LIM\_STARTUP}$	Peak current limit when switch is enabled (A version)		R_{ILIM} = 10kΩ to 50kΩ		2 × I_{CL}	6.5	A
$t_{LIM\_STARTUP\_DELAY}$	Delay time for device to remain in $I_{LIM\_STARTUP}$ level (A Version)					12	ms
I_{CL}	Current Limit level	Short circuit condition, V_{DS} = 1V	R_{ILIM} = 50kΩ	0.73	0.96	1.11	A
			R_{ILIM} = 25kΩ	1.5	1.98	2.3	A
			R_{ILIM} = 16.7kΩ	2.3	3.04	3.5	A
			R_{ILIM} = 12.5kΩ	3.15	4.15	4.77	A
			R_{ILIM} = 10kΩ	4	5.26	6.3	A
			R_{ILIM} = GND, open, or out of range(< 5kΩ, and > 150kΩ)	0.35	0.48	0.6	A
I_{CL_LINPK}	Overcurrent Limit Threshold(1)	Overload condition	R_{ILIM} = 25kΩ			1.5 × I_{CL}	A
I_{CL_ENPS}	Peak current enabling into permanent short		R_{ILIM} = 50kΩ			4 × I_{CL}	A
			R_{ILIM} = 25kΩ			3.3 × I_{CL}	A
			R_{ILIM} short to GND			5.7 × I_{CL}	A
I_{CL_ENPS2}	Peak current enabling into permanent short		R_{ILIM} = 10kΩ, t < $I_{LIM\_STARTUP\_DELAY}$			2 × $I_{LIM\_STARTUP}$	A
t_{IOS}	Short circuit response time	VS = 24V			0.5		µs
THERMAL SHUTDOWN CHARACTERISTICS							
T_{ABS}	Thermal shutdown			165	185		°C
T_{REL}	Relative thermal shutdown				77		°C
t_{RETRY}	Retry time (2)	Time from fault shutdown until switch re-enable (thermal shutdown).			2		ms
Fault Response	Fault reponse to Thermal Shutdown			Auto-retry			
T_{HYS}	Absolute Thermal shutdown hysteresis				10		°C
FAULT PIN CHARACTERISTICS							

6.5 Electrical Characteristics (continued)

V_S = 6V to 60V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{FAULT}	$\overline{\text{FAULT}}$ low output voltage	$I_{\overline{FAULT}}$ = 2.5mA				0.5	V
$t_{FAULT\_BLANKING}$	Fault blanking time during startup (A and B Version)		V_{DIAG_EN} = 5V, V_{EN} = 0 to 5V			12	ms
t_{FAULT_FLT}	Fault indication-time	Time between fault and $\overline{\text{FAULT}}$ asserting				75	µs
t_{FAULT_SNS}	Fault indication-time	V_{DIAG_EN} = 5V Time between fault and I_{SNS} settling at V_{SNSFH}				106	µs
CURRENT SENSE CHARACTERISTICS							
I_{KSNS2_EN}	Load current supported to enable K_{SNS2} when in K_{SNS} Mode	V_{EN} = V_{DIAG_EN} = 5V, V_{OL_ON} = GND		21	25	30	mA
I_{KSNS2_DIS}	Load current to disable K_{SNS2} when in K_{SNS2} Mode	V_{EN} = V_{DIAG_EN} = 5V, V_{OL_ON} = GND		75	85	105	mA
K_{SNS1}	Current sense ratio - Standard Sensing I_{OUT} / I_{SNS}	I_{OUT} = 1A, V_{OL_ON} = GND			800		A/A
K_{SNS2}	Current sense ratio - High Accuracy Sensing I_{OUT} / I_{SNS}	I_{OUT} = 20mA, V_{OL_ON} = 5V			24		A/A
I_{SNS}	Current sense current	V_{EN} = V_{DIAG_EN} = 5V, V_{OL_ON} = GND	I_{OUT} = 4A		5		mA
				–4		6	%
			I_{OUT} = 3.5A		4.375		mA
				–4		4	%
			I_{OUT} = 3A		3.75		mA
				–4		4	%
			I_{OUT} = 2A		2.5		mA
				–4		4	%
			I_{OUT} = 1A		1.25		mA
				–4		4	%
			I_{OUT} = 0.75A		0.9375		mA
				–6		6	%
			I_{OUT} = 0.5A		0.625		mA
				–6		6	%
			I_{OUT} = 250mA		0.3125		mA
				–10		10	%
			I_{OUT} = 150mA		0.1875		mA
				–10		10	%
			I_{OUT} = 60mA		0.075		mA
				–25		25	%
			I_{OUT} = 30mA		0.0375		mA
				–25		25	%

6.5 Electrical Characteristics (continued)

V_S = 6V to 60V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{SNS2}	Current sense current and accuracy for high accuracy sense mode	$V_{EN} = V_{DIAG\_EN}$ = 5V, V_{OL_ON} = 5V	I_{OUT} = 20mA		0.833		mA
				–6		6	%
			I_{OUT} = 10mA		0.404		mA
				–10		10	%
			I_{OUT} = 4mA		0.161		mA
				–12.5		12.5	%
			I_{OUT} = 2mA		0.0800		mA
				–15		15	%
			I_{OUT} = 1mA		0.0395		mA
				–20		20	%
SNS PIN CHARACTERISTICS							
V_{SNSFH}	V_{SNS} fault high-level	V_{DIAG_EN} = 5V		4.5	5	5.77	V
		V_{DIAG_EN} = 3.3V, R_{SNS}=Open		3.3	3.95	4.4	V
		$V_{DIAG\_EN} = V_{IH}$		2.9	3.2	3.5	V
I_{SNSFLT}	I_{SNS} fault high-level	$V_{DIAG\_EN} > V_{IH,DIAG\_EN}$		5.2	6.4		mA
$I_{SNSleak}$	I_{SNS} leakage	V_{DIAG_EN} = 5V, IL = 0mA				1.3	µA
V_{S_ISNS}	V_S for full current sense and fault functionality	V_{DIAG_EN} = 3.3V		5.9			V
		V_{DIAG_EN} = 5V		7.1			V
OPEN LOAD DETECTION CHARACTERISTICS							
V_{OL_OFF}	OFF state open-load (OL) detection voltage	V_{EN} = 0V, V_{DIAG_EN} = 5V		1.4	2	2.6	V
R_{OL_OFF}	OFF state open-load (OL) detection internal pull-up resistor	V_{EN} = 0V, V_{DIAG_EN} = 5V	V_S = 6V	110	133	150	kΩ
			V_S = 24V	114	140	166	kΩ
			V_S = 48V	120	140	166	kΩ
t_{OL_OFF}	OFF state open-load (OL) detection deglitch time	V_{EN} = 0V, V_{DIAG_EN} = 5V, When Vs – $V_{OUT} < V_{OL}$, duration longer than t_{OL}. Open load detected.			480	1050	µs
$t_{OL\_OFF\_1}$	OL_OFF and STB indication-time from EN falling	V_{EN} = 5V to 0V, V_{DIAG_EN} = 5V I_{OUT} = 0mA, V_{OUT} = Vs - V_{OL}			310	905	µs
$t_{OL\_OFF\_2}$	OL and STB indication-time from DIA_EN rising	V_{EN} = 0V, V_{DIAG_EN} = 0V to 5V I_{OUT} = 0mA, $V_{OUT} = V_S - V_{OL}$				1080	µs
OL_ON PIN CHARACTERISTICS							
V_{IL, OL_ON}	Input voltage low-level					0.8	V
V_{IH, OL_ON}	Input voltage high-level			1.5			V
V_{IHYS, OL_ON}	Input voltage hysteresis				282		mV
R_{OL_ON}	Internal pulldown resistor			0.7	1	1.3	MΩ
$I_{IL\_OL\_ON}$	Input current low-level	V_{OL_ON} = -1V		–25		0	µA
I_{IL, OL_ON}	Input current low-level	V_{OL_ON} = 0.8V		0.6	.8	1.2	µA
I_{IH, OL_ON}	Input current high-level	V_{OL_ON} = 5V		3	5	7	µA
DIAG_EN PIN CHARACTERISTICS							
$V_{IL, DIAG\_EN}$	Input voltage low-level	No GND Network				0.8	V
$V_{IH, DIAG\_EN}$	Input voltage high-level	No GND Network		1.5			V
$V_{IHYS, DIAG\_EN}$	Input voltage hysteresis				270		mV
R_{DIAG_EN}	Internal pulldown resistor			200	350	500	kΩ

6.5 Electrical Characteristics (continued)

V_S = 6V to 60V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{IL,\ DIAG\_EN}$	Input current low-level	V_{DIAG_EN} = 0.8V, V_{EN}=0V		2.9		µA
$I_{IH,\ DIAG\_EN}$	Input current high-level	V_{DIAG_EN} = 5V		14		µA
EN PIN CHARACTERISTICS						
$V_{IL,\ EN}$	Input voltage low-level	No GND Network			0.8	V
$V_{IH,\ EN}$	Input voltage high-level	No GND Network	1.5			V
$V_{IHYS,\ EN}$	Input voltage hysteresis			300		mV
R_{EN}	Internal pulldown resistor		200	350	500	kΩ
$I_{IL,\ EN}$	Input current low-level	V_{EN} = 0.8V		2.2		µA
$I_{IH,\ EN}$	Input current high-level	V_{EN} = 5V		14		µA

(1) The maximum current output under overload condition before current limit regulation.
(2) Data not tested in production.

6.6 SNS Timing Characteristics

V_S = 6V to 60V, T_A = –40°C to 125°C (unless otherwise noted), parameters not tested in production

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNS TIMING - CURRENT SENSE						
$t_{SNSION1}$	Settling time from rising edge of DIAG_EN 50% of V_{DIAG_EN} to 90% of settled ISNS	V_{EN}= 5V, V_{DIAG_EN} = 0V to 5V, V_{OL_ON} = 0V , R_{SNS} = 1kΩ, I_L = 1A			15	µs
		V_{EN} = 5V, V_{DIAG_EN} = 0V to 5V, V_{OL_ON} = 0V , R_{SNS} = 1kΩ, I_L = 50mA			80	µs
$t_{SNSION2}$	Settling time from rising edge of EN and DIAG_EN 50% of V_{DIAG_EN} V_{EN} to 90% of settled ISNS	V_{EN} = V_{DIAG_EN} = 0V to 5V V_S = 24V R_{SNS} = 1 kΩ, I_L = 1A			200	µs
$t_{SNSION3}$	Settling time from rising edge of EN 50% of V_{EN} to 90% of settled ISNS	V_{EN} = 0V to 5V, V_{DIAG_EN} = 5V R_{SNS} = 1kΩ, I_L = 1A			200	µs
$t_{SNSION4}$	Settling time from rising edge of OL_ON 50% of V_{OL_ON} to 90% of settled ISNS	V_{OL_ON} = 0 to 5V, V_{EN} = V_{DIAG_EN} = 5V R_{SNS} = 1kΩ, I_L = 6mA			60	µs
$t_{SNSION5}$	Settling time from falling edge of I_L < I_{KSNS2_EN} to 90% of settled ISNS	V_{OL_ON} = V_{EN} = V_{DIAG_EN} = 5V R_{SNS} = 1kΩ, I_L = 100mA to 10mA			60	µs
$t_{SNSION6}$	Settling time from Rising edge of I_L > $I_{KSNS2\_DIS.}$ to 90% of settled ISNS	V_{OL_ON} = V_{EN} = V_{DIAG_EN} = 5V R_{SNS} = 1kΩ, I_L = 10mA to 100mA			60	µs
$t_{KSNS2\_DIS\_DGL}$	Deglitch time for transition of I_L > $I_{KSNS2\_DIS.}$	V_{OL_ON} = V_{EN} = V_{DIAG_EN} = 5V R_{SNS} = 1kΩ, I_L = 10mA to 100mA			30	µs
$t_{SNSIOFF}$	Settling time from falling edge of DIAG_EN	V_{EN} = 5V, V_{DIAG_EN} = 5V to 0V R_{SNS} = 1kΩ, R_L = 48Ω			20	µs
$t_{SETTLEH}$	Settling time from rising edge of load step. 50% of V_{OL_ON} to 90% of settled ISNS	V_{EN} = V_{DIAG_EN} = 5V R_{SNS} = 1kΩ, I_{OUT} = 0.5A to 3A			20	µs
$t_{SETTLEL}$	Settling time from falling edge of load step. 50% of V_{OL_ON} to 10% of settled ISNS	V_{EN} = V_{DIAG_EN} = 5V R_{SNS} = 1kΩ, I_{OUT} = 3A to 0.5A			20	µs
$t_{TIMEOUT}$	Time to indicate VSNSFH due to VS-VOUT>2V. From rising edge of EN, DIAG_EN and OL_ON 50% of V_{DIA_EN} V_{EN} $V_{OL_ON}$to 50% of rising edge of VSNSFH	V_{DIAG_EN} = V_{EN} = V_{OL_ON} = 0V to 5V R_{SNS} = 1kΩ, I_{OUT} = 5mA C_{OUT} =50µF		245		µs

6.6 SNS Timing Characteristics (continued)

V_S = 6V to 60V, T_A = –40°C to 125°C (unless otherwise noted), parameters not tested in production

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SNSFH}	Assertion time for SNSFH From 50% rising edge of VSNSFH to 50% of falling edge of VSNSFH	V_{DIAG_EN} = V_{EN} = V_{OL_ON} = 0V to 5V R_{SNS} = 1kΩ, I_{OUT} = 5mA C_{OUT} =15μF	60			μs

6.7 Switching Characteristics

VS = 6V to 60V, T_A = –40°C to 125°C (unless otherwise noted), C_{OUT} = 22nF

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DR}	Turnon delay time (from delay or diagnostic)	V_S = 24V, R_L = 48Ω 50% of EN to 20% of VOUT		17	45	μs
t_{DF}	Turnoff delay time	V_S = 24V, R_L = 48Ω 50% of EN to 80% of VOUT	10	18	26	μs
SR_R	VOUT rising slew rate	V_S = 24V, 20% to 80% of V_{OUT}, R_L = 48Ω	2.3	3.6	4.6	V/μs
SR_F	VOUT falling slew rate	V_S = 24V, 80% to 20% of V_{OUT}, R_L = 48Ω	2.3	3.5	4.8	V/μs
t_{ON}	Turnon time	V_S = 24V, R_L = 48Ω 50% of EN to 80% of VOUT		20	40	μs
t_{OFF}	Turnoff time	V_S = 24V, R_L = 48Ω 50% of EN to 20% of VOUT		20	40	μs
t_{ON} - t_{OFF}	Turn-on and off matching	1ms ON time switch enable pulse	–25		70	μs
Δ_{PWM}	PWM accuracy - average load current	200μs enable pulse, V_S = 24V, R_L = 48Ω F = f_{max}	–15		15	%

6.8 Typical Characteristics

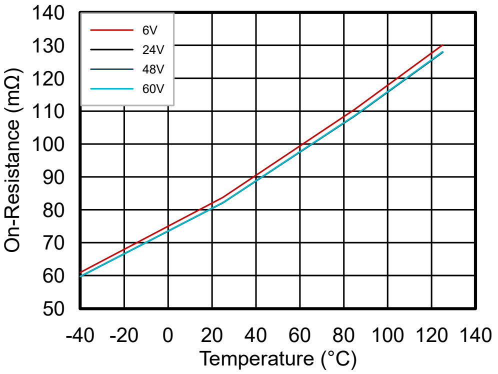
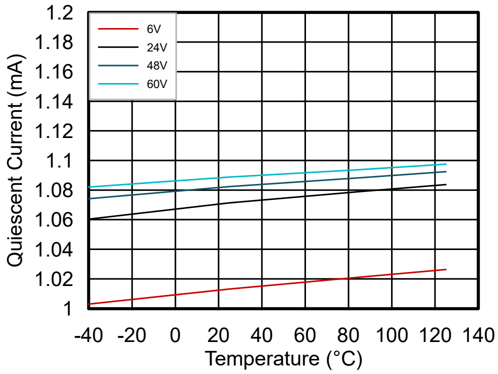
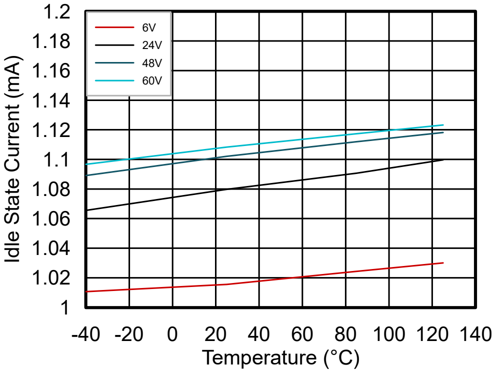


Figure 6-1. On-Resistance (R_{ON}) vs Temperature vs VS Supply Voltage



V_{EN} = 5 V V_{DIAG_EN} = 0 V

Figure 6-2. Quiescent Current ($I_{Q,\ VS}$) From VS Input Supply vs Temperature vs VS Voltage



V_{EN} = 0 V V_{DIAG_EN} = 0 V

Figure 6-3. Idle State Current ($I_{IDLE,\ VS}$) From VS Input Supply vs Temperature vs VS Voltage

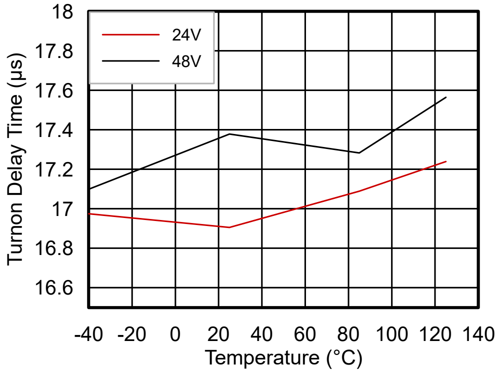


Figure 6-4. Turn-on Delay Time (t_{DR}) vs Temperature vs VS Voltage

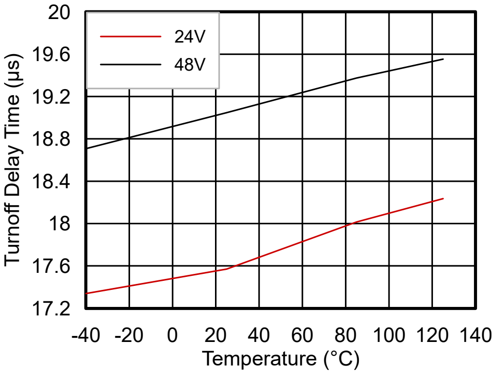


Figure 6-5. Turn-off Delay Time (t_{DF}) vs Temperature vs VS Voltage

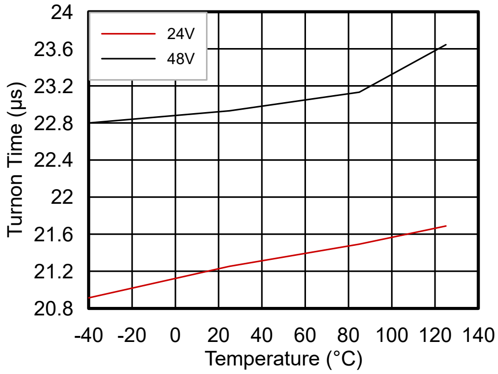


Figure 6-6. Turn-on Time (t_{ON}) vs Temperature vs VS Voltage

6.8 Typical Characteristics (continued)

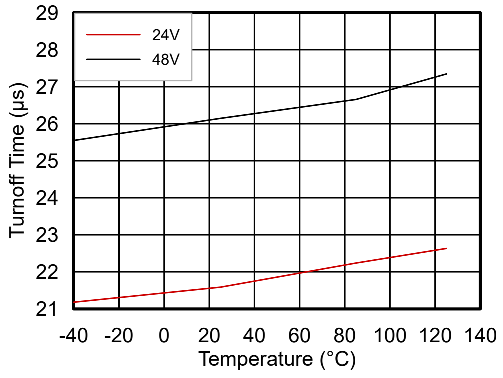
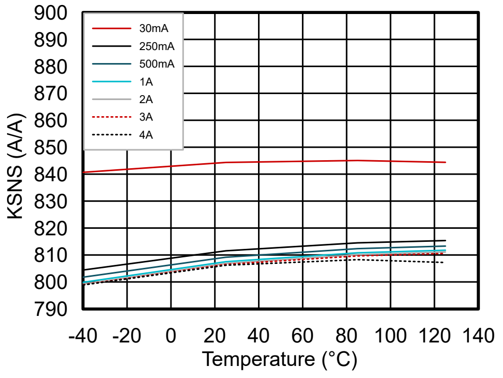
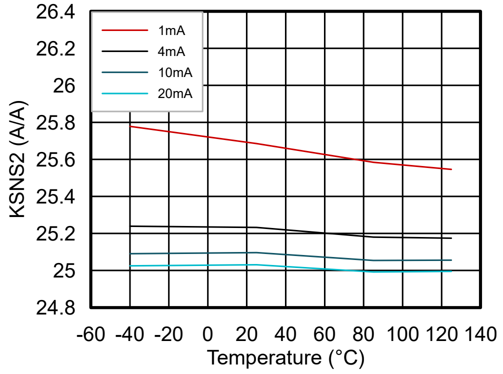


Figure 6-7. Turn-off Time (t_{OFF}) vs Temperature vs VS Voltage



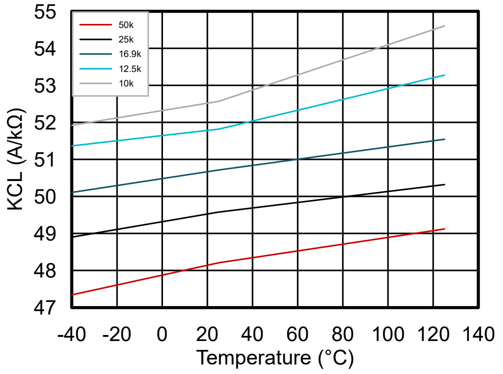
VS = 24 V

Figure 6-8. Current Sense Ratio (KSNS) vs Temperature vs Load Current



VS = 24 V

Figure 6-9. Current Sense Ratio ($KSNS_2$) vs Temperature vs Load Current



VS = 24 V

Figure 6-10. Current Limit Ratio (K_{CL}) vs Temperature vs R_{ILIM}

7 Parameter Measurement Information

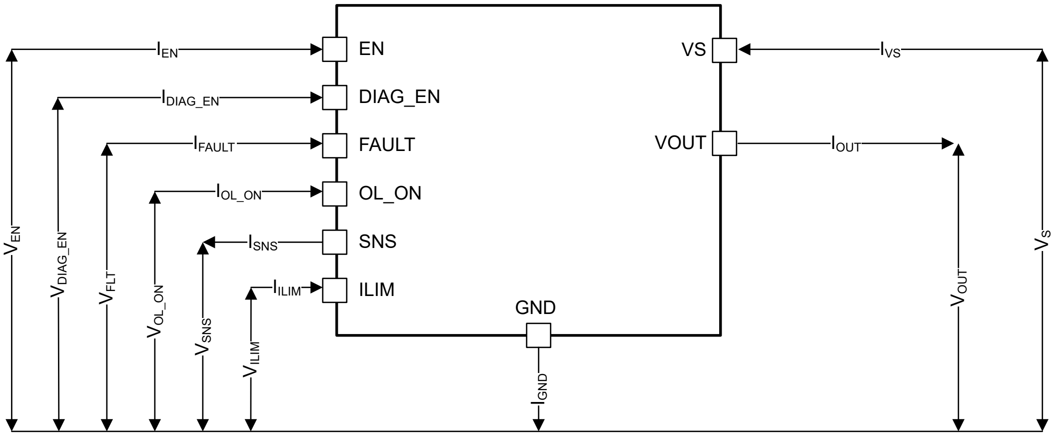
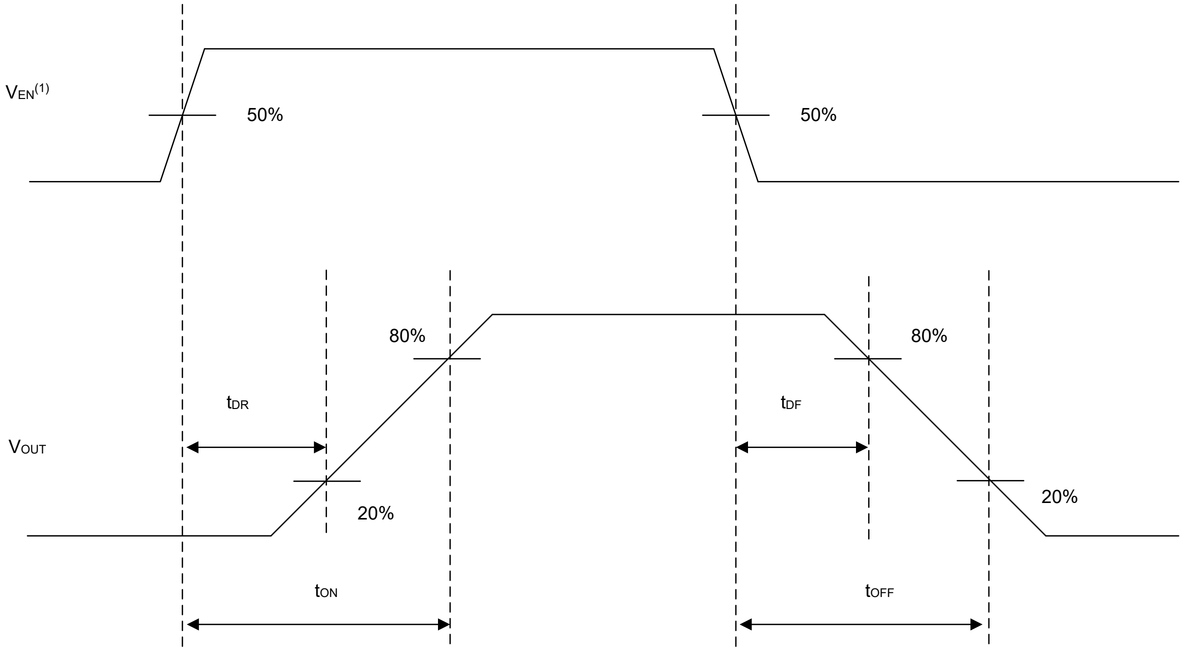
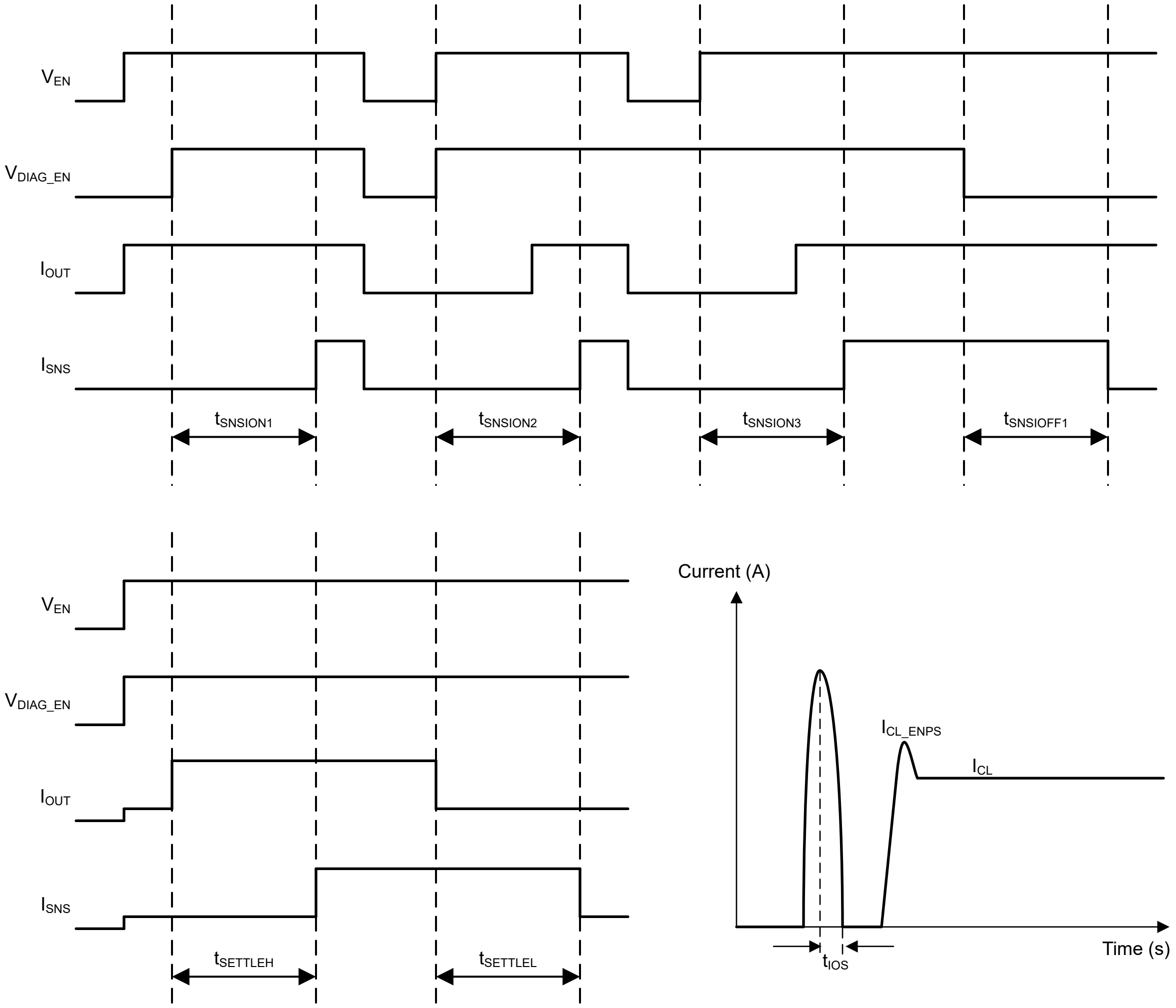


Figure 7-1. Parameter Definitions



(1) Rise and fall time of V_{EN} is 100 ns.

Figure 7-2. Switching Characteristics Definitions



Rise and fall times of control signals are 100 ns. Control signals include: EN, DIA_EN.

Figure 7-3. SNS Timing Characteristics Definitions

8 Detailed Description

8.1 Overview

The TPS281C100 is a single-channel, fully-protected, high-side power switch with an integrated NMOS power FET and charge pump. Full diagnostics and high-accuracy current-sense features enable intelligent control of the load. Low logic high threshold, V_{IH}, of 1.5V on the input pins allow use of MCU's down to 1.8V. A programmable current-limit function greatly improves the reliability of the whole system. The device diagnostic reporting has two pins to support both digital status and analog current-sense output, both of which can be set to the high-impedance state when diagnostics are disabled, for multiplexing the MCU analog or digital interface among devices.

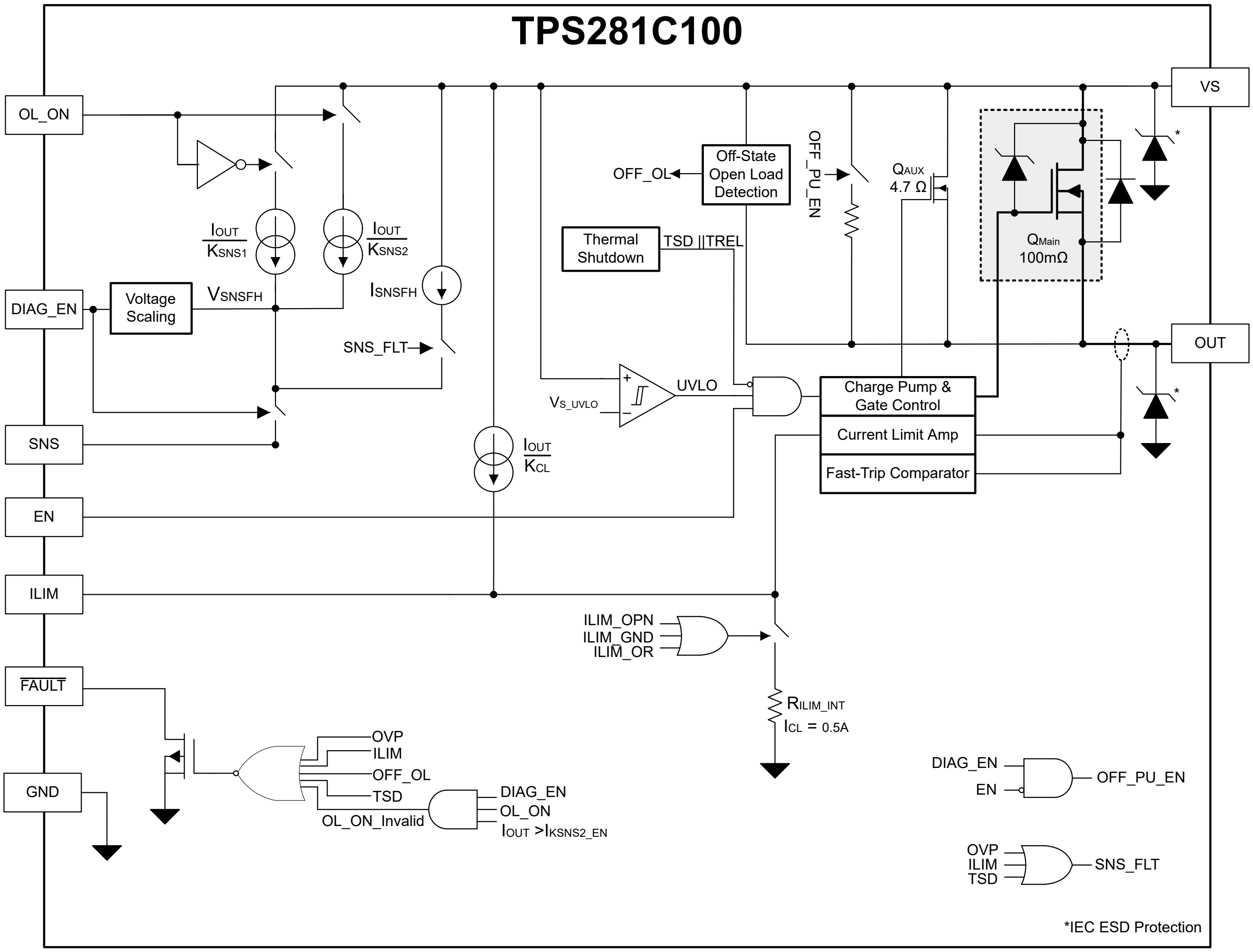
The digital status report is implemented with an open-drain structure on the fault pin. When a fault condition occurs, the pin is pulled down to GND. An external pullup is required to match the microcontroller supply level. High-accuracy current sensing allows a better real-time monitoring effect and more-accurate diagnostics without further calibration. A current mirror is used to source 1 / K_{SNS} of the load current, which is reflected as voltage on the SNS pin. K_{SNS} is a constant value across temperature and supply voltage. The SNS pin can also report a fault by forcing a voltage of V_{SNSFH} that scales with the diagnostic enable voltage so that the max voltage seen by the system's ADC is within an acceptable value. This removes the need for an external zener diode or resistor divider on the SNS pin.

The external high-accuracy current limit allows setting the current limit value by application. It highly improves the reliability of the system by clamping the inrush current effectively under start-up or short-circuit conditions. Also, it can save system costs by reducing PCB trace, connector size, and the preceding power-stage capacity. An internal current limit can also be implemented in this device. The lower value of the external or internal current-limit value is applied.

An active drain to source voltage clamp is built in to address switching off the energy of inductive loads, such as relays, solenoids, pumps, motors, and so forth. During the inductive switching-off cycle, both the energy of the power supply (E_{BAT}) and the load (E_{LOAD}) are dissipated on the high-side power switch itself. With the benefits of process technology and excellent IC layout, the TPS281C100x device can achieve excellent energy dissipation capacity, which can help save the external free-wheeling circuitry in most cases.

The TPS281C100x device can be used as a high-side power switch for a wide variety of resistive, inductive, and capacitive loads, including the low-wattage bulbs, LEDs, relays, solenoids, and heaters.

8.2 Functional Block Diagram



8.3 Device Functional Modes

8.4 Working Mode

The four working modes in the device are normal mode, normal mode with diagnostics, idle mode and idle mode with diagnostics.

Normal mode is when EN is high and DIAG_EN is low. In this mode, VS is having quiescent current of $I_{Q,VS}$, and the main FET is ON. With DIAG_EN low, no current sense information is available through the SNS pin.

Normal mode with Diagnostics is when both EN and DIAG_EN is high. In this mode, VS is having quiescent current of I_{Q,VS_DIAG}, and the main FET is ON. With DIAG_EN high, current sense information will be available through the SNS pin.

Idle mode is when both EN and DIAG_EN low. In this mode, main FET is OFF, and VS is consuming a current of $I_{IDLE,VS}$. There is extra current consumed in this state compared to the traditional shutdown state, due to having EFT detection circuitry being active. Additionally, there is a current sink at the output always active to keep the output near 0V. The output sink can sink up to $I_{OUT(OFF,SINK)}$.

Idle mode with diagnostics is when EN is low and DIAG_EN is high. In this mode, main FET is OFF, and VS is consuming a current of I_{IDLE,VS_DIAG}. With DIAG_EN high, the output pullup circuitry is active for open-load and short-to-VS detection, and there is no active output sink.

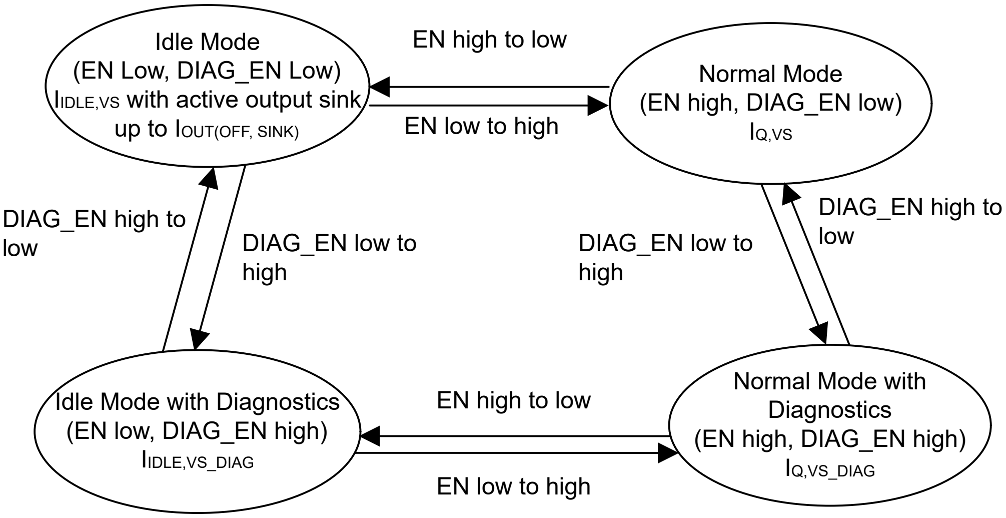


Figure 8-1. Work-Mode State Machine

8.5 Feature Description

8.5.1 Accurate Current Sense

The current-sense function is internally implemented, which allows a better real-time monitoring effect and more-accurate diagnostics without further calibration. A current mirror is used to source 1 / K_{SNS} of the load current, flowing out to the external resistor between the SNS pin and GND, and reflected as voltage on the SNS pin.

K_{SNS} is the ratio of the output current and the sense current. The accuracy values of K_{SNS} quoted in the electrical characteristics do take into consideration temperature and supply voltage. Each device was internally calibrated while in production, so post-calibration by users is not required in most cases.

The maximum voltage out on the SNS pin is clamped to V_{SNSFH} which is the fault voltage level. In order to make sure that this voltage is not higher than the system can tolerate, TI has correlated the voltage coming in on the DIAG_EN pin with the maximum voltage out on the SNS pin. If DIAG_EN is between V_{IH} and 3.3 V, the maximum output on the SNS pin will be ~3.3 V. However, if the voltage at DIAG_EN is above 3.3 V, then the fault SNS voltage, V_{SNSFH}, will track that voltage up to 5 V. This is done because the GPIO voltage output that is powering the diagnostics through DIAG_EN, will be close to the maximum acceptable ADC voltage within the same microcontroller. Therefore, the sense resistor value, R_{SNS}, can be chosen to maximize the range of currents needed to be measured by the system. The R_{SNS} value should be chosen based on application need. The maximum usable R_{SNS} value is bounded by the ADC minimum acceptable voltage, $V_{ADC,min}$, for the smallest load current needed to be measured by the system, $I_{LOAD,min}$. The minimum acceptable R_{SNS} value has to ensure the V_{SNS} voltage is below the V_{SNSFH} value so that the system can determine faults. This difference between the maximum readable current through the SNS pin, $I_{LOAD,max} \times R_{SNS}$, and the V_{SNSFH} is called the headroom voltage, V_{HR}. The headroom voltage is determined by the system but is important so that there is a difference between the maximum readable current and a fault condition. Therefore, the minimum RSNS value has to be the V_{SNSFH} minus the V_{HR} times the sense current ratio, K_{SNS} divided by the maximum load current the system needs to measure, $I_{LOAD,max}$. This boundary equation can be seen in Equation 1.

$$V_{ADC,min} \times K_{SNS} / I_{LOAD,min} \le R_{SNS} \le (V_{SNSFH} - V_{HR}) \times K_{SNS} / I_{LOAD,max} \quad (1)$$

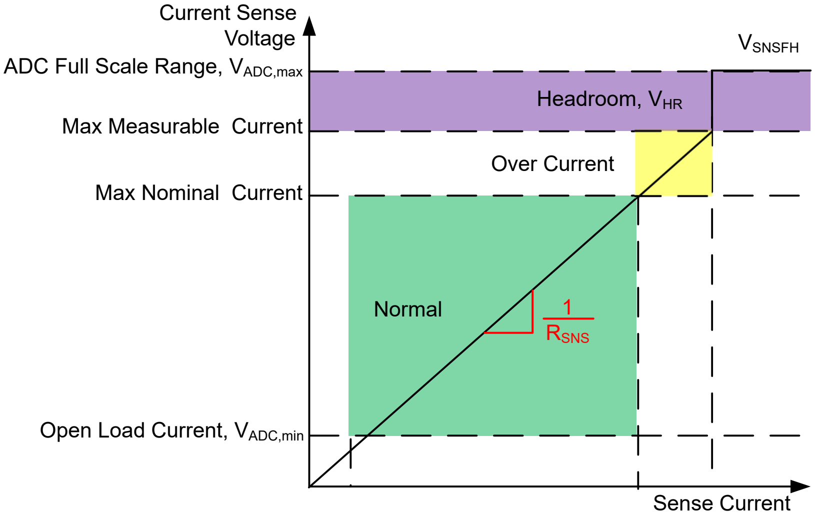


Figure 8-2. Voltage Indication on the Current-Sense Pin

The maximum current the system wants to read, $I_{LOAD,max}$, needs to be below the current limit threshold because once the current limit threshold is tripped the V_{SNS} value will go to V_{SNSFH}. Additionally, currents being measured should be below 4 A to ensure that the current sense output is not saturated.

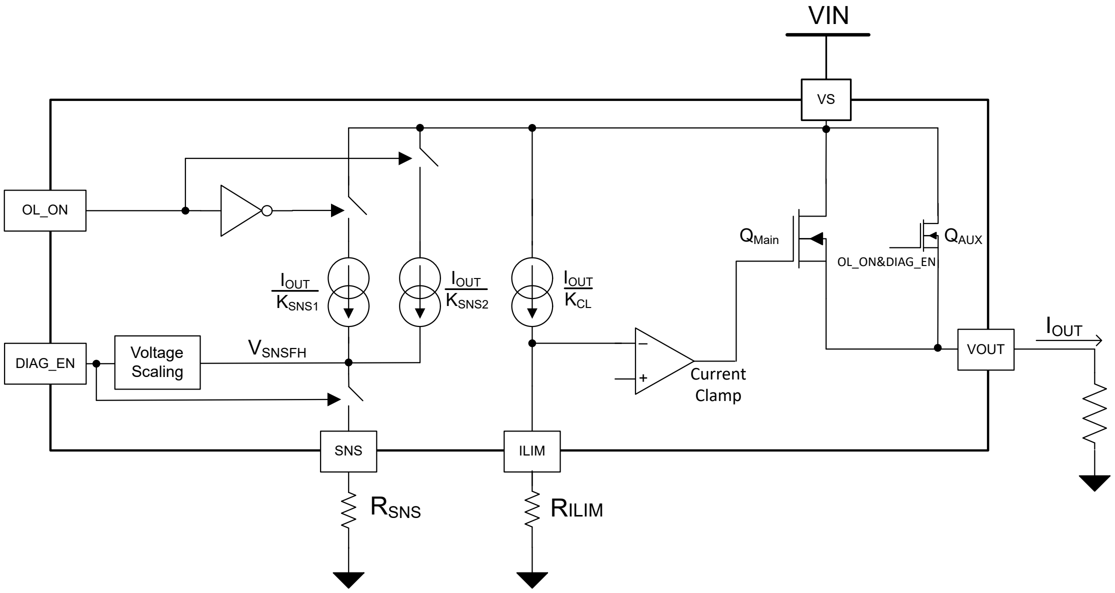


Figure 8-3. Current-Sense and Current-Limit Block Diagram

Since this scheme adapts based on the voltage coming in from the MCU. There is no need to have a zener diode on the SNS pin to protect from high voltages.

8.5.1.1 High Accuracy Sense Mode

In some applications, having accurate current sensing at lower load currents can be critical to distinguish between a real load and a fault scenario such as an open load condition(Wire-Break). To address this challenge, TPS281C100 implements a high accuracy sense mode that enables customers to achieve ±12.5% at 4mA load. This mode will be activated when diagnostics are enabled(DIAG_EN=HI), OL_ON = HI and I_{Load}<I_{KSNS2_EN} . To achieve this high accuracy , the device increases its main path resistance to improve its sense accuracy while high accuracy sensing is active. TI recommends users to disable this accuracy sense mode by setting OL_ON=LO if the load starts to increase beyond 20 mA. This will proactively prevent any higher power dissipation states.

In other scenarios such as a sudden load step where the system might not be fast enough to react to the change in SNS output current. For this case, in order to prevent a high-power dissipation state given by the increased resistance. TPS281C100 senses the load flowing through the VS to VOUT path to be less than I_{KSNS2_DIS}. If the load increases beyond I_{KSNS2_DIS} the FET resistance will revert back to its lowest resistance and high accuracy sense mode will be disabled. This will result in $\overline{\text{FAULT}}$ being asserted to signal that high accuracy sense mode has been disabled. This will ensure the lowest power dissipation when higher loads are being driven. In addition to this, the user can PWM the OL_ON pin to disable the high resistance mode and minimize power losses further.

However, even if accuracy is achieved by the device; Depending on the current sense ratio, system ADCs can struggle to measure lower load currents accurately due to the low voltages that would need to be read by the ADC. As an example, a 6 mA I_{Load} will be represented as ~7.5 mV using RSNS=1kOhm with a current sense ratio of 800. For a 10-bit 5 V ADC the 7.5 mV output is just over 1 LSB (4.88 mV). This does not provide enough margin to accurately measure this current for the ADC and likely a higher resolution would need to be used.

Therefore, in order to enable lower ADC resolution requirements and to accurately sense low load currents when operating in high accuracy sense mode, TPS281C100 decreases its current sense ratio to 24. With a sense ratio of 24, the 6 mA I_{Load} will be represented as 250 mV using RSNS=1kOhm when operating in high accuracy sense mode. This equals to 51 LSBs of margin for the same 10-bit ADC or even for an 8-bit ADC the output would still provide > 12 LSBs of headroom.

Full Protection and Diagnostics for full device states.

Table 8-1. Current Sensing Operation Modes

Conditions	EN	VOUT	OL_ON	KSNS	SNS	$\overline{\text{FAULT}}$	Behavior	Recovery
Normal Standard Sensing	L	L	L	800	0	Hi-Z	Normal	
	H	H	L	800	I_{Load} / K_{SNS}	Hi-Z	Normal	
High Accuracy Sense Normal Operation	H	H	H	24	I_{Load} / K_{SNS2}	Hi-Z	Enables low sense ratio for high accuracy sensing and FAULT stays Hi-Z since valid condition is met I_{Load}<I_{KSNS2_EN}.	
High Accuracy Sense Invalid Range	H	H	H	800	I_{Load} / K_{SNS}	L	FAULT is asserted signaling that high accuracy sensing is not enabled since I_{Load}>I_{KSNS2_DIS}	Clears when load falls below I_{KSNS2_EN} or OL_ON is reset to LO.

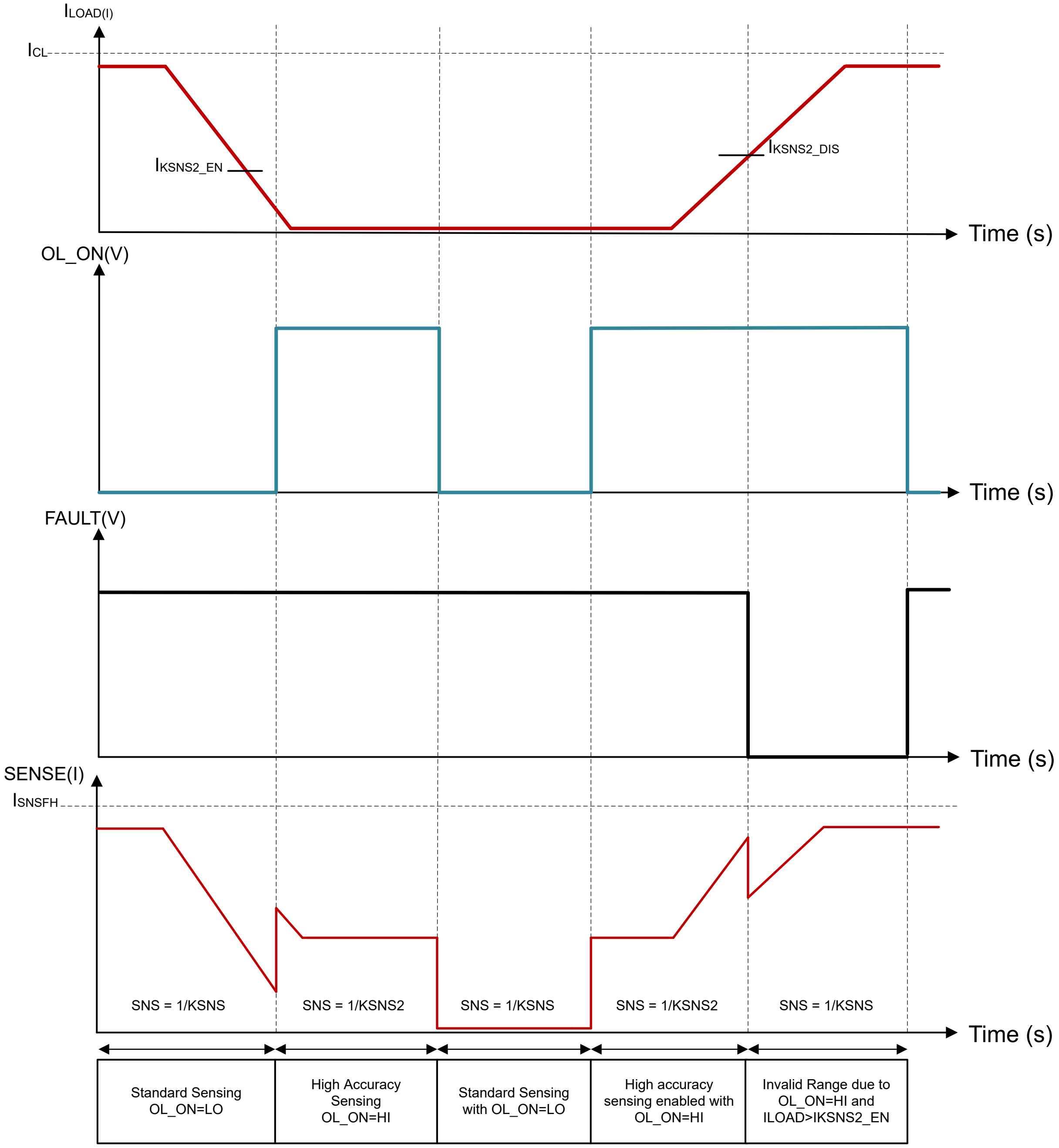


Figure 8-4. High Accuracy Sensing FAULT Indication

8.5.2 Programmable Current Limit

A high-accuracy current limit allows higher reliability, which protects the power supply during short circuit or power up. Also, it can save system costs by reducing PCB traces, connector size, and the capacity of the preceding power stage.

Current limit offers protection from overstressing to the load and integrated power FET. Current limit holds the current at the set value, and pulls up the SNS pin to V_{SNSFH} and asserts the $\overline{\text{FAULT}}$ pin as diagnostic reports. The two current-limit thresholds are:

- External programmable current limit: An external resistor, $R_{ILIM}$is used to set the channel current limit. When the current through the device exceeds I_{CL} (current limit threshold), a closed loop steps in immediately. V_{GS} voltage regulates accordingly, leading to the V_{DS} voltage regulation. When the closed loop is set up, the current is clamped at the set value. The external programmable current limit provides the capability to set the current-limit value by application.

  Additionally this value can be dynamically changed by changing the resistance on the ILIM pin. This can be seen in the Applications Section.
- Internal current limit: I_{LIM} pin open or pin shorted to ground -- If the external current limit is out of range on the lower end or the I_{LIM} pin is shorted to ground, the internal current limit is fixed and typically 0.5A. This works as a safety power limiting mechanism during failures with shorts or open connections with PCB overstress.

Both the internal current limit ($I_{lim,nom}$) and external programmable current limit are always active when V_S is powered and EN is high. The lower value one (of I_{LIM} and the external programmable current limit) is applied as the actual current limit. The typical deglitch time for the current limit to assert is 2.5μs.

Note that if a GND network is used (which leads to the level shift between the device GND and board GND), the ILIM pin must be connected with device GND. Calculate R_{LIM} from the typical I_{CL} value desired with Equation 2.

$$R_{ILIM} = K_{CL} / I_{CL} \tag{2}$$

The R_{ILIM} value calculated here will correspond to a typical value of the current limit. For the R_{ILIM} value listed in the data sheet, the min and max current limit values are given in the electrical characteristic table. For any R_{ILIM} values in between, linear interpolation can be used to estimate the min and max values.

The minimum value for the current limit listed in the electrical characteristic table includes the variation for $\overline{\text{FAULT}}$ assertion. When designing the module to ensure the $\overline{\text{FAULT}}$ signal is not asserted during nominal operation, the minimum current limit needs to be above the nominal operation current. An example is given in Section 9.2.2.1.

For better protection from a hard short-to-GND condition (when V_S and input are high and a short to GND happens suddenly), an open-loop fast-response behavior is set to turn off the channel, before the current-limit closed loop is set up. With this fast response, the device can achieve better inrush-suppression performance.

8.5.2.1 Short-Circuit and Overload Protection

TPS281C100 provides output short-circuit protection to ensure that the device will prevent current flow in the event of a low impedance path to GND, removing the risk of damage or significant supply droop. The device is guaranteed to protect against short-circuit events regardless of the state of the ILIM pins and with up to 60 V supply at 125°C.

On-State Short-Circuit Behavior shows the behavior of TPS281C100 when a short-circuit occurs and the device is in the on-state and already outputting current. When the internal pass FET is fully enabled, the current clamping settling time is slower so to ensure overshoot is limited, the device implements a fast trip level at a level I_{OVCR}. When this fast trip threshold is hit, the device immediately shuts off for a short period of time before quickly re-enabling and clamping the current to I_{CL} level after a brief transient overshoot to the higher peak current (I_{CL_ENPS}) level. The device will then keep the current clamped at the regulation current limit until the thermal shutdown temperature is hit and the device will safely shut-off.

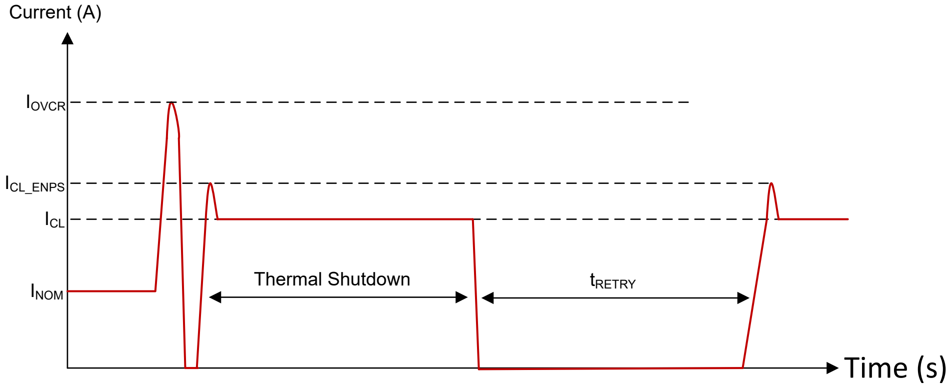


Figure 8-5. On-State Short-Circuit Behavior

Overload Behavior shows the behavior of the TPS281C100 when there is a small change in impedance that sends the load current above the I_{CL} threshold. The current rises to I_{CL_LINPK} above the regulation level. Then the current limit regulation loop kicks in and the current drops to the I_{CL} value.

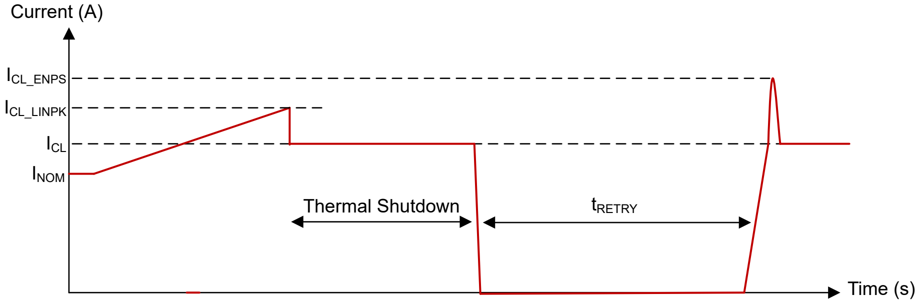


Figure 8-6. Overload Behavior

In all of these cases, the internal thermal shutdown is safe to hit repetitively. There is no device risk or lifetime reliability concerns from repeatedly hitting this thermal shutdown level.

8.5.2.2 Capacitive Charging

Capacitive Charging Circuit shows the typical set up for a capacitive load application and the internal blocks that function when the device is used. Note that all capacitive loads will have an associated "load" in parallel with the capacitor that is described as a resistive load but in reality it can be inductive or resistive.

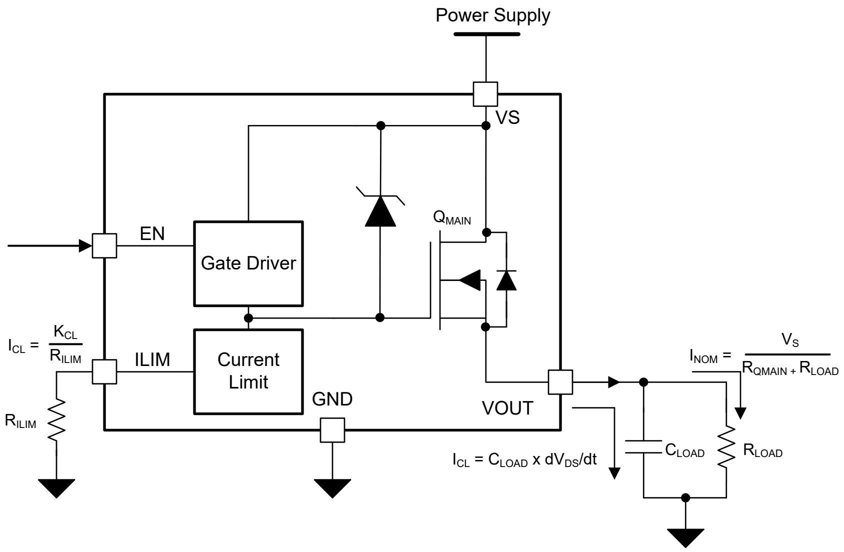


Figure 8-7. Capacitive Charging Circuit

The first thing to check is that the nominal DC current, I_{NOM}, is acceptable for the TPS281C100 device. This can easily be done by taking the $R_{\theta JA}$ from the Thermal Section and multiplying the RON of the TPS281C100 and the INOM with it, add the ambient temperature and if that value is below the thermal shutdown value the device can operate with that load current. For an example of this calculation see the Applications Section.

The second key care about for this application is to make sure that the capacitive load can be charged up completely without the device hitting thermal shutdown. This is because if the device hits thermal shutdown during the charging, the resistive nature of the load in parallel with the capacitor will start to discharge the capacitor over the duration the TPS281C100 is off. Note that there are some application with high enough load impedance that the TPS281C100 hitting thermal shutdown and trying again is acceptable; however, for the majority of applications the system should be designed so that the TPS281C100 does not hit thermal shutdown while charging the capacitor.

With the current clamping feature of the TPS281C100, capacitors can be charged up at a lower inrush current than other high current limit switches. This lower inrush current means that the capacitor will take a little longer to charge all the way up. However, to minimize this longer charge time during startup, TPS281C100A implements an inrush current handling feature described in Figure 8-8. When the EN pin goes high to turn on the high side switch, the device will default its current limit threshold to $I_{LIM\_STARTUP}$ for a duration of $I_{LIM\_STARTUP\_DELAY.}$ During this delay period, a capacitive load can be charged at a higher rate than what typical I_{CL} would allow and FAULT will be masked to prevent unwanted Fault triggers. After $I_{LIM\_STARTUP\_DELAY}$, the current limit will default back to I_{CL} and Fault will work normally.

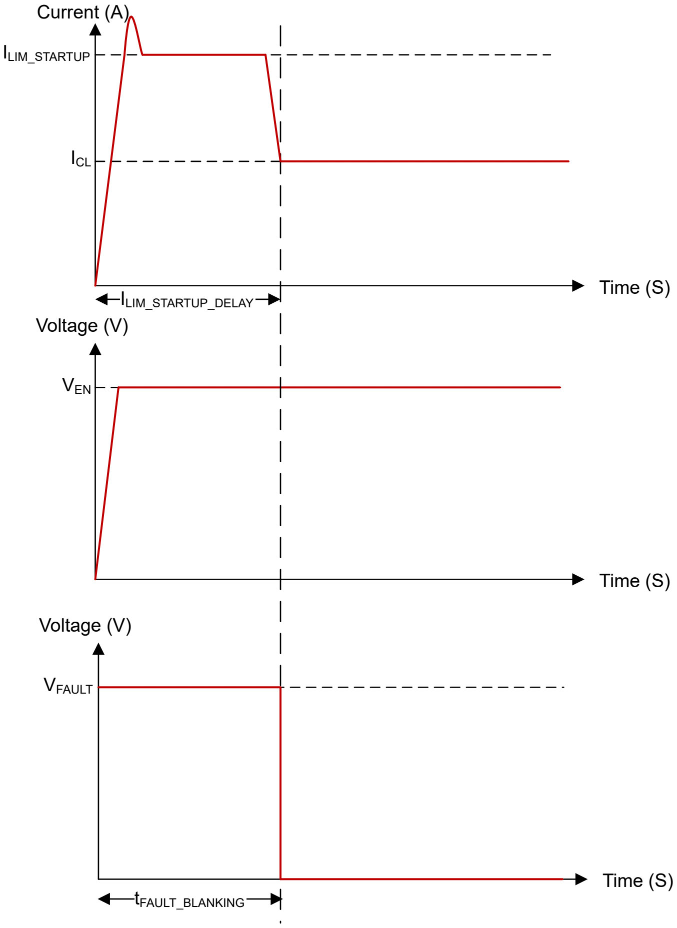


Figure 8-8. Inrush Current Handling

The initial inrush current period when the current limit is higher enables two different system advantages when driving loads:

- Enables higher load current to be supported for a period of time of the order of milliseconds to drive high inrush current loads like incandescent bulb loads.
- Enables fast capacitive load charging. In some situations, it is ideal to charge capacitive loads at a higher current than the DC current to ensure quick supply bring up. This architecture allows a module to quickly charge a capacitive load using the initial higher inrush current limit and then use a lower current limit to reliably protect the module under overload or short circuit conditions.

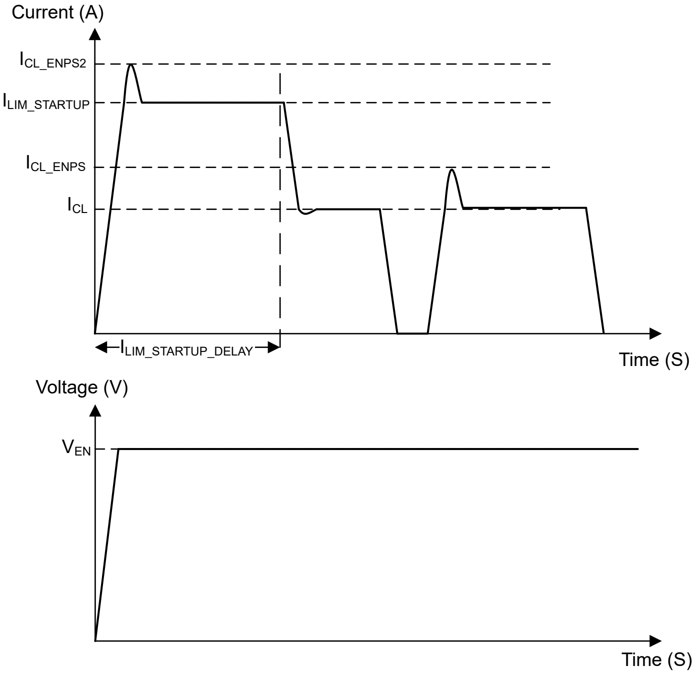


Figure 8-9. Auto-retry Behavior Before ILIM_STARTUP_DELAY

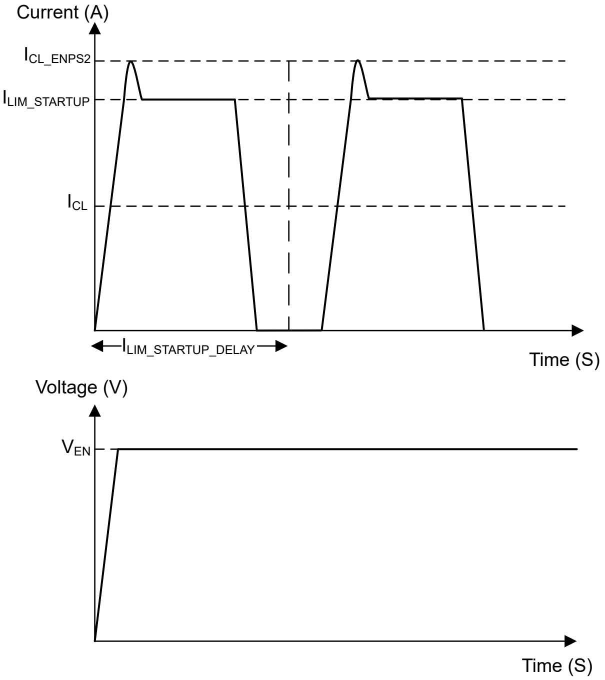


Figure 8-10. Auto-retry Behavior After ILIM_STARTUP_DELAY

While in current limiting mode, at any level, the device will have a high power dissipation. If the FET temperature exceeds the over-temperature shutdown threshold, the device will turn off just the channel that is overloaded. After cooling down, the device will re-try. If the device is turning off prematurely on start-up, it is recommended to improve the PCB thermal layout, lower the current limit to lower power dissipation, or decrease the inrush current (capacitive loading).

For more information about capacitive charging with high side switches see the How to drive Capacitive loads application note. This application note has information about the thermal modeling available along with quick ways to estimate if a high side switch will be able to charge a capacitor to a given voltage.

8.5.3 Inductive-Load Switching-Off Clamp

When an inductive load is switching off, the output voltage is pulled down to negative, due to the inductance characteristics. The power FET may break down if the voltage is not clamped during the current-decay period. To protect the power FET in this situation, internally clamp the drain-to-source voltage, namely $V_{DS,clamp}$, the clamp diode between the drain and gate.

$$V_{DS,Clamp} = V_S - V_{OUT} \tag{3}$$

During the current-decay period (T_{DECAY}), the power FET is turned on for inductance-energy dissipation. Both the energy of the power supply (E_S) and the load (E_{LOAD}) are dissipated on the high-side power switch itself, which is called E_{HSD}. If resistance is in series with inductance, some of the load energy is dissipated in the resistance.

$$E_{HSD} = E_S + E_{LOAD} = E_S + E_L - E_R \tag{4}$$

From the high-side power switch's view, E_{HSD} equals the integration value during the current-decay period.

$$E_{HSD} = \int_0^{T_{DECAY}} V_{DS,clamp} \times I_{OUT}(t)\,dt \tag{5}$$

$$T_{DECAY} = \frac{L}{R} \times \ln\left(\frac{R \times I_{OUT(MAX)} + |V_{OUT}|}{|V_{OUT}|}\right) \tag{6}$$

$$E_{HSD} = L \times \frac{V_{BAT} + |V_{OUT}|}{R^2} \times \left[R \times I_{OUT(MAX)} - |V_{OUT}| \ln\left(\frac{R \times I_{OUT(MAX)} + |V_{OUT}|}{|V_{OUT}|}\right)\right] \tag{7}$$

When R approximately equals 0, E_{HSD} can be given simply as:

$$E_{HSD} = \frac{1}{2} \times L \times I^2_{OUT(MAX)} \frac{V_{BAT} + |V_{OUT}|}{R^2} \tag{8}$$

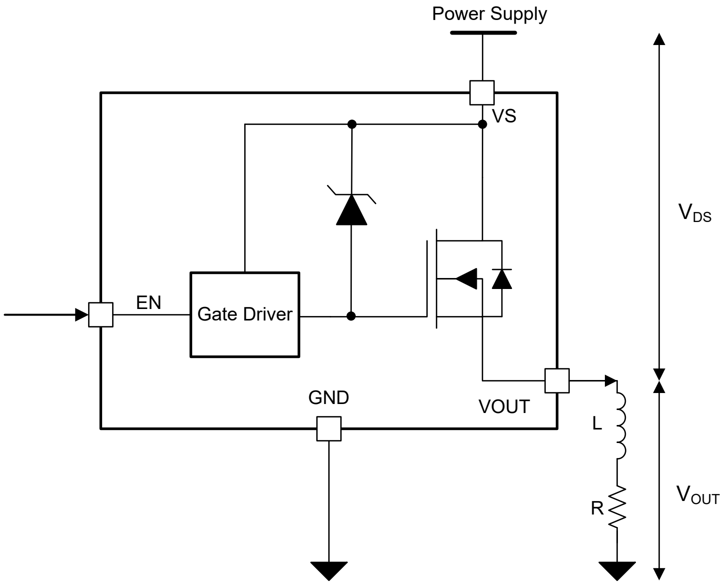


Figure 8-11. Driving Inductive Load

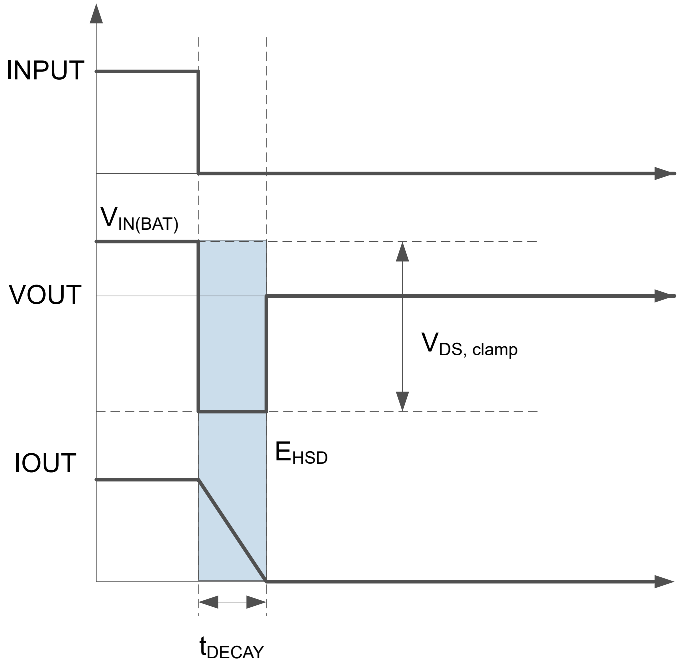


Figure 8-12. Inductive-Load Switching-Off Diagram

As discussed previously, when switching off, battery energy and load energy are dissipated on the high-side power switch, which leads to the large thermal variation. For each high-side power switch, the upper limit of the maximum safe power dissipation depends on the device intrinsic capacity, ambient temperature, and board dissipation condition.

8.5.4 Inductive Load Demagnetization

When switching off an inductive load, the inductor can impose a negative voltage on the output of the switch. The TPS281C100 includes voltage clamps between VS and VOUT to limit the voltage across the FETs and demagnetize load inductance if there is any. The negative voltage applied at the OUT pin drives the discharge of inductor current. Figure 8-13 shows the device discharging a 400-mH load.

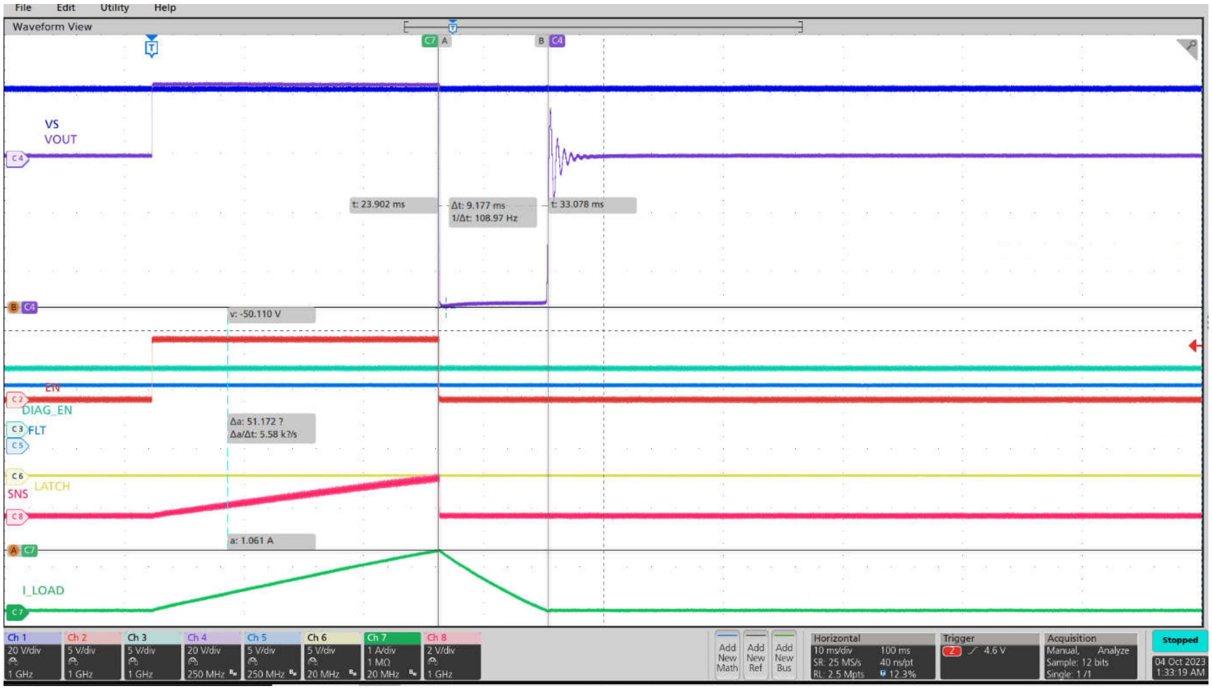


Figure 8-13. TPS281C100 Inductive Discharge (400 mH)

The maximum acceptable load inductance is a function of the energy dissipated in the device and therefore the load current and the inductive load. The maximum energy and the load inductance the device can withstand for one pulse inductive dissipation at 125°C is shown in Figure 8-14. The device can withstand 40% of this energy for one million inductive repetitive pulses with a 2-Hz repetitive pulse. If the application parameters exceed this device limit, use a protection device like a freewheeling diode to dissipate the energy stored in the inductor.

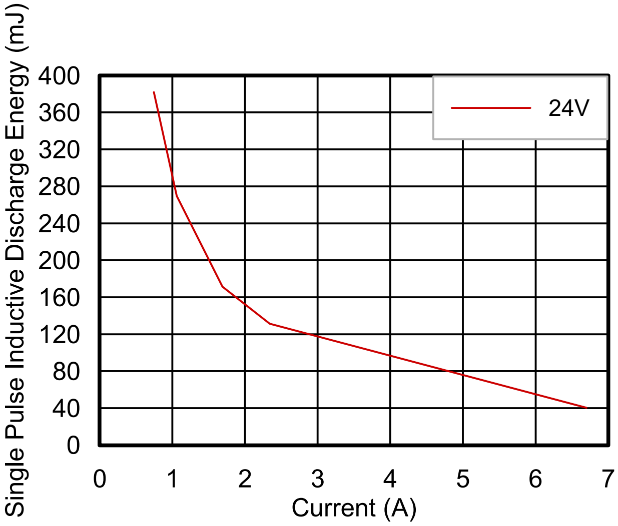


Figure 8-14. TPS281C100 Inductive Load Discharge Energy Capability at 125°C and 24 V Supply

8.5.5 Full Protections and Diagnostics

Current Sensing is active when DIAG_EN enabled. When DIAG_EN is low, current sense is disabled. The SNS output is in high-impedance mode.

Table 8-2. DIAG_EN Logic Table

DIAG_EN	EN Condition	Protections and Diagnostics
HIGH	HIGH	See Fault Table
	LOW	
LOW	HIGH	Diagnostics disabled and SNS output is set to high Impedance. Protection is normal and $\overline{\text{FAULT}}$ continues to indicate TSD or ILIM.
	LOW	

Table 8-3. Status Table (DIAG_EN=HIGH)

Conditions	EN	VOUT	OL_ON	$\overline{\text{FAULT}}$	SNS	Behavior	Recovery
Normal Standard Sensing	L	L	L	Hi-Z	0	Normal	
	H	H	L	Hi-Z	I_{Load} / K_{SNS}	Normal	
High Accuracy Sense Invalid Range	H	H	H	L	I_{Load} / K_{SNS}	FAULT is asserted signaling that high accuracy sensing is not enabled since $I_{Load}>I_{KSNS2\_EN}$	Clears when load falls below I_{KSNS2_EN} or OL_ON is reset to LO.
High Accuracy Sense Normal Operation	H	H	H	Hi-Z	I_{Load} / K_{SNS2}	Enables the K_{SNS2} sense ratio for high accuracy sensing and FAULT stays Hi-Z since valid condition is met $I_{Load}<I_{Ksns2\_EN}$.	
Overcurrent	H	V_S - $I_{LIM}*R_{LOAD}$	x	L	V_{SNSFH}	Holds the current at the current limit until thermal shutdown	
STG, Relative Thermal Shutdown, Absolute Thermal Shutdown	H	H/L	x	L	V_{SNSFH}	Shuts down when devices hits relative or absolute thermal shutdown	Auto retries when $T_{HYS}$is met and it has been longer than t_{RETRY} amount of time
Open Load	H	H	L	Hi-Z	I_{Load} / K_{SNS} = ~0	Normal behavior, user can judge if it is an open load or not	
	H	H	H	Hi-Z	I_{Load} / K_{SNS2} = ~0	Normal behavior, user can judge if it is an open load or not	
	L	H	L	L	V_{SNSFH}	Internal pullup resistor is active. If V_S – V_{OUT} < V_{OL} then fault active	Clears when fault goes away
Reverse Polarity	x	x	x	x	x	Channel turns on to lower power dissipation. Current into ground pin is limited by external ground network	

8.5.5.1 Open-Load Detection

On-State Open Load Detection

When the main channel is enabled faults are diagnosed by reading the voltage on the SNS or $\overline{\text{FLT}}$ pin and judged by the user. A benefit of high-accuracy current sense is that this device can achieve a very low open-load detection threshold, which correspondingly expands the normal operation region. As explained in section high accuracy sense mode, this mode can be used to sense low currents accurately.

Off-State Open Load Detection

In the off state, if a load is connected, the output voltage is pulled to 0V. In the case of an open load, the output voltage is close to the supply voltage, $V_S – V_{OUT} < V_{ol,off}$. The FLT pin goes low to indicate the fault to the MCU, and the SNS pin is pulled up to I_{SNSFH}. There is always a leakage current $I_{ol,off}$ present on the output, due to the internal logic control path or external humidity, corrosion, and so forth. Thus, TI implimented an internal pullup resistor to offset the leakage current. This pullup current should be less than the output load current to avoid false detection in the normal operation mode. To reduce the standby current, TI implimented a switch in series with the pullup resistor controlled by the DIAG_EN pin. The pull up resistor value is R_{OL_OFF}.

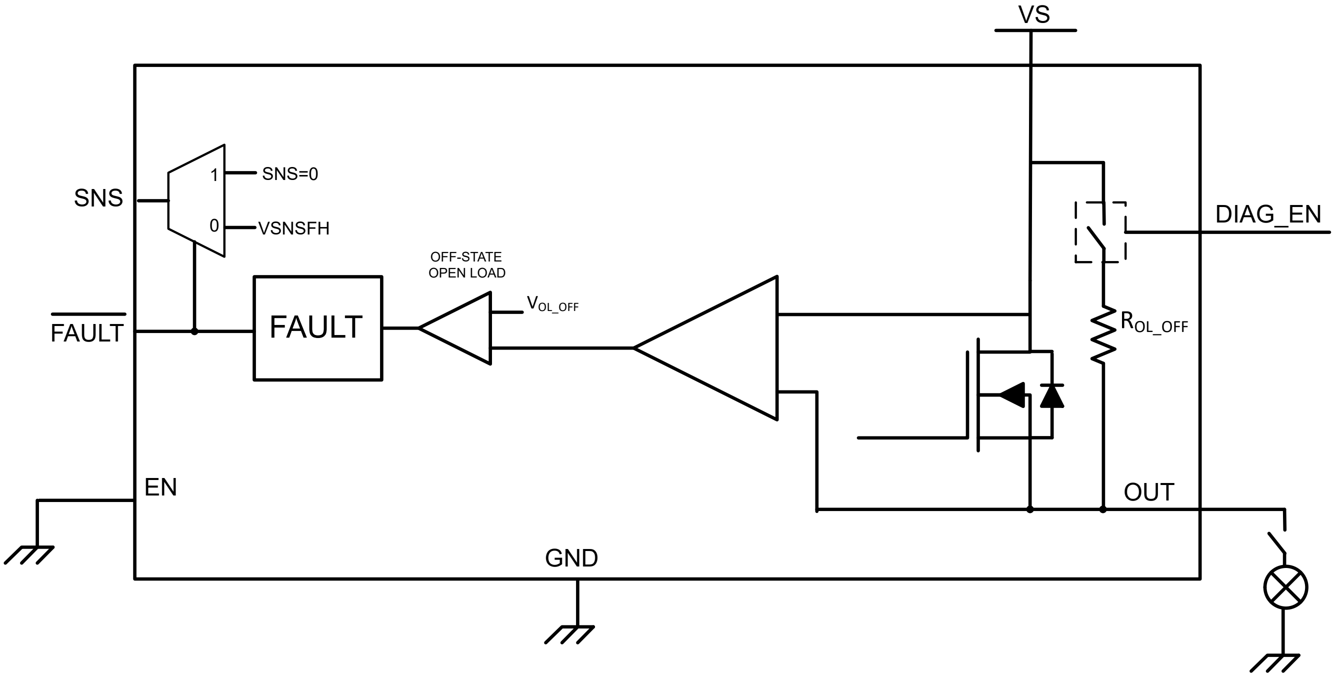


Figure 8-15. Off-State Open-Load Detection Circuit

8.5.5.2 Thermal Protection Behavior

The thermal protection behavior can be split up into 2 categories of events that can happen. Thermal behavior shows each of these categories.

1. **Relative thermal shutdown**: The device is enabled into an over current event. The DIAG_EN pin is high so that diagnostics can be monitored on SNS and FLT. The output current rises up to the I_{ILIM} level and the FLT goes low while the SNS goes to V_{SNSFH}. With this large amount of current going through the junction temperature of the FET increases rapidly with respect to the controller temperature. When the power FET temperature rises T_{REL} amount above the controller junction temperature $\Delta T = T_{FET} – T_{CON} > T_{REL}$, the device shuts down. The faults are continually shown on SNS and FLT and the part waits for the t_{RETRY} timer to expire. When t_{RETRY} timer expires, since EN is still high, the device will come back on into this I_{ILIM} condition.
2. **Absolute thermal shutdown**: In this case, the ambient temperature is now much higher than the previous case. The device is still enabled in an over current event with DIAG_EN high. However, in this case the junction temperature rises up and hits an absolute reference temperature, TABS, and then shuts down. The device will not recover until both $T_J < T_{ABS} – T_{hys}$ and the t_{RETRY} timer has expired.

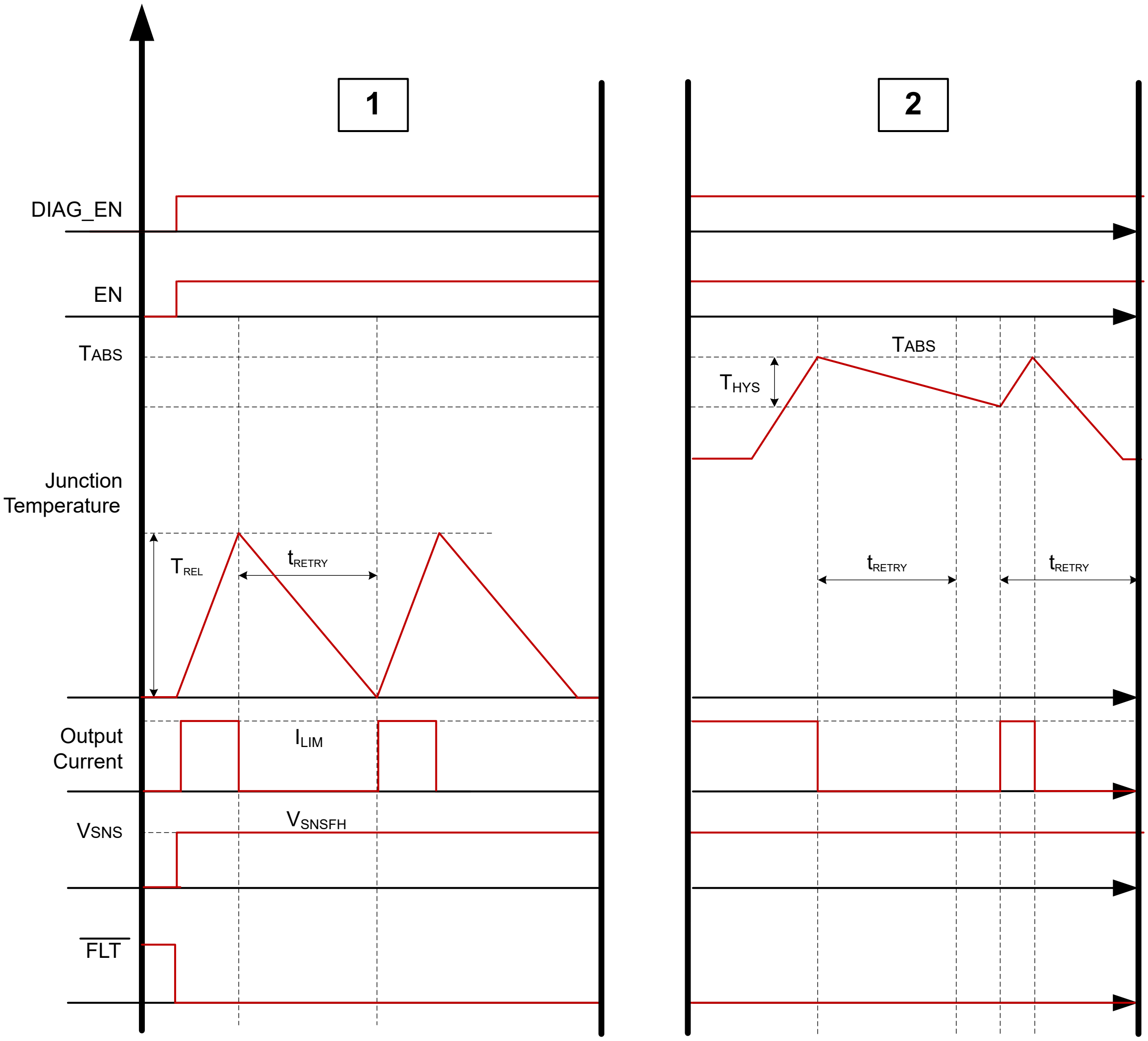


Figure 8-16. Thermal Behavior

8.5.5.3 Undervoltage Lockout (UVLO) Protection

The device monitors the supply voltage V_S to prevent unpredicted behaviors in the event that the supply voltage is too low. When the supply voltage falls down to V_{UVLOF}, the output stage is shut down automatically. When the supply rises up to V_{UVLOR}, the device turns on. If an overcurrent event trips the UVLO threshold, the device will shut off and come back on into a current limit safely.

8.5.5.4 Reverse Polarity Protection

Method 1: Blocking diode connected with VBB. Both the device and load are protected when in reverse polarity. The blocking diode does not allow any of the current to flow during reverse battery condition.

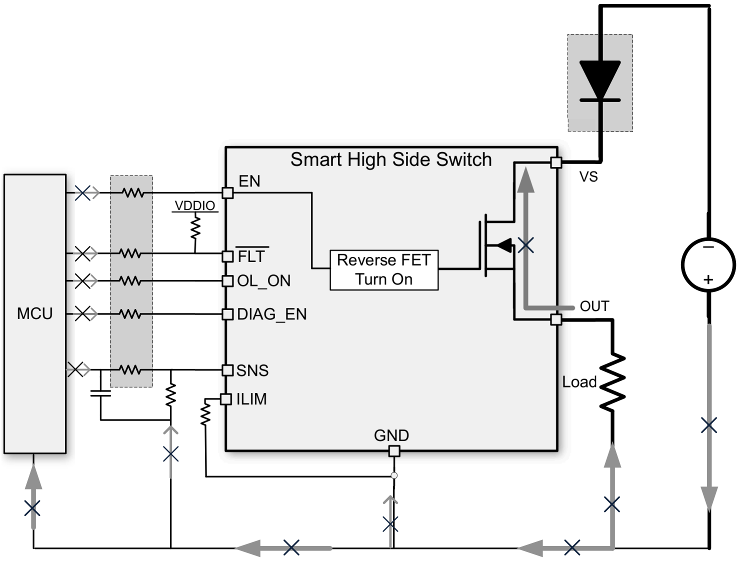


Figure 8-17. Reverse Protection With Blocking Diode

Method 2 (GND network protection): Only the high-side device is protected under this connection. The load reverse loop is limited by the load itself. Note when reverse polarity happens, the continuous reverse current through the power FET should be less than I_{rev}. Of the three types of ground pin networks, TI strongly recommends type 3 (the resistor and diode in parallel). No matter what types of connection are between the device GND and the board GND, if a GND voltage shift happens, ensure the following proper connections for the normal operation:

- Leave the NC pin floating or connect to the device GND. TI recommends to leave floating.
- Connect the current limit programmable resistor to the device GND.

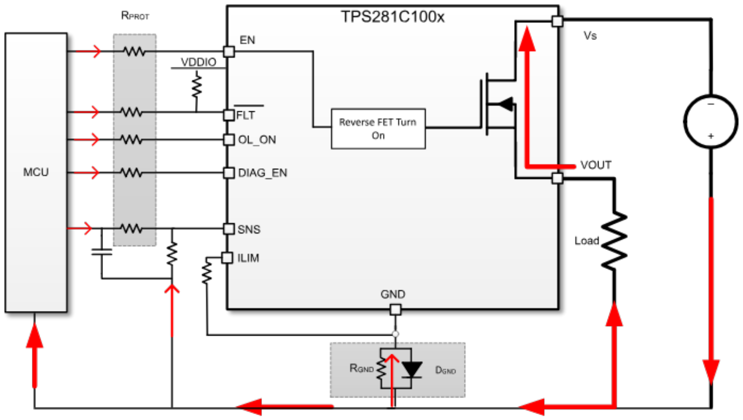


Figure 8-18. Reverse Protection With GND Network

- **Type 1 (resistor):** The higher resistor value contributes to a better current limit effect when the reverse battery or negative ISO pulses. However, it leads to higher GND shift during normal operation mode. Also, consider the resistor's power dissipation.

  $$R_{GND} \le \frac{V_{GNDshift}}{I_{nom}} \tag{9}$$

  $$R_{GND} \ge \frac{(-V_{CC})}{(-I_{GND})} \tag{10}$$

  where

  - $V_{GNDshift}$ is the maximum value for the GND shift, determined by the HSS and microcontroller. TI suggests a value ≤ 0.6 V.
  - I_{nom} is the nominal operating current.
  - $-V_{CC}$ is the maximum reverse voltage seen on the battery line.
  - $-I_{GND}$ is the maximum reverse current the ground pin can withstand, which is available in the *Section 6.1*.

  If multiple high-side power switches are used, the resistor can be shared among devices.
- **Type 2 (diode):** A diode is needed to block the reverse voltage, which also brings a ground shift (≈ 600 mV). However, an inductive load is not acceptable to avoid an abnormal status when switching off.
- **Type 3 (resistor and diode in parallel (recommended)):** A peak negative spike may occur when the inductive load is switching off, which may damage the HSD or the diode. So, TI recommends a resistor in parallel with the diode when driving an inductive load. The recommended selection are 4.7-kΩ resistor in parallel with an I_F > 100-mA diode. If multiple high-side switches are used, the resistor and diode can be shared among devices.

8.5.5.5 Protection for MCU I/Os

In many conditions, such as the negative surge pulse, or the loss of battery with an inductive load, a negative potential on the device GND pin may damage the MCU I/O pins [more likely, the internal circuitry connected to the pins]. Therefore, the serial resistors between MCU and HSS are required.

Also, for proper protection against loss of GND, TI recommends 10 kΩ resistance for the RPROT resistors.

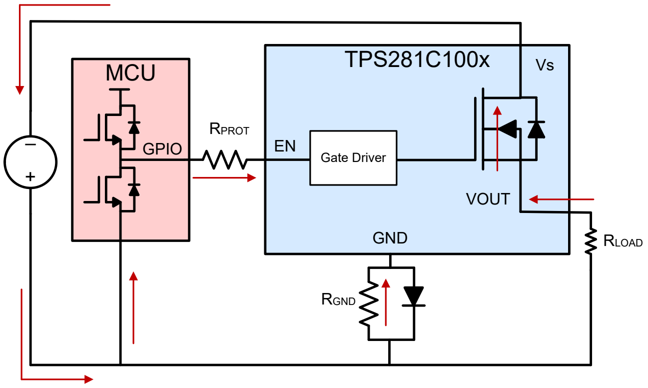


Figure 8-19. MCU IO Protections

8.5.5.6 Diagnostic Enable Function

The diagnostic enable pin, DIAG_EN, offers multiplexing of the microcontroller diagnostic input for current sense or digital status, by sharing the same sense resistor and ADC line or I/O port among multiple devices.

In addition, this pin can be used to manage power dissipation by the device. During the ouput-on period, if no continious sense output diagnositcs are required, the diagnostic disable feature will lower the operating current. On the other hand, the output-off period, the diagnostic disable function lowers the current consumption for the standby condition.

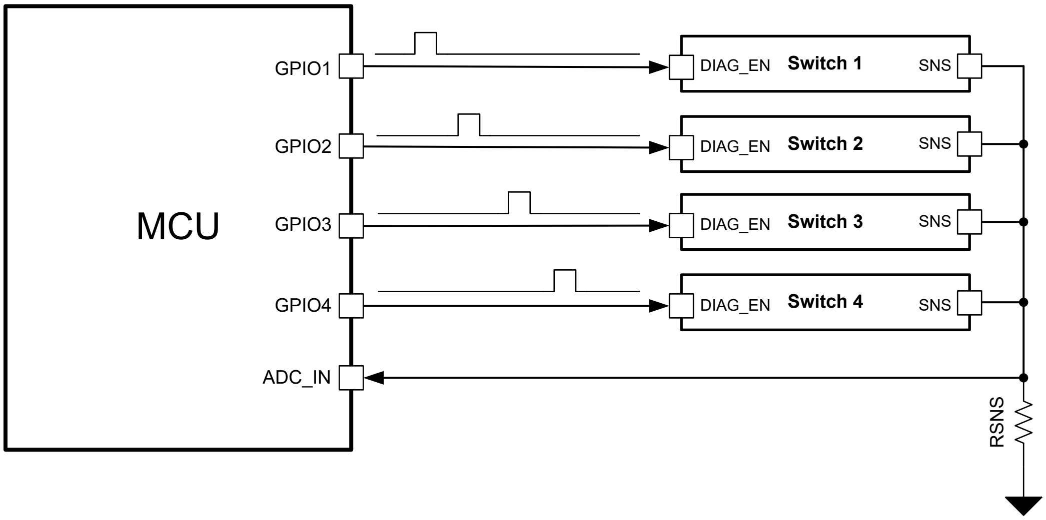


Figure 8-20. Resistor sharing

8.5.5.7 Loss of Ground

The ground connection may be lost either on the device level or on the module level. If the ground connection is lost and the supply voltage is less than 48V, the channel output will be disabled irrespective of the EN input level. If the switch was already disabled when the ground connection was lost, the outputs will remain disabled even when the channels are enabled. The steady state current from the output to the load that remains connected to the system ground is below the level specified in the *Specifications* section of this document. When the ground is reconnected, normal operation will resume.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.2 Typical Application

The Typical Application Circuit shows an example of how to design the external circuitry parameters.

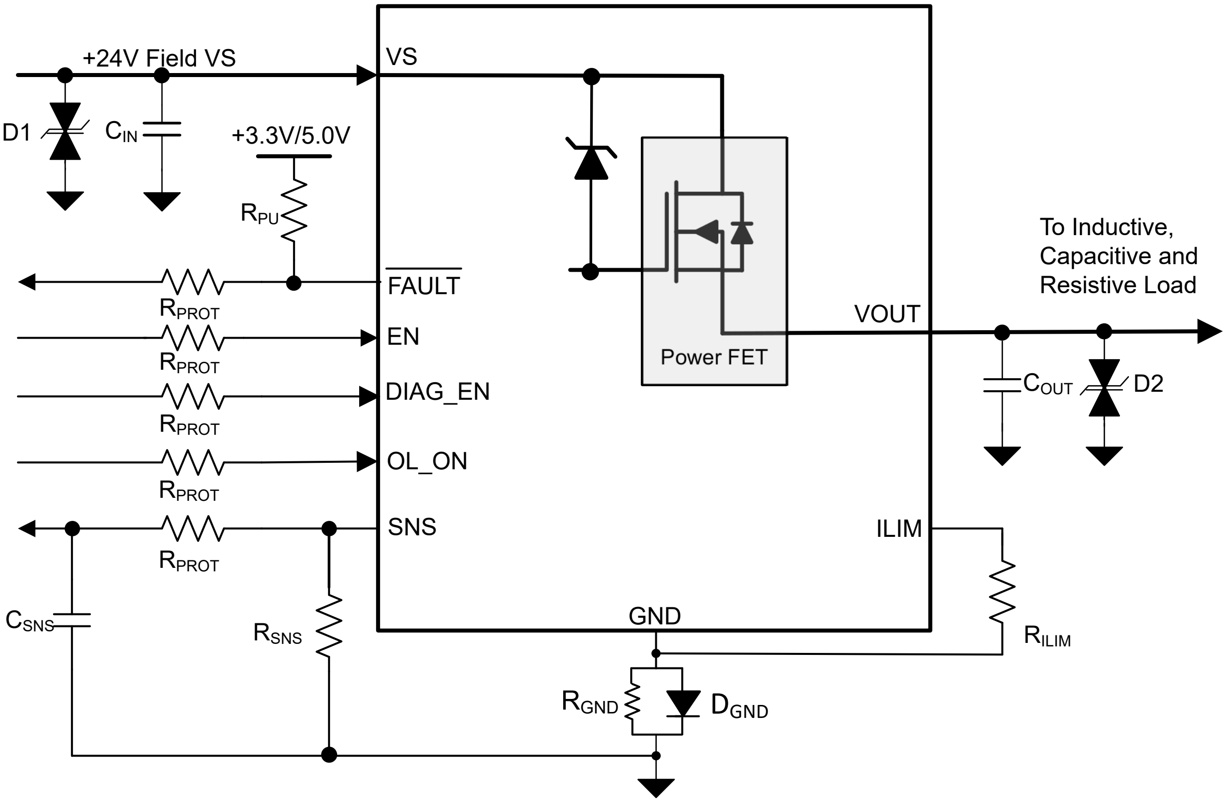


Figure 9-1. Typical Application Circuit

9.2.1 Design Requirements

Component	Typical Value	Purpose
D1	SMBJ36A	Clamp surge voltages at the supply input. Mandatory if surge protection is needed. Please refer to Section 9.2.1.2.
D2	SMBJ33CA	Clamp surge voltages at the supply output. Mandatory if surge protection is needed. Please refer to Section 9.2.1.2.
CIN1	100 nF	Stabilize the input supply and filter out low frequency noise.
CIN2	4.7 nF	Filtering of voltage transients (for example, ESD, IEC 61000-4-5) and improved emissions.
RPROT	10 kΩ	Protection resistor for microcontroller and device I/O pins - Optional for reverse polarity protection
RILIM	10 kΩ – 50 kΩ	Set current limit threshold
RSNS	1 kΩ	Translate the sense current into sense voltage.
CSNS	1 nF	Coupled with RPROT on the SNS line creates a low pass filter to filter out noise going into the ADC of the MCU.
CVOUT	22 nF	Improves EMI performance, filtering of voltage transients
RGND	4.7 kΩ	Stabilize GND potential during turn-off of inductive load - Optional for reverse polarity protection
DGND	BAS21 Diode	Keeps GND close to system ground during normal operation - Optional for reverse polarity protection

9.2.1.1 IEC 61000-4-4 EFT

The TPS281C100 is designed to survive against IEC 61000-4-4 electrical fast transient (EFT) with minimum of 22 nF output capacitance. The device can pass ± 2 kV EFT at VS and VOUT ports. When EN is low, device will remain OFF during the EFT pulse, and functions normally after the pulse. When EN is high, the device will withstand the pulse and functions normally afterwards.

For active EFT detection during OFF state, TPS281C100 has the detection circuitry active when in the OFF state. It will introduce higher OFF state current $I_{IDLE,\ VS}$ or $I_{IDLE,\ VS\_DIAG}$ compared to the usual shutdown current in other high-side switches.

In addition, when DIAG_EN is low, the device enables a current sink at the output that can sink up to $I_{OUT\ (OFF,\ SINK)}$ of current at the output. This is to help offset any leakage current from the device during the EFT, and keep the output voltage close to 0 V during the OFF state and EFT events. When DIAG_EN is high, there is OFF state pull-up resistance that pulls up the output voltage close to VS. In this case, the output current sink is not active.

9.2.1.2 IEC 61000-4-5 Surge

To pass the IEC61000-4-5 surge for TPS281C100, both input and output TVS diodes are needed to help absorb the surge energy. There are certain requirements on the input and output TVS diodes selection listed below.

Output TVS requirements:

Output TVS can serve two purposes: absorb the surge energy for the output surge, and help demagnetize the inductive energy during an inductive turn off. To ensure the output TVS clamps before the internal VDS clamp comes in during an output surge event, the clamping voltage the TVS needs to be selected so that VS + $V_{TVS,\ CLMAP} < V_{DS,\ Clamp,\ min}$. For standard 24V input system, **SMBJ33CA** is recommended at the output.

Input TVS requirements:

Input TVS needs to be selected so it doesn't interfere with normal operation. The reverse standoff voltage of the input TVS needs to be greater than the normal operation input voltage. The other requirement is that the input TVS needs to be equal or higher voltage rated than the output TVS, and it ensures that the surge energy is clamped by the output TVS instead of the input TVS when there is a output surge. For standard 24V input system, **SMBJ36A** is recommended at the input. Please note that a uni-directional TVS at the input is needed so the absolute minimum voltage of the device is not violated for negative input surge.

9.2.2 Detailed Design Procedure

9.2.2.1 Selecting RILIM

The current limit set level TPS281C100 must allow for the maximum DC current with margin but minimize the energy in the switch and the load on the input supply during a fault condition by minimizing the current limit.

The nominal current limit should be set such that the worst case (lowest) current limit will be higher than the maximum nominal load current. If the application is a 500 mA digital output module, with the max current to be 1A, then there are two ways to set the current limit.

First way is to use the resistor value listed in the electrical characteristic table. 25 kΩ R_{ILIM} resistor setting will set the current limit minimum level to be 1.5 A, which is above the maximum nominal load current. If the high end of the setting 2.3 A is acceptable in the application, then 25 kΩ R_{ILIM} resistance can be used.

If the application wants to minimize the maximum current seen by the module as much as possible, then the current limit resistor needs to be chosen so that the minimum current limit level is as close to the maximum load current as possible. To obtain the minimum current limit to be 1 A, the typical current limit needed to be scaled for the same ratio 1 × 1.32 = 1.32 A. By linear interpolation, we can find the K_{CL} value at 1.32 A typical current limit is 48.5 A * kΩ.

$$R_{ILIM} = K_{CL} / I_{CL} \tag{11}$$

The calculated value of R_{ILIM} is 36.7 kΩ, and the closest 1% standard resistor value is 36.5 kΩ.

9.2.2.2 Selecting RSNS

Table 9-1 shows the requirements for the load current sense in this application. The K_{SNS} value is specified for the device and can be found in the *Specifications* section.

Table 9-1. R_{SNS} Calculation Parameters

PARAMETER	EXAMPLE VALUE
Current Sense Ratio (K_{SNS1})	800
Current Sense Ratio (K_{SNS2})	24
Largest diagnosable load current	3 A
Smallest diagnosable load current	4 mA
Full-scale ADC voltage	5.0 V
ADC resolution	10 bit

The load current measurement up to 3 A ensures that even in the event of a overload but below the set current limit, the MCU can register and react by turning off the FET while the low level of 4 mA allows for accurate measurement of low load currents and enable the distinction open load faults from supported nominal load currents. For load currents < 50 mA, the customer can enable high accuracy sensing to change the sense ratio from KSNS1 to KSNS2. This prevents the requirement of a higher resolution ADC and it also increases sense accuracy. Go to high accuracy sensing for more information.

The R_{SNS} resistor value should be selected such that the largest diagnosable load current puts the SNS pin voltage (V_{SNS}) at about 90% of the ADC full-scale. With this design, any ADC value above 80% of full scale (FS) can be considered a fault. Additionally, the R_{SNS} resistor value should ensure that the smallest diagnosable load current does not cause V_{SNS} to fall below at a least a few LSB of the ADC.

With the given example values, a 1.0-kΩ sense resistor satisfies both requirements.

Table 9-2. V_{SNS} Calculation

Sense Mode	OL_ON	LOAD (A)	SENSE RATIO	I_{SNS} (mA)	R_{SNS} (Ω)	V_{SNS} (V)	% of 5-V ADC
Standard Sensing	LO	3 A	800	3.75	1000	3.75	75%
High Accuracy Sensing	HI	0.004 A	24	0.166	1000	0.166	3.3% (~34 LSBs)

9.3 Power Supply Recommendations

The TPS281C100 device is designed to operate in a 24-V industrial system. The allowed supply voltage range (VS pin) is 6 V to 60 V as measured at the VS pin with respect to the GND pin of the device. In this range the device meets full parametric specifications as listed in the Section 6.5 table. The device is also designed to withstand voltage transients beyond this range such as SELV supply failures.

It is recommended to place a 0.1uF capacitor at the Vs supply input to stabilize the input supply and filter out low frequency noise. The power supply must be able to withstand all transient load current steps. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance can be required on the input.

9.4 Layout

9.4.1 Layout Guidelines

To prevent thermal shutdown, T_J must be less than 125°C. If the output current is very high, the power dissipation may be large. The HTSSOP and WSON packages have good thermal impedance. However, the PCB layout is very important. Good PCB design can optimize heat transfer, which is absolutely essential for the long-term reliability of the device.

- Maximize the copper coverage on the PCB to increase the thermal conductivity of the board. The major heat-flow path from the package to the ambient is through the copper on the PCB. Maximum copper is extremely important when there are not any heat sinks attached to the PCB on the other side of the board opposite the package.
- Add as many thermal vias as possible directly under the package ground pad to optimize the thermal conductivity of the board.
- All thermal vias should either be plated shut or plugged and capped on both sides of the board to prevent solder voids. To ensure reliability and performance, the solder coverage should be at least 85%.

9.4.1.1 EMC Considerations

9.4.2 Layout Example

9.4.2.1 PWP Layout Without a GND Network

Without a GND network, tie the thermal pad directly to the board GND copper for better thermal performance.

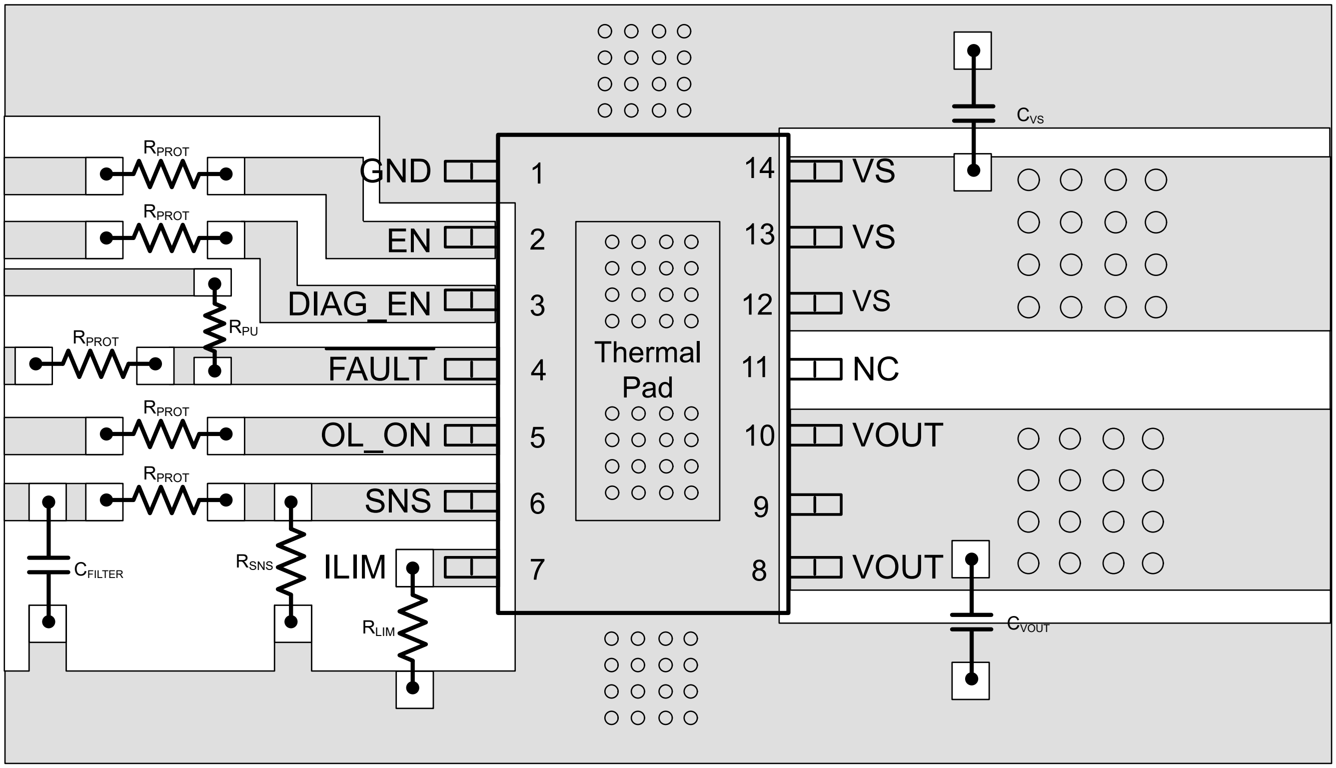


Figure 9-2. PWP Layout Without a GND Network

9.4.2.2 PWP Layout With a GND Network

With a GND network, tie the thermal pad with a single trace through the GND network to the board GND copper.

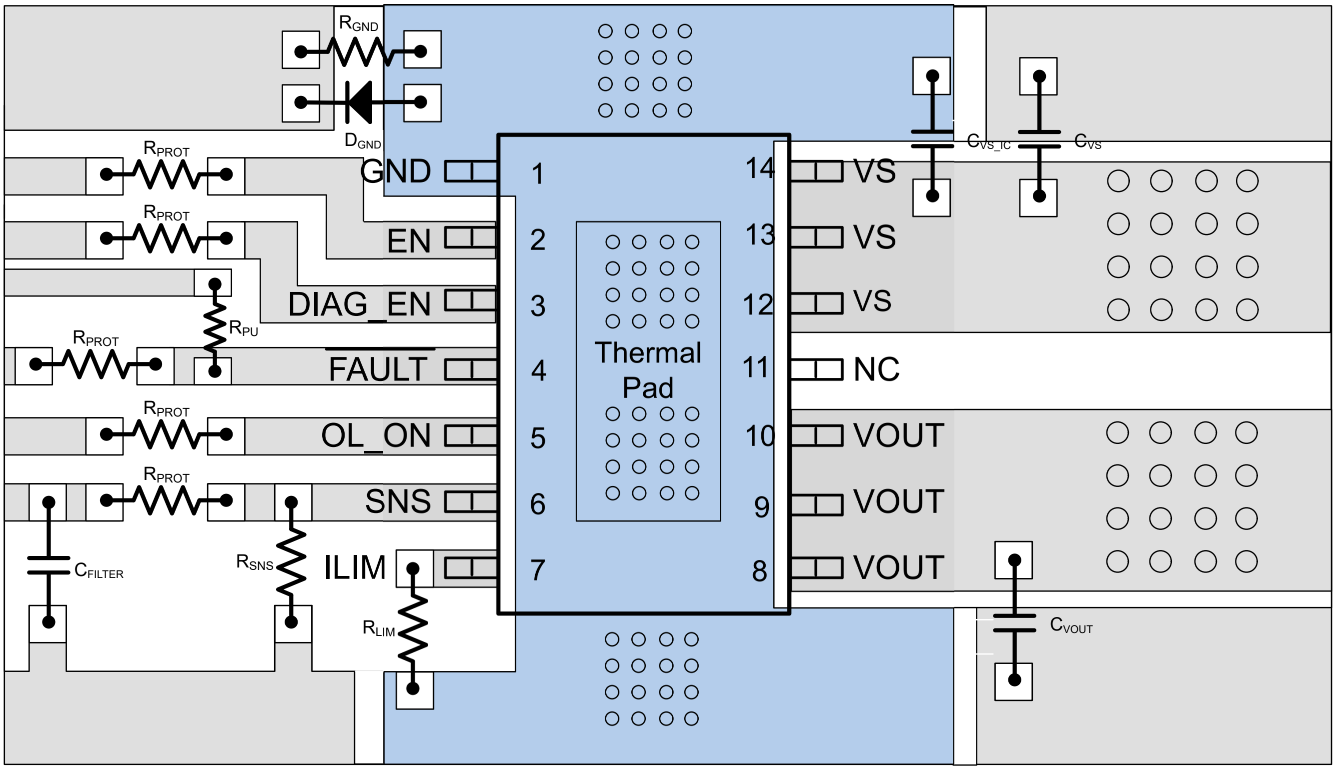


Figure 9-3. PWP Layout With a GND Network

9.4.2.3 DNT Layout Without a GND Network

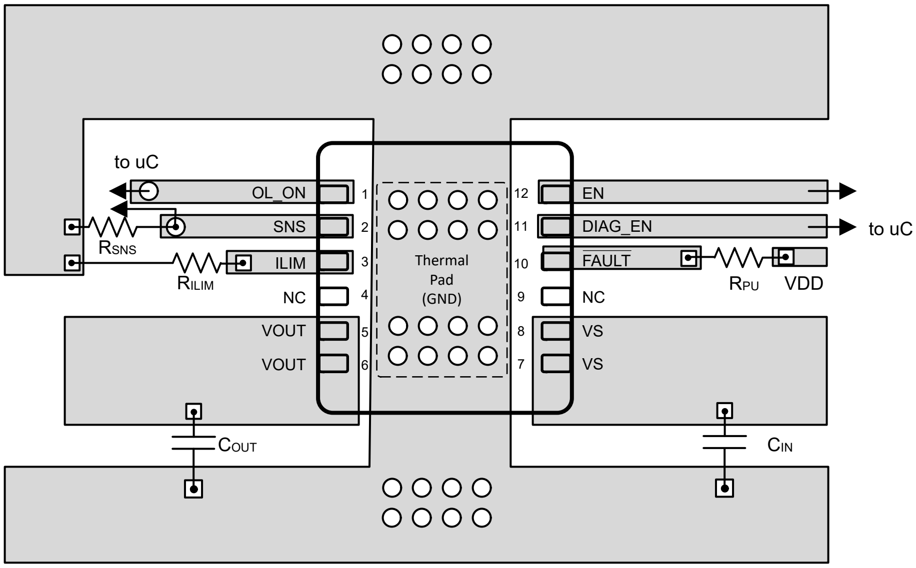


Figure 9-4. DNT Layout Without a GND Network

9.4.3 Thermal Considerations

This device possesses thermal shutdown (TABS) circuitry as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the thermal-shutdown trip point. If the junction temperature exceeds the thermal-shutdown trip point, the output turns off. When the junction temperature falls below the thermal-shutdown trip point, the output turns on again.

Calculate the power dissipated by the device according to Equation 12.

$$P_T = I_{OUT}{}^2 \times R_{DSON} + V_S \times I_{NOM} \tag{12}$$

where

- P_T = Total power dissipation of the device

After determining the power dissipated by the device, calculate the junction temperature from the ambient temperature and the device thermal impedance.

$$T_J = T_A + R_{\theta JA} \times P_T \tag{13}$$

For more information please see How to Drive Resistive, Inductive, Capacitive, and Lighting Loads.

10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.3 Trademarks

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10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2024) to Revision A (September 2024)	Page
• Updated the *Electrical Characteristics* section for B version	6

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS281C100ADNTR	Active	Production	WSON (DNT) | 12	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	281C0
TPS281C100ADNTR.A	Active	Production	WSON (DNT) | 12	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	281C0
TPS281C100BDNTR	Active	Production	WSON (DNT) | 12	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	B81C0

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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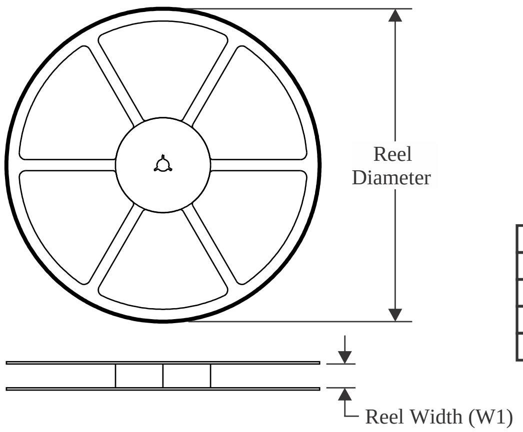
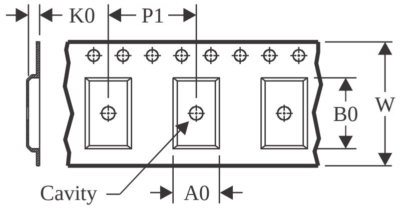
TAPE AND REEL INFORMATION

REEL DIMENSIONS

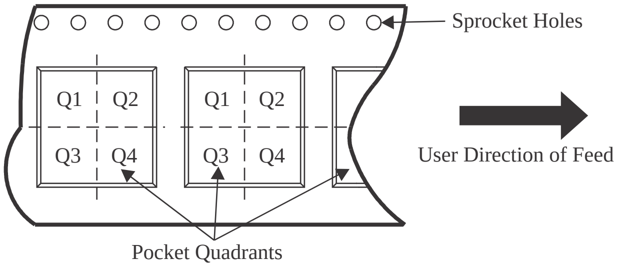


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

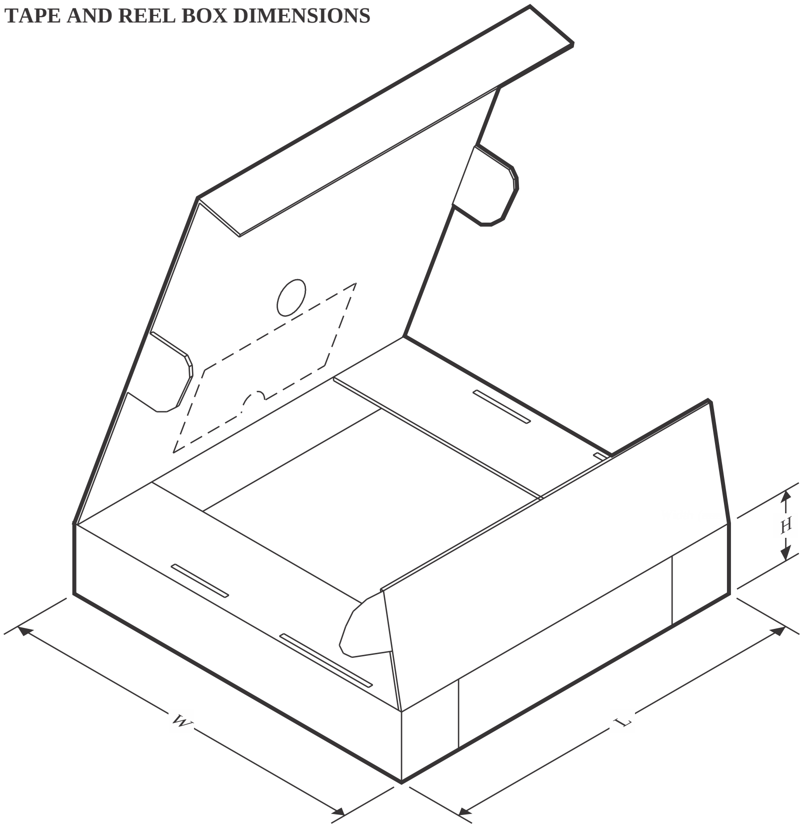
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

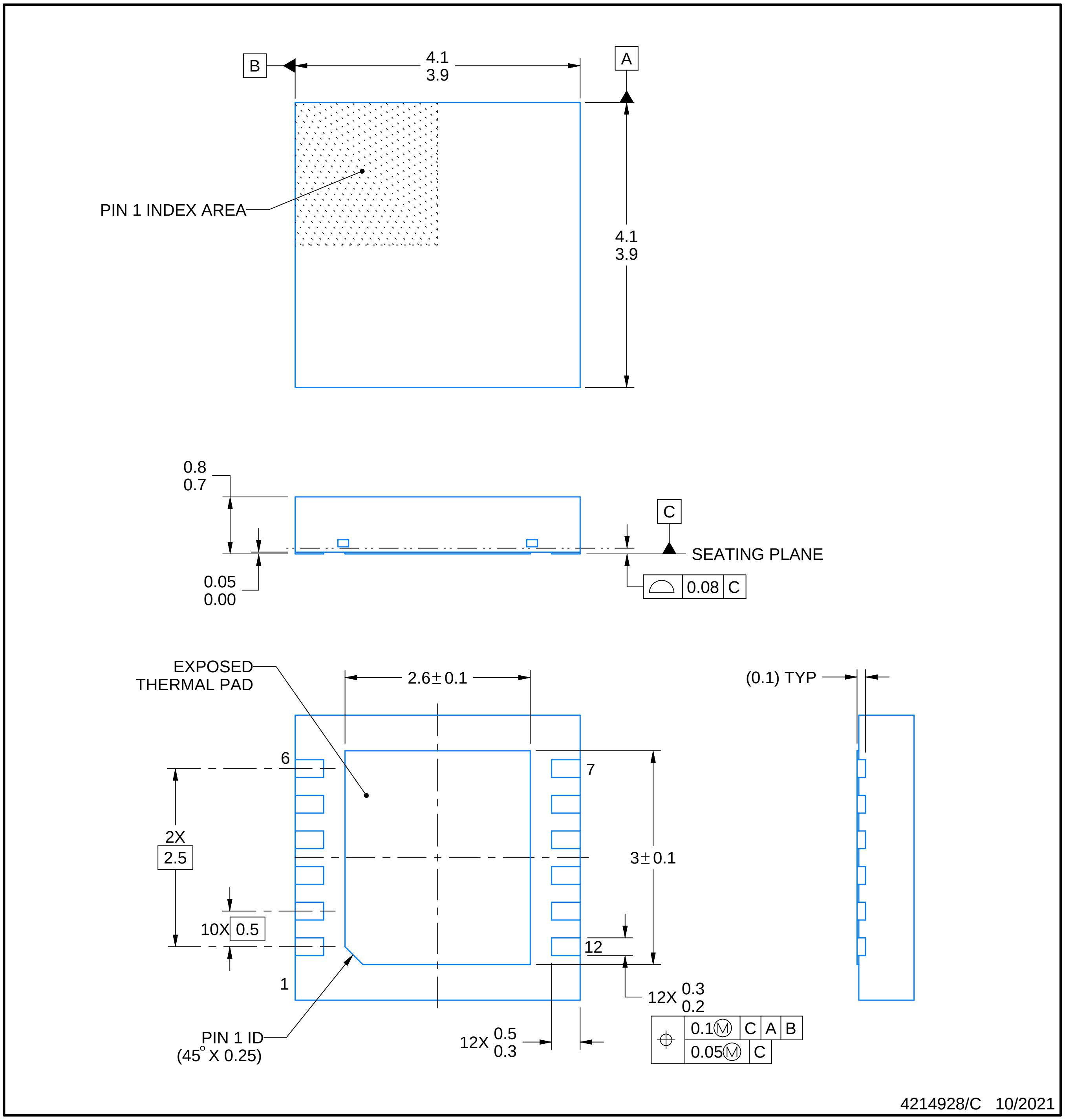
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS281C100ADNTR	WSON	DNT	12	5000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS281C100BDNTR	WSON	DNT	12	5000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



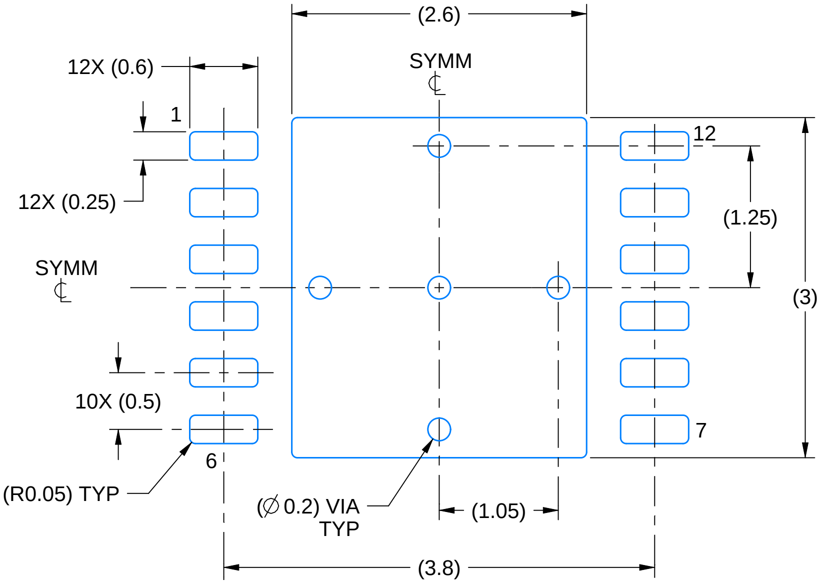
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS281C100ADNTR	WSON	DNT	12	5000	367.0	367.0	35.0
TPS281C100BDNTR	WSON	DNT	12	5000	367.0	367.0	35.0

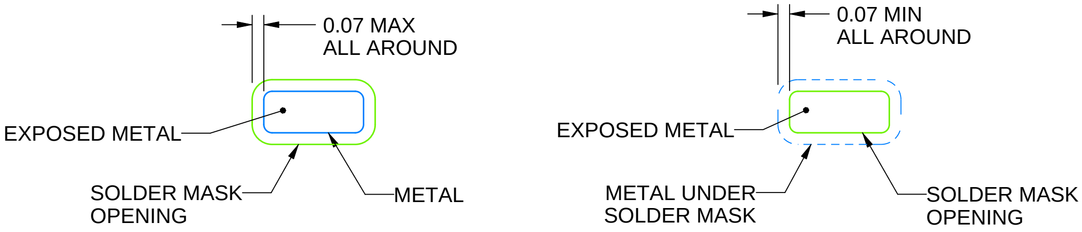


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



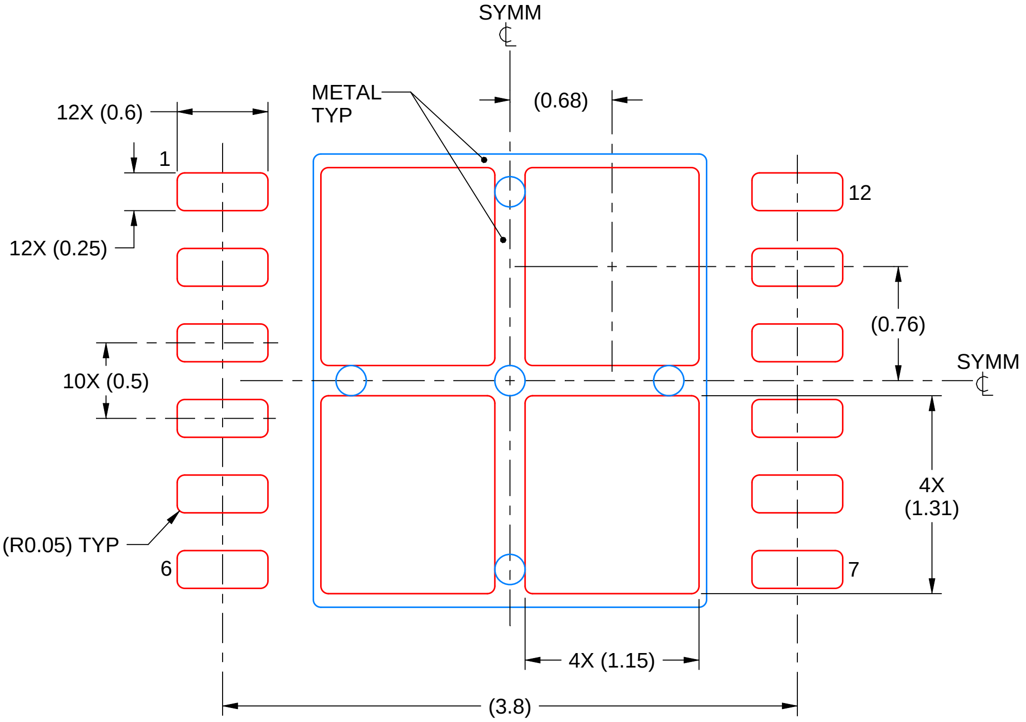
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
77% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

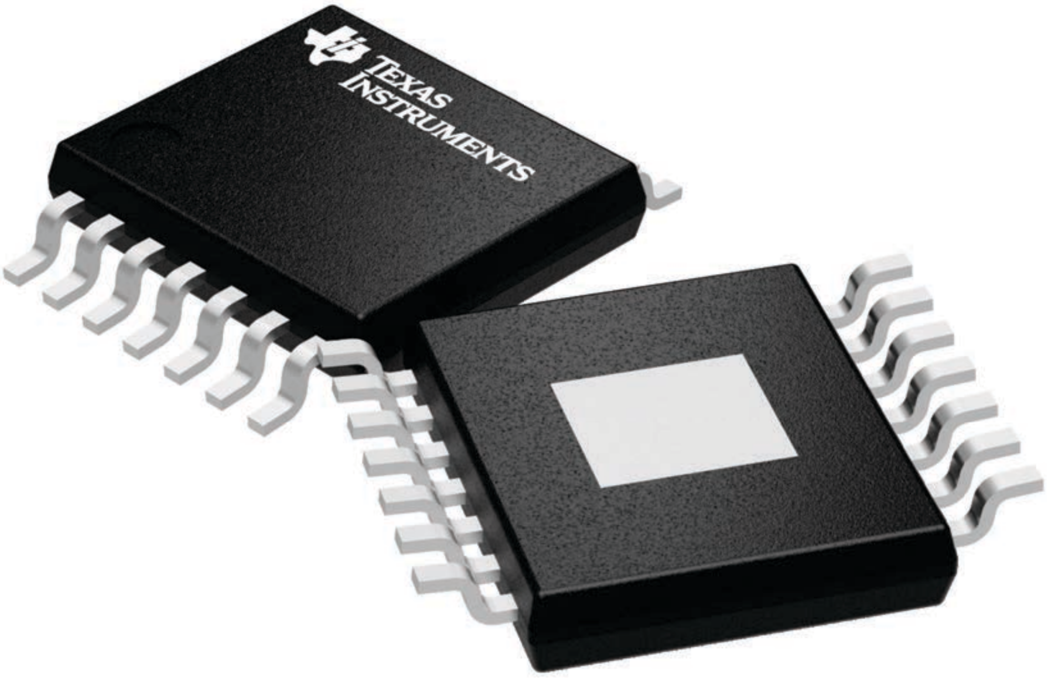
PWP 14

PowerPAD TSSOP - 1.2 mm max height

4.4 x 5.0, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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