

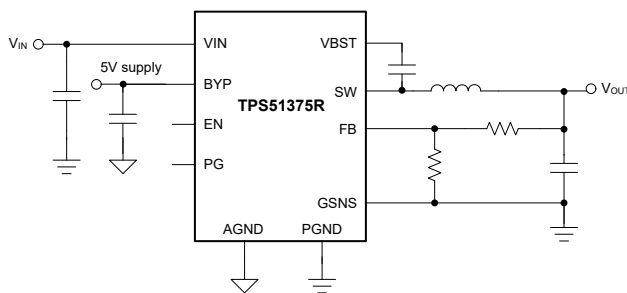
TPS51375R 4.5V to 24V, 12A Continuous Current, 26A Maximum Current, Synchronous Buck Converter

1 Features

- 4.5V to 24V input voltage range
- 0.6V to 5.5V output voltage
- Integrated 10mΩ and 5mΩ FETs
- Supports 12A continuous output current
- 270uA low quiescent current
- ±1% reference voltage accuracy (25°C)
- D-CAP3™ control mode architecture control for fast transient response optimizing 0.77V output
- Support POSCAP and all MLCC output capacitor
- Differential remote sensing
- ULQ™ extended battery life during system standby
- Built-in output discharge function
- Integrated power-good indicator
- Fixed 600kHz switching frequency
- 26A fixed OC limit
- Fixed 1.0ms soft-start time
- Large duty cycle operation
- Cycle-by-cycle overcurrent protection
- Latched output OV and UV protections
- Non-latched UVLO and OT protections
- –40°C to 125°C operating junction temperature
- 19-pin, 3.0mm × 4.0mm, HotRod™ WQFN package
- Create a custom design using the TPS51375R with the [WEBENCH® Power Designer](#)

2 Applications

- [Notebook and PC computers](#)
- Ultrabook, [handheld tablet computers](#)
- [Industrial PC, single-board computers](#)
- [Non-military drone](#)
- Distributed power systems



Simplified Schematic

3 Description

The device is a monolithic, 12A, synchronous buck converter with integrated MOSFETs that enables high efficiency and offers ease-of-use with minimum external component count for space-conscious power systems. The TPS51375R employs D-CAP3 control mode that provides fast transient response and excellent line and load regulation with internal compensation. The ULQ extended battery life feature is extremely beneficial for long battery life in low power operation. The large duty operation greatly improves the load transient performance when input voltage is low.

Other features include differential remote sensing, Eco-mode operation for high light load efficiency, body braking for load transient improvement under low output voltage. TPS51375R supports VCCPRIM_VNNAON power rails in Intel Meteor Lake and Arrow Lake platform.

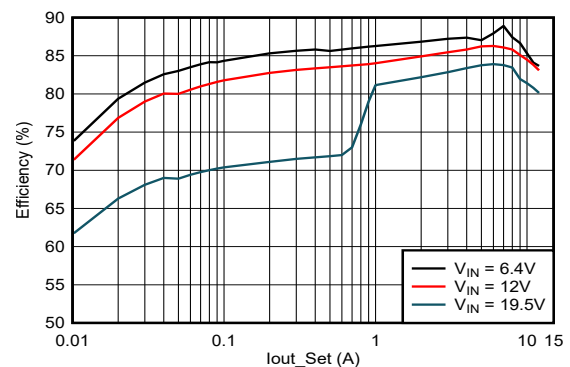
The TPS51375R integrates a power-good indicator and provides an output discharge function. The device provides complete protection, including OVP, UVP, OCP, OTP, and UVLO. The device is available in a 19-pin, 3.0mm × 4.0mm HotRod package, and the junction temperature is specified from –40°C to 125°C.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
TPS51375R	VBH (WQFN-FCRLF, 19)	4mm × 3mm

(1) For more information, see [Section 10](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Efficiency vs Output Current ($V_{OUT} = 0.77V$)



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4 Pin Configuration and Functions

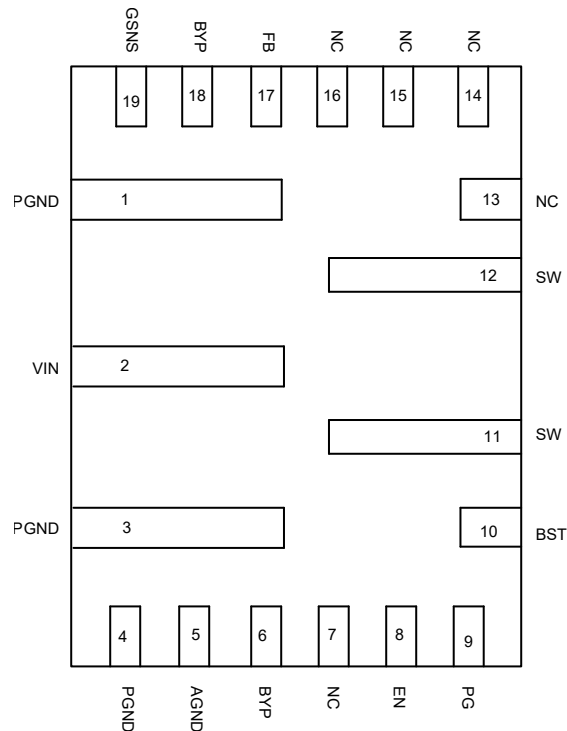


Figure 4-1. 19-Pin WQFN-FCRLF, VBH Package (Top View)

Table 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
PGND	1, 3, 4	G	Power GND terminal for the controller circuit and the internal circuitry.
VIN	2	P	Input voltage supply pin for the control circuitry. Connect the input decoupling capacitors between VIN and PGND.
AGND	5	G	Ground of internal analog circuitry. Connect AGND to PGND at a single point close to AGND.
BYP	6, 18	O	External 5V bypass power supply input. Decouple this pin to GND with a 2.2µF ceramic capacitor. This BYP external voltage must come after VIN voltage on and quit before VIN off.
NC	7, 13 – 16		Leave the pin floating or connect to GND.
EN	8	I	Enable input of buck converter.
PG	9	O	Power-good indicator pin. This pin asserts low if the output voltage of buck is out of range due to thermal shutdown, dropout, over-voltage, EN shutdown or during slow start.
BST	10	I	Boot-strap pin. Supply high side gate driver. Connect a 0.1µF ceramic capacitor between this pin and the SW pin.
SW	11, 12	O	Switching node connection to the inductor and bootstrap capacitor for buck. This pin voltage swings from a diode voltage below the ground up to input voltage of buck.
FB	17	I	Output feedback. Connect FB to the output voltage with a feedback resistor divider.
GSNS	19	I	The return connection for a remote voltage sensing configuration. Short to AGND for single-end sense configuration.

(1) I = input, O = output, P = power, G = ground

5 Specifications

5.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
Input voltage	VIN	-0.3	28	V
Input voltage	VBST	-0.3	34	V
Input voltage	VBST – SW	-0.3	6	V
Input voltage	EN, FB , BYP	-0.3	6	V
Output voltage	SW	-1	28	V
Output voltage	SW (10ns transient)	-4	28	V
Output voltage	PG	-0.3	6	V
Operating junction temperature	T _J	-40	150	°C
Storage temperature	T _{stg}	-55	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage range	VIN	5.5		24	V
Input voltage range	VBST	-0.1		29.5	V
Input voltage range	VBST – SW	-0.1		5.5	V
Input voltage range	EN, FB, BYP	-0.1		5.5	V
Output voltage range	SW	-1		24	V
Output voltage range	PG	-0.1		5.5	V
Output current range	Continuous IOU			12	A
Operating junction temperature	T _J	-40		125	°C

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		DEVICE		UNIT
		VBH (QFN, JDEC)		
		19 PINS		
R _{θJA}	Junction-to-ambient thermal resistance	72.7	29.86	°C/W
R _{θJB}	Junction-to-board thermal resistance	18.7	Not Applicable ⁽²⁾	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	50.1	Not Applicable ⁽²⁾	°C/W
ψ _{JT}	Junction-to-top characterization parameter	1.8	1.93	°C/W

5.4 Thermal Information (continued)

THERMAL METRIC ⁽¹⁾		DEVICE		UNIT
		VBH (QFN, JDEC)		
		19 PINS		
ψ_{JB}	Junction-to-board characterization parameter	18.4	NA	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.
- (2) The thermal simulation setup is not applicable to a TI EVM layout.

5.5 Electrical Characteristics

Unless otherwise noted, $V_{EN} = 5V$; $T_J = -40^{\circ}C$ to $+125^{\circ}C$, Typical values are at $T_J = 25^{\circ}C$ and $V_{IN} = 12V$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY (VIN)						
I_{VIN}	VIN supply current (quiescent)	No load, $V_{EN} = 5V$, non-switching		270		μA
I_{INSDN}	VIN shutdown current	No load, $V_{EN} = 0V$, PG open		3		μA
ENABLE (EN), MODE						
$V_{EN(ON)}$	EN threshold high-level	$T_J = 25^{\circ}C$	1			V
$V_{EN(OFF)}$	EN threshold low-level	$T_J = 25^{\circ}C$			0.4	V
R_{EN}	EN pull down resistor			150		k Ω
BYP						
$V_{BYP_UVLO_R}$	BYP undervoltage lockout rising threshold			4.2		V
$V_{BYP_UVLO_F}$	BYP undervoltage lockout falling threshold			3.5		V
$V_{BYP_I_SHDN}$	BYP shutdown current (EN = LOW)			10		μA
V_{BYP_IQ}	BYP quiescent current (EN = HIGH)			650		μA
OUTPUT VOLTAGE (VOUT)						
V_{FB}	FB voltage	$T_J = 25^{\circ}C$	594	600	606	mV
DUTY CYCLE and FREQUENCY CONTROL						
$t_{ON(min)}$	Minimum ON pulse width			60		ns
$t_{OFF(min)}$	Minimum OFF pulse width			130		ns
SOFT-START						
t_{SS}	Internal fixed soft start			1		ms
POWER SWITCHES (SW)						
$R_{DSON(HS)}$	High-side MOSFET on-resistance	$T_J = 25^{\circ}C$		10		m Ω
$R_{DSON(LS)}$	Low-side MOSFET on-resistance	$T_J = 25^{\circ}C$		5		m Ω
CURRENT LIMIT						
$I_{OCL(VALLEY)}$	Low-side valley current limit	Valley current limit on LS FET, $-40^{\circ}C \leq T_J \leq 125^{\circ}C$	22	26	30	A
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	OVP trip threshold			120		%
t_{OVPDLY}	OVP latch-off propagation deglitch time			256		μs
V_{UVP}	UVP trip threshold		55	60	65	%
t_{UVPDLY}	UVP latch-off propagation deglitch time			200		μs
POWER GOOD (PG)						
$t_{PGDLY(Rise)}$	PG delay rising	PG from low to high		160		μs
$t_{PGDLY(Fall)}$	PG delay falling	PG from high to low		30		μs
V_{PGTH}	PG threshold when FB falling (fault)	V_{FB} falling (fault), percentage of V_{FB}		83		%
V_{PGTH}	PG threshold when FB rising (good)	V_{FB} rising (good), percentage of V_{FB}		90		%
V_{PG_L}	PG sink current capability	$I_{OL} = 4mA$			0.4	V
I_{PGLK}	PG leak current	$V_{PG} = 5.5V$			1	μA
OUTPUT DISCHARGE						

5.5 Electrical Characteristics (continued)

Unless otherwise noted, $V_{EN} = 5V$; $T_J = -40^{\circ}C$ to $+125^{\circ}C$, Typical values are at $T_J = 25^{\circ}C$ and $V_{IN} = 12V$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{DIS}	Discharge resistance	$T_J = 25^{\circ}C$, $V_{EN} = 0V$, $V_{SW} = 0.5V$		50		Ω
THERMAL SHUTDOWN						
$T_{J(SD)}$	Thermal shutdown threshold			160		$^{\circ}C$
$T_{J(HYS)}$	Thermal shutdown hysteresis ⁽¹⁾			20		$^{\circ}C$

- (1) These parameters are provided for reference only, and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

5.6 Typical Characteristics

$T_J = -40^{\circ}\text{C}$ to 125°C , $V_{IN} = 12\text{V}$, unless otherwise noted.

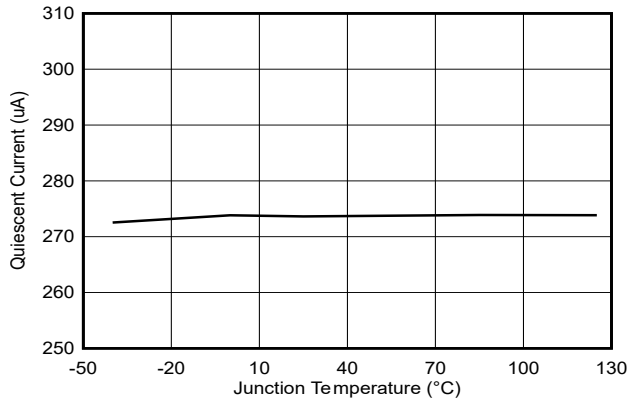


Figure 5-1. Supply Current vs Junction Temperature

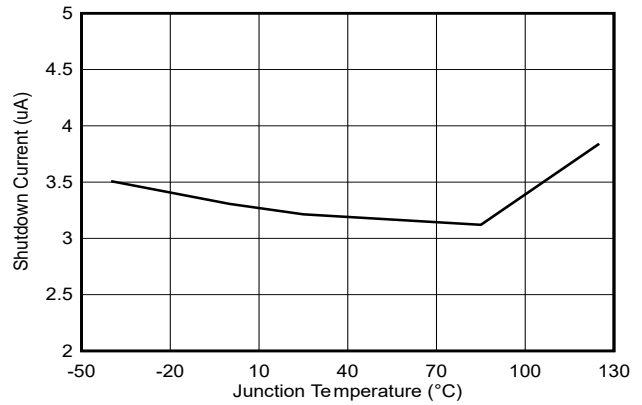


Figure 5-2. Shutdown Current vs Junction Temperature

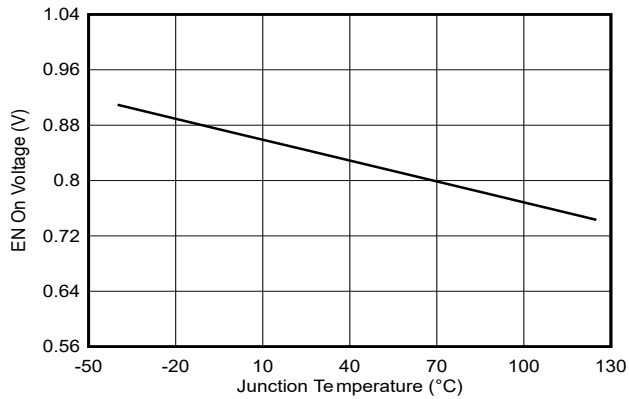


Figure 5-3. Enable On Voltage vs Junction Temperature

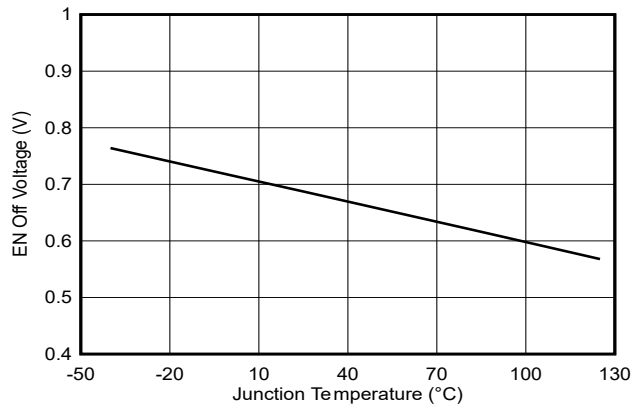


Figure 5-4. Enable Off Voltage vs Junction Temperature

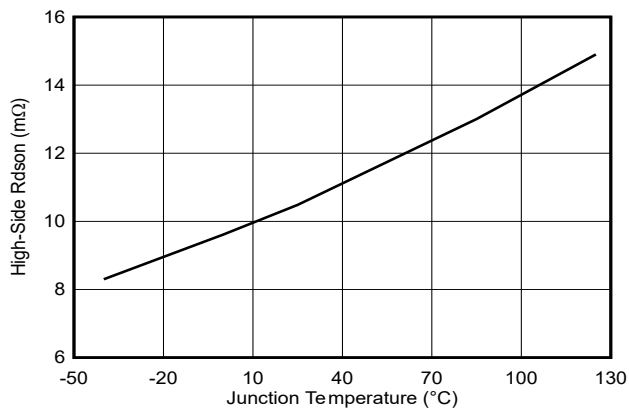


Figure 5-5. High-Side $R_{DS(on)}$ vs Junction Temperature

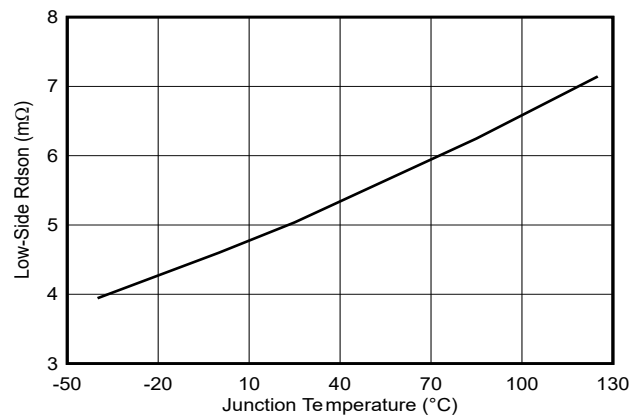


Figure 5-6. Low-Side $R_{DS(on)}$ vs Junction Temperature

5.6 Typical Characteristics (continued)

$T_J = -40^{\circ}\text{C}$ to 125°C , $V_{IN} = 12\text{V}$, unless otherwise noted.

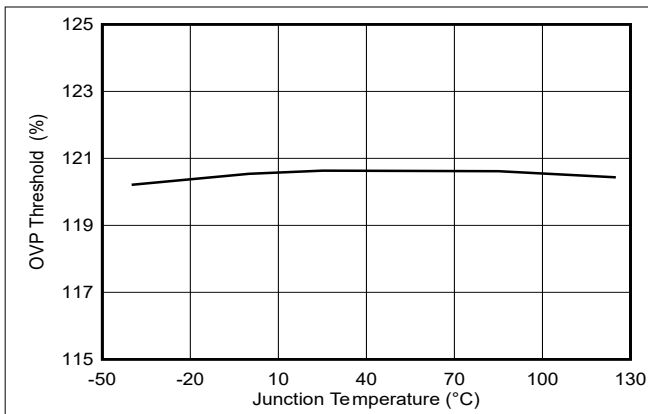


Figure 5-7. OVP Threshold vs Junction Temperature

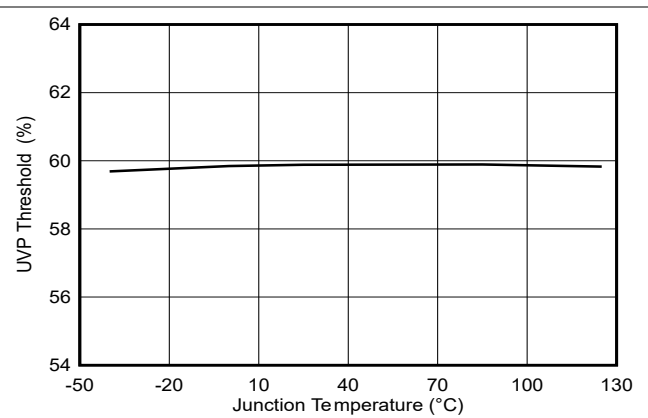


Figure 5-8. UVP Threshold vs Junction Temperature

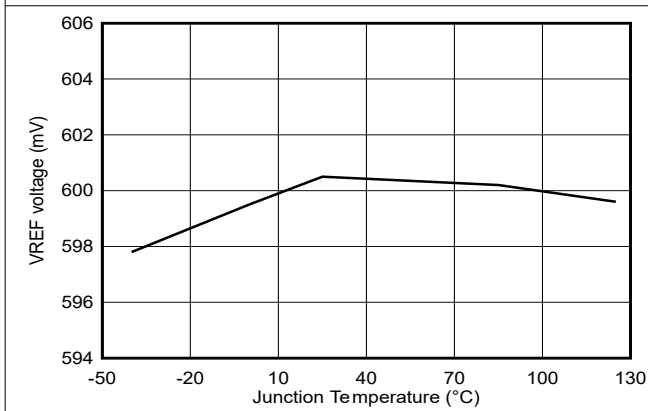


Figure 5-9. VREF Voltage vs Junction Temperature

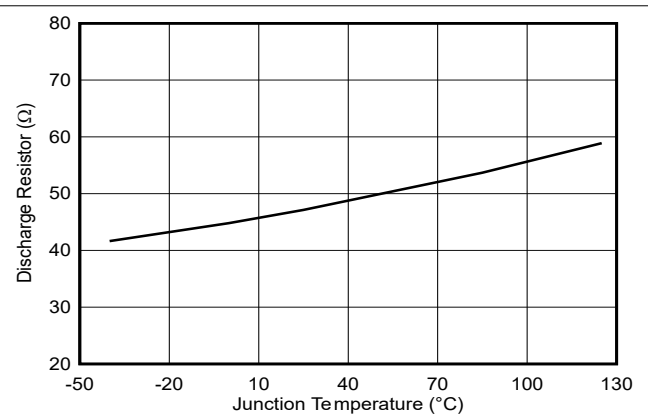


Figure 5-10. Discharge Resistor vs Junction Temperature

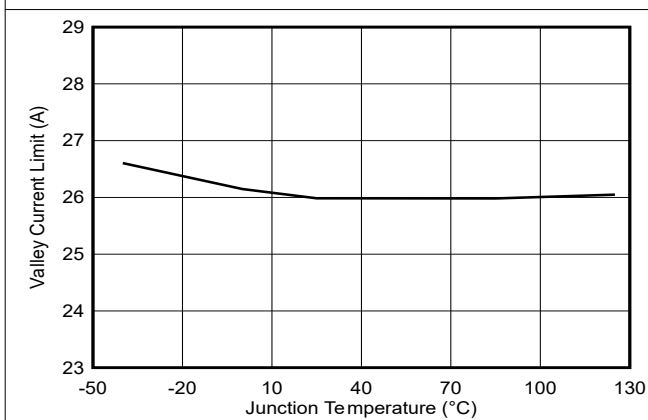


Figure 5-11. Valley Current Limit vs Junction Temperature

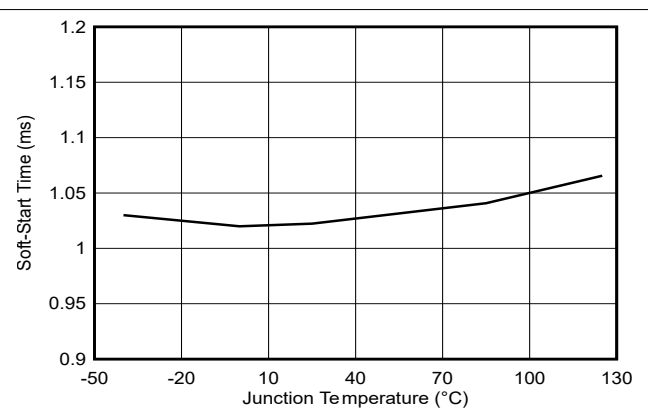


Figure 5-12. Soft-Start Time vs Junction Temperature

5.6 Typical Characteristics (continued)

$T_J = -40^{\circ}\text{C}$ to 125°C , $V_{IN} = 12\text{V}$, unless otherwise noted.

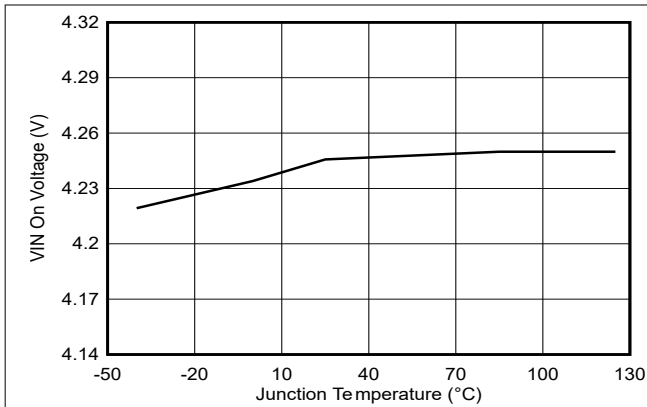


Figure 5-13. VIN UVLO Rising vs Junction Temperature

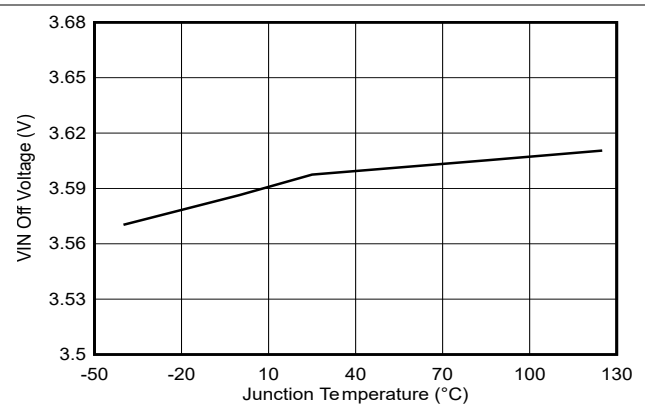


Figure 5-14. VIN UVLO Falling vs Junction Temperature

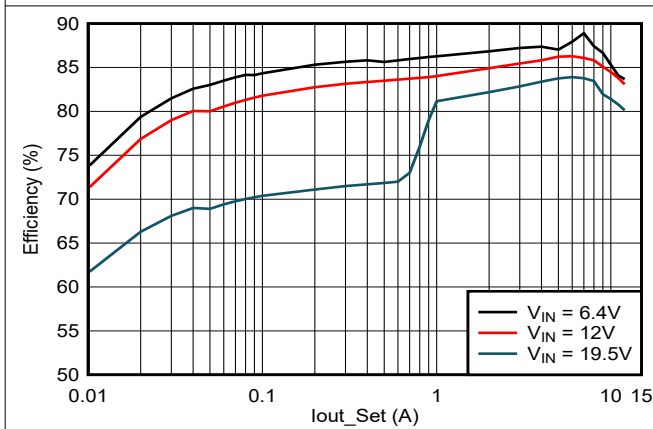


Figure 5-15. Efficiency vs Load Current, $F_{SW} = 600\text{kHz}$, $V_{OUT} = 0.77\text{V}$

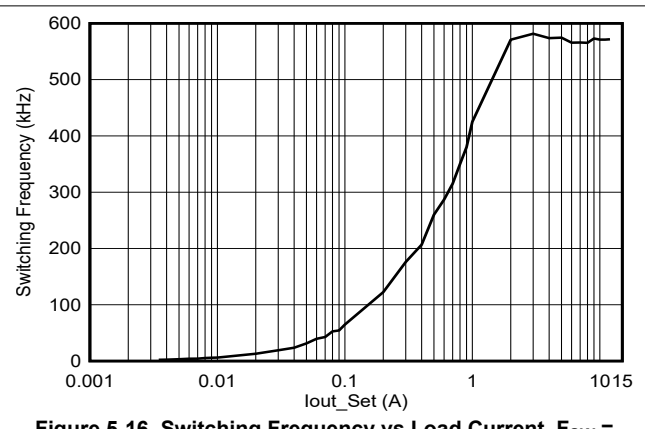


Figure 5-16. Switching Frequency vs Load Current, $F_{SW} = 600\text{kHz}$

6 Detailed Description

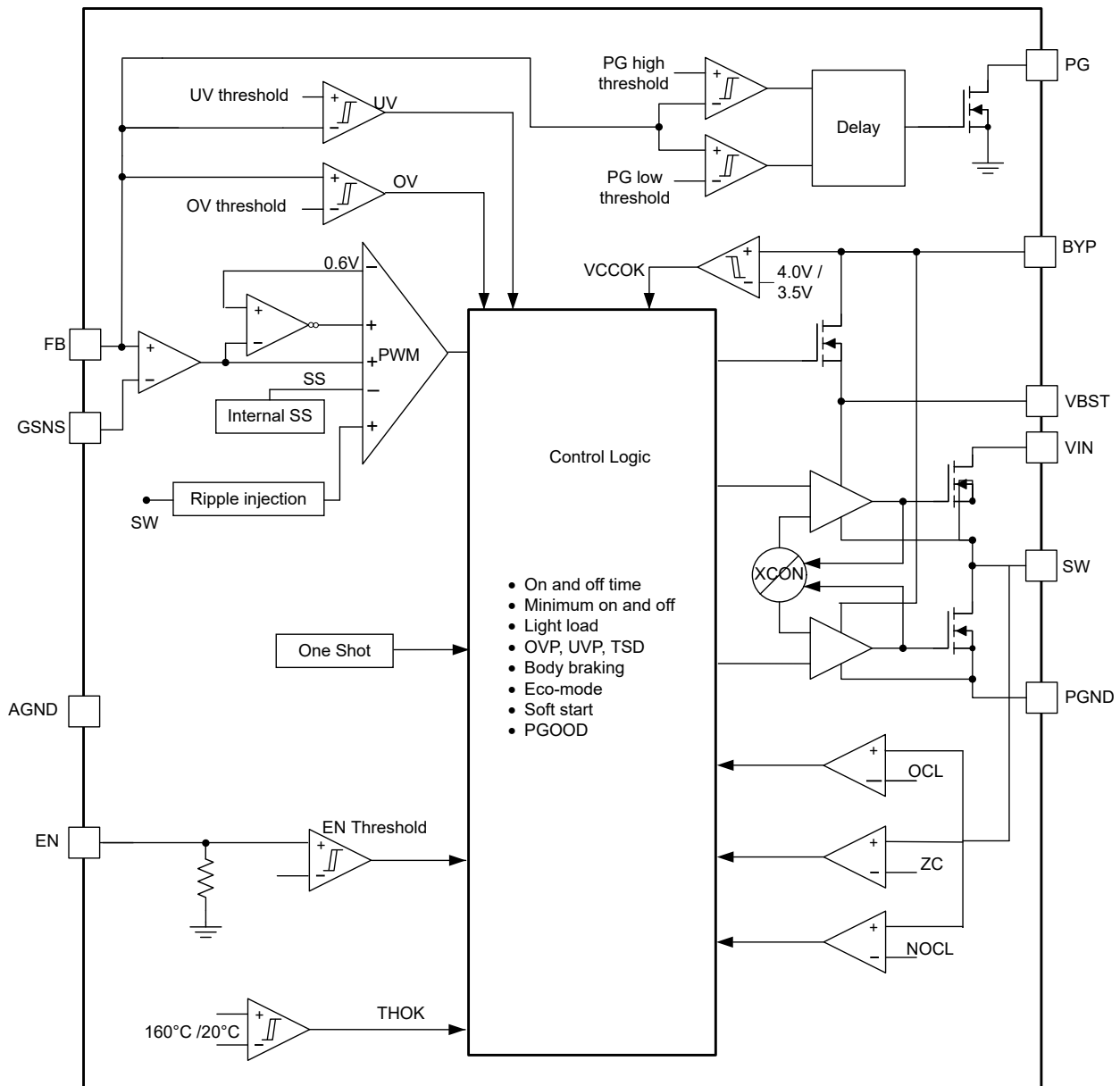
6.1 Overview

TPS51375R is a 12A, peak 26A, integrated FET, synchronous step-down converter which can operate from 4.5V to 24V input voltage (VIN), and the output voltage is from 0.6V to 5.5V. The device has 10mΩ and 5mΩ integrated MOSFETs that enable high efficiency up to 12A. The device employs D-CAP3 control mode that provides fast transient response with no external compensation components and an accurate feedback voltage. The control topology provides seamless transition between CCM operating mode at higher load condition and DCM, Eco-mode operation at lighter load condition. DCM, Eco-mode allows the TPS51375R to maintain high efficiency at light load. D-CAP3 control mode allows the use of low equivalent series resistance (ESR) output capacitors such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors.

TPS51375R needs 5V external supply to bias for all internal circuitry. This external voltage must come after VIN voltage on and quit before VIN off. The undervoltage lockout (UVLO) circuit monitors the BYP pin voltage to protect the internal circuitry from low input voltages. TPS51375R has an internal pulldown current source on the EN pin, require external pullup circuit to enable buck converter.

TPS51375R supports 600kHz switching frequency. The internal soft-start time is fixed 1ms to simplify the design circuit and reduce the external components.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 PWM Operation and D-CAP3™ Control Mode

The main control loop of the buck is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP3 control mode. The D-CAP3 control mode combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. The D-CAP3 control mode is stable even with virtually no ripple at the output. The TPS51375R also includes an error amplifier that makes the output voltage high accurate.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after an internal one-shot timer expires. This one-shot duration is set proportional to the converter input voltage, V_{IN} , and is

inversely proportional to the output voltage, V_{OUT} , to maintain a pseudo-fixed frequency over the input voltage range, therefore called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ripple generation circuit is added to the reference voltage to emulate the output ripple. This action enables the use of low-ESR output capacitors such as multi-layered ceramic caps (MLCC). No external current sense network or loop compensation is required for D-CAP3 control mode.

For any control topology that is compensated internally, there is a range of the output filter the control topology can support. The output filter used with the TPS51375R is a low-pass L-C circuit. This L-C filter has a double-pole frequency calculated in [Equation 1](#).

$$f_P = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} \quad (1)$$

At low frequencies, the overall loop gain is set by the external output set-point resistor divider network and the internal gain of the TPS51375R. The low-frequency L-C double pole has a 180 degree lag in-phase. At the output filter frequency, the gain rolls off at a -40dB per decade rate and the phase drops rapidly. The internal ripple generation network introduces a mid-frequency zero that reduces the gain roll off from -40dB to -20dB per decade and increases the phase to 90 degree one decade above the zero frequency. The inductor and capacitor selected for the output filter must be such that the double pole is placed close enough to the mid-frequency zero so that the phase boost provided by this mid-frequency zero provides adequate phase margin for the stability requirement. The crossover frequency of the overall system must typically be targeted to be less than one-third of the switching frequency (F_{SW}).

6.3.2 Remote Sense

The TPS51375R device offers remote sense function through the FB and GSNS pins. Remote sense function compensates a potential voltage drop on the PCB traces, thus helps maintain V_{OUT} tolerance under steady state operation and load transient event. Connecting the FB voltage divider resistors to the remote location allows sensing the output voltage at a remote location. The connections from the FB voltage divider resistors to the remote location must be a pair of PCB traces with at least 12-mil trace width, and must implement Kelvin sensing across a high bypass capacitor of $0.1\mu\text{F}$ or higher. The ground connection of the remote sensing signal must be connected to the GSNS pin. The V_{OUT} connection of the remote sensing signal must be connected to the feedback resistor divider with the lower feedback resistor, RFB_LS, terminated at the GSNS pin. To maintain stable output voltage and minimize the ripple, the pair of remote sensing lines must stay away from any noise sources, such as inductor and SW nodes, or high frequency clock lines. TI recommends to shield the pair of remote sensing lines with ground planes above and below. Single-ended V_o sensing is often used for local sensing. For this configuration, connect the higher FB resistor, RFB_HS, to a high-frequency local bypass capacitor of $0.1\mu\text{F}$ or higher, and short GSNS to AGND.

6.3.3 Body Braking

During load step down, the converter senses the amplitude of the output voltage change. If the output voltage change is big enough, TPS51375R implements a body braking function that turns off both high-side and low-side FET and allows power to dissipate through the low-side body diode, reducing overshoot. This approach is effective, while having some impact on efficiency during transient.

6.3.4 BYP pin Function

The BYP pin is the input for the external 5V supply needed to bias all the internal circuitry and MOSFET gate drivers. The BYP pin must be bypassed with a $2.2\mu\text{F}$ capacitor. The UVLO circuit monitors the BYP pin voltage and disables the output when BYP pin voltage falls below the UVLO threshold. This BYP external voltage must come after V_{IN} voltage on and quit before V_{IN} off.

6.3.5 Soft Start

The TPS51375R has an internal 1ms soft start. When the EN pin becomes high, the internal soft-start function begins ramping up the reference voltage to the PWM comparator. If the output capacitor is prebiased at start-up, the device initiates switching and starts ramping up only after the internal reference voltage becomes greater

than the feedback voltage V_{FB} . This scheme makes sure that the converters ramp up smoothly into regulation point.

6.3.6 Large Duty Operation

The TPS51375R can support large duty operation by the internal T_{ON} extension function. When $V_{IN}/V_{OUT} < 1.18$ and the V_{FB} keeps lower than internal V_{REF} , the switching frequency is allowed to smoothly drop to make T_{ON} extended to implement the large duty operation and also improve the performance of the load transient performance. The TPS51375R can support up to 98% duty cycle operation.

6.3.7 Power Good

The Power-Good (PGOOD) pin is an open-drain output. TI recommends a pullup resistor of 100k Ω to pull the voltage up to BYP. After V_{FB} is between 90% and 115% of the target output voltage, the PGOOD is pulled high after a 200 μ s deglitch time. The PGOOD pin is pulled low when:

- FB pin voltage is lower than 83% or greater than 120% of the target output voltage
- In OVP, UVP, or thermal shutdown event
- During the soft-start period

6.3.8 Overcurrent Protection and Undervoltage Protection

The TPS51375R has overcurrent protection and undervoltage protection. The output overcurrent protection (OCP) is implemented using a cycle-by-cycle low-side MOSFET valley current detection. The switching current is monitored by measuring the MOSFET drain to source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on-time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{OUT} . If the monitored current is above the OCL level, the converter maintains low-side FET on and delays the creation of a new pulse, even the voltage feedback loop requires one, until the current level becomes OCL level or lower. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of overcurrent protection. When the load current is higher than the $I_{OCL(VALLEY)}$ added by one half of the peak-to-peak inductor ripple current, the OCP is triggered and the output current is being limited, the output voltage tends to drop because the load demand is higher than what the converter can support. When the output voltage falls below 60% of the target voltage, the UVP comparator detects the fall, and the device is shut off after a wait time of 200 μ s. This protection is a latched function. The fault latching can be reset by EN going low or BYP power cycling.

6.3.9 Overvoltage Protection

The TPS51375R has an overvoltage protection feature. When the output voltage becomes higher than 120% of the target voltage, the OVP comparator output goes high, and the output discharges and latches after a wait time of 256 μ s. This function is a latching operation, so this function must reset by EN going low or VIN power cycling.

6.3.10 UVLO Protection

The VIN undervoltage lockout (UVLO) protection monitors the VIN pin voltage to protect the internal circuitry from low input voltage. When the VIN voltage is lower than the UVLO threshold voltage, the device shuts off and outputs are discharged to prevent misoperation of the device. The converter begins operation again when the input voltage exceeds the threshold by a hysteresis of 650mV (typical). This protection is a non-latch protection.

6.3.11 Output Voltage Discharge

TPS51375R has a 50ohm discharge switch that discharges the output VOUT through the Vout pin during any event of fault like output overvoltage, output undervoltage, thermal shutdown, or if the VIN voltage is below the UVLO and when the EN pin voltage is below the turn-on threshold.

6.3.12 Standby Operation

The TPS51375R can be placed in standby mode by pulling the EN pin low. The device operates with a shutdown current of 3µA when in standby condition. EN pin is pulled low internally. When floating, the part is disabled by default.

6.3.13 Thermal Shutdown

The TPS51375R monitors the internal die temperature. If the temperature exceeds the threshold value (typically 160°C), the device is shut off and the output is discharged. This protection is a non-latch protection. The device restarts operation when the temperature goes below the thermal shutdown threshold.

6.4 Device Functional Modes

6.4.1 Advanced Eco-mode Control

The advanced Eco-mode control schemes to maintain high light load efficiency. As the output current decreases from heavy load conditions, the inductor current is also reduced and eventually comes to a point where the rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode. The on-time is kept almost the same as in continuous conduction mode so that discharging the output capacitor with smaller load current to the level of the reference voltage takes longer. This action makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high. Use [Equation 2](#) to calculate the light load current where the transition to Eco-mode operation happens ($I_{OUT(LL)}$).

$$I_{OUT(LL)} = \frac{1}{2 \times L_{OUT} \times F_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (2)$$

After identifying the application requirements, design the output inductance (L_{OUT}) so that the inductor peak-to-peak ripple current is approximately between 20% and 40% of $I_{OUT(max)}$ (peak current in the application). Sizing the inductor properly so that the valley current does not hit the negative low-side current limit is important.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The schematic in [Figure 7-1](#) shows a typical application for TPS51375R with 0.77V output. This design converts an input voltage range of 4.5V to 24V down to 0.77V with a maximum continuous output current of 12A.

7.2 Typical Application

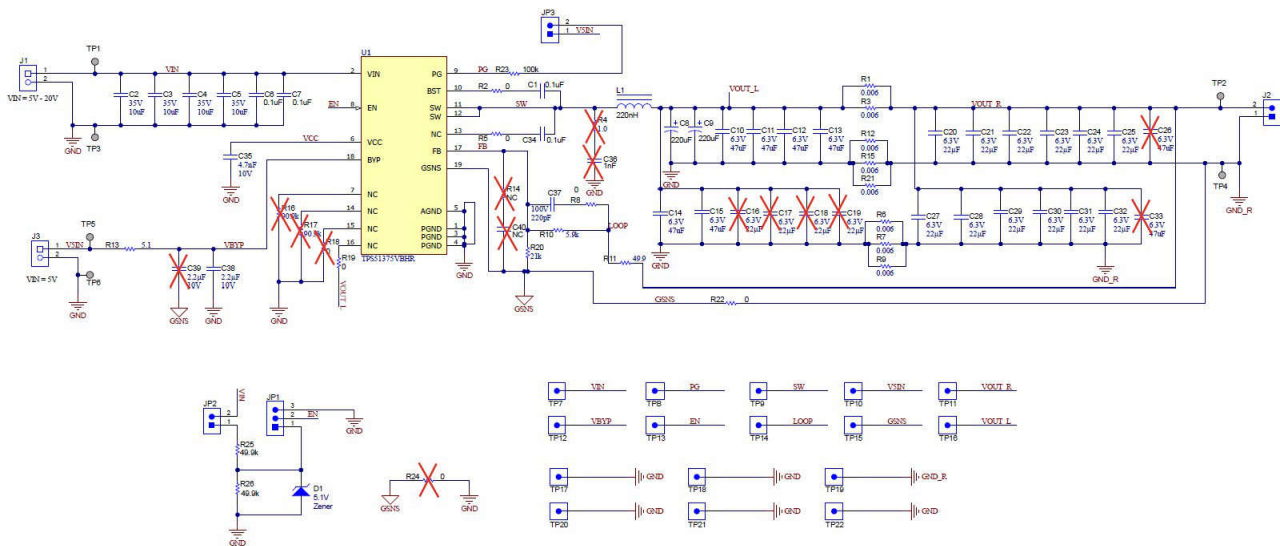


Figure 7-1. VCCPRIM_VNNAON 0.77V, 12A Continuous Current Reference Design

7.2.1 Design Requirements

[Table 7-1](#) lists the design parameters for this example.

Table 7-1. Design Parameters

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage		0.77		V
I_{OUT}	Output current		12		A
V_{IN}	Input voltage	4.5	19.5	24	V
$V_{OUT(ripple)}$	Output voltage ripple	0A – 12A loading	10		mV _{P-P}
$V_{OUT(min)}$	Minimum output voltage	0A – 10A loading, 10A/us	720		mV
$V_{OUT(max)}$	Maximum output voltage	7A – 17A loading, 10A/us		827.5	mV
F_{SW}	Switching frequency		600		kHz
R_{PATH_VOUT}	VOUT path parasitic resistance		3		mΩ
R_{PATH_GND}	GND path parasitic resistance		1.5		mΩ
T_A	Ambient temperature		25		°C

7.2.2 Detailed Design Procedure

7.2.2.1 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the TPS51375R device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

7.2.2.2 External Component Selection

7.2.2.2.1 Remote Sense Amplifier and Adjusting the Output Voltage

Remote sensing of the output voltage is provided through a dedicated high speed, low offset instrumentation type amplifier. Connect the output voltage setting resistive divider described below from the output voltage sensing point to the GSNS pin. The center point is to be connected to the FB pin. Note the GSNS pin is to be tied to the converter output voltage return at a location near to the load. The output voltage is programmed with a resistor divider from the converter output (V_{OUT}) to the FB pin as shown in [Figure 7-2](#). Use 1% tolerance or better divider resistors.

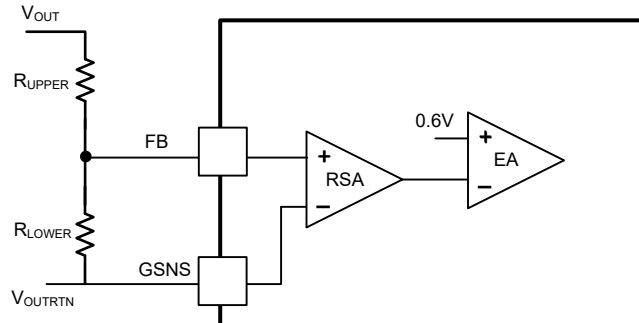


Figure 7-2. FB Resistor Divider With Remote Sense

To change the output voltage of the application, change the value of the upper feedback resistor. By changing this resistor, the user can change the output voltage above 0.6V. See [Equation 3](#).

$$V_{OUT} = 0.6 \times \left(1 + \frac{R_{UPPER}}{R_{LOWER}} \right) \quad (3)$$

7.2.2.2.2 Inductor Selection

The inductor ripple current is filtered by the output capacitor. A higher inductor ripple current means the output capacitor must have a ripple current rating higher than the inductor ripple current. See [Table 7-3](#) for recommended inductor values.

Use [Equation 4](#) and [Equation 5](#) to calculate the RMS and peak currents through the inductor. Make sure that the inductor is rated to handle these currents.

$$I_{L(rms)} = \sqrt{I_{OUT}^2 + \frac{1}{12} \times \left[\frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{V_{IN(max)} \times L_{OUT} \times F_{SW}} \right]^2} \quad (4)$$

$$I_{L(peak)} = I_{OUT} + \frac{I_{OUT(ripple)}}{2} \quad (5)$$

Under transient and short-circuit conditions, the inductor current can increase up to the current limit of the device. Choosing an inductor with a saturation current higher than the peak current under current limit condition is safe.

7.2.2.2.3 Output Capacitor Selection

After selecting the inductor, the output capacitor must be optimized. In D-CAP3 control mode, the regulator reacts within one cycle to the change in the duty cycle, so good transient performance can be achieved without needing large amounts of output capacitance. The recommended output capacitance range is given in [Table 7-2](#) and [Table 7-3](#). Ceramic capacitors have low ESR making ESR ripple negligible, otherwise the maximum ESR of the capacitor must be less than $V_{OUT(ripple)}/I_{OUT(ripple)}$.

Table 7-2. Recommended Component Values for VCCPRIM_VNNAON

V _{OUT} (V)	R _{LOWER} (kΩ)	R _{UPPER} (kΩ)	L _{OUT} (μH)	C _{OUT(min)} (μF)	C _{OUT(max)} (μF)	R _{FF} (kΩ)	C _{FF} (pF)
0.77	21	5.9	0.15	500	1000	NA	220

Table 7-3. Recommended Component Values for General Purpose Application

V _{OUT} (V)	F _{sw} (kHz)	L _{OUT} (μH)	C _{OUT(min)} (μF)	C _{OUT(max)} (μF)	R _{FF} (kΩ)	C _{FF} (pF)
3.3	600	1.5	88	198	NA	30
5.0	600	1.5	88	198	NA	30

7.2.2.2.4 Input Capacitor Selection

The TPS51375R requires input decoupling capacitors on power supply input pin VIN, and the bulk capacitors are needed depending on the application. Use [Equation 6](#) to calculate the minimum input capacitance required.

$$C_{IN(min)} = \frac{I_{OUT} \times V_{OUT}}{V_{IN(ripple)} \times V_{IN} \times F_{SW}} \quad (6)$$

TI recommends using a high-quality X5R or X7R input decoupling capacitors of nominal 44μF/35V on the input voltage pin VIN. The voltage rating on the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the application. Use [Equation 7](#) to calculate the input ripple current:

$$I_{CIN(rms)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN(min)}} \times \frac{(V_{IN(min)} - V_{OUT})}{V_{IN(min)}}} \quad (7)$$

7.2.2.2.5 Bootstrap Capacitor Selection

A 0.1μF ceramic capacitor must be connected between the BST and SW pins for proper operation. The capacitor must be rated for at least 10V to minimize DC bias derating.

A resistor can be added in series with the BST capacitor to slow down the turn-on of the high-side MOSFET and reduce overshoot rising edge overshoot on the SW pin. This action comes with the tradeoff of more power loss and lower efficiency. As a best practice, include a 0Ω placeholder in prototype designs in case parasitic inductance in the PCB layout results in more voltage overshoot at the SW pin than is normal. This practice helps keep the voltage within the ratings of the device and reduces the high frequency noise on the SW node.

7.2.3 Application Curves

Figure 7-3 through Figure 7-18 apply to the circuit of Figure 7-1. $V_{IN} = 12V$, $F_{SW} = 600kHz$, $T_A = 25^\circ C$, unless otherwise specified.

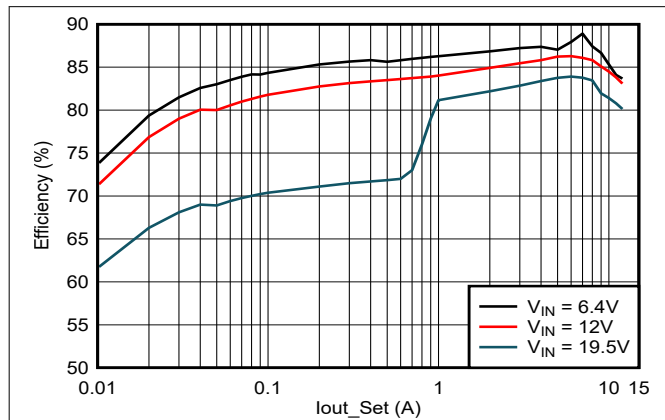


Figure 7-3. Efficiency Curve ($V_{OUT} = 0.77V$)

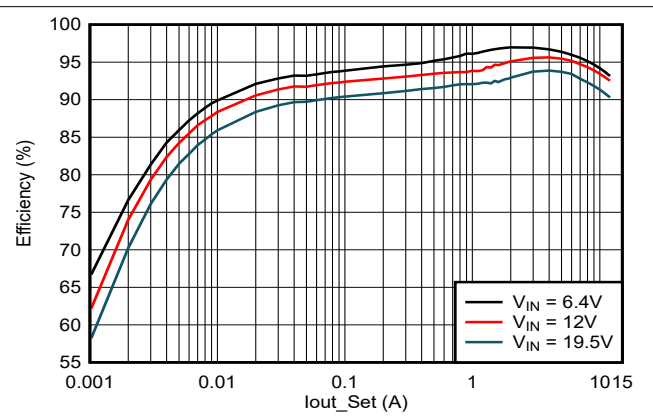


Figure 7-4. Efficiency Curve ($V_{OUT} = 3.3V$)

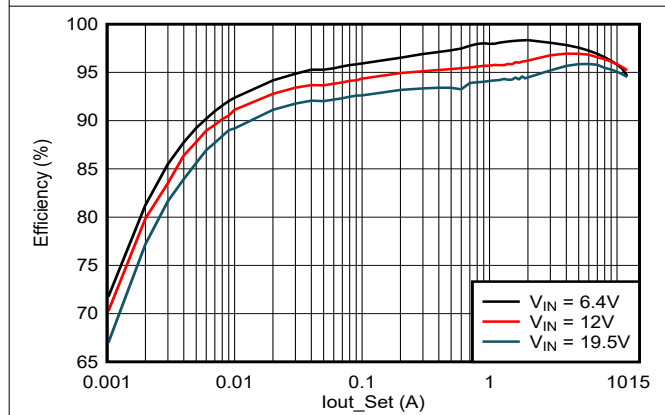


Figure 7-5. Efficiency Curve ($V_{OUT} = 5V$)

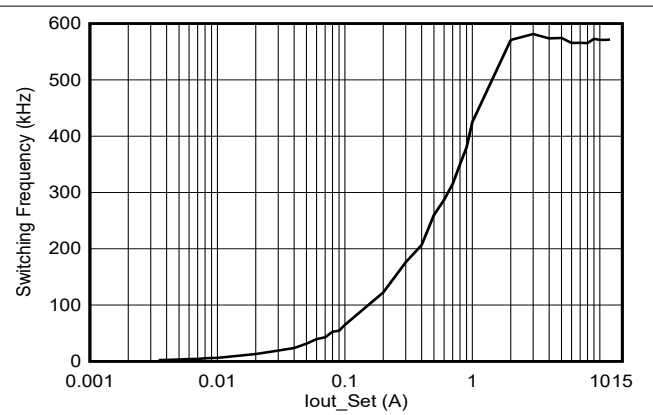


Figure 7-6. Switching Frequency vs Output Load

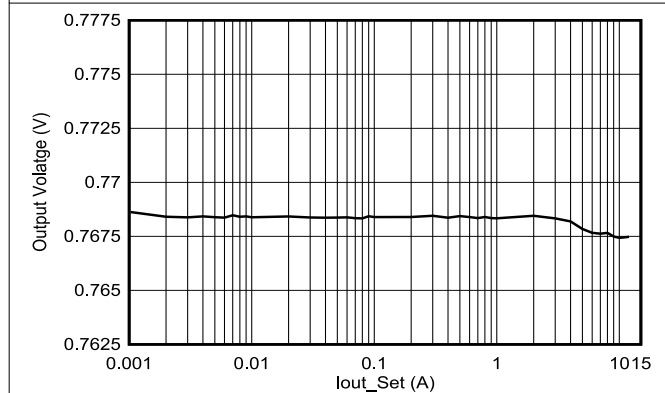


Figure 7-7. Load Regulation, $V_{IN} = 12V$

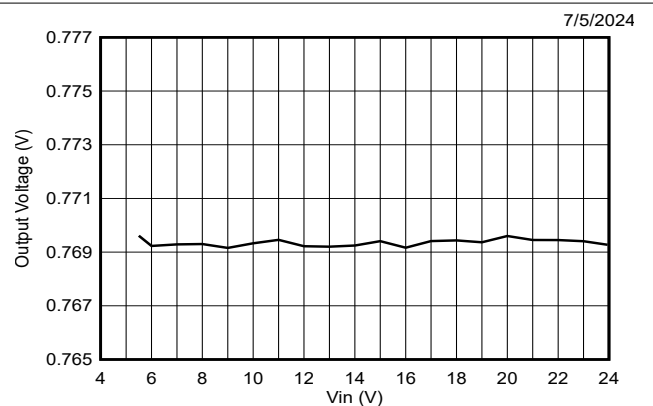


Figure 7-8. Line Regulation, $I_{OUT} = 12A$

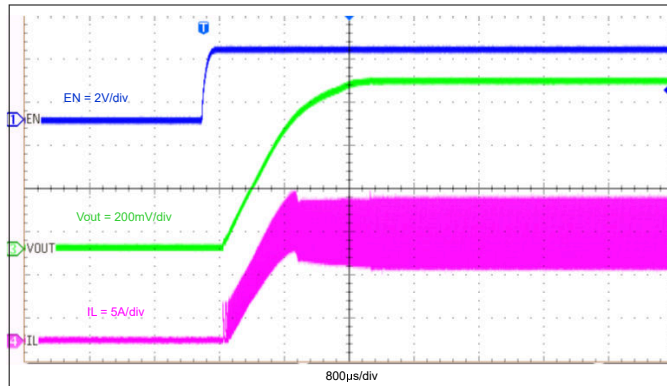


Figure 7-9. Start-Up Through EN, $I_{OUT} = 12A$

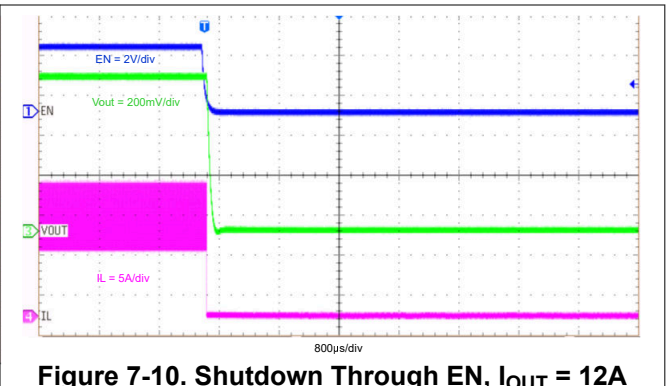


Figure 7-10. Shutdown Through EN, $I_{OUT} = 12A$

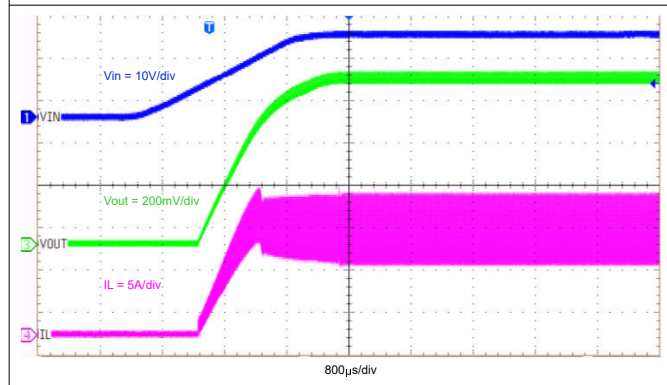


Figure 7-11. Start-Up Relative to VIN Rising, $I_{OUT} = 12A$

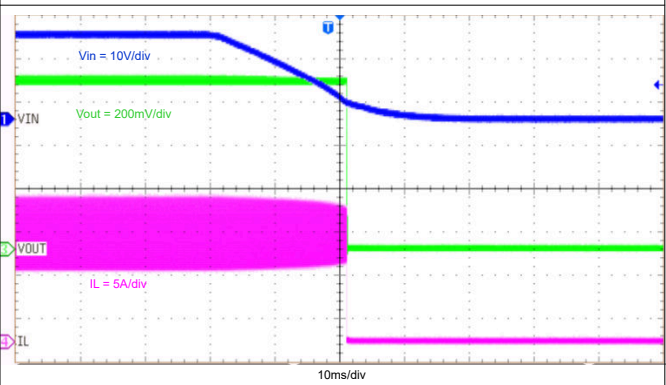


Figure 7-12. Shutdown Relative to VIN Falling, $I_{OUT} = 12A$

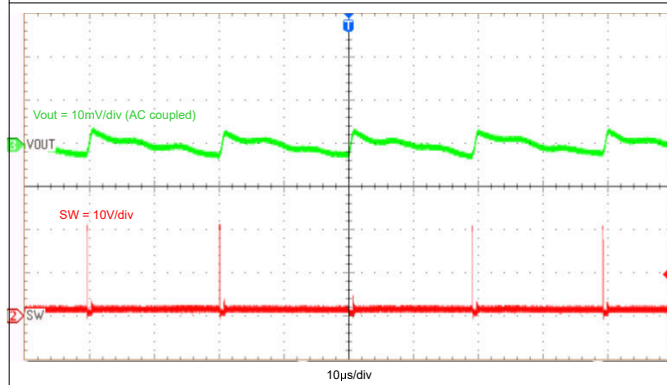


Figure 7-13. Output Voltage Ripple, $I_{OUT} = 0.1A$

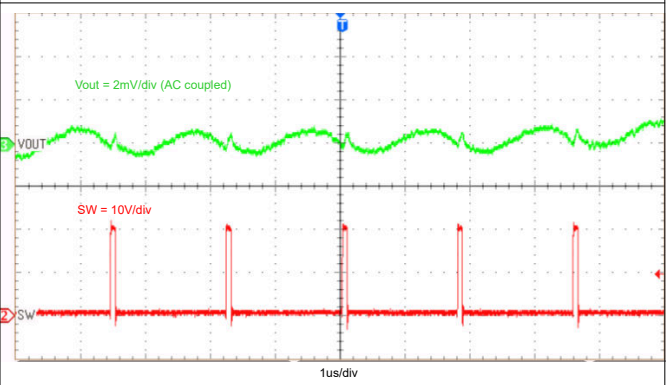
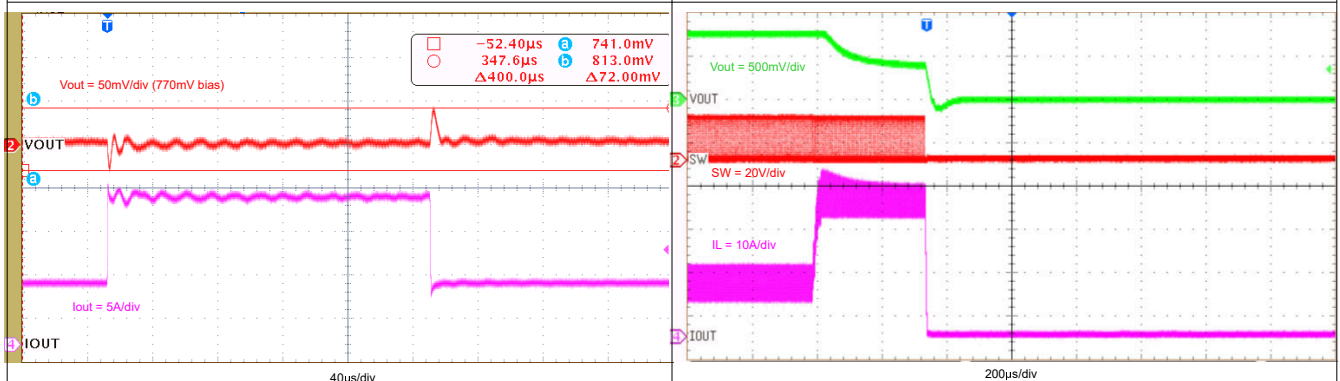
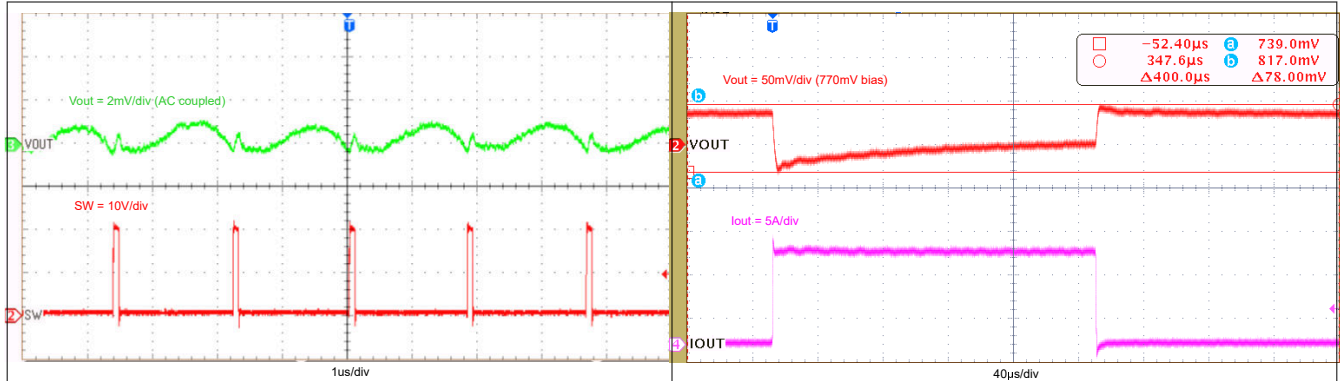


Figure 7-14. Output Voltage Ripple, $I_{OUT} = 6A$



7.3 Power Supply Recommendations

The TPS51375R is intended to be powered by a well-regulated DC voltage. The input voltage range is 4.5V to 24V. The TPS51375R is a buck converter. The input supply voltage must be greater than the desired output voltage for proper operation. Input supply current must be appropriate for the desired output current. If the input voltage supply is located far away from the TPS51375R circuit, TI recommends some additional input bulk capacitance. Typical values are 100 μ F to 470 μ F.

7.4 Layout

7.4.1 Layout Guidelines

- Make note that the PCB layout of any DC/DC converter is critical to the excellent performance of the design. Bad PCB layout can disrupt the operation of a good schematic design. Even if the converter regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore, the EMI performance of the converter is dependent on the PCB layout to a great extent. In a buck converter, the most critical PCB feature is the loop formed by the input capacitors and power ground. This loop carries large transient currents that can cause large transient voltages when reacting with the trace inductance. These unwanted transient voltages disrupt the proper operation of the converter. Because of this fact, the traces in this loop must be wide and short, and the loop area as small as possible to reduce the parasitic inductance.
- Use a four-layer PCB for good thermal performance and with maximum ground plane. 3-inch \times 2.75-inch, top and bottom layer PCB with 2oz copper is used as example.
- Place the decoupling capacitors right across VIN and BYP as close as possible.
- Place output inductors and capacitors with IC at the same layer. The SW routing must be as short as possible to minimize EMI, and must be a wide plane to carry big current. Enough vias must be added to the PGND connection of output capacitors and also as close to the output pin as possible.
- Place BST resistor and capacitor with IC at the same layer, close to BST and SW plane. TI recommends > 10-mil width trace to reduce line parasitic inductance.
- Make feedback 10 mil and routed away from the switching node, BST node, or other high speed digital signal.
- Make VIN trace wide to reduce the trace impedance and provide enough current capability.
- Place multiple vias under the device near VIN and PGND and near input capacitors to reduce parasitic inductance and improve thermal performance.

7.4.2 Layout Example

Figure 7-19 shows the recommended top-side layout. Component reference designators are the same as the circuit shown in [TPS51375 Step-Down Converter Evaluation Module EVM user's guide](#).

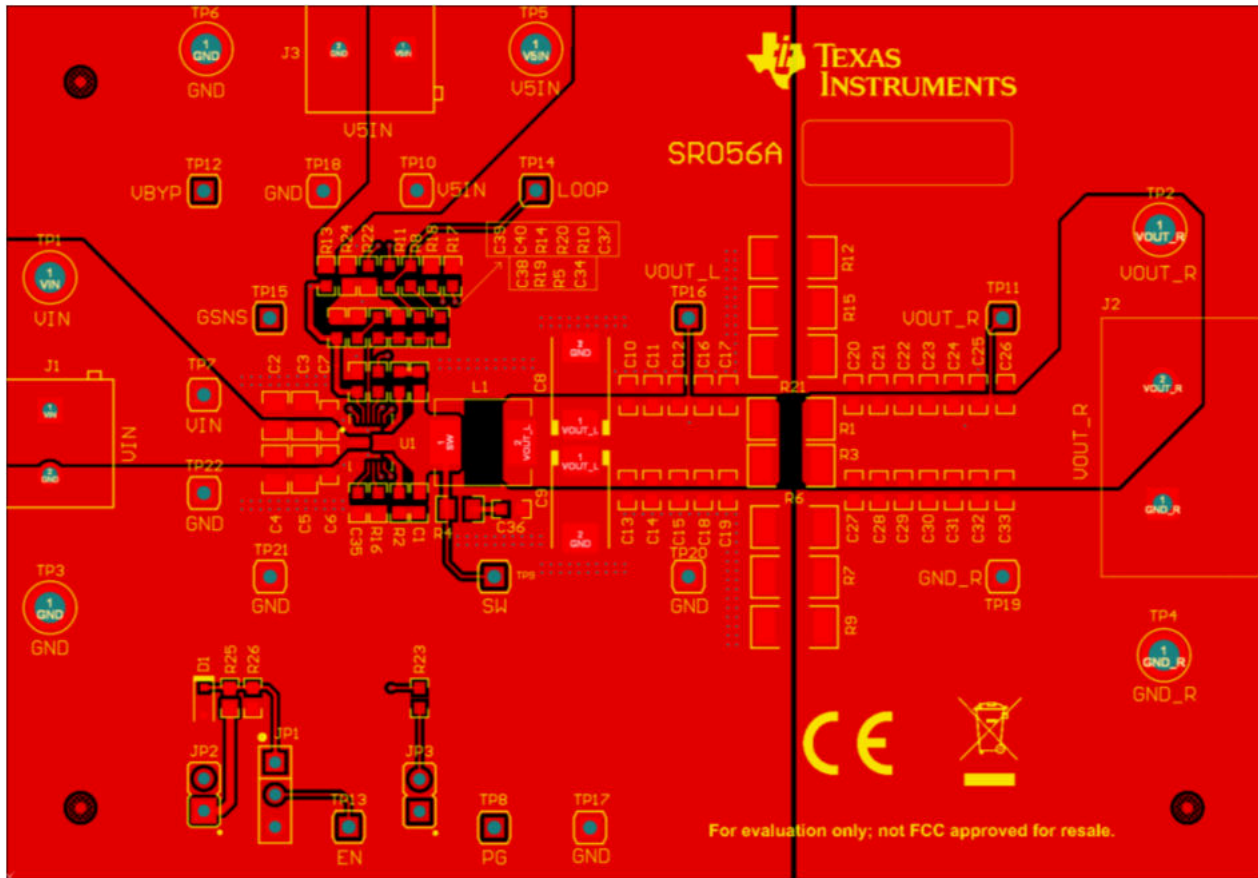


Figure 7-19. Top-Side Layout

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the TPS51375R device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
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- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

Texas Instruments, [TPS51375 Step-Down Converter Evaluation Module EVM user's guide](#)

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

DATE	REVISION	NOTES
April 2026	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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