# 3-V TO 6-V INPUT, 3-A OUTPUT SYNCHRONOUS-BUCK PWM SWITCHER WITH INTEGRATED FETs (SWIFT™)

## FEATURES

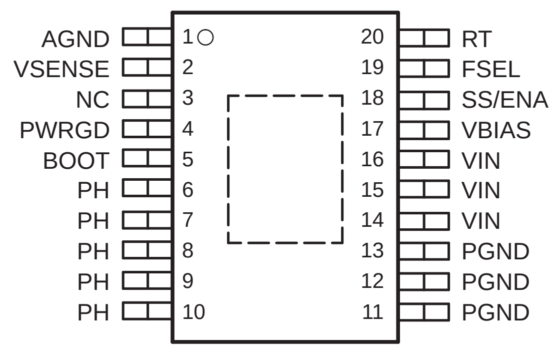
- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree** (1)
- **60-mΩ MOSFET Switches for High Efficiency at 3-A Continuous Output Source or Sink Current**
- **0.9 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V Fixed Output Voltage Device With 1% Initial Accuracy**
- **Internally Compensated for Low Parts Count**
- **Fast Transient Response**
- **Wide PWM Frequency: Fixed 350 kHz, 550 kHz, or Adjustable 280 kHz to 700 kHz**
- **Load Protected by Peak Current Limit and Thermal Shutdown**
- **Integrated Solution Reduces Board Area and Total Cost**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

## APPLICATIONS

- **Low-Voltage, High-Density Systems With Power Distributed at 5 V or 3.3 V**
- **Point of Load Regulation for High Performance DSPs, FPGAs, ASICs, and Microprocessors**
- **Broadband, Networking and Optical Communications Infrastructure**
- **Automotive Telematics**

**PWP PACKAGE**
**(TOP VIEW)**




NC − No internal connection

## DESCRIPTION/ORDERING INFORMATION

As A member of the SWIFT family of dc/dc regulators, the TPS54311, TPS54312, TPS54313, TPS54314, TPS54315 and TPS54316 low-input-voltage high-output current synchronous-buck PWM converter integrates all required active components. Included on the substrate with the listed features are a true, high performance, voltage error amplifier that provides high performance under transient conditions; an undervoltage-lockout circuit to prevent start-up until the input voltage reaches 3 V; an internally and externally set slow-start circuit to limit in-rush currents; and a power good output useful for processor/logic reset, fault signaling, and supply sequencing.

The TPS54311, TPS54312, TPS54313, TPS54314, TPS54315 and TPS54316 devices are available in a thermally enhanced 20-pin TSSOP (PWP) PowerPAD™ package, which eliminates bulky heatsinks. Texas Instruments provides evaluation modules and the SWIFT designer software tool to aid in quickly achieving high-performance power supply designs to meet aggressive equipment development cycles.

## ORDERING INFORMATION(1)

| $T_J$ | OUTPUT VOLTAGE | PACKAGED DEVICES PLASTIC HTSSOP (PWP)(2) | TOP SIDE MARKING |
|---|---|---|---|
| –55°C to 125°C | 0.9 V | TPS54311MPWPREP | TPS54311 |
| | 1.2 V | TPS54312MPWPREP | TPS54312 |
| | 1.5 V | TPS54313MPWPREP | TPS54313 |
| | 1.8 V | TPS54314MPWPREP | TPS54314 |
| | 2.5 V | TPS54315MPWPREP | TPS54315 |
| | 3.3 V | TPS54316MPWPREP | TPS54316 |

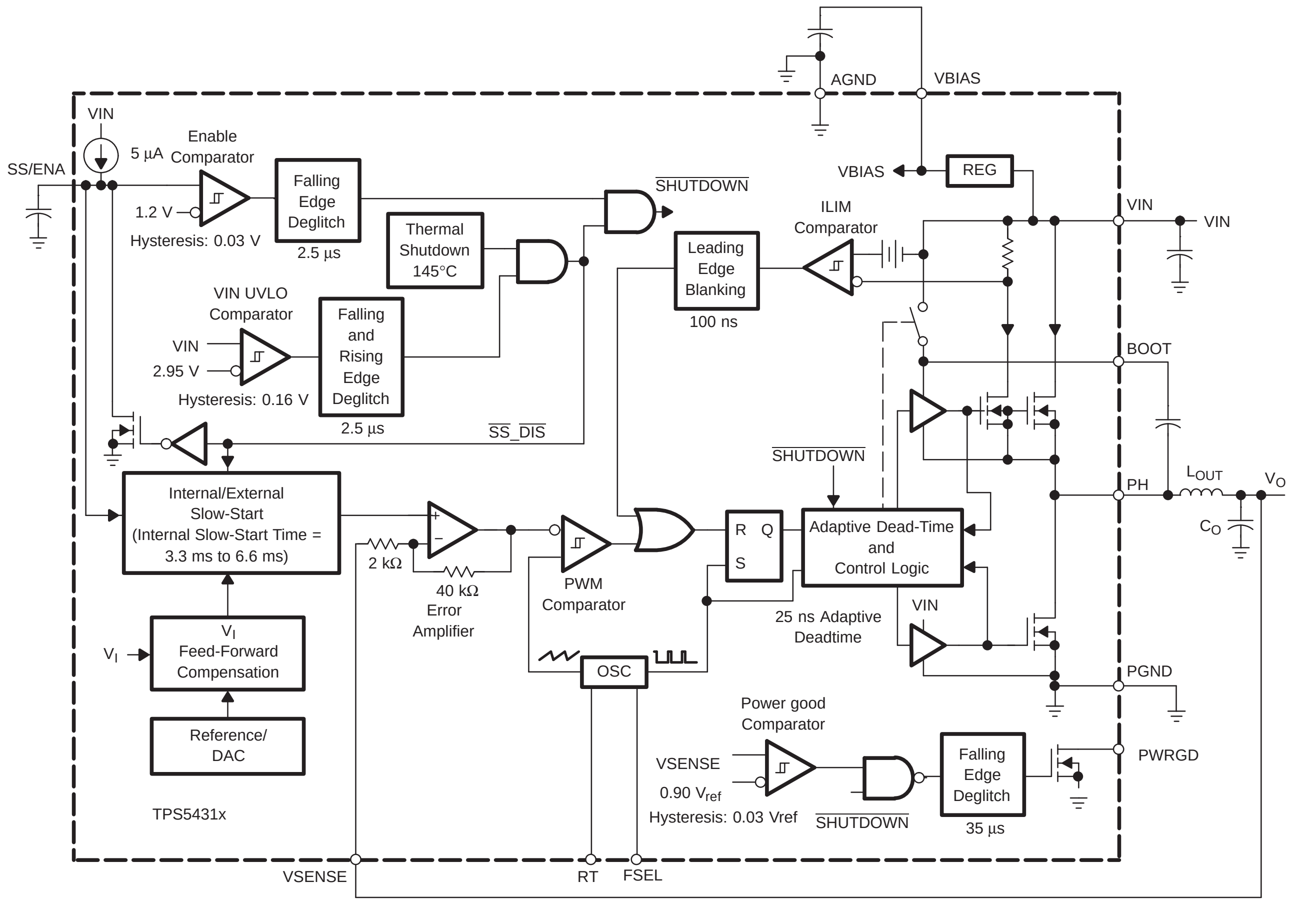
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) The PWP package is taped and reeled as indicated by the R suffix. See application section of data sheet for PowerPAD drawing and layout information

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

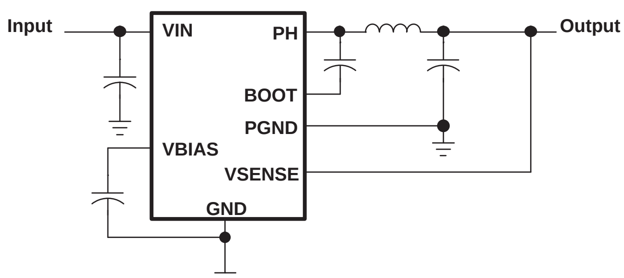
## TERMINAL FUNCTIONS

| TERMINAL NAME | TERMINAL NO. | DESCRIPTION |
|---|---|---|
| AGND | 1 | Analog ground. Return for compensation network/output divider, slow-start capacitor, VBIAS capacitor, RT resistor and FSEL pin. Make PowerPAD connection to AGND. |
| BOOT | 5 | Bootstrap input. 0.022-µF to 0.1-µF low-ESR capacitor connected from BOOT to PH generates floating drive for the high-side FET driver. |
| FSEL | 19 | Frequency select input. Provides logic input to select between two internally set switching frequencies. |
| NC | 3 | No connection |
| PGND | 11–13 | Power ground. High current return for the low-side driver and power MOSFET. Connect PGND with large copper areas to the input and output supply returns, and negative terminals of the input and output capacitors. |
| PH | 6–10 | Phase input/output. Junction of the internal high and low-side power MOSFETs, and output inductor. |
| PWRGD | 4 | Power good open drain output. Hi-Z when VSENSE ≥ 90% $V_{ref}$, otherwise PWRGD is low. Note that output is low when SS/ENA is low or internal shutdown signal active. |
| RT | 20 | Frequency setting resistor input. Connect a resistor from RT to AGND to set the switching frequency, $f_s$. |
| SS/ENA | 18 | Slow-start/enable input/output. Dual function pin which provides logic input to enable/disable device operation and capacitor input to externally set the start-up time. |
| VBIAS | 17 | Internal bias regulator output. Supplies regulated voltage to internal circuitry. Bypass VBIAS pin to AGND pin with a high quality, low ESR 0.1-µF to 1-µF ceramic capacitor. |
| VIN | 14–16 | Input supply for the power MOSFET switches and internal bias regulator. Bypass VIN pins to PGND pins close to device package with a high quality, low ESR 1-µF to 10-µF ceramic capacitor. |
| VSENSE | 2 | Error amplifier inverting input. Connect directly to output voltage sense point. |

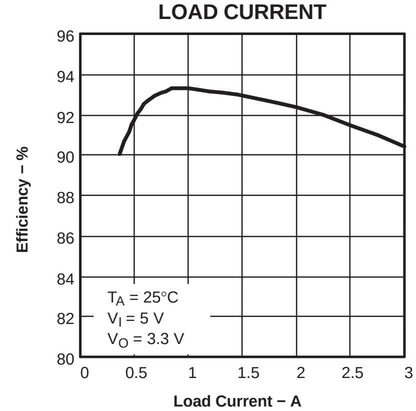
## FUNCTIONAL BLOCK DIAGRAM




### Simplified Schematic




### EFFICIENCY vs LOAD CURRENT



## Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_I$ | Input voltage range | VIN, SS/ENA, FSEL | –0.3 | 7 | V |
| | | RT | –0.3 | 6 | |
| | | VSENSE | –0.3 | 4 | |
| | | BOOT | –0.3 | 17 | |
| $V_O$ | Output voltage range | VBIAS, PWRGD, COMP | –0.3 | 7 | V |
| | | PH | –0.6 | 10 | |
| $I_O$ | Source current | PH | Internally Limited | | |
| | | COMP, VBIAS | | 6 | mA |
| | Sink current | PH | | 6 | A |
| | | COMP | | 6 | mA |
| | | SS/ENA,PWRGD | | 10 | mA |
| | Voltage differential | AGND to PGND | | ±0.3 | V |
| $T_J$ | Operating virtual junction temperature range | | –55 | 150 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |
| | Lead temperature 1,6 mm (1/16 in) from case for 10 s | | | 300 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_I$ | Input voltage range | 3 | | 6 | V |
| $T_J$ | Operating junction temperature | –55 | | 125 | °C |

## Package Dissipation Ratings(1)(2)

| PACKAGE | THERMAL IMPEDANCE JUNCTION-TO-AMBIENT | $T_A$ = 25°C POWER RATING | $T_A$ = 70°C POWER RATING | $T_A$ = 85°C POWER RATING |
|---|---|---|---|---|
| 20-Pin PWP with solder | 26°C/W | 3.85 W(3) | 2.12 W | 1.54 W |
| 20-Pin PWP without solder | 57.5°C/W | 1.73 W | 0.96 W | 0.69 W |

(1) For more information on the PWP package, see the Texas Instruments technical brief (SLMA002).
(2) Test board conditions:
  a. 3 in × 3 in, 2 layers, Thickness: 0.062 in
  b. 1.5 oz copper traces located on the top of the PCB
  c. 1.5 oz copper ground plane on the bottom of PCB
  d. Ten thermal vias (see the recommended land pattern in the Applications section of this data sheet)
(3) Maximum power dissipation may be limited by overcurrent protection.

## Electrical Characteristics

$T_J$ = –55°C to 125°C, VIN = 3 V to 6 V (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **SUPPLY VOLTAGE, VIN** | | | | | |
| $V_{IN}$ Input voltage range | | 3 | | 6 | V |
| Quiescent current | $f_s$ = 350 kHz, FSEL ≤ 0.8 V, RT open | | 6.2 | 9.6 | mA |
| | $f_s$ = 550 kHz, FSEL ≥ 2.5 V, Phase pin open, | | 8.4 | 12.8 | |
| | Shutdown, SS/ENA = 0 V | | 1 | 1.4 | |
| **UNDER VOLTAGE LOCK OUT** | | | | | |
| Start threshold voltage, UVLO | | | 2.95 | 3 | V |
| Stop threshold voltage, UVLO | | 2.7 | 2.8 | | |
| Hysteresis voltage, UVLO | | | 0.14 | | V |
| Rising and falling edge deglitch, UVLO(1) | | | 2.5 | | µs |
| **BIAS VOLTAGE** | | | | | |
| Output voltage, VBIAS | $I_{(VBIAS)}$ = 0 | 2.7 | 2.8 | 2.95 | V |
| Output current, VBIAS(2) | | | | 100 | µA |
| **OUTPUT VOLTAGE** | | | | | |
| $V_O$ Output Voltage, TPS54311 | $T_J$ = 25°C, $V_{IN}$ = 5.0 V | | 0.9 | | V |
| | 3 ≤ $V_{IN}$ ≤ 6V, 0 ≤ $I_L$ ≤ 3A, –55°C ≤ $T_J$ ≤ 125°C | –3.0% | | 3.0% | |
| TPS54312 | $T_J$ = 25°C, $V_{IN}$ = 5.0 V | | 1.2 | | V |
| | 3 ≤ $V_{IN}$ ≤ 6V, 0 ≤ $I_L$ ≤ 3A, –55°C ≤ $T_J$ ≤ 125°C | –3.0% | | 3.0% | |
| TPS54313 | $T_J$ = 25°C, $V_{IN}$ = 5.0 V | | 1.5 | | V |
| | 3 ≤ $V_{IN}$ ≤ 6V, 0 ≤ $I_L$ ≤ 3A, –55°C ≤ $T_J$ ≤ 125°C | –3.0% | | 3.0% | |
| TPS54314 | $T_J$ = 25°C, $V_{IN}$ = 5.0 V | | 1.8 | | V |
| | 3 ≤ $V_{IN}$ ≤ 6V, 0 ≤ $I_L$ ≤ 3A, –55°C ≤ $T_J$ ≤ 125°C | –3.0% | | 3.0% | |
| TPS54315 | $T_J$ = 25°C, $V_{IN}$ = 5.0 V | | 2.5 | | V |
| | 3 ≤ $V_{IN}$ ≤ 6V, 0 ≤ $I_L$ ≤ 3A, –55°C ≤ $T_J$ ≤ 125°C | –3.0% | | 3.0% | |
| TPS54316 | $T_J$ = 25°C, $V_{IN}$ = 5.0 V | | 3.3 | | V |
| | 3 ≤ $V_{IN}$ ≤ 6V, 0 ≤ $I_L$ ≤ 3A, –55°C ≤ $T_J$ ≤ 125°C | –3.0% | | 3.0% | |
| **REGULATION** | | | | | |
| Line regulation(1)(3) | $I_L$ = 1.5 A, 350 ≤ $f_s$ ≤ 550 kHz, | | 0.21 | | %/V |
| Load regulation(1)(3) | $I_L$ = 0 A to 3 A, 350 ≤ $f_s$ ≤ 550 kHz, | | 0.21 | | %/A |
| **OSCILLATOR** | | | | | |
| Internally set free-running frequency range | FSEL ≤ 0.8 V, RT open | 255 | 350 | 450 | kHz |
| | FSEL ≥ 2.5 V, RT open | 400 | 550 | 700 | |
| Externally set free-running frequency range | RT = 180 kΩ (1% resistor to AGND)(1) | 252 | 280 | 308 | kHz |
| | RT = 160 kΩ (1% resistor to AGND) | 290 | 312 | 350 | |
| | RT = 68 kΩ (1% resistor to AGND)(1) | 663 | 700 | 762 | |
| High-level threshold voltage at FSEL | | 2.5 | | | V |
| Low-level threshold voltage at FSEL | | | | 0.8 | V |
| Pulse duration, FSEL(1) | | 50 | | | ns |
| Frequency range, FSEL(1)(4) | | 330 | | 700 | kHz |
| Ramp valley(1) | | | 0.75 | | V |

(1) Specified by design
(2) Static resistive loads only
(3) Specified by the circuit used in Figure 10.
(4) To ensure proper operation when RC filter is used between external clock and FSEL pin, the recommended values are R ≤ 1 kΩ and C ≤ 68 pF.

## Electrical Characteristics (continued)

$T_J$ = –55°C to 125°C, VIN = 3 V to 6 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Ramp amplitude (peak-to-peak)(1) | | | 1 | | V |
| | Minimum controllable on time(1) | | | | 200 | ns |
| | Maximum duty cycle(1) | | 90% | | | |
| **ERROR AMPLIFIER** | | | | | | |
| | Error amplifier open loop voltage gain(1) | | | 26 | | dB |
| | Error amplifier unity gain bandwidth(1) | | 3 | 5 | | MHz |
| **PWM COMPARATOR** | | | | | | |
| | PWM comparator propagation delay time, PWM comparator input to PH pin (excluding dead time) | 10-mV overdrive(1) | | 70 | 85 | ns |
| **SLOW-START/ENABLE** | | | | | | |
| | Enable threshold voltage, SS/ENA | | 0.82 | 1.2 | 1.4 | V |
| | Enable hysteresis voltage, SS/ENA(5) | | | 0.03 | | V |
| | Falling edge deglitch, SS/ENA(5) | | | 2.5 | | µs |
| | Internal slow-start time(5) | | 3.5 | 4.5 | 5.4 | ms |
| | Charge current, SS/ENA | SS/ENA = 0 V | 2.5 | 5 | 8 | µA |
| | Discharge current, SS/ENA | SS/ENA = 0.2 V, $V_I$ = 2.7 V | 1.2 | 2.3 | 4 | mA |
| **POWER GOOD** | | | | | | |
| | Power good threshold voltage | VSENSE falling | | 90 | | $\%V_{ref}$ |
| | Power good hysteresis voltage(5) | | | 3 | | $\%V_{ref}$ |
| | Power good falling edge deglitch(5) | | | 35 | | µs |
| | Output saturation voltage, PWRGD | $I_{(sink)}$ = 2.5 mA | | 0.18 | 0.3 | V |
| | Leakage current, PWRGD | $V_I$ = 6.0 V | | | 1 | µA |
| **CURRENT LIMIT** | | | | | | |
| | Current limit trip point | $V_I$ = 3 V, output shorted | 4 | 6.5 | | A |
| | Current limit leading edge blanking time(5) | | | 100 | | ns |
| | Current limit total response time(5) | | | 200 | | ns |
| **THERMAL SHUTDOWN** | | | | | | |
| | Thermal shutdown trip point(5) | | 135 | 150 | 165 | °C |
| | Thermal shutdown hysteresis(5) | | | 10 | | °C |
| **OUTPUT POWER MOSFETS** | | | | | | |
| $r_{DS(on)}$ | Power MOSFET switches | $V_I$ = 6 V(6) | | 59 | 88 | mΩ |
| | | $V_I$ = 3 V(6) | | 85 | 136 | mΩ |

(5) Specified by design
(6) Matched MOSFETs, low side $r_{DS(on)}$ production tested, high side $r_{DS(on)}$ specified by design.

# TYPICAL CHARACTERISTICS

**DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE**

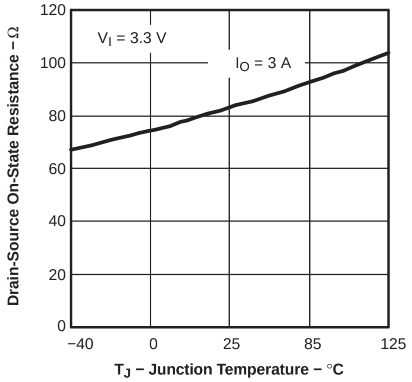



Figure 1.

**DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE**

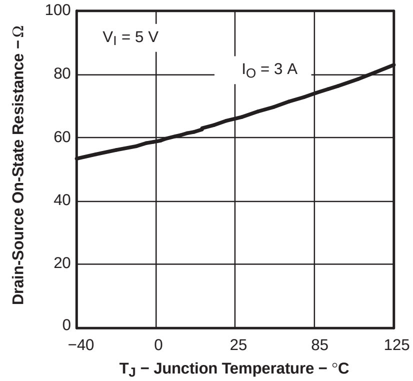



Figure 2.

**INTERNALLY SET OSCILLATOR FREQUENCY vs JUNCTION TEMPERATURE**

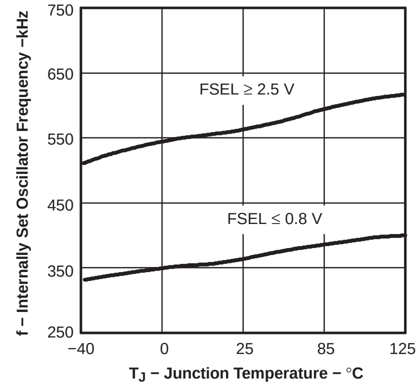



Figure 3.

**EXTERNALLY SET OSCILLATOR FREQUENCY vs JUNCTION TEMPERATURE**

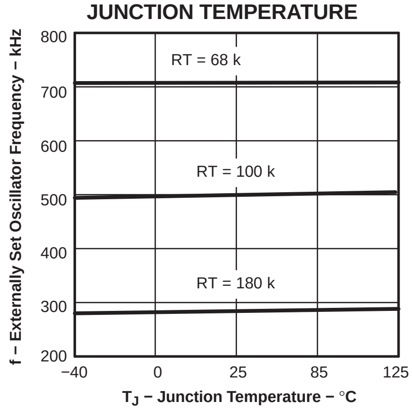



Figure 4.

**VOLTAGE REFERENCE vs JUNCTION TEMPERATURE**

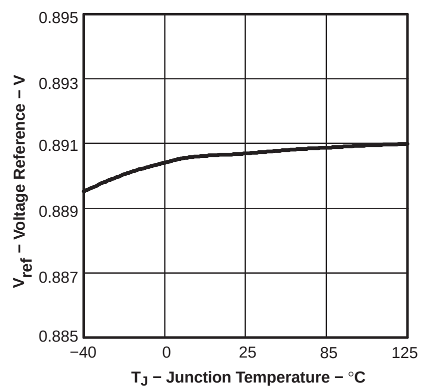



Figure 5.

**OUTPUT VOLTAGE REGULATION vs INPUT VOLTAGE**

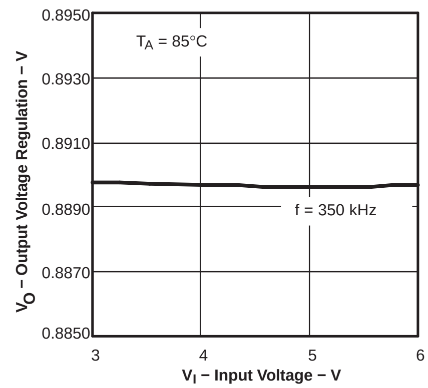



Figure 6.

**ERROR AMPLIFIER OPEN LOOP RESPONSE**

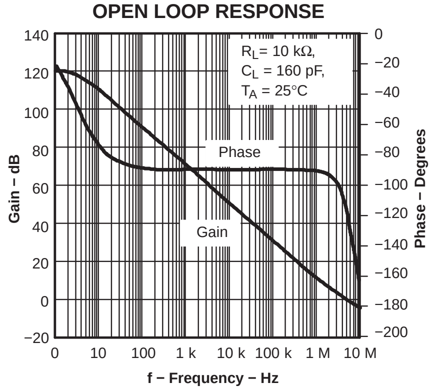



Figure 7.

**INTERNAL SLOW-START TIME vs JUNCTION TEMPERATURE**

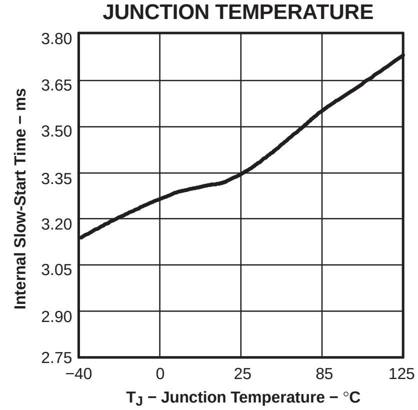



Figure 8.

**DEVICE POWER LOSSES vs LOAD CURRENT**

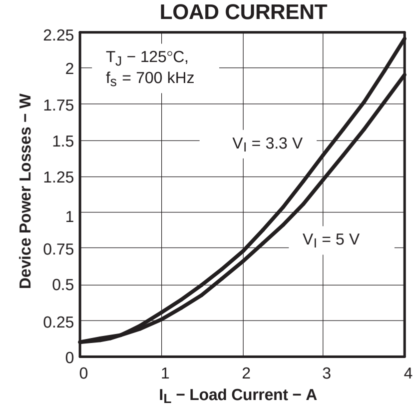



Figure 9.

## APPLICATION INFORMATION

Figure 10 shows the schematic diagram for a typical TPS54314 application. The TPS54314 (U1) can provide up to 3 A of output current at a nominal output voltage of 1.8 V. For proper thermal performance, the PowerPAD underneath the TPS54314 integrated circuit needs to be soldered to the printed circuit board.

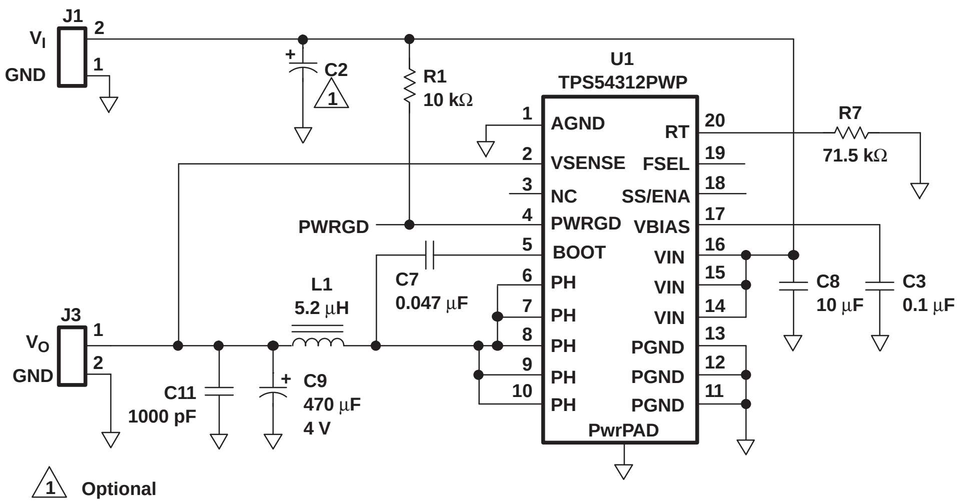



**Figure 10. TPS54314 Schematic**

## INPUT VOLTAGE

The input to the circuit is a nominal 5 VDC, applied at J1. The optional input filter (C2) is a 220-µF POSCAP capacitor, with a maximum allowable ripple current of 3 A. C8 is the decoupling capacitor for the TPS54314 and must be located as close to the device as possible.

## FEEDBACK CIRCUIT

The output voltage of the converter is fed directly into the VSENSE pin of the TPS54314. The TPS54314 is internally compensated to provide stability of the output under varying line and load conditions.

## OPERATING FREQUENCY

In the application circuit, a 700 kHz operating frequency is selected by leaving FSEL open and connecting a 71.5 kΩ resistor between the RT pin and AGND. Different operating frequencies may be selected by varying the value of R3 using equation 1:

$$R = \frac{500\ \text{kHz}}{\text{Switching Frequency}} \times 100\ \text{k}\Omega \qquad (1)$$

Alternately, preset operating frequencies of 350 kHz or 550 kHz my be selected by leaving RT open and connecting the FSEL pin to AGND or VIN, respectively.

## OUTPUT FILTER

The output filter is composed of a 5.2-µH inductor and 470-µF capacitor. The inductor is a low dc resistance (16-mΩ) type, Sumida CDRH104R-5R2. The capacitor used is a 4-V POSCAP with a maximum ESR of 40 mΩ. The output filter components work with the internal compensation network to provide a stable closed loop response for the converter.

## APPLICATION INFORMATION (continued)

### GROUNDING AND PowerPAD LAYOUT

The TPS54311-16 has two internal grounds (analog and power). Inside the TPS54311-16, the analog ground ties to all of the noise sensitive signals, while the power ground ties to the noisier power signals. The PowerPAD must be connected directly to AGND. Noise injected between the two grounds can degrade the performance of the TPS54311-16, particularly at higher output currents. However, ground noise on an analog ground plane can also cause problems with some of the control and bias signals. For these reasons, separate analog and power ground planes are recommended. These two planes should tie together directly at the IC to reduce noise between the two grounds. The only components that should tie directly to the power ground plane are the input capacitor, the output capacitor, the input voltage decoupling capacitor, and the PGND pins of the TPS54311-16. The layout of the TPS54311-16 evaluation module is representative of a recommended layout for a 4-layer board. Documentation for the TPS54311-16 evaluation module can be found on the Texas Instruments web site under the TPS54311-16 product folder and in the application note, Texas Instruments literature number SLVA111.

### LAYOUT CONSIDERATIONS FOR THERMAL PERFORMANCE

For operation at full rated load current, the analog ground plane must provide adequate heat dissipating area. A 3 inch by 3 inch plane of 1 ounce copper is recommended, though not mandatory, depending on ambient temperature and airflow. Most applications have larger areas of internal ground plane available, and the PowerPAD should be connected to the largest area available. Additional areas on the top or bottom layers also help dissipate heat, and any area available should be used when 3 A or greater operation is desired. Connection from the exposed area of the PowerPAD to the analog ground plane layer should be made using 0.013 inch diameter vias to avoid solder wicking through the vias. Six vias should be in the PowerPAD area with four additional vias located under the device package. The size of the vias under the package, but not in the exposed thermal pad area, can be increased to 0.018. Additional vias beyond the ten recommended that enhance thermal performance should be included in areas not under the device package.

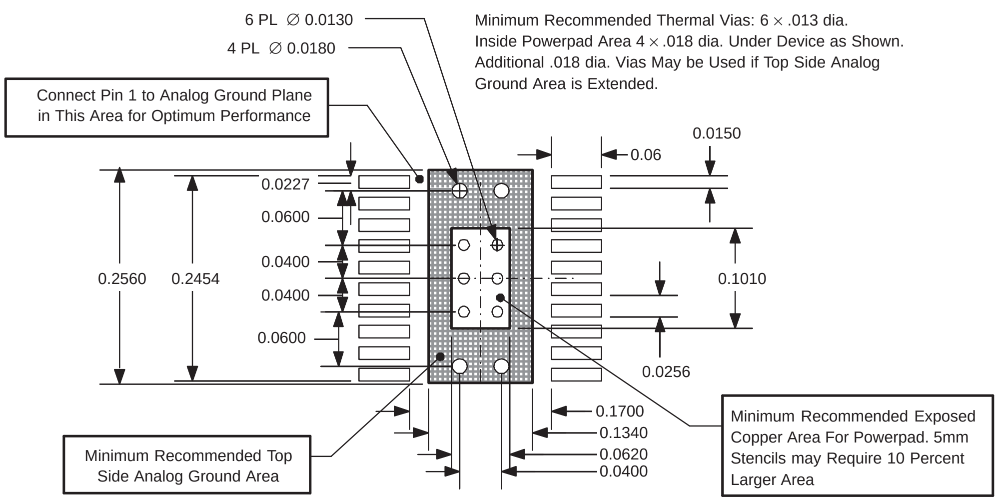



**Figure 11. Recommended Land Pattern for 20-Pin PWP PowerPAD**

## PERFORMANCE GRAPHS

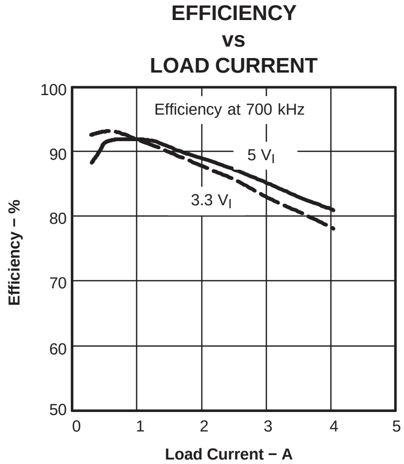



Figure 12.

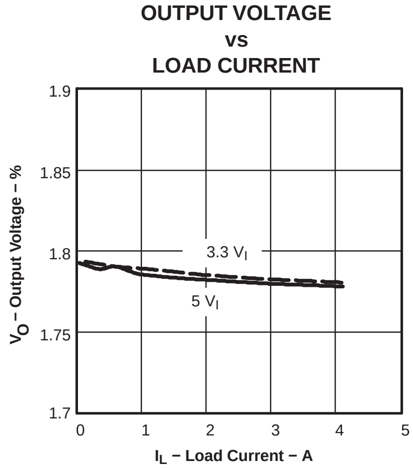



Figure 13.

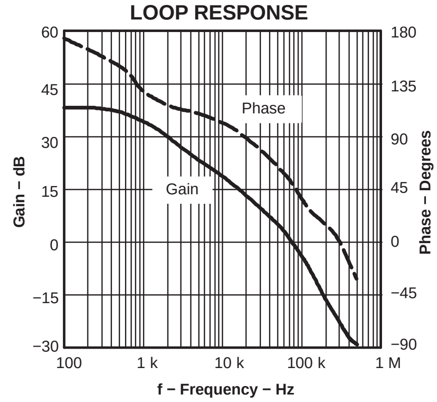



Figure 14.

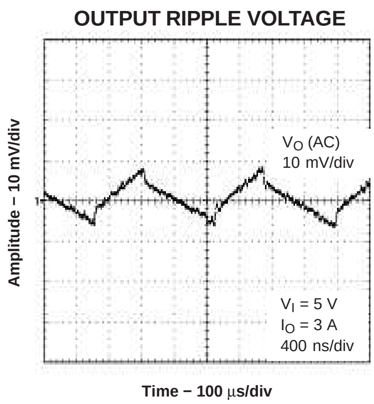



Figure 15.

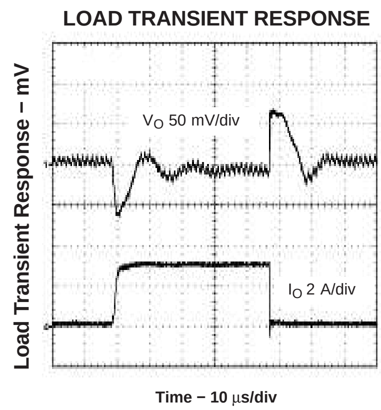



Figure 16.

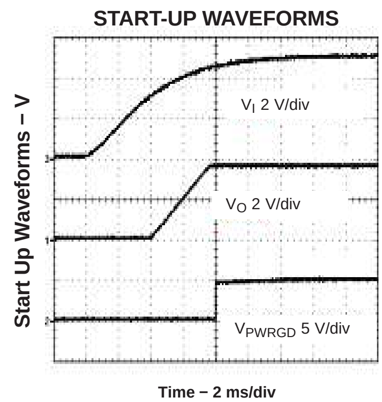
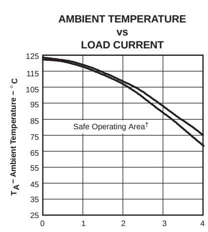



Figure 17.




† Safe operating area is applicable to the test board conditions listed in the *Dissipation Rating Table* section of this data sheet.

Figure 18.

## DETAILED DESCRIPTION

### Under Voltage Lock Out (UVLO)

The TPS54311-16 incorporates an under voltage lockout circuit to keep the device disabled when the input voltage (VIN) is insufficient. During power up, internal circuits are held inactive until VIN exceeds the nominal UVLO threshold voltage of 2.95 V. Once the UVLO start threshold is reached, device start-up begins. The device operates until VIN falls below the nominal UVLO stop threshold of 2.8 V. Hysteresis in the UVLO comparator, and a 2.5-µs rising and falling edge deglitch circuit reduce the likelihood of shutting the device down due to noise on VIN.

## PERFORMANCE GRAPHS (continued)

### Slow-Start/Enable (SS/ENA)

The slow-start/enable pin provides two functions; first, the pin acts as an enable (shutdown) control by keeping the device turned off until the voltage exceeds the start threshold voltage of approximately 1.2 V. When SS/ENA exceeds the enable threshold, device start up begins. The reference voltage fed to the error amplifier is linearly ramped up from 0 V to 0.891 V in 3.35 ms. Similarly, the converter output voltage reaches regulation in approximately 3.35 ms. Voltage hysteresis and a 2.5-µs falling edge deglitch circuit reduce the likelihood of triggering the enable due to noise.

| DEVICE | OUTPUT VOLTAGE | SLOW START |
|---|---|---|
| TPS54311 | 0.9 V | 3.3 ms |
| TPS54312 | 1.2 V | 4.5 ms |
| TPS54313 | 1.5 V | 5.6 ms |
| TPS54314 | 1.8 V | 3.3 ms |
| TPS54315 | 2.5 V | 4.7 ms |
| TPS54316 | 3.3 V | 6.1 ms |

The second function of the SS/ENA pin provides an external means of extending the slow-start time with a low-value capacitor connected between SS/ENA and AGND. Adding a capacitor to the SS/ENA pin has two effects on start-up. First, a delay occurs between release of the SS/ENA pin and start up of the output. The delay is proportional to the slow-start capacitor value and lasts until the SS/ENA pin reaches the enable threshold. The start-up delay is approximately:

$$t_d = C_{(SS)} \times \frac{1.2\ \text{V}}{5\ \mu\text{A}} \tag{2}$$

Second, as the output becomes active, a brief ramp-up at the internal slow-start rate may be observed before the externally set slow-start rate takes control and the output rises at a rate proportional to the slow-start capacitor. The slow-start time set by the capacitor is approximately:

$$t_{(SS)} = C_{(SS)} \times \frac{0.7\ \text{V}}{5\ \mu\text{A}} \tag{3}$$

The actual slow-start is likely to be less than the above approximation due to the brief ramp-up at the internal rate.

### VBIAS Regulator (VBIAS)

The VBIAS regulator provides internal analog and digital blocks with a stable supply voltage over variations in junction temperature and input voltage. A high quality, low-ESR, ceramic bypass capacitor is required on the VBIAS pin. X7R or X5R grade dielectrics are recommended because their values are more stable over temperature. The bypass capacitor should be placed close to the VBIAS pin and returned to AGND. External loading on VBIAS is allowed, with the caution that internal circuits require a minimum VBIAS of 2.7 V and external loads on VBIAS with ac or digital switching noise may degrade performance. The VBIAS pin may be useful as a reference voltage for external circuits.

### Voltage Reference

The voltage reference system produces a precise $V_{ref}$ signal by scaling the output of a temperature stable bandgap circuit. During manufacture, the bandgap and scaling circuits are trimmed to produce 0.891 V at the output of the error amplifier, with the amplifier connected as a voltage follower. The trim procedure adds to the high precision regulation of the TPS54311-16, since it cancels offset errors in the scale and error amplifier circuits.

### Oscillator and PWM Ramp

The oscillator frequency can be set to internally fixed values of 350 kHz or 550 kHz using the FSEL pin as a static digital input. If a different frequency of operation is required for the application, the oscillator frequency can be externally adjusted from 280 kHz to 700 kHz by connecting a resistor to the RT pin to ground and floating the FSEL pin. The switching frequency is approximated by the following equation, where R is the resistance from RT to AGND:

$$\text{SWITCHING FREQUENCY} = \frac{100\ \text{k}\Omega}{\text{R}} \times 500\ \text{kHz} \tag{4}$$

External synchronization of the PWM ramp is possible over the frequency range of 330 kHz to 700 kHz by driving a synchronization signal into FSEL and connecting a resistor from RT to AGND. Choose an RT resistor that sets the free-running frequency to 80% of the synchronization signal. Table 1 summarizes the frequency selection configurations.

**Table 1. Summary of the Frequency Selection Configurations**

| SWITCHING FREQUENCY | FSEL PIN | RT PIN |
|---|---|---|
| 350 kHz, internally set | Float or AGND | Float |
| 550 kHz, internally set | ≥2.5 V | Float |
| Externally set 280 kHz to 700 kHz | Float | R = 68 k to 180 k |
| Externally synchronized frequency(1) | Synchronization signal | R = RT value for 80% of external synchronization frequency |

(1) To ensure proper operation when RC filter is used between external clock and FSEL pin, the recommended values are R ≤ 1 kΩ and C ≤ 68 pF.

### Error Amplifier

The high performance, wide bandwidth, voltage error amplifier is gain limited to provide internal compensation of the control loop. The user is given limited flexibility in choosing output L and C filter components. Inductance values of 4.7 µH to 10 µH are typical and available from several vendors. The resulting designs exhibit good noise and ripple characteristics, along with exceptional transient response. Transient recovery times are typically in the range of 10 µs to 20 µs.

### PWM Control

Signals from the error amplifier output, oscillator, and current limit circuit are processed by the PWM control logic. Referring to the internal block diagram, the control logic includes the PWM comparator, OR gate, PWM latch, and portions of the adaptive dead-time and control logic block. During steady-state operation below the current limit threshold, the PWM comparator output and oscillator pulse train alternately reset and set the PWM latch. Once the PWM latch is set, the low-side FET remains on for a minimum duration set by the oscillator pulse duration. During this period, the PWM ramp discharges rapidly to its valley voltage. When the ramp begins to charge back up, the low-side FET turns off and high-side FET turns on. As the PWM ramp voltage exceeds the error amplifier output voltage, the PWM comparator resets the latch, thus turning off the high-side FET and turning on the low-side FET. The low-side FET remains on until the next oscillator pulse discharges the PWM ramp.

During transient conditions, the error amplifier output could be below the PWM ramp valley voltage or above the PWM peak voltage. If the error amplifier is high, the PWM latch is never reset and the high-side FET remains on until the oscillator pulse signals the control logic to turn the high-side FET off and the low-side FET on. The device operates at its maximum duty cycle until the output voltage rises to the regulation set-point, setting VSENSE to approximately the same voltage as $V_{ref}$. If the error amplifier output is low, the PWM latch is continually reset and the high-side FET does not turn on. The low-side FET remains on until the VSENSE voltage decreases to a range that allows the PWM comparator to change states. The TPS54311-16 is capable of sinking current continuously until the output reaches the regulation set-point.

If the current limit comparator trips for longer than 100 ns, the PWM latch resets before the PWM ramp exceeds the error amplifier output. The high-side FET turns off and low-side FET turns on to decrease the energy in the output inductor and consequently the output current. This process is repeated each cycle in which the current limit comparator is tripped.

### Dead-Time Control and MOSFET Drivers

Adaptive dead-time control prevents shoot-through current from flowing in both N-channel power MOSFETs during the switching transitions by actively controlling the turn-on times of the MOSFET drivers. The high-side driver does not turn on until the gate drive voltage to the low-side FET is below 2 V. The low-side driver does not turn on until the voltage at the gate of the high-side MOSFETs is below 2 V. The high-side and low-side drivers are designed with 300-mA source and sink capability to quickly drive the power MOSFETs gates. The low-side driver is supplied from VIN, while the high-side drive is supplied from the BOOT pin. A bootstrap circuit uses an external BOOT capacitor and an internal 2.5-Ω bootstrap switch connected between the VIN and BOOT pins. The integrated bootstrap switch improves drive efficiency and reduces external component count.

### Overcurrent Protection

The cycle by cycle current limiting is achieved by sensing the current flowing through the high-side MOSFET and differential amplifier and comparing it to the preset overcurrent threshold. The high-side MOSFET is turned off within 200 ns of reaching the current limit threshold. A 100-ns leading edge blanking circuit prevents false tripping of the current limit. Current limit detection occurs only when current flows from VIN to PH when sourcing current to the output filter. Load protection during current sink operation is provided by thermal shutdown.

### Thermal Shutdown

The device uses the thermal shutdown to turn off the power MOSFETs and disable the controller if the junction temperature exceeds 150°C. The device is released from shutdown when the junction temperature decreases to 10°C below the thermal shutdown trip point and starts up under control of the slow-start circuit. Thermal shutdown provides protection when an overload condition is sustained for several milliseconds. With a persistent fault condition, the device cycles continuously; starting up by control of the soft-start circuit, heating up due to the fault, and then shutting down upon reaching the thermal shutdown point.

### Power Good (PWRGD)

The power good circuit monitors for under voltage conditions on VSENSE. If the voltage on VSENSE is 10% below the reference voltage, the open-drain PWRGD output is pulled low. PWRGD is also pulled low if VIN is less than the UVLO threshold, or SS/ENA is low, or thermal shutdown is asserted. When VIN = UVLO threshold, SS/ENA = enable threshold, and VSENSE > 90% of $V_{ref}$, the open drain output of the PWRGD pin is high. A hysteresis voltage equal to 3% of $V_{ref}$ and a 35-µs falling edge deglitch circuit prevent tripping of the power good comparator due to high frequency noise.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS54311MPWPREP | Active | Production | HTSSOP (PWP) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | TPS54311 |
| TPS54311MPWPREP.A | Active | Production | HTSSOP (PWP) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | TPS54311 |
| TPS54312MPWPREP | Active | Production | HTSSOP (PWP) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | TPS54312 |
| TPS54312MPWPREP.A | Active | Production | HTSSOP (PWP) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | TPS54312 |
| TPS54313MPWPREP | Active | Production | HTSSOP (PWP) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | TPS54313 |
| TPS54313MPWPREP.A | Active | Production | HTSSOP (PWP) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | TPS54313 |
| TPS54314MPWPREP | Active | Production | HTSSOP (PWP) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | TPS54314 |
| TPS54314MPWPREP.A | Active | Production | HTSSOP (PWP) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | TPS54314 |
| TPS54315MPWPREP | Active | Production | HTSSOP (PWP) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | TPS54315 |
| TPS54315MPWPREP.A | Active | Production | HTSSOP (PWP) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | TPS54315 |
| TPS54316MPWPREP | Active | Production | HTSSOP (PWP) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | TPS54316 |
| TPS54316MPWPREP.A | Active | Production | HTSSOP (PWP) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | TPS54316 |
| V62/06657-01XE | Active | Production | HTSSOP (PWP) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | TPS54311 |
| V62/06657-02XE | Active | Production | HTSSOP (PWP) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | TPS54312 |
| V62/06657-03XE | Active | Production | HTSSOP (PWP) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | TPS54313 |
| V62/06657-04XE | Active | Production | HTSSOP (PWP) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | TPS54314 |
| V62/06657-05XE | Active | Production | HTSSOP (PWP) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | TPS54315 |
| V62/06657-06XE | Active | Production | HTSSOP (PWP) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | TPS54316 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TPS54311-EP, TPS54312-EP, TPS54313-EP, TPS54314-EP, TPS54315-EP, TPS54316-EP :**

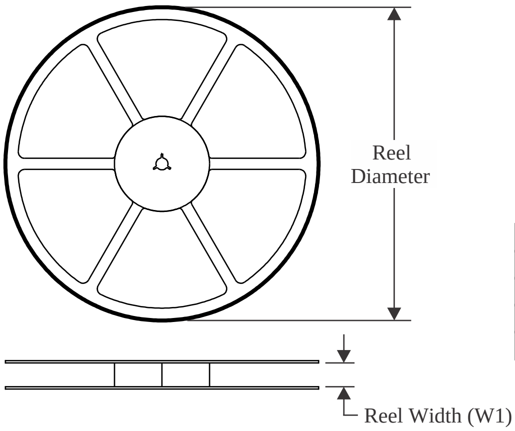
- Catalog : TPS54311, TPS54312, TPS54313, TPS54314, TPS54315, TPS54316

NOTE: Qualified Version Definitions:

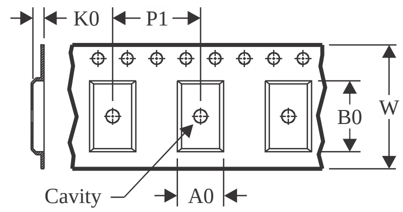
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

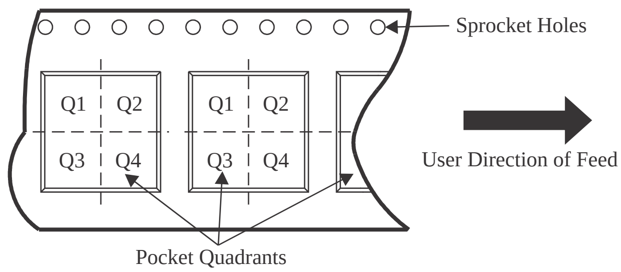



### TAPE DIMENSIONS




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

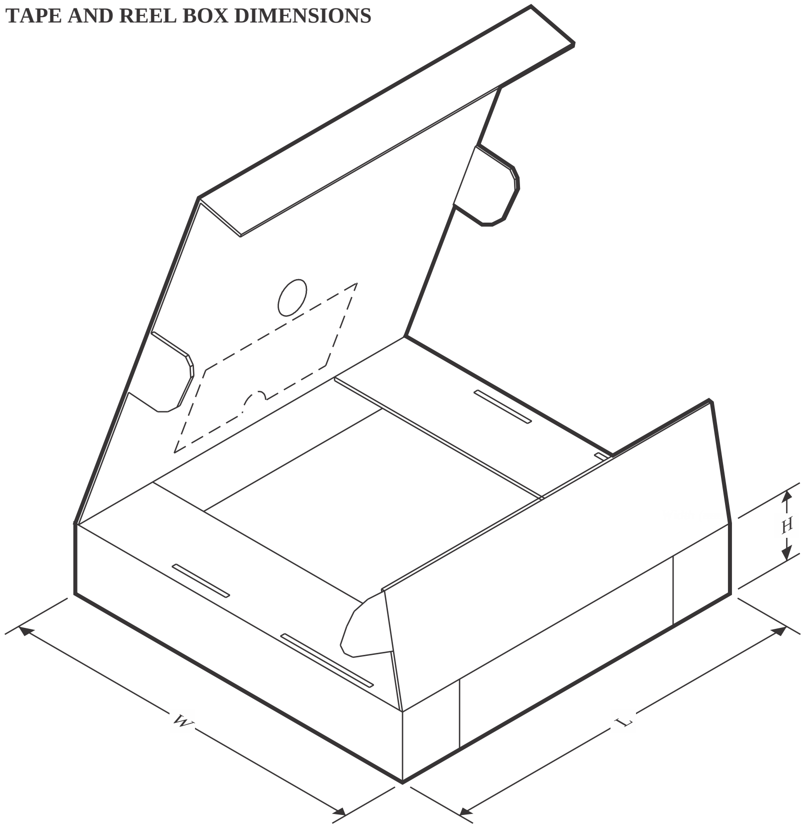
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS54311MPWPREP | HTSSOP | PWP | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| TPS54312MPWPREP | HTSSOP | PWP | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| TPS54313MPWPREP | HTSSOP | PWP | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| TPS54314MPWPREP | HTSSOP | PWP | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| TPS54315MPWPREP | HTSSOP | PWP | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| TPS54316MPWPREP | HTSSOP | PWP | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |

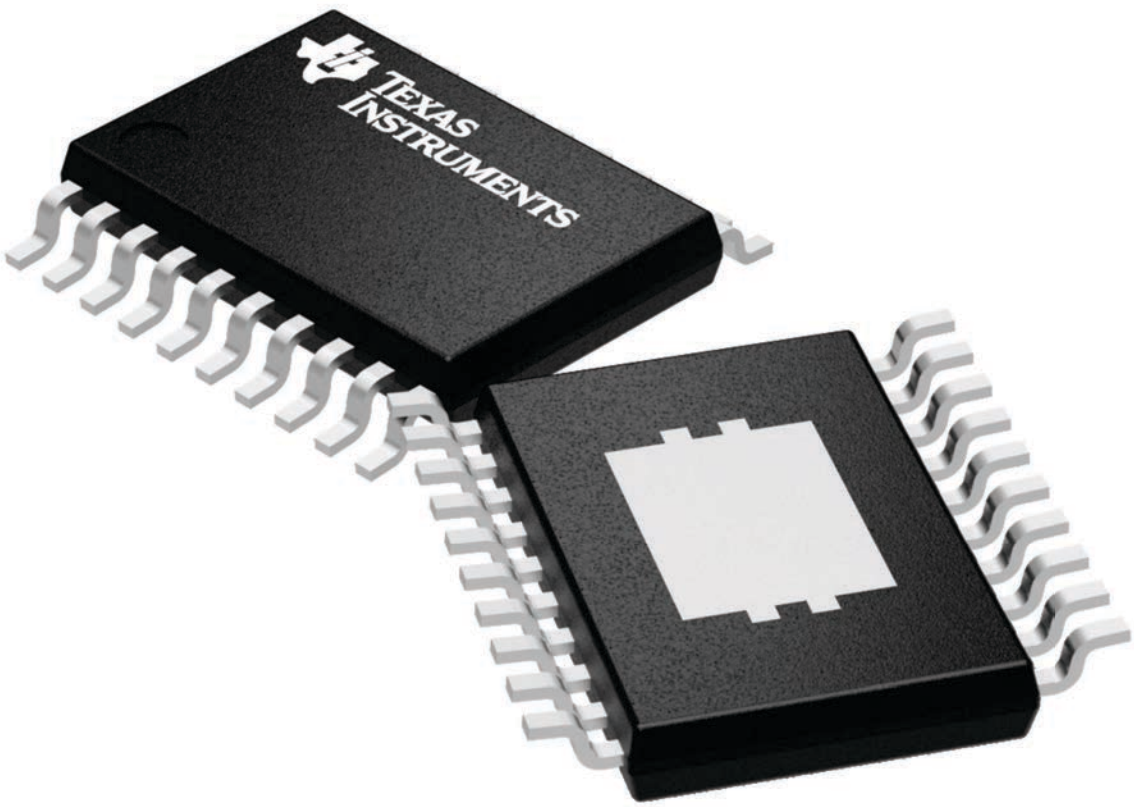
TAPE AND REEL BOX DIMENSIONS



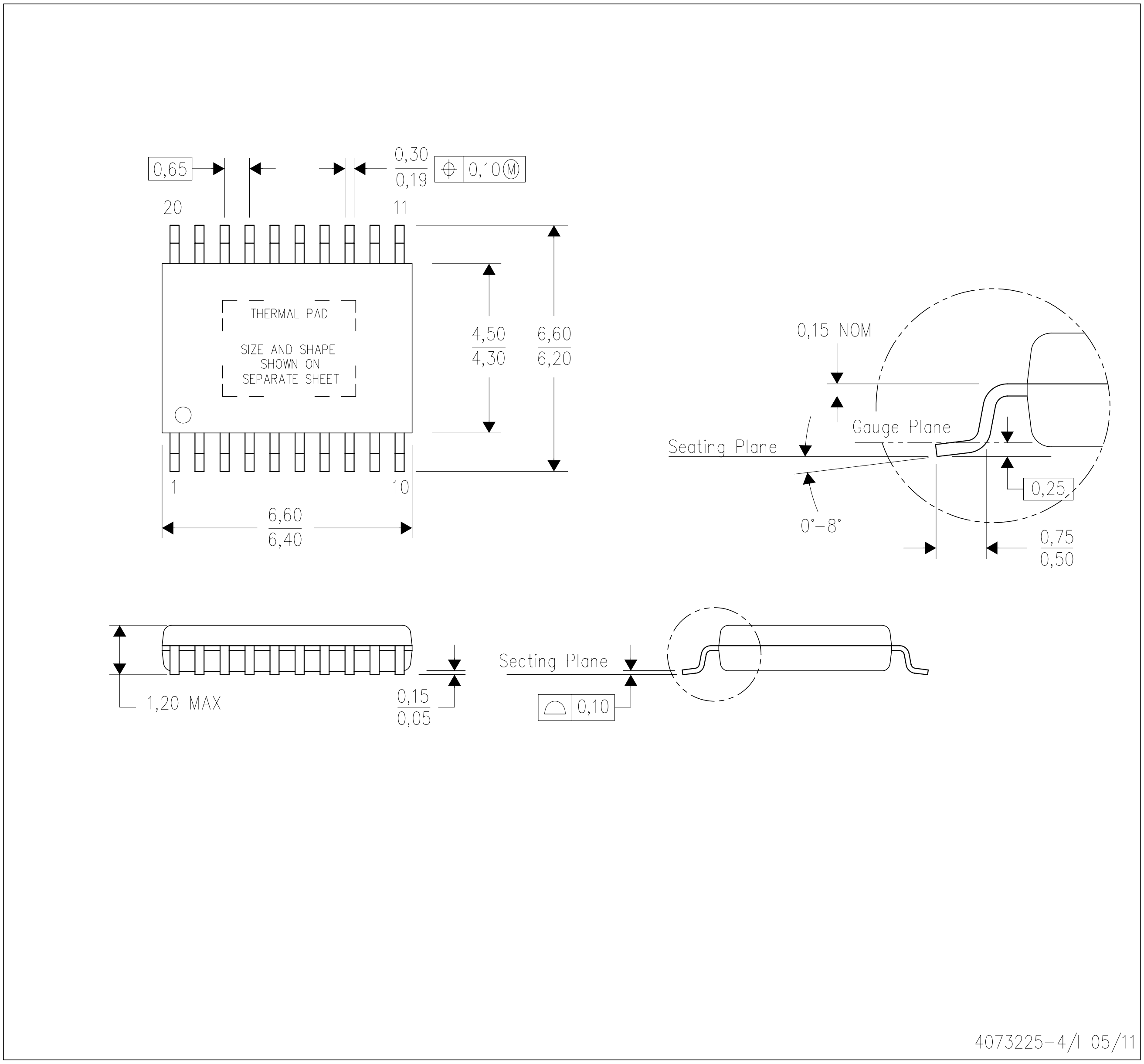

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS54311MPWPREP | HTSSOP | PWP | 20 | 2000 | 350.0 | 350.0 | 43.0 |
| TPS54312MPWPREP | HTSSOP | PWP | 20 | 2000 | 350.0 | 350.0 | 43.0 |
| TPS54313MPWPREP | HTSSOP | PWP | 20 | 2000 | 350.0 | 350.0 | 43.0 |
| TPS54314MPWPREP | HTSSOP | PWP | 20 | 2000 | 350.0 | 350.0 | 43.0 |
| TPS54315MPWPREP | HTSSOP | PWP | 20 | 2000 | 350.0 | 350.0 | 43.0 |
| TPS54316MPWPREP | HTSSOP | PWP | 20 | 2000 | 350.0 | 350.0 | 43.0 |

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO-153

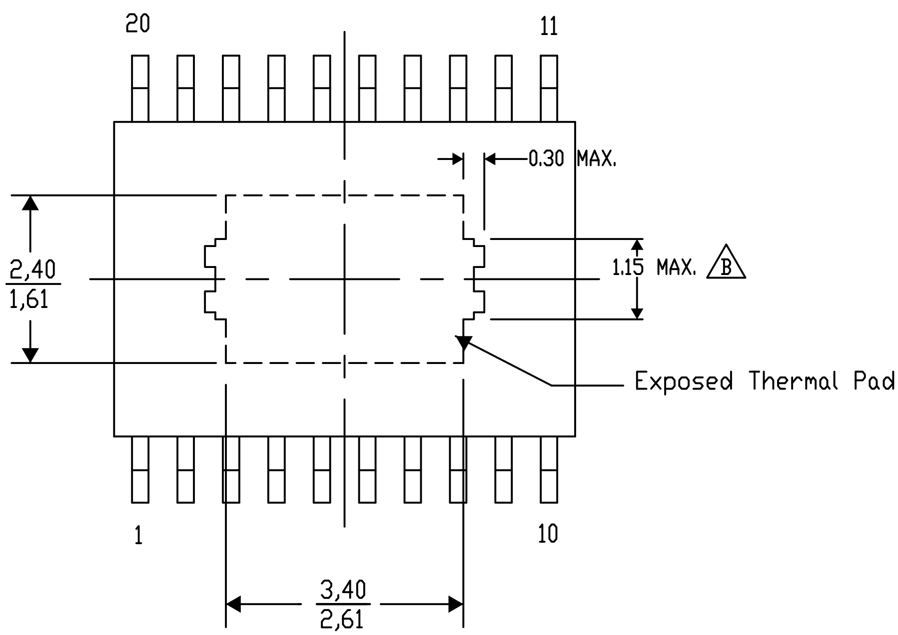
PWP (R-PDSO-G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Top View

Exposed Thermal Pad Dimensions

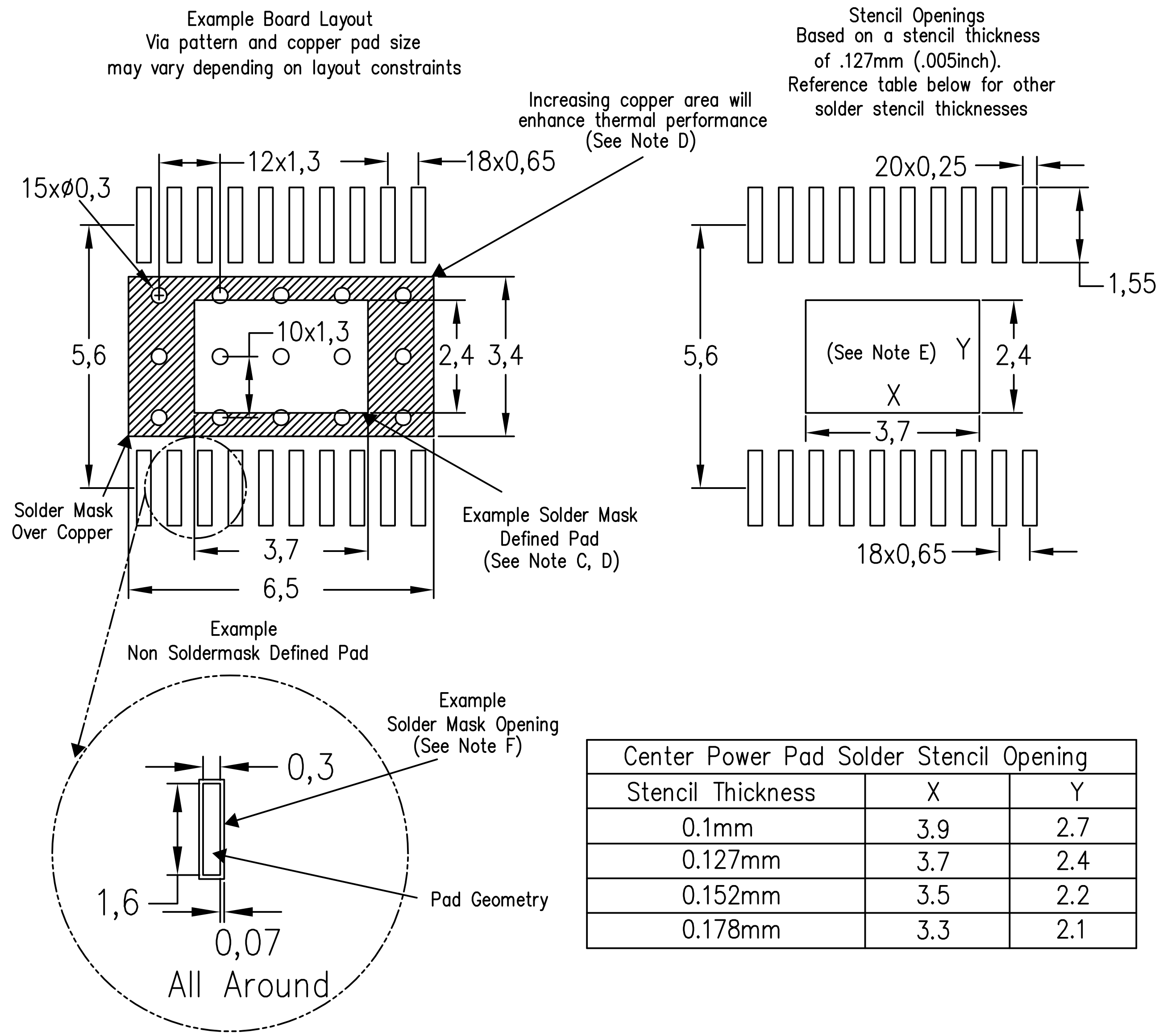
4206332-15/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G20) PowerPAD™ PLASTIC SMALL OUTLINE




| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 3.9 | 2.7 |
| 0.127mm | 3.7 | 2.4 |
| 0.152mm | 3.5 | 2.2 |
| 0.178mm | 3.3 | 2.1 |

4207609-8/W 09/15

NOTES:

A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.

D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC-7351 is recommended for alternate designs.

E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.