

TPS60101 REGULATED 3.3-V 100-mA LOW-NOISE CHARGE PUMP DC/DC CONVERTER

SLVS214B – JUNE 1999 – REVISED AUGUST 2008

features

- Up to 100-mA Output Current
- Less Than 5-mV_{pp} Output Voltage Ripple
- No Inductors Required/Low EMI
- Regulated 3.3-V ±4% Output
- Only Four External Components Required
- Up to 90% Efficiency
- 1.8-V to 3.6-V Input Voltage Range
- 50-μA Quiescent Supply Current
- 0.05-μA Shutdown Current
- Load Isolated in Shutdown
- Space-Saving Thermally-Enhanced TSSOP PowerPAD™ Package
- Evaluation Module Available (TPS60100EVM-131)

description

The TPS60101 step-up, regulated charge pump generates a 3.3-V ±4% output voltage from a 1.8-V to 3.6-V input voltage (two alkaline, NiCd, or NiMH batteries). Output current is 100 mA from a 2-V input. Only four external capacitors are needed to build a complete low-noise dc/dc converter. The push-pull operating mode of two single-ended charge pumps assures the low output voltage ripple as current is continuously transferred to the output. From a 2-V input, the TPS60101 can start into full load with loads as low as 33 Ω.

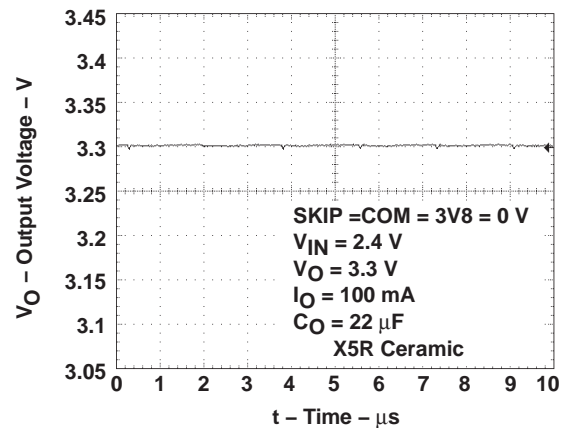
The TPS60101 features either constant frequency mode to minimize noise and output voltage ripple or the power-saving pulse-skip mode to extend battery life at light loads. The TPS60101 switching frequency is 300 kHz. The logic shutdown function reduces the supply current to 1-μA (max) and disconnects the load from the input. Special current-control circuitry prevents excessive current from being drawn from the battery during start-up. This DC/DC converter requires no inductors and has low EMI. It is available in the small 20-pin TSSOP PowerPAD™ package (PWP).

applications

Replaces DC/DC Converters With Inductors in

- Battery-Powered Applications
- Two Battery Cells to 3.3-V Conversion
- Portable Instruments
- Battery-Powered Microprocessor and DSP Systems
- Miniature Equipment
- Backup-Battery Boost Converters
- PDAs
- Laptops
- Handheld Instrumentation
- Medical Instruments
- Cordless Phones

output voltage ripple



typical operating circuit

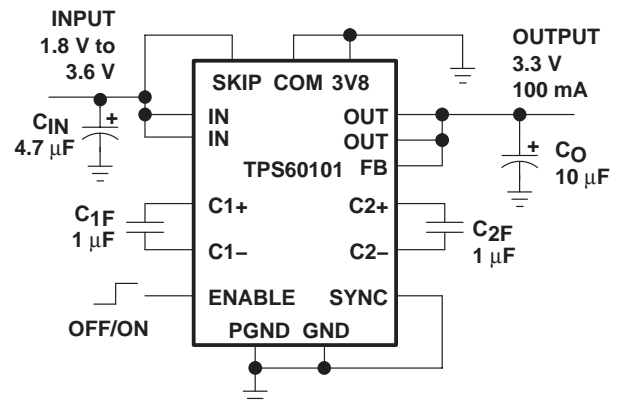


Figure 1



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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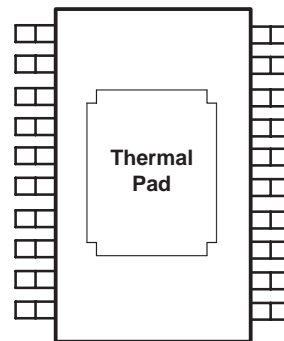
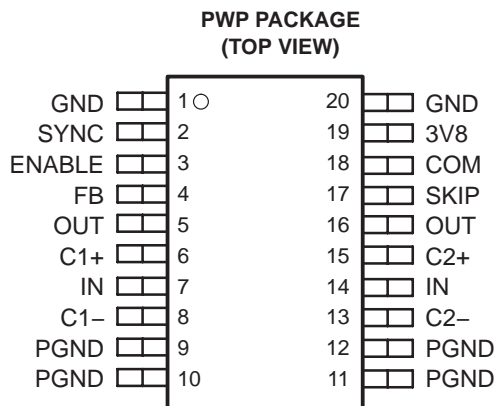


Figure 2. Bottom View of PWP Package, Showing the Thermal Pad

AVAILABLE OPTIONS

| |
|-------------------------|
| PACKAGE |
| TSSOP† (PWP) |
| TPS60101PWP |

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TPS60101PWPR).

Terminal Functions

| TERMINAL NAME | NO. | I/O | DESCRIPTION |
|---------------|-------|-----|--|
| 3V8 | 19 | I | Mode selection. When 3V8 is logic low the charge pump operates in the regulated 3.3-V mode. When 3V8 is connected to IN the regulator operates in preregulated 3.8-V mode. |
| C1+ | 6 | | Positive terminal of the charge-pump capacitor C _{1F} |
| C1- | 8 | | Negative terminal of the charge-pump capacitor C _{1F} |
| C2+ | 15 | | Positive terminal of the charge-pump capacitor C _{2F} |
| C2- | 13 | | Negative terminal of the charge-pump capacitor C _{2F} |
| COM | 18 | I | Mode selection. When COM is logic low the charge pump operates in push-pull mode to minimize output ripple. When COM is connected to IN the regulator operates in single-ended mode requiring only one flying capacitor. |
| ENABLE | 3 | I | ENABLE Input. The device turns off, the output disconnects from the input, and the supply current decreases to 0.05 μA when ENABLE is a logic low. ENABLE High may only be applied when VIN is inside the recommended operating range. |
| FB | 4 | I | FEEDBACK input. Connect FB to OUT as close to the load as possible to achieve best regulation. Resistive divider is on chip to match internal reference voltage of 1.22 V. |
| GND | 1, 20 | | GROUND. Analog ground for internal reference and control circuitry. Connect to PGND through a short trace. |
| IN | 7, 14 | I | Supply Input. Connect to an input supply in the 1.8-V to 3.6-V range. Bypass IN to GND with a (C _O /2) μF capacitor. Connect both INs through a short trace. |
| OUT | 5, 16 | O | Regulated power output. Connect both OUTs through a short trace and bypass OUT to GND with the output filter capacitor C _O . V _O = 3.3 V when 3V8 = low and V _O = 3.8 V when 3V8 = high. |
| PGND | 9–12 | | PGND power ground. Charge-pump current flows through this pin. Connect all PGNDs together. |
| SKIP | 17 | I | Mode selection. When SKIP is logic low, the charge pump operates in constant-frequency mode. Output ripple and noise are minimized in this mode. When SKIP is connect to IN, the device operates in pulse skip mode. Quiescent current is lowest in this mode. |
| SYNC | 2 | I | Selection for external clock signal. Connect to GND to use the internally generated clock signal. Connect to IN for external synchronization. In this case, the clock signal needs to be fed through 3V8 and the device operates in the regulated 3.3-V mode. |

absolute maximum ratings (unless otherwise noted)†‡

| | |
|--|--------------------------------|
| Input voltage range, V_I (IN, OUT, ENABLE, SKIP, COM, 3V8, FB, SYNC) | –0.3 V to 5.5 V |
| Differential input voltage, V_{ID} (C1+, C2+ to GND) | –0.3 V to ($V_{OUT} + 0.3$ V) |
| Differential input voltage, V_{ID} (C1–, C2– to GND) | –0.3 V to ($V_{IN} + 0.3$ V) |
| Continuous total power dissipation | See Dissipation Rating Tables |
| Continuous output current | 150 mA |
| Storage temperature range, T_{stg} | –55°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10s | 260°C |
| Maximum junction temperature, T_J | 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ V_{ENABLE} , V_{SKIP} , V_{COM} , V_{3V8} and V_{SYNC} can exceed V_{IN} up to the maximum rated voltage without increasing the leakage current drawn by these mode select inputs.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURE (see Figure 3)

| PACKAGE | $T_A \leq 25^\circ\text{C}$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 70^\circ\text{C}$ POWER RATING | $T_A = 85^\circ\text{C}$ POWER RATING |
|---------|---|---|--|--|
| PWP | 700 mW | 5.6 mW/°C | 448 mW | 364 mW |

DISSIPATION RATING TABLE 2 – CASE TEMPERATURE (see Figure 4)

| PACKAGE | $T_C \leq 62.5^\circ\text{C}$ POWER RATING | DERATING FACTOR ABOVE $T_C = 62.5^\circ\text{C}$ | $T_C = 70^\circ\text{C}$ POWER RATING | $T_C = 85^\circ\text{C}$ POWER RATING |
|---------|---|---|--|--|
| PWP | 25 W | 285.7 mW/°C | 22.9 W | 18.5 W |

DISSIPATION DERATING CURVES[§]
vs
FREE-AIR TEMPERATURE

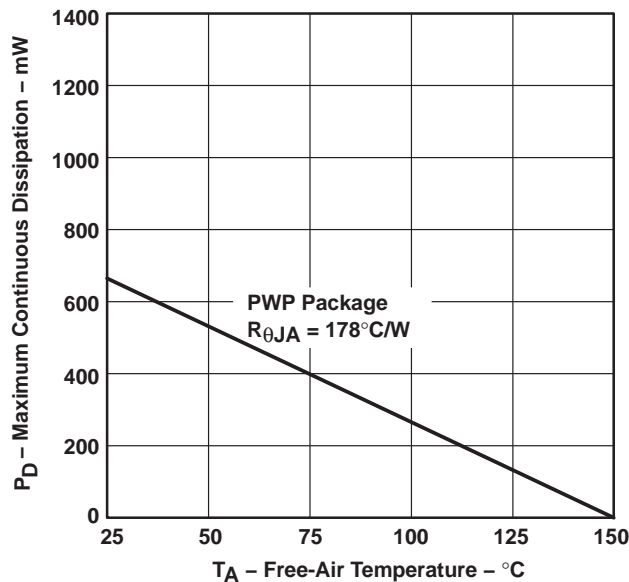


Figure 3

MAXIMUM CONTINUOUS DISSIPATION[§]
vs
CASE TEMPERATURE

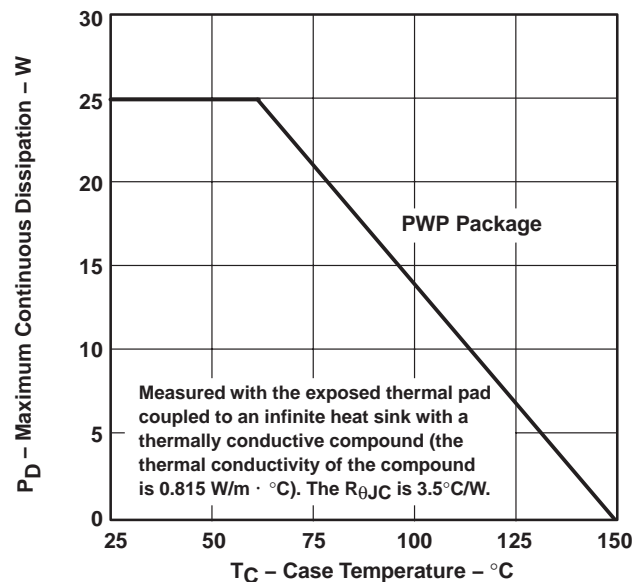


Figure 4

[§] Dissipation rating tables and figures are provided for maintenance of junction temperature at or below absolute maximum temperature of 150°C. It is recommended not to exceed a junction temperature of 125°C.

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electrical characteristics at $C_{IN} = 10 \mu\text{F}$, $C_{1F} = C_{2F} = 2.2 \mu\text{F}^\dagger$, $C_O = 22 \mu\text{F}$, $T_C = -40^\circ\text{C}$ to 85°C , $V_{IN} = 2\text{V}$, $V_{FB} = V_O$, $V_{ENABLE} = V_{IN}$, $V_{SKIP} = V_{IN}$ or 0V and $V_{COM} = V_{3V8} = V_{SYNC} = 0\text{V}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|---------------------|--------------|----------------------------|------------------|
| V_{IN} Input voltage | | 1.8 | | 3.6 | V |
| $V_{IN(UV)}$ Input undervoltage lockout threshold | | | 1.6 | 1.8 | V |
| $I_O(MAX)$ Maximum output current | | 100 | | | mA |
| V_O Output voltage | $1.8\text{V} < V_{IN} < 2\text{V}$, $V_O(\text{Start-Up}) = 3.3\text{V}$, $T_C = 25^\circ\text{C}$ | 3.17 | 3.3 | 3.43 | V |
| | $2\text{V} < V_{IN} < 3.3\text{V}$, $0 < I_O < 100\text{mA}$ | 3.17 | 3.3 | 3.43 | |
| | $3.3\text{V} < V_{IN} < 3.6\text{V}$, $0 < I_O < 100\text{mA}$ | 3.17 | 3.3 | 3.47 | |
| $V_O(RIP)$ Output voltage ripple | $I_O = 100\text{mA}$, $V_{SKIP} = 0\text{V}$ | | 5 \ddagger | | mV _{PP} |
| $I_O(LEAK)$ Output leakage current | $V_{IN} = 2.4\text{V}$, $V_{ENABLE} = 0\text{V}$ | | | 1 | μA |
| I_Q Quiescent current (no-load input current) | $V_{SKIP} = V_{IN} = 2.4\text{V}$ $V_{SKIP} = 0\text{V}$, $V_{IN} = 2.4\text{V}$ | | 50 | 90 | μA |
| | | | 1.5 | | mA |
| $I_{DD(SDN)}$ Shutdown supply current | $V_{IN} = 2.4\text{V}$, $V_{ENABLE} = 0\text{V}$ | | 0.05 | 1 | μA |
| $f_{OSC(int)}$ Internal switching frequency | $V_{IN} = 2.4\text{V}$ | 200 | 300 | 400 | kHz |
| $f_{OSC(ext)}$ External clock frequency | $V_{SYNC} = V_{IN}$, $V_{IN} = 1.8\text{V}$ to 3.6V | 400 | 600 | 800 | kHz |
| External clock duty cycle | $V_{SYNC} = V_{IN}$, $V_{IN} = 1.8\text{V}$ to 3.6V | | 20% | 80% | |
| Efficiency | $I_O = 50\text{mA}$ | | 80% | | |
| V_{INL} Input voltage low, ENABLE, SKIP, COM, 3V8, SYNC | $V_{IN} = 1.8\text{V}$ | | | $0.3 \times V_{IN}$ | V |
| V_{INH} Input voltage high, ENABLE, SKIP, COM, 3V8, SYNC | $V_{IN} = 3.6\text{V}$ | $0.7 \times V_{IN}$ | | | V |
| $I_I(LEAK)$ Input leakage current, ENABLE, SKIP, COM, 3V8, SYNC | $V_{ENABLE} = V_{SKIP} = V_{COM} = V_{3V8} =$ $V_{SYNC} = V_{GND}$ or V_{IN} | | 0.01 | 0.1 | μA |
| Output load regulation | $V_O = 3.3\text{V}$, $T_C = 25^\circ\text{C}$ | | | | $\%/\text{mA}$ |
| Output line regulation | $2\text{V} < V_{IN} < 3.3\text{V}$, $I_O = 50\text{mA}$, $V_O = 3.3\text{V}$, $T_C = 25^\circ\text{C}$ | | 0.6 | | $\%/V$ |
| Short circuit current | $V_{IN} = 2.4\text{V}$, $T_C = 25^\circ\text{C}$ | | | $V_O = 0\text{V}$, 125 | mA |

\dagger Use only ceramic capacitors with X5R or X7R dielectric as flying capacitors.

\ddagger Achieved with $C_O = 22 \mu\text{F}$ X5R dielectric ceramic capacitor

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electrical characteristics for preregulated 3.8-V Mode ($V_{(3V8)} = V_{IN}$), at $C_{IN} = 10 \mu\text{F}$, $C_{1F} = C_{2F} = 2.2 \mu\text{F}$ †, $C_O = 22 \mu\text{F}$, $T_C = -40^\circ\text{C}$ to 85°C , $V_{IN} = 2.4 \text{ V}$, $V_{FB} = V_O$, $V_{ENABLE} = V_{IN}$, $V_{SKIP} = V_{IN}$ or 0 V and $V_{COM} = V_{SYNC} = 0 \text{ V}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------|--|---|-----|------|-----|---------------|
| V_{IN} | Input voltage | | 2.2 | | 3.6 | V |
| $I_{O(MAX)}$ | Maximum output current | | 100 | | | mA |
| V_O | Output voltage | $2.2 \text{ V} < V_{IN} < 3.6 \text{ V}$, $0 < I_O < 100 \text{ mA}$ | 3.6 | 3.8 | 4 | V |
| $I_{O(LEAK)}$ | Output leakage current | $V_{ENABLE} = 0 \text{ V}$ | | | 1 | μA |
| I_Q | Quiescent current (no-load input current) | $V_{SKIP} = V_{IN}$ | | 60 | | μA |
| | | $V_{SKIP} = 0 \text{ V}$ | | 2 | | mA |
| $I_{DD(SDN)}$ | Shutdown supply current | $V_{ENABLE} = 0 \text{ V}$ | | 0.05 | 1 | μA |
| f_{OSC} | Internal switching frequency | | 200 | 300 | 400 | kHz |
| | Short circuit current | $V_O = 0 \text{ V}$, $T_C = 25^\circ\text{C}$ | | 125 | | mA |

† Use only ceramic capacitors with X5R or X7R dielectric as flying capacitors.

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TYPICAL CHARACTERISTICS†

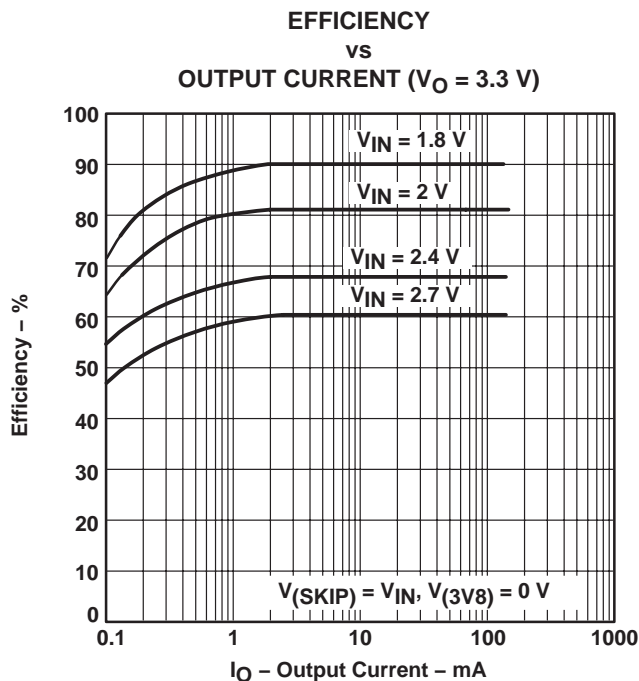


Figure 5

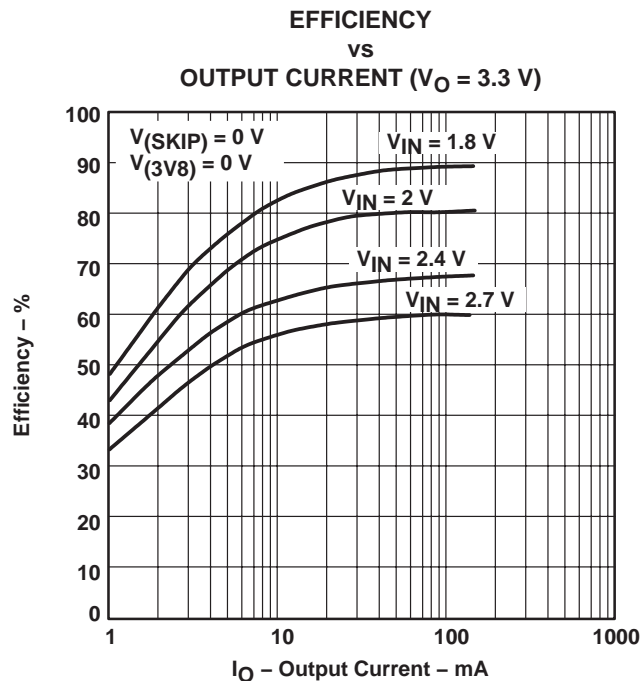


Figure 6

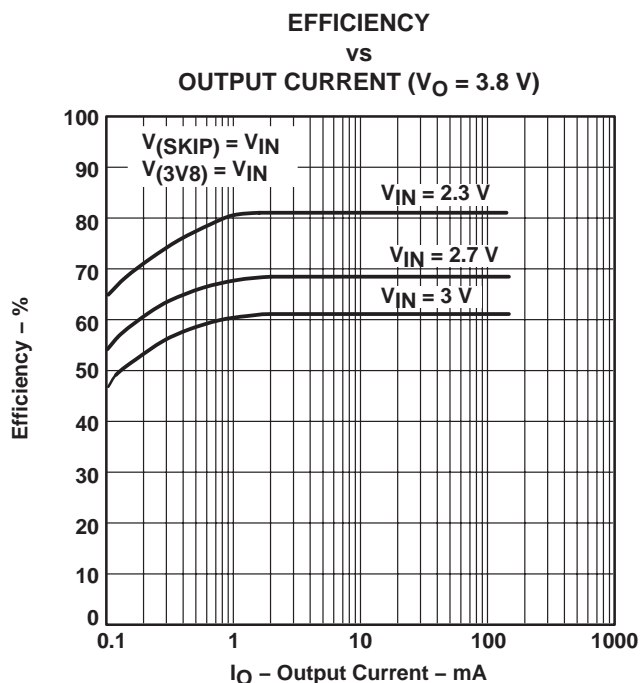


Figure 7

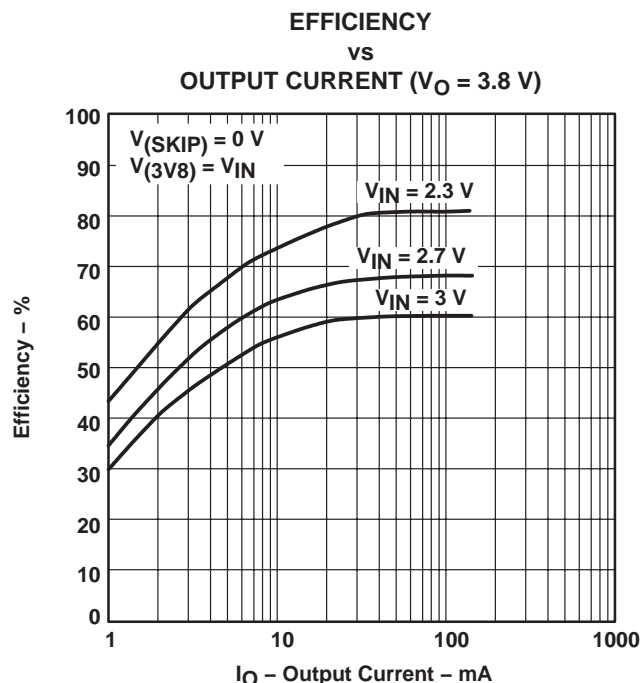


Figure 8

† $T_C = 25^\circ\text{C}$, $V_{COM} = V_{SYNC} = 0\text{ V}$, $C_{IN} = 10\ \mu\text{F}$, $C_{1F} = C_{2F} = 2.2\ \mu\text{F}$, $C_O = 22\ \mu\text{F}$, unless otherwise noted

TYPICAL CHARACTERISTICS†

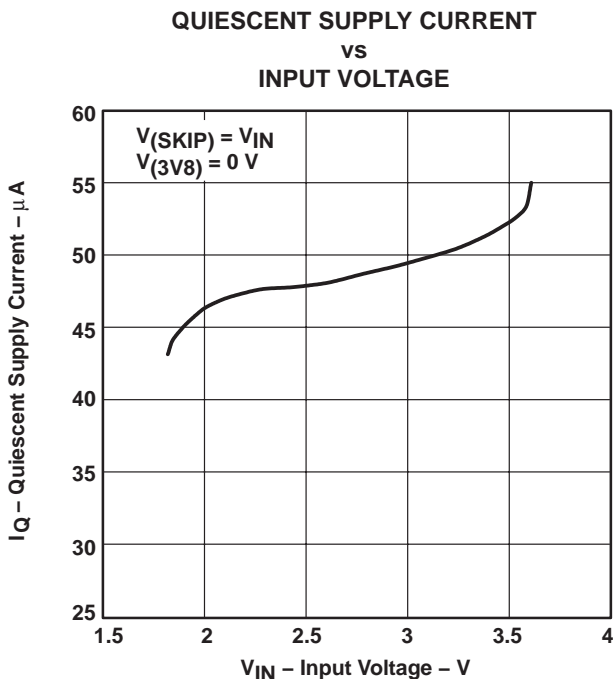


Figure 9

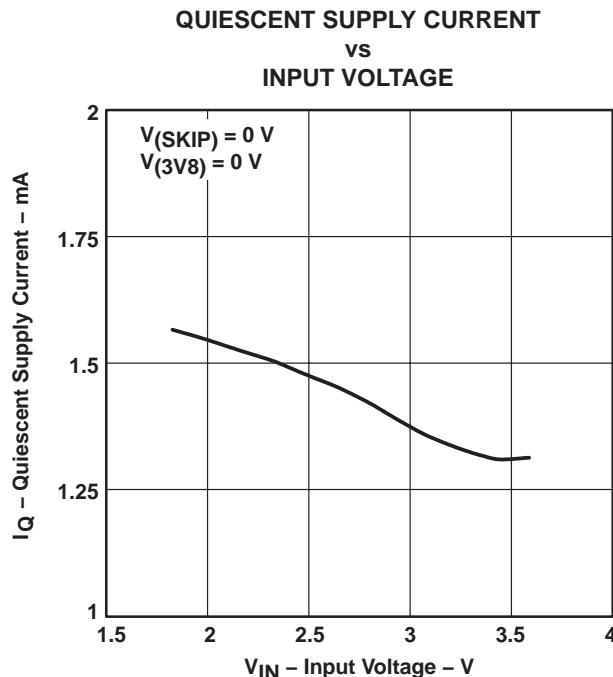


Figure 10

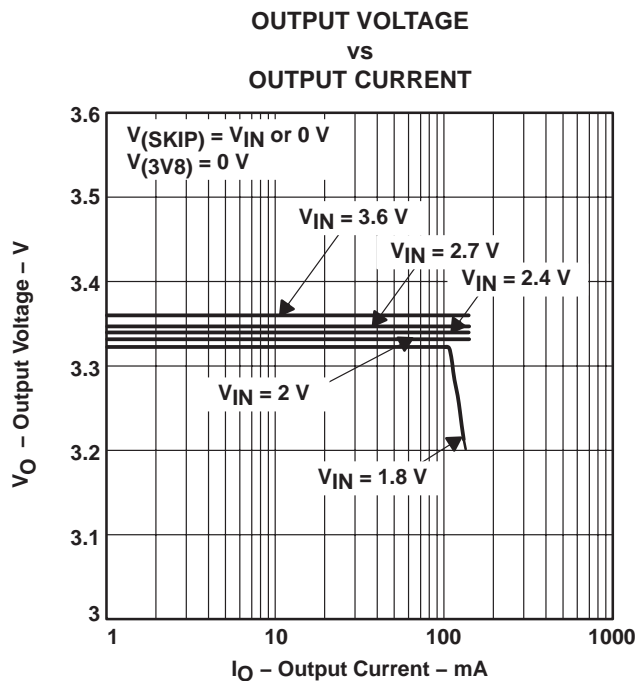


Figure 11

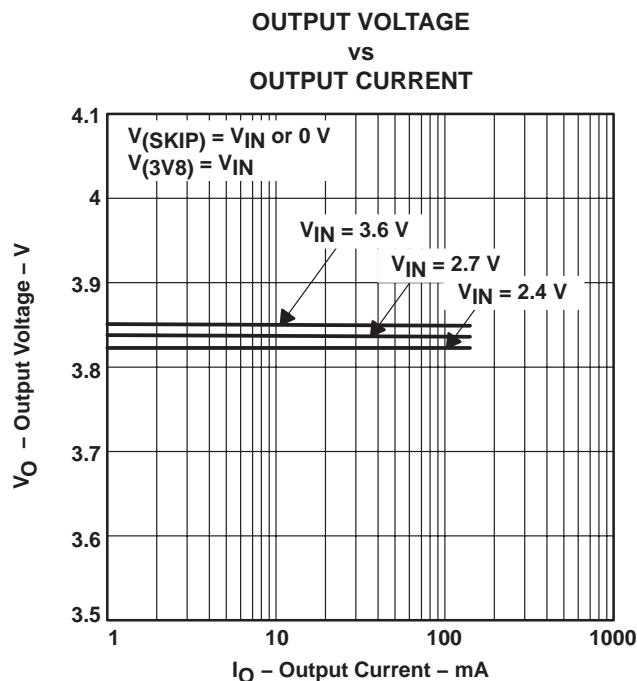


Figure 12

† $T_C = 25^\circ\text{C}$, $V_{\text{COM}} = V_{\text{SYNC}} = 0 \text{ V}$, $C_{\text{IN}} = 10 \mu\text{F}$, $C_{1F} = C_{2F} = 2.2 \mu\text{F}$, $C_O = 22 \mu\text{F}$, unless otherwise noted

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TYPICAL CHARACTERISTICS†

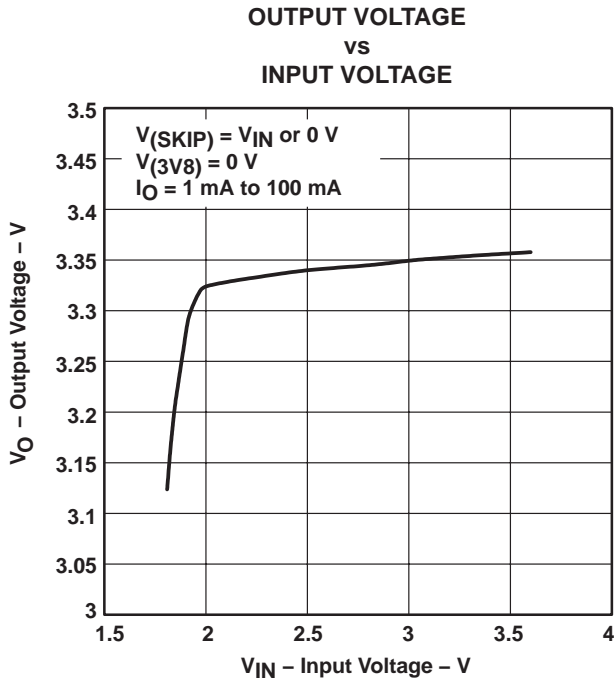


Figure 13

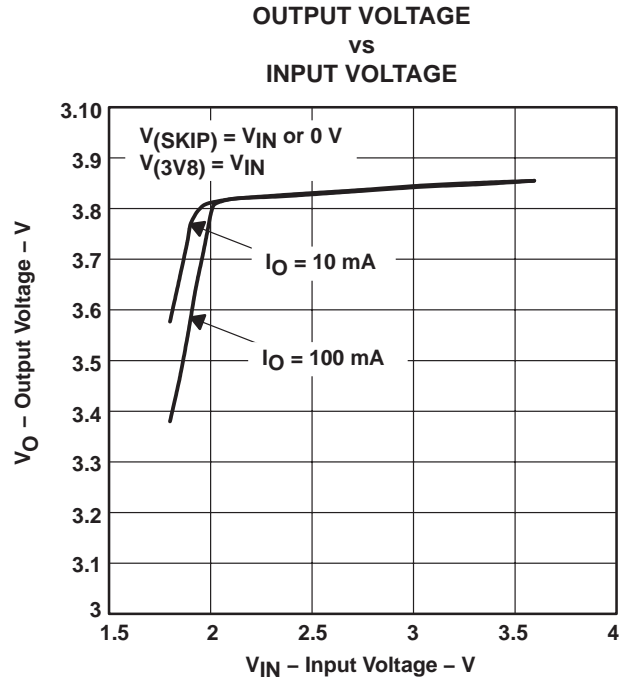


Figure 14

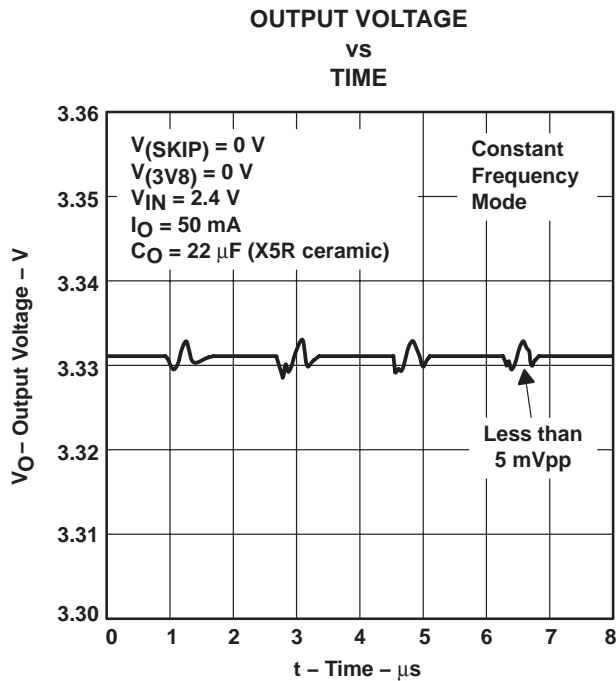


Figure 15

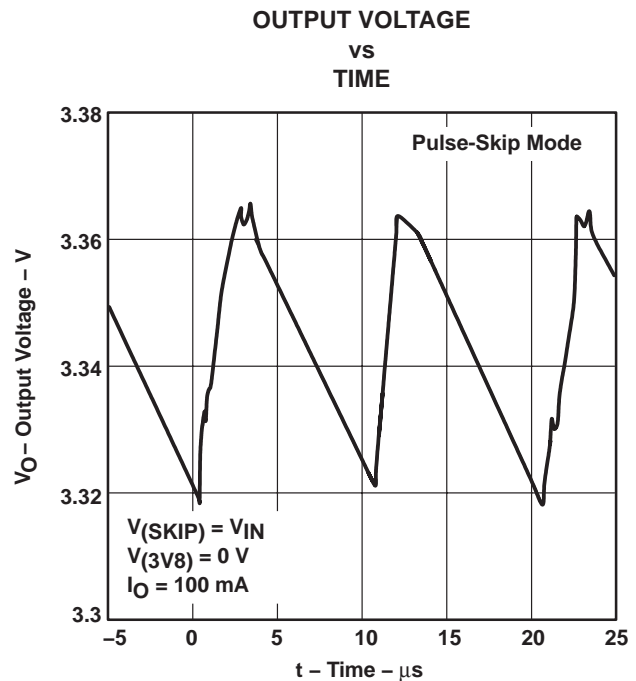


Figure 16

† $T_C = 25^\circ\text{C}$, $V_{COM} = V_{SYNC} = 0\text{ V}$, $C_{IN} = 10\ \mu\text{F}$, $C_{1F} = C_{2F} = 2.2\ \mu\text{F}$, $C_O = 22\ \mu\text{F}$, unless otherwise noted

TYPICAL CHARACTERISTICS†

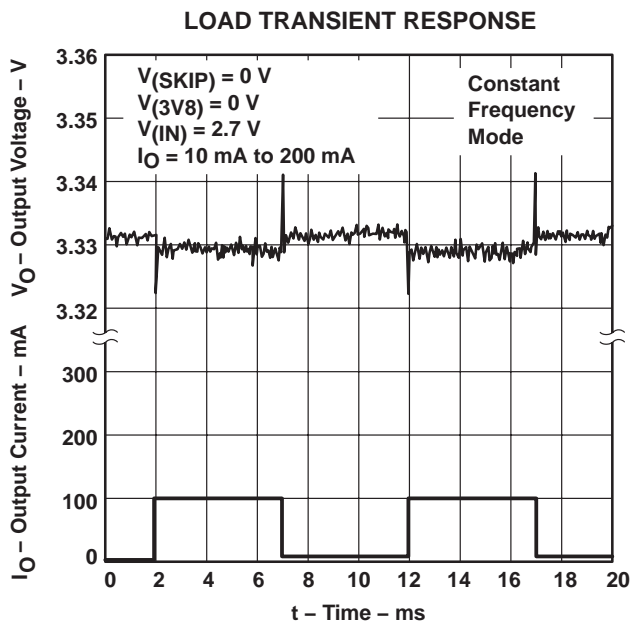


Figure 17

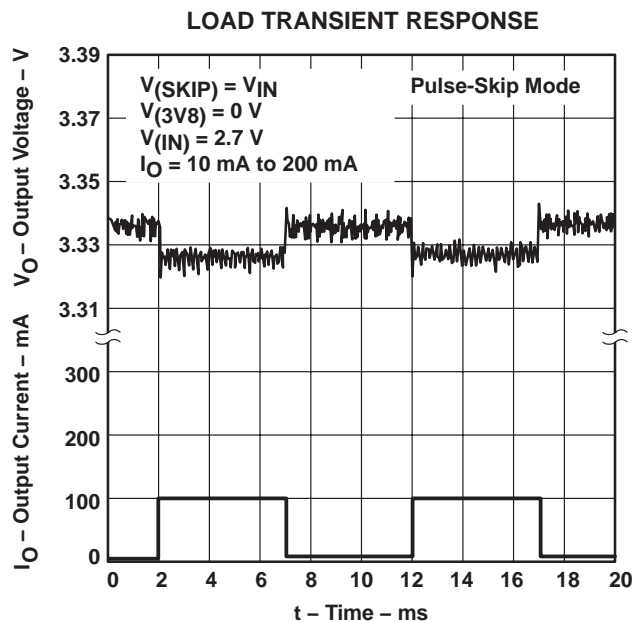


Figure 18

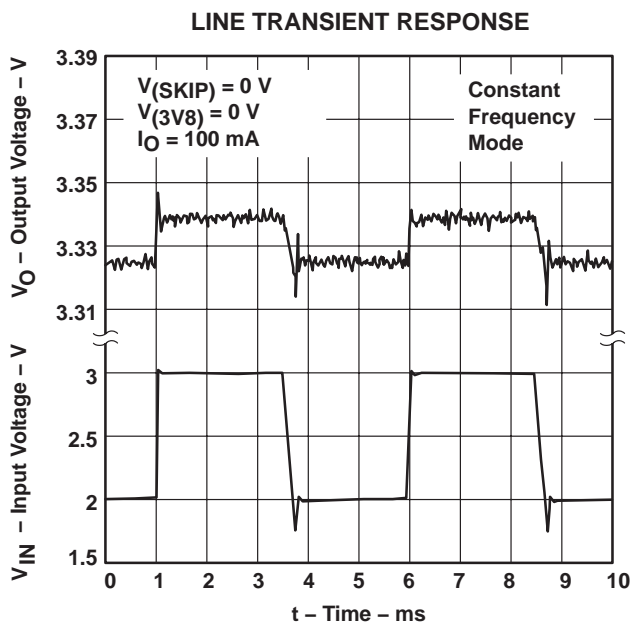


Figure 19

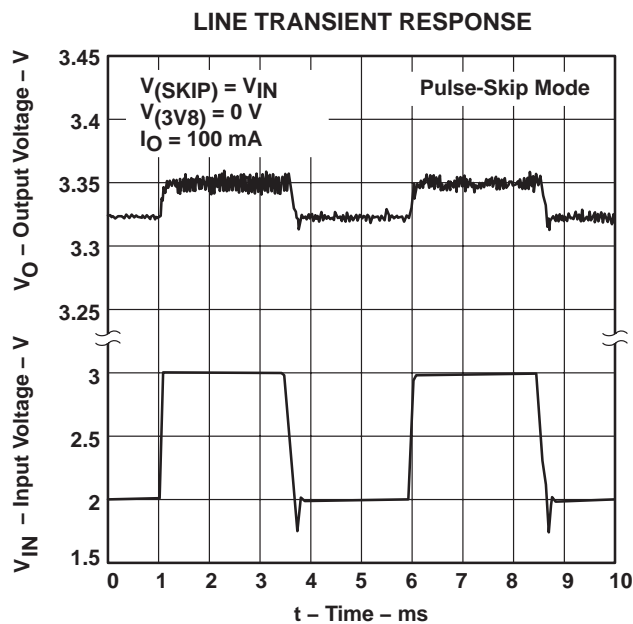


Figure 20

† $T_C = 25^\circ\text{C}$, $V_{COM} = V_{SYNC} = 0\text{ V}$, $C_{IN} = 10\ \mu\text{F}$, $C_{1F} = C_{2F} = 2.2\ \mu\text{F}$, $C_O = 22\ \mu\text{F}$, unless otherwise noted

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TYPICAL CHARACTERISTICS†

**FREQUENCY SPECTRUM
 CONSTANT FREQUENCY MODE‡**

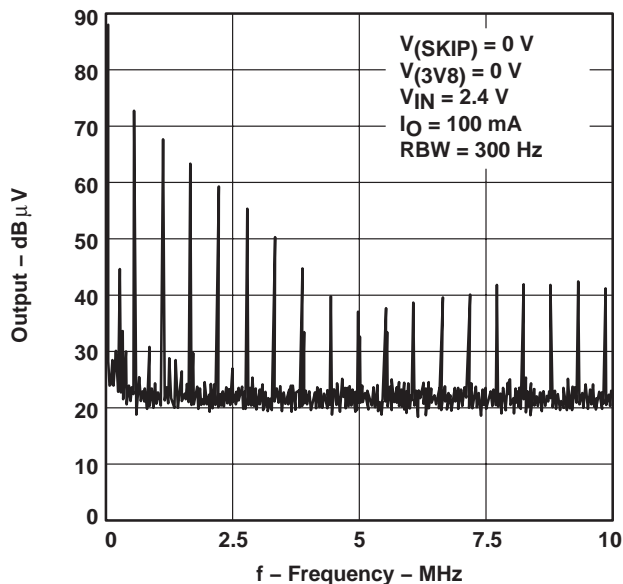


Figure 21

**FREQUENCY SPECTRUM
 PULSE-SKIP MODE‡**

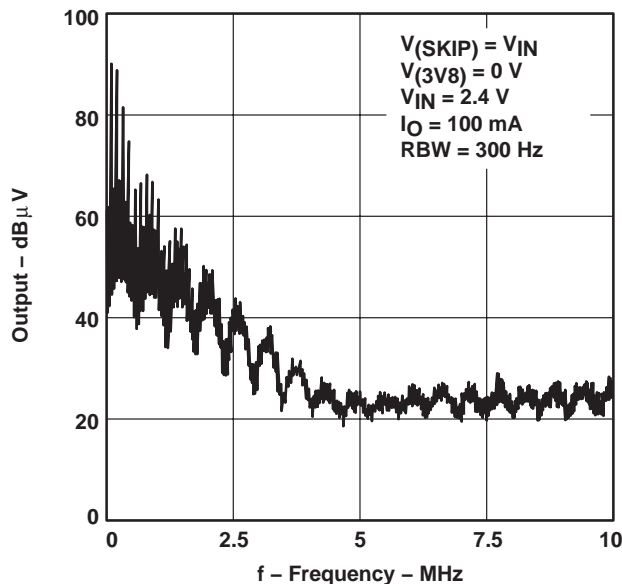


Figure 22

**FREQUENCY SPECTRUM
 CONSTANT FREQUENCY MODE‡**

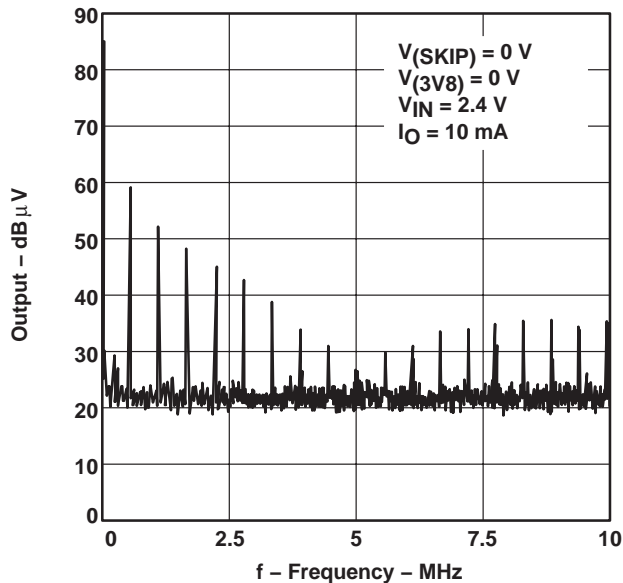


Figure 23

**FREQUENCY SPECTRUM
 PULSE-SKIP MODE‡**

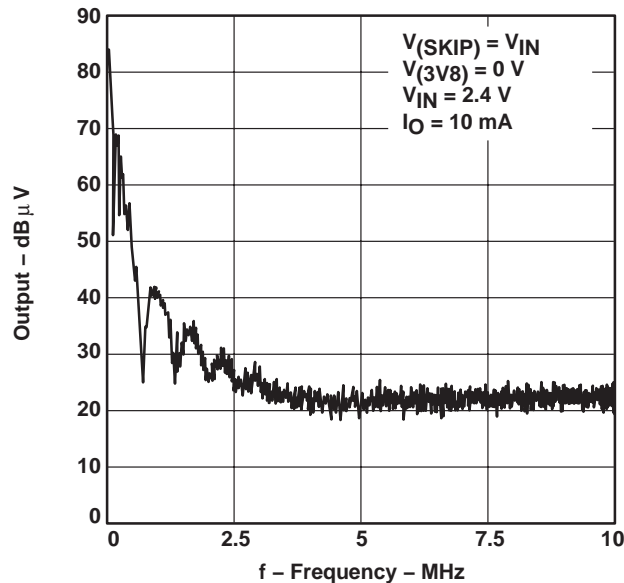
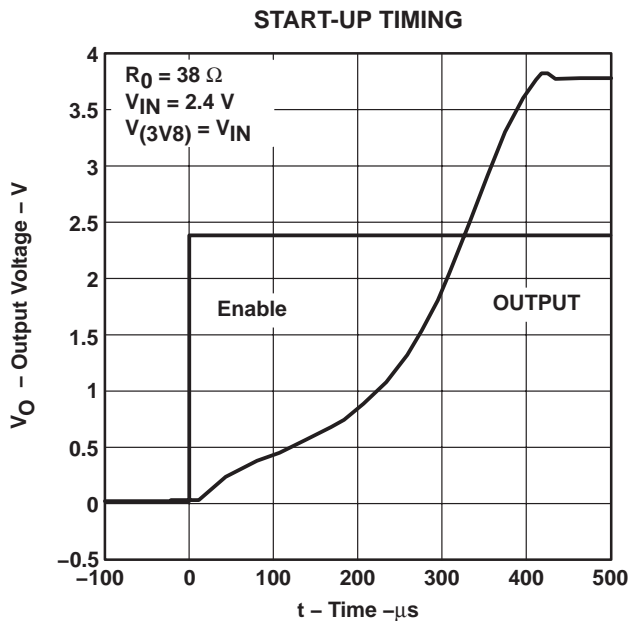
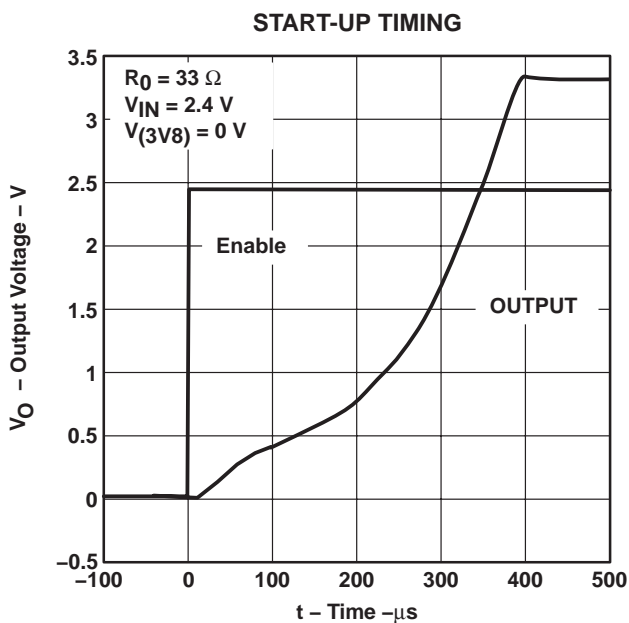
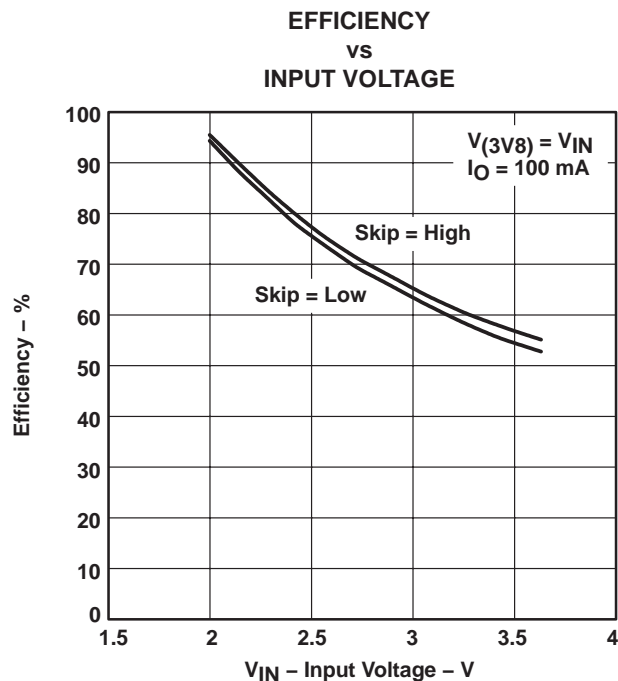
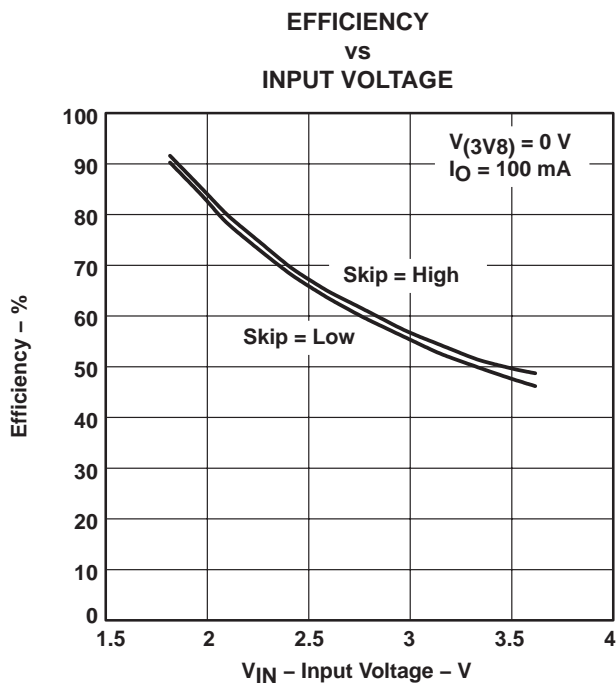


Figure 24

† $T_C = 25^\circ\text{C}$, $V_{COM} = V_{SYNC} = 0\text{ V}$, $C_{IN} = 10\ \mu\text{F}$, $C_{1F} = C_{2F} = 2.2\ \mu\text{F}$, $C_O = 22\ \mu\text{F}$, unless otherwise noted

‡ Test circuit: TPS60100EVM-131 with TPS60101

TYPICAL CHARACTERISTICS†



† TC = 25°C, VCOM = VSYNC = 0 V, CIN = 10 μF, C1F = C2F = 2.2 μF, CO = 22 μF, unless otherwise noted

TPS60101

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detailed description

operating principle

The TPS60101 charge pump provides a regulated 3.3-V output from a 1.8-V to 3.6-V input. It delivers a maximum load current of 100 mA. Designed specifically for space critical battery powered applications, the complete charge pump circuit requires only four external capacitors. The circuit can be optimized for highest efficiency at light loads or lowest output noise. The TPS60101 consists of an oscillator, a 1.22-V bandgap reference, an internal resistive feedback circuit, an error amplifier, high current MOSFET switches, a shutdown/start-up circuit, and a control circuit (Figure 29)

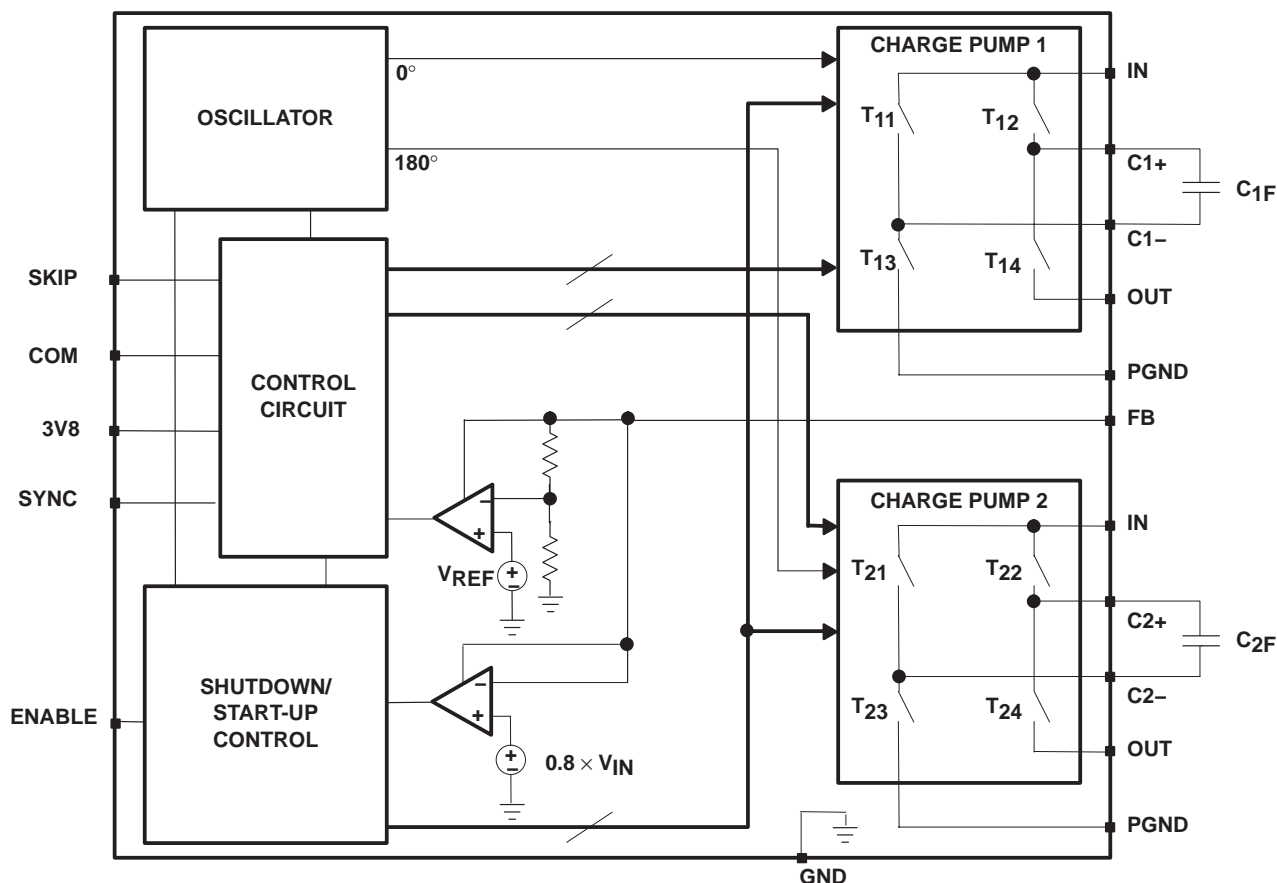


Figure 29. Functional Block Diagram TPS60101

The oscillator runs at a 50% duty cycle. The device consists of two single-ended charge pumps which operate with 180° phase shift. Each single ended charge pump transfers charge into its transfer capacitor (C_{XF}) in one half of the period. During the other half of the period (transfer phase), C_{XF} is placed in series with the input to transfer its charge to C_O . While one single-ended charge pump is in the charge phase, the other one is in the transfer phase. This operation guarantees an almost constant output current which ensures a low output ripple.

If the clock were to run continuously, this process would eventually generate an output voltage equal to two times the input voltage (hence the name doubler). In order to provide a regulated fixed output voltage of 3.3 V, the TPS60101 uses either pulse-skip mode or constant-frequency mode. Pulse-skip mode and constant-frequency mode are externally selected via the SKIP input pin.

detailed description (continued)

start-up procedure

During start-up, i.e. when ENABLE is set from logic low to logic high, the switches T12 and T14 (charge pump 1), and the switches T22 and T24 (charge pump 2) are conducting to charge up the output capacitor until the output voltage V_O reaches $0.8 \times V_{IN}$. When the start-up comparator detects this limit, the IC begins to operate in the mode selected with SKIP, COM and 3V8. This start-up charging of the output capacitor guarantees a short start-up time and eliminates the need for a Schottky diode between IN and OUT.

pulse-skip mode

In pulse-skip mode (SKIP = high), the error amplifier disables switching of the power stages when it detects an output higher than 3.3 V. The oscillator halts. The IC then skips switching cycles until the output voltage drops below 3.3 V. Then the error amplifier reactivates the oscillator and switching of the power stages starts again. The pulse-skip regulation mode minimizes operating current because it does not switch continuously and deactivates all functions except bandgap reference and error amplifier when the output is higher than 3.3 V. When switching is disabled from the error amplifier, the load is also isolated from the input. SKIP is a logic input and should not remain floating. The typical operating circuit of the TPS60101 in pulse skip mode is shown in Figure 1.

constant-frequency mode

When SKIP is low, the charge pump runs continuously at the frequency f_{OSC} . The control circuit, fed from the error amplifier, controls the charge on C_{1F} and C_{2F} by driving the gates of the FETs T12/T13 and T22/T23, respectively. When the output voltage falls, the gate drive increases, resulting in a larger voltage across C_{1F} and C_{2F} . This regulation scheme minimizes output ripple. Since the device switches continuously, the output noise contains well-defined frequency components, and the circuit requires smaller external capacitors for a given output ripple. However, constant-frequency mode, due to higher operating current, is less efficient at light loads than pulse-skip mode.

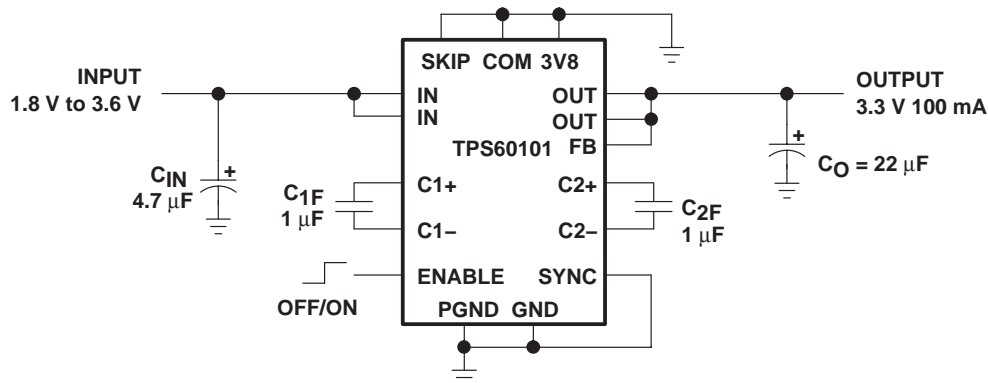


Figure 30. Typical Operating Circuit TPS60101 in Constant Frequency Mode

Table 1. Tradeoffs Between Operating Modes

| FEATURE | PULSE-SKIP MODE (SKIP = High) | CONSTANT-FREQUENCY MODE (SKIP = Low) |
|--|----------------------------------|---|
| Best light-load efficiency | X | |
| Smallest external component size for a given output ripple | | X |
| Output ripple amplitude | Small amplitude | Very small amplitude |
| Output ripple frequency | Variable | Constant |
| Load regulation | Very good | Good |

NOTE: Even in pulse-skip mode the output ripple amplitude is small if the push-pull operating mode is selected via COM.

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detailed description (continued)

push-pull operating mode

In push-pull operating mode (COM = low), the two single-ended charge pumps operate with 180° phase shift. The oscillator signal has a 50% duty cycle. Each single-ended charge pump transfers charge into its transfer capacitor (C_{XF}) in one-half of the period. During the other half of the period (transfer phase), C_{XF} is placed in series with the input to transfer its charge to C_O . While one single-ended charge pump is in the charge phase, the other one is in the transfer phase. This operation guarantees an almost constant output current which ensures a low output ripple. COM is a logic input and should not remain floating. The typical operating circuit of the TPS60101 in push-pull mode is shown in Figure 1 and Figure 30.

single-ended operating mode

When COM is high, the device runs in single-ended operating mode. The two single-ended charge pumps operate in parallel without phase shift. They transfer charge into the transfer capacitor (C_F) in one half of the period. During the other half of the period (transfer phase), C_F is placed in series with the input to transfer its charge to C_O . In single-ended operating mode only one transfer capacitor ($C_F = C_{1F} + C_{2F}$) is required, resulting in less board space.

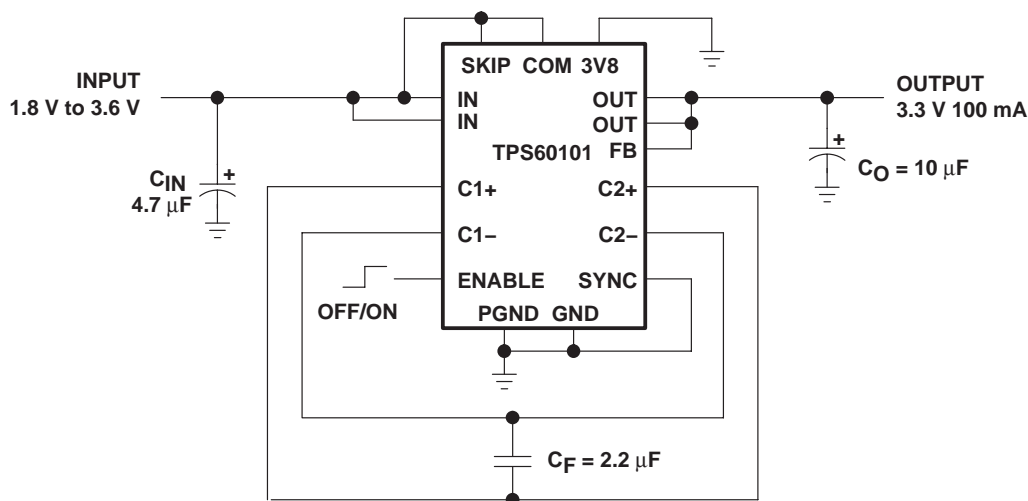


Figure 31. Typical Operating Circuit TPS60101 in Single-Ended Operating Mode

Table 2. Tradeoffs Between Operating Modes

| FEATURE | PUSH-PULL MODE (COM = Low) | SINGLE-ENDED MODE (COM = High) |
|-------------------------|-------------------------------|-----------------------------------|
| Output ripple amplitude | Small amplitude | Large amplitude |
| Smallest board space | | X |

regulated 3.3 V operating mode

In regulated 3.3-V operating mode (3V8 = low) the device provides a regulated 3.3-V output from a 1.8-V to 3.6-V input. 3V8 is a logic input and should not remain floating. The typical operating circuit of the TPS60101 in (3.3 V) regulated mode is shown in Figure 1 and Figure 30.

pre-regulated 3.8 V operating mode

When 3V8 is high, the device provides a preregulated 3.8-V output from a 2.2-V to 3.6-V input. This mode should be used if a tighter output voltage tolerance is a major concern. In this case the charge pump generates the input voltage for a low-dropout regulator.

detailed description (continued)

shutdown

Driving ENABLE low places the device in shutdown mode. This disables all switches, the oscillator, and control logic. The device typically draws 0.05- μ A (1- μ A max) of supply current in this mode. Leakage current drawn from the output is as low as 1 μ A max. The device exits shutdown once ENABLE is set high level. The typical no-load shutdown exit time is 10 μ s. When the device is in shutdown, the load is isolated from the input and the output is high impedance.

external clock signal

If the device operates at a user defined frequency, an external clock signal can be used. Therefore, SYNC needs to be connected to IN and the external oscillator signal can drive 3V8. The maximum external frequency is limited to 800 kHz. The switching frequency of the converter is half of the external oscillator frequency. It is recommended to operate the charge pump in constant-frequency mode if an external clock signal is used so that the output noise contains only well-defined frequency components.

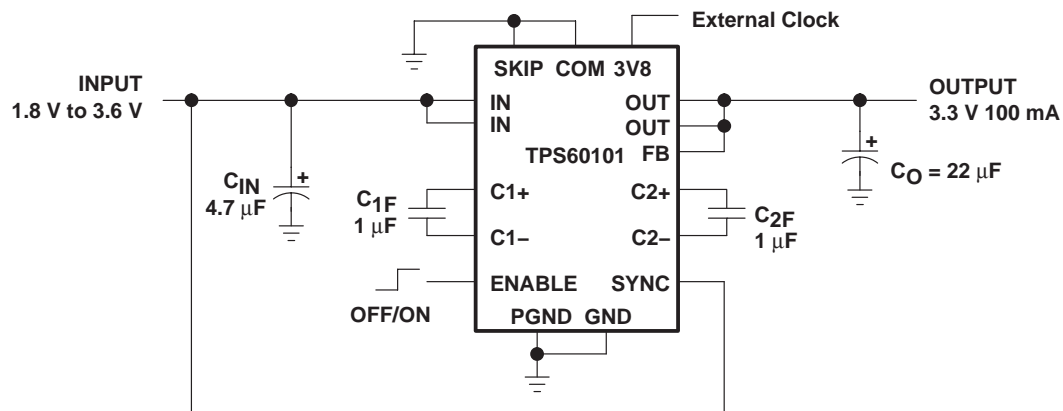


Figure 32. Typical Operating Circuit TPS60101 With External Synchronization

undervoltage lockout

The TPS60101 has an undervoltage lockout feature that deactivates the device and places it in shutdown mode when the input voltage falls below 1.6 V.

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APPLICATION INFORMATION

capacitor selection

The TPS60101 requires only four external capacitors as shown in the basic application circuit. Their values are closely linked to the output current capacity, output noise requirements, and mode of operation. Generally, the transfer capacitors (C_{XF}) will be the smallest.

The input capacitor improves system efficiency by reducing the input impedance and stabilizes the input current. C_{IN} is recommended to be about two to four times as large as C_{XF} .

The output capacitor (C_O) can be selected from 5-times to 50-times larger than C_{XF} , depending on the mode of operation and ripple tolerance[†]. Tables 3 and 4 show capacitor values recommended for low quiescent-current operation (pulse-skip mode) and for low output voltage ripple operation (constant-frequency mode). A recommendation is given for smallest size.

Table 3. Recommended Capacitor Values for Low Quiescent-Current Operation[†] (pulse-skip mode)

| V_{IN} [V] | I_O [mA] | C_{IN} [μ F] | | C_{XF} [μ F] | C_O [μ F] | | OUTPUT VOLTAGE RIPPLE V_{PP} [mV] |
|--------------|------------|---------------------|-----------|---------------------|------------------|----------|-------------------------------------|
| | | TANTALUM | CERAMIC | | TANTALUM | CERAMIC | |
| 2.4 | 50 | 4.7 | | 1 | 10 | | 135 |
| 2.4 | 50 | | 4.7 (X7R) | 1 | | 10 (X5R) | 125 |
| 2.4 | 100 | 4.7 | | 1 | 10 | | 70 |
| 2.4 | 100 | | 4.7 (X7R) | 1 | | 10 (X5R) | 65 |

[†] All measurements are done with additional 1- μ F X7R ceramic capacitors at input and output.

Table 4. Recommended Capacitor Values for Low Output Voltage Ripple Operation[†] (constant-frequency mode)

| V_{IN} [V] | I_O [mA] | C_{IN} [μ F] | | C_{XF} [μ F] | C_O [μ F] | | OUTPUT VOLTAGE RIPPLE V_{PP} [mV] |
|--------------|------------|---------------------|-----------|---------------------|------------------|----------|-------------------------------------|
| | | TANTALUM | CERAMIC | | TANTALUM | CERAMIC | |
| 2.4 | 50 | 4.7 | | 1 | 22 | | 5 |
| 2.4 | 50 | | 4.7 (X7R) | 1 | | 22 (X5R) | 3 |
| 2.4 | 100 | 4.7 | | 1 | 22 | | 10 |
| 2.4 | 100 | | 4.7 (X7R) | 1 | | 22 (X5R) | 5 |

[†] All measurements are done with additional 1- μ F X7R ceramic capacitors at input and output.

[†] In constant-frequency mode always select $C_O \geq 22 \mu$ F

APPLICATION INFORMATION

For the TPS60101, the smallest board space size can be achieved using Sprague's 595D-series tantalum capacitors for input and output. However, with the trend towards high capacitance ceramic capacitors in smaller size packages, these type of capacitors might become competitive in size soon.

Table 5. Recommended Capacitors

| MANUFACTURER | PART NUMBER | CAPACITANCE | TYPE |
|--------------|-----------------|-------------|----------|
| Taiyo Yuden | LMK212BJ105KG-T | 1 μ F | Ceramic |
| | LMK212BJ225MG-T | 2.2 μ F | Ceramic |
| | LMK316BJ475KL-T | 4.7 μ F | Ceramic |
| | JMK316BJ106ML-T | 10 μ F | Ceramic |
| | LMK432BJ226MM-T | 22 μ F | Ceramic |
| AVX | 0805ZC105KAT2A | 1 μ F | Ceramic |
| | 1206ZC225KAT2A | 2.2 μ F | Ceramic |
| | TPSC475035R0600 | 4.7 μ F | Tantalum |
| | TPSC106025R0500 | 10 μ F | Tantalum |
| | TPSC226016R0375 | 22 μ F | Tantalum |
| Sprague | 595D475X0016A2T | 4.7 μ F | Tantalum |
| | 595D106X0010A2T | 10 μ F | Tantalum |
| | 595D226X06R3A2T | 22 μ F | Tantalum |
| | 595D226X06R3B2T | 22 μ F | Tantalum |
| | 595D226X0020C2T | 22 μ F | Tantalum |
| Kemet | T494B475M010AS | 4.7 μ F | Tantalum |
| | T494C106M010AS | 10 μ F | Tantalum |
| | T494C226M010AS | 22 μ F | Tantalum |

Table 6 lists the manufacturers of recommended capacitors. In most applications surface-mount tantalum capacitors will be the right choice. However, ceramic capacitors will provide the lowest output voltage ripple due to their typically lower ESR.

Table 6. Recommended Capacitor Manufacturers

| MANUFACTURER | CAPACITOR TYPE | INTERNET |
|--------------|--|--|
| Taiyo Yuden | X7R/X5R ceramic | www.t-yuden.com |
| AVX | X7R/X5R ceramic TPS-series tantalum | www.avxcorp.com |
| Sprague | 595D-series tantalum 593D-series tantalum | www.vishay.com |
| Kemet | T494-series tantalum | www.kemet.com |

power dissipation

The power dissipated in the TPS60101 depends on output current and is approximated by:

$$P_{DISS} = I_O \times (2 V_{IN} - V_O) \text{ for } I_Q \ll I_O$$

P_{DISS} must be less than that allowed by the package rating. See the ratings for 20-PowerPAD™ package power-dissipation limits and deratings.

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APPLICATION INFORMATION

layout

All capacitors should be soldered in close proximity to the IC. A PCB layout proposal for a two-layer board is given in Figure 33. Care has been taken to connect both single-ended charge pumps symmetrically to the load to achieve optimized output voltage ripple performance. The proposed layout also provides improved thermal performance as the exposed leadframe is soldered to the PCB. The bottom layer of the PCB is a ground plane only. All ground areas on the PCB should be connected. Connect ground areas on top layer to the bottom layer via through hole connections.

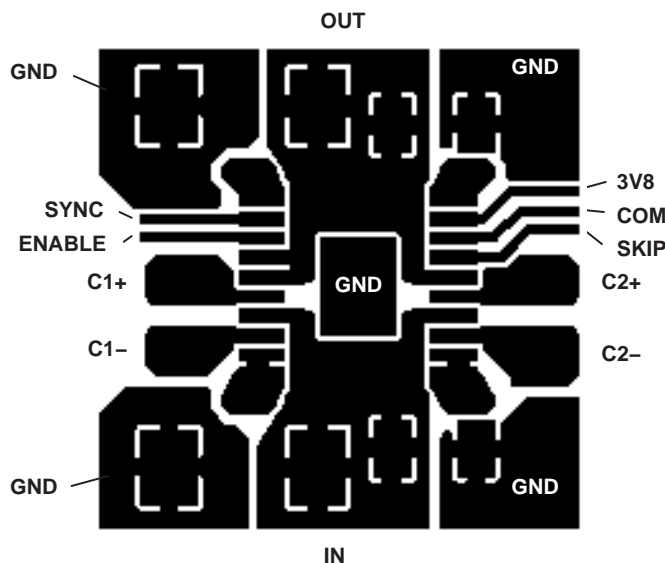


Figure 33. Recommended PCB Layout for TPS60101 (top view)

The evaluation module designed for the TPS60100 can, with slight modifications, be used for evaluation of the TPS60101. The EVM can be ordered under literature code SLVP131 or under product code TPS60100EVM-131.

APPLICATION INFORMATION

applications proposals

TPS60101 with LC output filter for ultra low ripple

For applications where extremely low output ripple is required, a small LC filter is recommended. This is shown in Figure 34. The addition of a small inductor and filter capacitor will reduce the output ripple well below what could be achieved with capacitors alone. The corner frequency of 500 kHz was chosen above the 300 kHz switching frequency to avoid loop stability issues in case the feedback is taken from the output of the LC filter. Leaving the feedback (FB) connection point before the LC filter, the filter capacitance value can be increased to achieve even higher ripple attenuation without affecting stability margin.

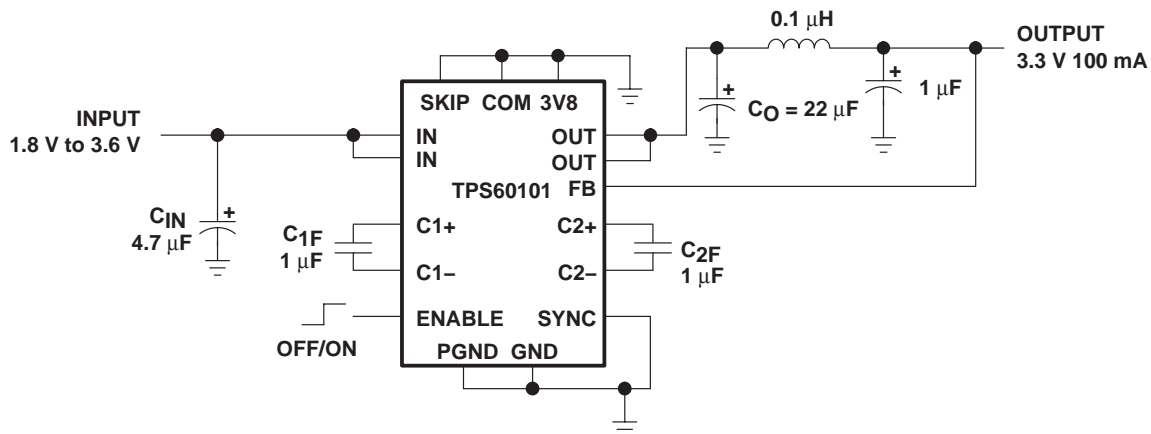


Figure 34. TPS60101 With LC Filter for Ultra Low Output Ripple Applications

related information

application reports

For more application information see:

- *PowerPAD™ Application Report* (Literature Number: SLMA002)
- *TPS6010x/TPS6011x Charge Pump Application Report* (Literature Number: SLVA070)

device family products

Other devices in this family are:

| PART NUMBER | LITERATURE NUMBER | DESCRIPTION |
|-------------|-------------------|---|
| TPS60100 | SLVS213 | Regulated 3.3-V, 200-mA Low-Noise Charge Pump DC/DC Converter |
| TPS60110 | SLVS215 | Regulated 5-V, 300-mA Low-Noise Charge Pump DC/DC Converter |
| TPS60111 | SLVS216 | Regulated 5-V, 150-mA Low-Noise Charge Pump DC/DC Converter |

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------------|---------------|----------------------|-------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| TPS60101PWP | Active | Production | HTSSOP (PWP) 20 | 70 TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TPS60101 |
| TPS60101PWP.A | Active | Production | HTSSOP (PWP) 20 | 70 TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TPS60101 |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| TPS60101PWP | PWP | HTSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| TPS60101PWP.A | PWP | HTSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |

GENERIC PACKAGE VIEW

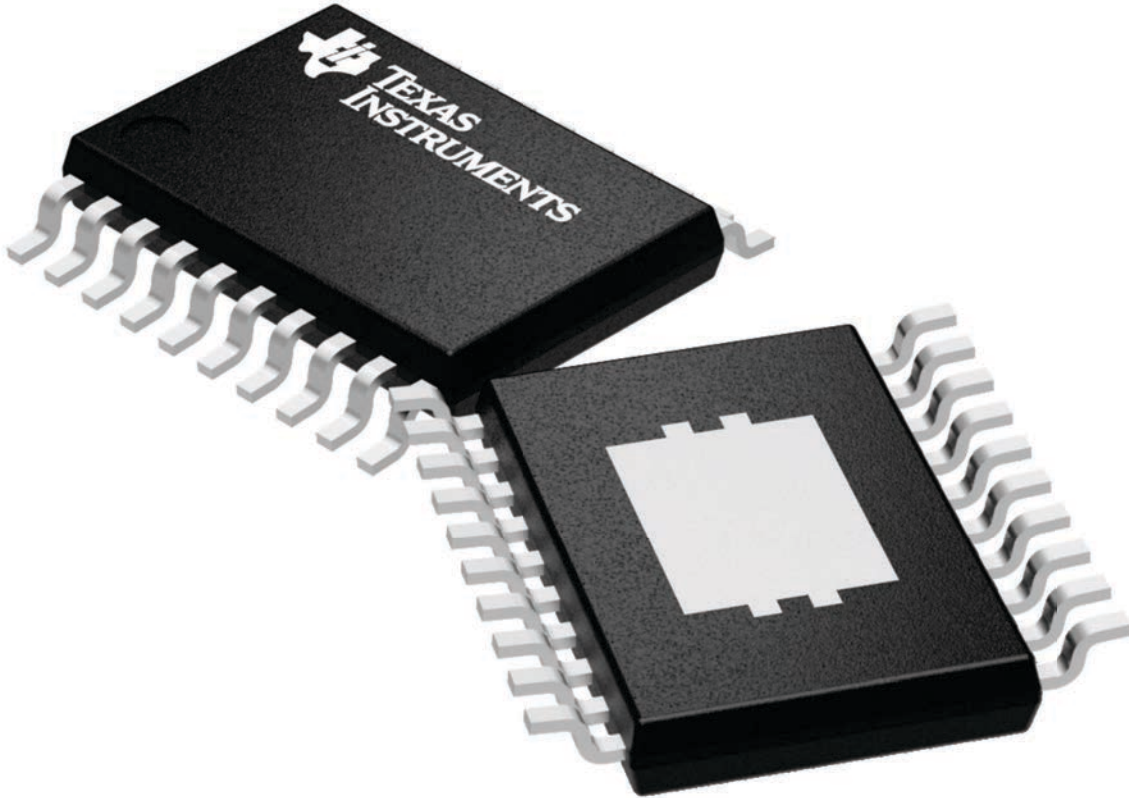
PWP 20

HTSSOP - 1.2 mm max height

6.5 x 4.4, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

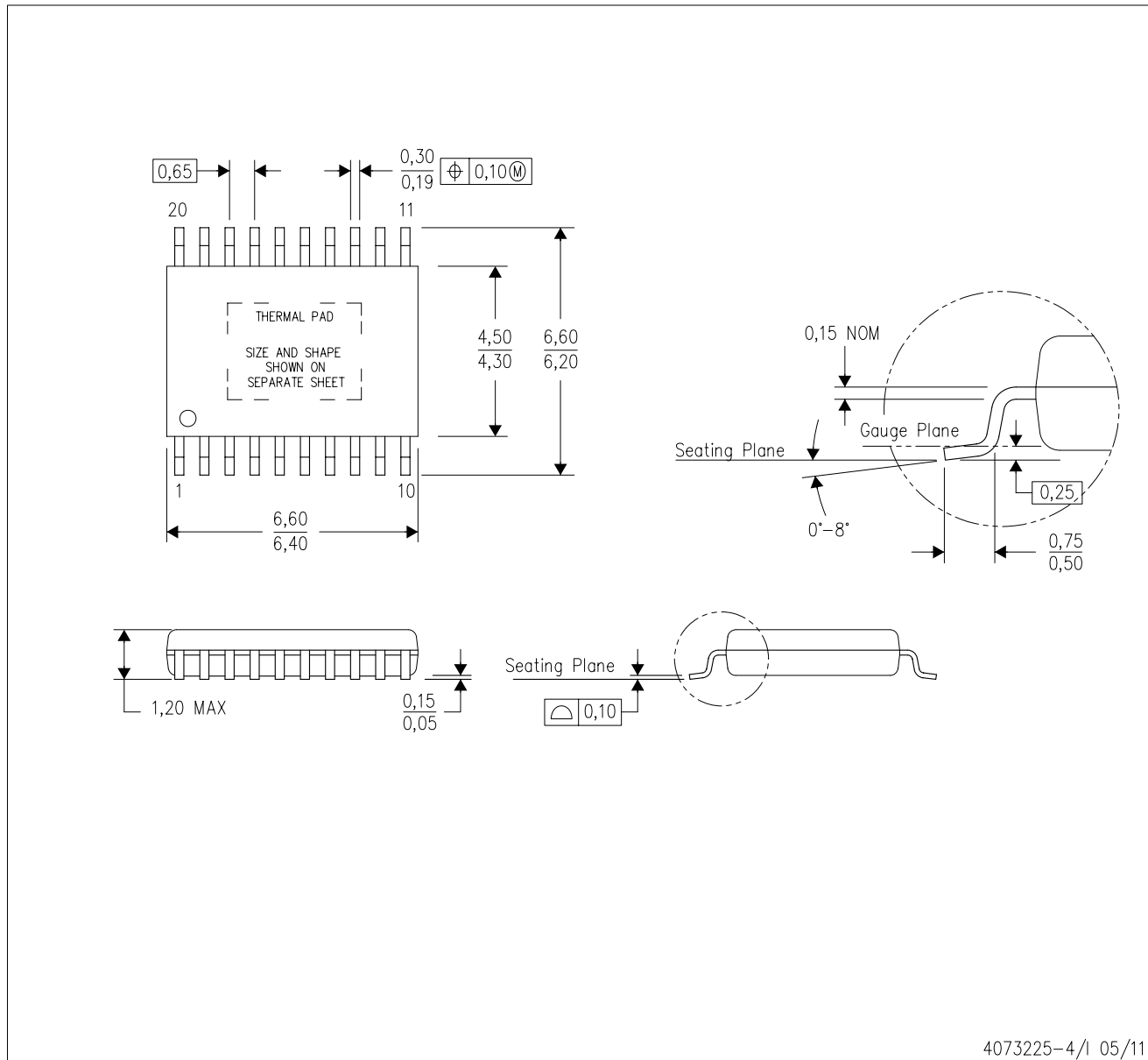


4224669/A

MECHANICAL DATA

PWP (R-PDSO-G20)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

THERMAL PAD MECHANICAL DATA

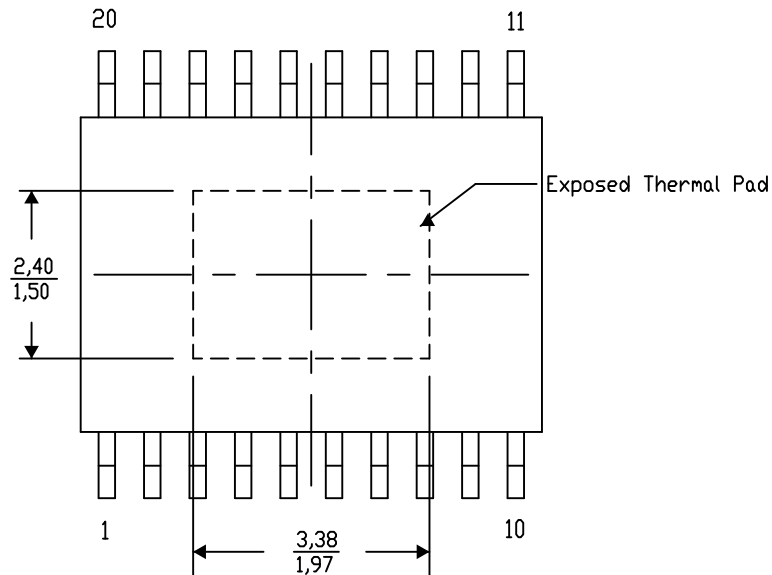
PWP (R-PDSO-G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

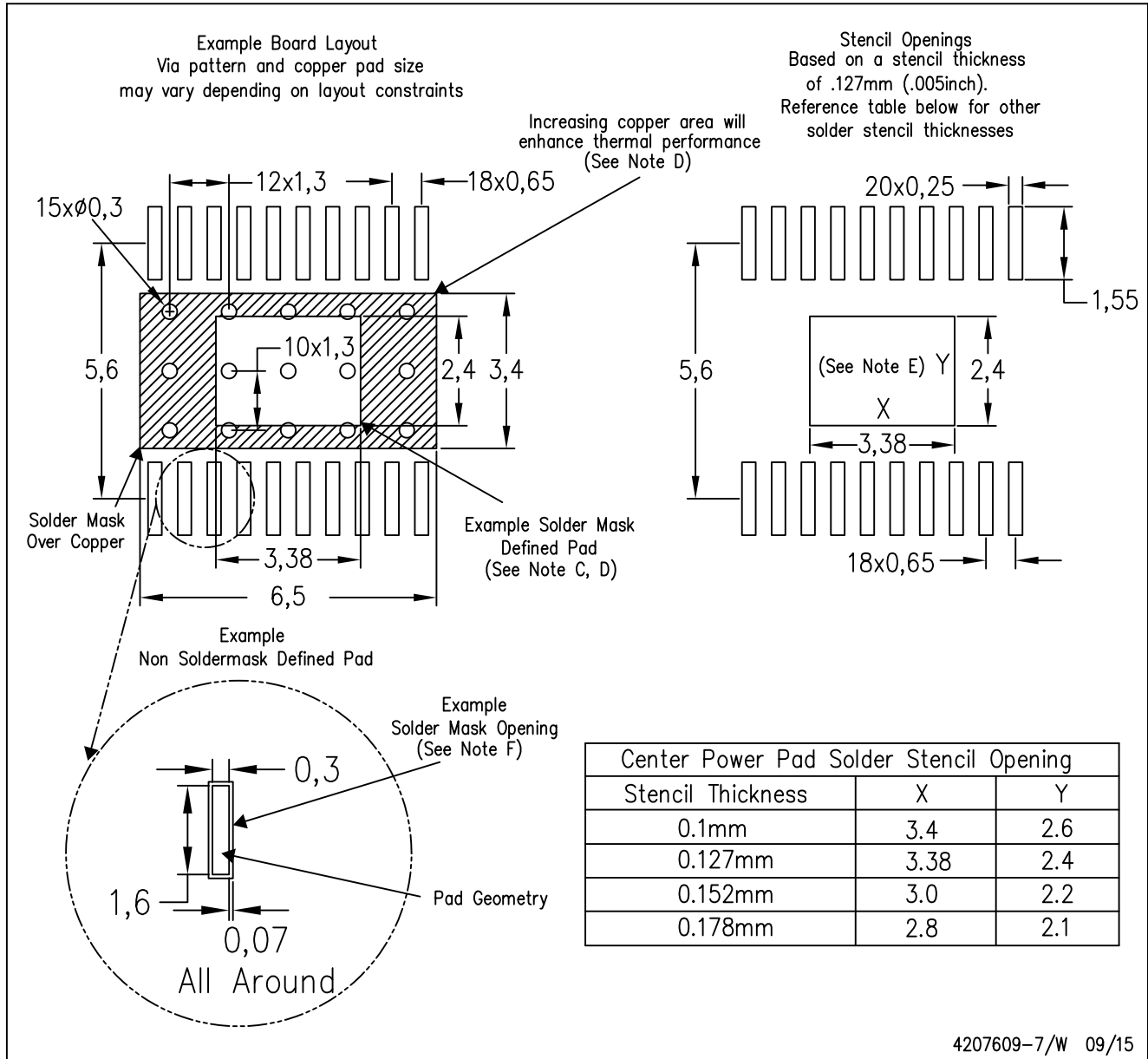
4206332-19/AO 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G20)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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