TPS61371 16V, 3.8A Synchronous Boost With Load Disconnect

1 Features

- Input voltage range: 2.7V to 5.5V
- Output voltage range: up to 16V
  - I^2C programmable V_{OUT} through FB V_{ref}
- On-resistance:
  - Low-side FET - 35mΩ
  - High-side + disconnect FET - 106mΩ
- Switch peak current limit: 3.8A typical
- Quiescent current from V_{IN}: 125µA
- Quiescent current from V_{OUT}: 10µA
- Shutdown current from V_{IN}: 2.5µA
- Switching frequency: 1.5MHz
- Soft-start time: 1.5ms
- Auto PFM and forced PWM selectable
- Load disconnect during shutdown
- Output discharge selectable
- External loop compensation
- Output short and overvoltage protection with latch type
- 2.5mm × 2.5mm × 0.8mm (max) HotRod™ lite WQFN package

2 Applications

- RF PA driver
- SSD
- Backup power
- Optical sensor driver

3 Description

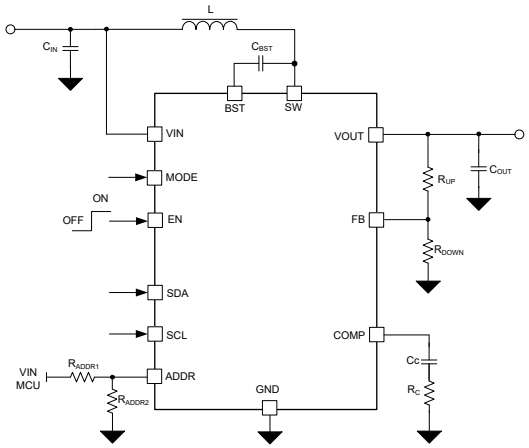
The TPS61371 is a fully-integrated synchronous boost converter with the load disconnect built-in. The device supports output voltage up to 16V with a 3.8A current limit. The output voltage can be changed either by the feedback resistors or by the I^2C controlled reference voltage V_{REF}. The input voltage ranges from 2.7V to 5.5V supporting applications powered by a single-cell Lithium-ion battery or 5V bus.

The TPS61371 uses the peak current mode with the adaptive off-time control topology. The device works in PWM operation of 1.5MHz at moderate-to-heavy loads. At the light load conditions, the device can be configured in either auto PFM or forced PWM operation. The mode is determined by the connection of the MODE pin and the I^2C register. Auto PFM mode has the benefit of high efficiency at light load while forced PWM operation keeps the switching frequency constant across the whole load range. The TPS61371 has a soft start to minimize the inrush current during start-up. The TPS61371 features of the load disconnect during shutdown and provides latch type overvoltage and output short protections. In addition, the device implements thermal shutdown protection.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS61371	VAR (WQFN-HR, 14)	2.5mm × 2.5mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Circuit

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4 Pin Configuration and Functions

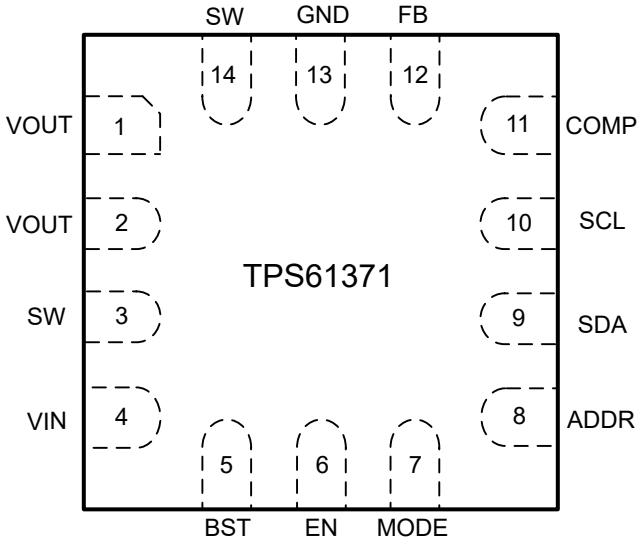


Figure 4-1. VAR Package, 14-Pin WQFN-HR (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NUMBER	NAME		
1, 2	VOUT	PWR	Boost converter output
3, 14	SW	PWR	The switching node pin of the converter. This pin is connected to the drain of the internal low-side FET and the source of the internal high-side FET. The pin-3 and pin-14 SW must be connected together. And put the inductor close to the pin-3 SW
4	VIN	I	IC power supply input
5	BST	O	Power supply for the high-side FET gate driver. A capacitor must be connected between this pin and the SW pin.
6	EN	I	Enable logic input. Logic low level disables the device output. Logic high level and CONVERTER_EN = 1 enable the device output.
7	MODE	I	Operation mode selection pin. MODE = high, the device is in forced PWM mode and keeps the switching frequency constant across the whole load range, regardless of what the FPWM bit is set to MODE = low, the device work mode depends on the FPWM bit (bit = 0: auto PFM mode; bit = 1: FPWM mode).
8	ADDR	I	I^2C target address set pin. See also Table 6-2.
9	SDA	I/O	I^2C serial interface data. Pull this pin up to the I^2C bus voltage with a resistor.
10	SCL	I	I^2C serial interface clock. Pull this pin up to the I^2C bus voltage with a resistor.
11	COMP	O	Output of the internal error amplifier. The loop compensation network must be connected between this pin and GND.
12	FB	I	Output voltage feedback. A resistor divider connecting to this pin sets the default output voltage.
13	GND	—	Ground

(1) PWR = power, I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range at terminals(2)	BST	–0.3	SW + 6	V
Voltage range at terminals(2)	SW, VOUT	-0.3	19	V
Voltage range at terminals(2)	VIN, EN, COMP, FB, MODE, ADDR, SDA, SCL	–0.3	6	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network ground terminal.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ (1)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(2)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(3)	±500	

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500V HBM is possible with the necessary precautions.
(3) Level listed above is the passing level per ANSI/ESDA/JEDEC JS-002. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250V CDM is possible with the necessary precautions.

5.3 Recommended Operating Conditions

Over operating free-air temperature range unless otherwise noted.

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.7		5.5	V
V_{OUT}	Output voltage	5		16	V
T_J	Operating junction temperature	–40		125	°C

5.4 Thermal Information

THERMAL METRIC[1]		TPS61371 VAR - 14 PINS Standard	TPS61371 VAR - 14 PINS EVM[2]	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	75.44	55.81	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.38	NA	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25.04	NA	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.75	3.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	25.1	26.58	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) Measured on TPS61371EVM, 4-layer, 2oz copper 60mm × 47mm PCB.

5.5 Electrical Characteristics

V_{IN} = 2.7V to 5.5V and V_{OUT} = 5V to 16V, T_J = -40°C to 125°C , Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage range		2.7		5	V
V_{IN_UVLO}	Input voltage undervoltage lockout (UVLO) threshold, rising	V_{OUT} = 12V, T_J = - 40 °C to 12°C		2.55	2.7	V
	Input voltage undervoltage lockout (UVLO) threshold, falling			2.40	2.5	V
V_{POR_UVLO}	Positive-going POR threshold voltage	V_{OUT} = 12V, T_J = - 40°C to 125°C	1.73	2.0	2.28	V
V_{POR_UVLO}	Negative-going POR threshold voltage	V_{OUT} = 12V, T_J = - 40°C to 125°C	1.65	1.90	2.16	V
V_{POR_UVLO}	POR threshold voltage hysteresis	V_{OUT} = 12V, T_J = - 40°C to 125°C		100		mV
I_{Q_VIN}	Quiescent current into VIN pin	IC enabled, no switching, V_{IN} = 2.7V to 5.5V, V_{OUT} = 5V to 16V, T_J = – 40°C to 85°C		125	165	µA
I_{Q_VOUT}	Quiescent current into VOUT pin	IC enabled, no switching, V_{IN} = 2.7V, V_{OUT} = 5V to 16V, T_J = – 40°C to 85°C		10	26	µA
I_{SD_VIN}	Shutdown current from VIN to GND	V_{IN} = 2.7V to 5.5V, V_{OUT} = SW = 0V, EN = 0, T_J = - 40°C to 85°C		0.85	2.5	µA
I_{SD_VIN}	Shutdown current from VIN to GND	V_{IN} = 3.3V, V_{OUT} = SW = 0V, EN = 0, T_J = - 40°C to 85°C		0.85	1.5	µA
I_{SD_SW}	Shutdown current from SW to GND and VOUT	SW = V_{IN} = 3.3V, V_{OUT} = 0 V, EN = 0 , T_J = - 40 °C to 85 °C		0.01	2	µA
OUTPUT VOLTAGE						
V_{OUT}	Output voltage range		4.5		16	V
V_{REF}	Reference voltage on FB pin		0.324		0.959	V
V_{REF}	Minimum Reference voltage on FB pin		0.319	0.324	0.329	V
V_{REF}	Maximum Reference voltage on FB pin		0.944	0.959	0.974	V
V_{REF}	Default Reference voltage on FB pin		0.585	0.594	0.603	V
	AUTO PFM mode Vref=default	V_{IN} = 4V, V_{OUT} = 12V, T_J = 25°C		1.016		Vref
I_{FB_LKG}	Leakage current into FB pin				30	nA
V_{REF_SLEW}	Reference_Slew Rate	Bit = 0	3.366	3.96	4.554	mV/10uS
V_{REF_SLEW}	Reference_Slew Rate	Bit = 1	5.61	6.60	7.59	mV/10uS
$R_{DISCHARGE}$	Output discharge resistor	EN_DISCH_VOUT_R Bit=01	80	100	120	Ω
$R_{DISCHARGE}$	Output discharge resistor	EN_DISCH_VOUT_R Bit=10	240	300	360	Ω
POWER SWITCHES						
$T_{DISCHARGE}$	Output discharge delay time	0x01[4:3] = 00	35	50	70	µs
$T_{DISCHARGE}$	Output discharge delay time	0x01[4:3] = 01	70	100	140	µs
$T_{DISCHARGE}$	Output discharge delay time	0x01[4:3] = 10	105	150	210	µs
$T_{DISCHARGE}$	Output discharge delay time	0x01[4:3] = 11	140	200	280	µs

5.5 Electrical Characteristics (continued)

V_{IN} = 2.7V to 5.5V and V_{OUT} = 5V to 16V, T_J = -40°C to 125°C , Typical values are at T_J = 25°C, unless otherwise noted.

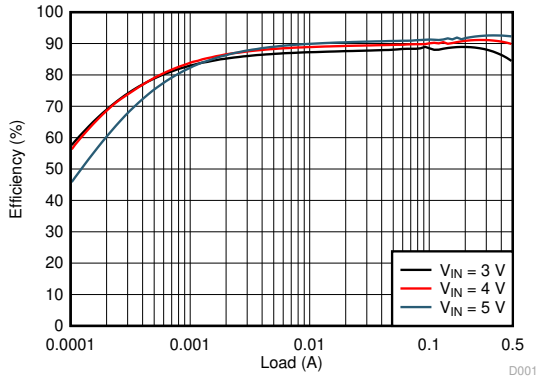
PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$R_{DS(on)}$	Low-side FET on resistance	V_{IN} = 3.3V, V_{OUT} = 12V, T_J = 25°C		35		mΩ
	High-side + Dis connect FET on resistance	V_{IN} = 3.3V, V_{OUT} = 12V, T_J = 25°C		106		mΩ
CURRENT LIMIT						
I_{LIM}	Current Limit (Auto PFM)	V_{IN} = 3V to 4.5V, V_{OUT} = 5V to 16V, T_J = -40°C to 125°C	3.4	3.8	4.3	A
	Current Limit (Forced PWM)	V_{IN} = 3V to 4.5V, V_{OUT} = 5V to 16V, T_J = -40°C to 125°C	3.28	3.6	4.0	A
EN, MODE, SDA, SCL, ADDR LOGICS						
V_{IH}	EN, MODE pin high level input voltage				1.2	V
V_{IL}	EN, MODE pin low level input voltage		0.4			V
V_{HYS}	EN, MODE pin Hysteresis			100		mV
V_{IH}	ADDR, SDA, SCL pin high level input voltage				1.2	V
V_{IL}	ADDR, SDA, SCL pin low level input voltage		0.4			V
$T_{DEGLITCH}$	EN, MODE deglitch time rising / falling	V_{IN} = 3.3V, V_{OUT} = 12V, T_J = 25°C		13		µs
R_{PD}	EN, MODE pulldown resistor	V_{IN} = 3.3V, V_{OUT} = 12V, T_J = 25°C		800		kΩ
SWITCHING CHARACTER						
f_{SW}	Switch frequency	V_{IN} = 3V to 4.5V, V_{OUT} = 5V to 12V, T_J = -40°C to 125°C	1.2	1.5	1.7	MHz
f_{SW_FOLD}	Switch frequency foldback	V_{IN} = 3.3V, T_J = -40°C to 125°C	470	535	600	kHz
V_{FSW_LOW}	Threshold for fsw foldback (1.5 MHz normal)	V_{IN} = 3.3V, T_J = -40°C to 125°C	15%	20%	25%	%
$V_{FSW\_LOW\_HSY}$	Hysteresis for fsw foldback	V_{IN} = 3.3V, T_J = 25°C		150		mV
TIMING						
t_{ON_MIN}	Minimum on time	V_{IN} = 3.3V, T_J =-40°C to 125°C		75	95	ns
t_{SS}	Soft-start time	V_{IN} = 3.3V, V_{OUT} = 12V, T_J = 25°C	1.2	1.5	1.8	ms
t_{SCP}	SCP deglitch time	V_{IN} = 3.3V, V_{OUT} = 12V, T_J = 25°C		135		µs
ERROR AMPLIFIER						
V_{COMPH}	COMP output high voltage Auto PFM	V_{IN} = 3.3V, V_{OUT} = 12V, T_J = 25°C, V_{FB} = V_{REF} - 200mV		1.4		V
	COMP output high voltage Forced PWM	V_{IN} = 3.3V, V_{OUT} = 12V, T_J = 25°C, V_{FB} = V_{REF} - 200mV		1.5		V
V_{COMPL}	COMP output low voltage Auto PFM	V_{IN} = 3.3V, V◦$_{OUT}$ = 12V, T_J = 25°C, V_{FB} = V_{REF} + 200mV		0.8		V
	COMP output low voltage Forced PWM	V_{IN} = 3.3V, V_{OUT} = 12V, T_J = 25°C, V_{FB} = V_{REF} + 200mV		0.6		V
Gm	Error amplifier trans conductance	V_{IN} = 3.3V, V_{OUT} = 12V, T_J = 25°C		175		µs
I_{SINK_EA}	Sink current of COMP	V_{IN} = 3.3V, T_J = 25°C, V_{FB} = V_{REF} + 200mV		20		µA
I_{SOURCE_EA}	Source current of COMP	V_{IN} = 3.3V, T_J = 25°C, V_{FB} = V_{REF} - 200mV		20		µA
PROTECTION						
V_{REF_OVP}	Reference Overvoltage protection	V_{IN} = 2.7V to 5.5V, T_J = -40°C to 125°C	1.20	1.25	1.30	Vref
V_{OUT_OVP}	Output overvoltage protection threshold	V_{IN} = 2.7V to 5.5V, T_J = -40°C to 125°C	16.5	17.3	18	V
THERMAL						
T_{SD}	Thermal shutdown threshold	V_{IN} = 3.3V, V_{OUT} = 12V		150		C
T_{SD_HYS}	Thermal shutdown hysteresis	V_{IN} = 3.3V, V_{OUT} = 12V		20		C

5.6 I2C Timing Requirements

T_J = -40°C to 150°C, V_{CC} = 5V. Typical values are at T_J = 25°C, unless otherwise noted.

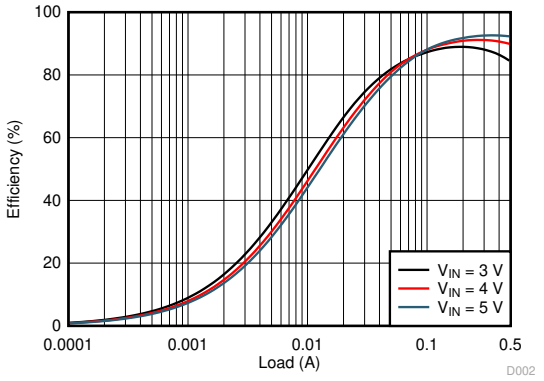
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I2C TIMING						
f_{SCL}	SCL clock frequency		100		1000	kHz
t_{BUF}	Bus free time between a STOP and START condition	Fast mode plus	0.5			µs
$t_{HD(STA)}$	Hold time (repeated) START condition		260			ns
t_{LOW}	Low period of the SCL clock		0.5			µs
t_{HIGH}	High period of the SCL clock		260			ns
$t_{SU(STA)}$	Setup time for a repeated START condition		260			ns
$t_{SU(DAT)}$	Data setup time		50			ns
$t_{HD(DAT)}$	Data hold time		0			µs
t_{RCL}	Rise time of SCL signal				120	ns
t_{RCL1}	Rise time of SCL signal after a repeated START condition and after an ACK bit				120	ns
t_{FCL}	Fall time of SCL signal				120	ns
t_{RDA}	Rise time of SDA signal				120	ns
t_{FDA}	Fall time of SDA signal				120	ns
$t_{SU(STO)}$	Setup time of STOP condition		260			ns
C_B	Capacitive load for SDA and SCL				200	pF

5.7 Typical Characteristics



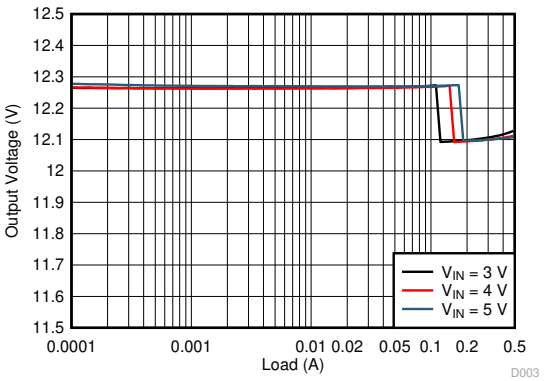
V_{OUT} = 11V L = 1µH Auto PFM

Figure 5-1. Efficiency vs Load



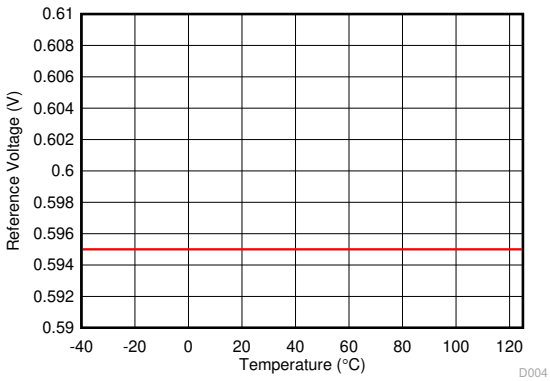
V_{OUT} = 11V L = 1µH Forced PWM

Figure 5-2. Efficiency vs Load



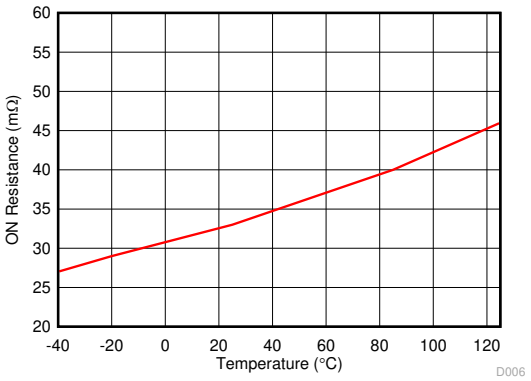
V_{OUT} = 12V L = 1µH Auto PFM

Figure 5-3. Load Regulation



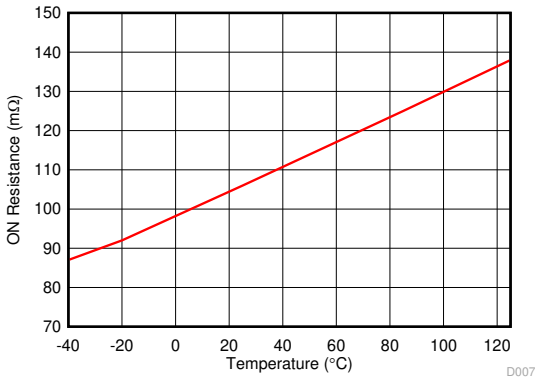
V_{IN} = 4V

Figure 5-4. Reference Voltage vs Temperature



V_{IN} = 4V V_{OUT} = 11V

Figure 5-5. Low-Side RDS_{ON} vs Temperature



V_{IN} = 4V V_{OUT} = 11V

Figure 5-6. High-side RDS_{ON} vs Temperature

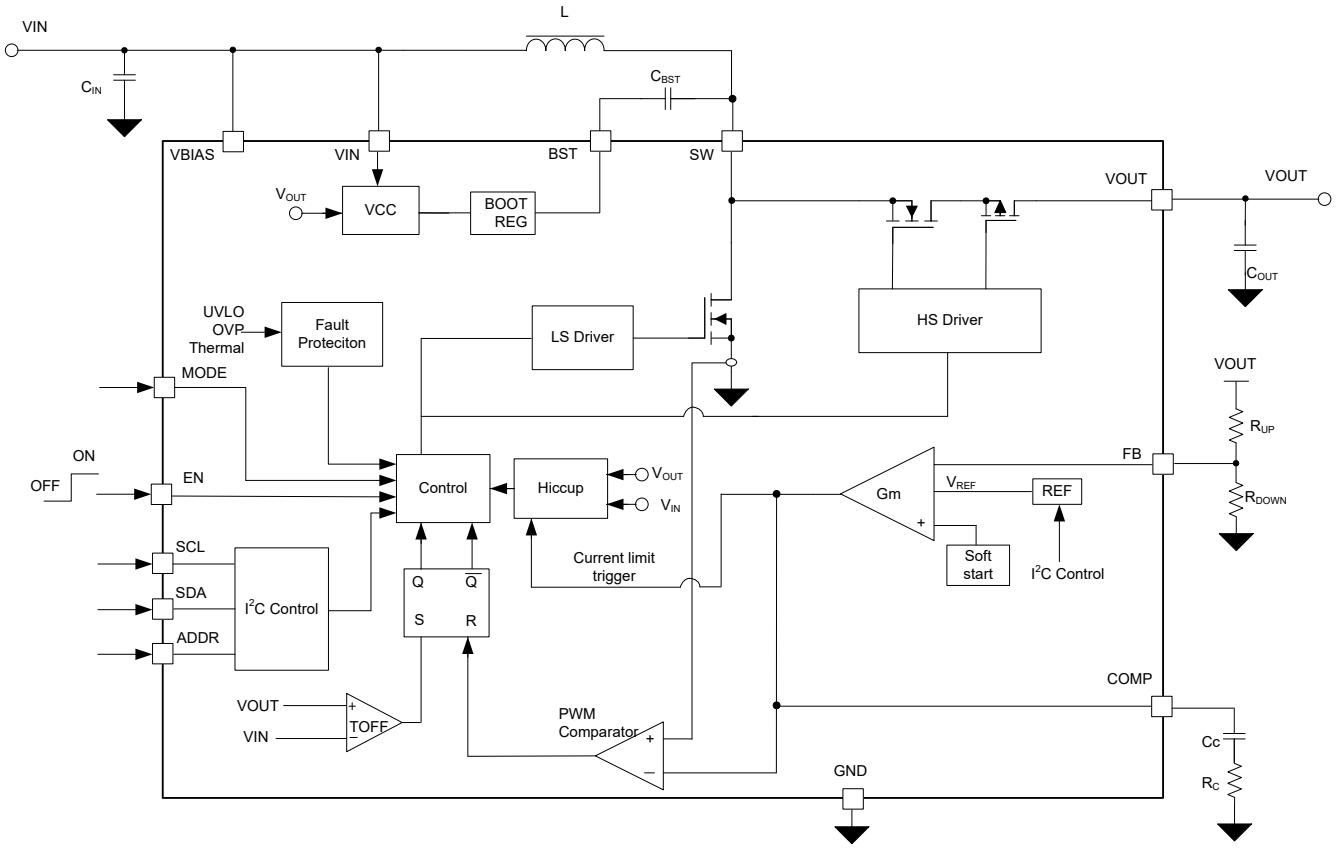
6 Detailed Description

6.1 Overview

The TPS61371 is a highly-integrated, synchronous boost converter to support 16V output with load disconnect and short protection built-in. The TPS61371 supports input voltage ranging from 2.7V to 5.5V. The TPS61371 uses the peak current mode with adaptive off-time control topology to regulate the output voltage. The TPS61371 operates at a quasi-constant frequency pulse width modulation (PWM) at moderate to heavy load current. At the beginning of each cycle, the low-side FET turns on and the inductor current ramps up to reach a peak current determined by the output of the error amplifier (EA). When the peak current preset value determined by the output trips of the EA, the low-side FET turns off. As long as the low-side FET turns off, the high-side FET turns on after a short delay time to avoid the shoot through. The duration of low-side FET off state is determined by the V_{IN} / V_{OUT} ratio.

High efficiency is achieved at light load as the TPS61371 operates in PFM operation. The device can be also configured at forced PWM mode to keep the frequency constant across the whole load range and to have more immunity against noise sensitive applications. The work mode depends on the FPWM bit in the CONTROL register. See also the FPWM bit in Table 7-3 for detailed I^2C settings.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Undervoltage Lockout

The undervoltage lockout (UVLO) circuit prevents the device from malfunctioning at the low input voltage of the battery from the excessive discharge. The device is ready to operate after the rising V_{IN} trips the UVLO threshold and disables the output stage of the converter once V_{IN} is below the UVLO falling threshold.

The status of the I^2C programing interface is decided only by the V_{IN}. That is, regardless of the status of the EN pin and CONVERTEN_EN.

- The I^2C programing interface is active after V_{IN} is higher than UVLO.
- The programing interface is inactive and all the I^2C registers are cleared and reset to the default values after V_{IN} is lower than UVLO.

6.3.2 Enable and Disable

When the input voltage is above the UVLO threshold, both the EN pin and the CONVERTER_EN register bit determine the output state. The default CONVERTER_EN bit is 1. See the Table 6-1 for detailed settings.

Table 6-1. EN Configuration Table

VIN	EXTERNAL EN PIN	CONVERTER_EN	DEVICE STATE	OUTPUT STATE
Below UVLO	x	x	Device disable	No output
Above UVLO	Low	0	I^2C programming interface active	No output
Above UVLO	Low	1	I^2C programming interface active	No output
Above UVLO	High	0	I^2C programming interface active	No output
Above UVLO	High	1	Device active	Output enabled

6.3.3 Output Voltage Setting

There are two ways to adjust the output voltage: change the feedback resistor divider and change the reference voltage.

- When using an external output voltage feedback resistor divider, use Equation 1 to calculate the output voltage with the reference voltage V_{ref} at the FB pin.

$$V_{OUT} = V_{ref} \times \left(1 + \frac{R_{UP}}{R_{DOWN}}\right) \quad (1)$$

- The TPS61371 has a 7-bit DAC to adjust the V_{ref} by I^2C control. The adjustable V_{ref} range is 0.324V to 0.959V with a minimum step of 5mV. The default V_{ref} is 0.594V. See Table 7-5 for the detailed VREF setting.

When the VO_Falling discharge bit is enabled, an additional dummy 100Ω resistor load is added at output, so that the output voltage rising and falling slew rate are same even with no load. After the output voltage reach the new target value, the discharge resistor is removed automatically.

6.3.4 Reference Voltage Slew Rate

The customer can program the output voltage by adjusting the reference voltage through the I2C interface. Two V_{ref} slew rates are available, controlled by the REFERENCE_SLEW_RATE bit in the CONTROL register.

- When REFERENCE_SLEW_RATE = 0, Vref slew rate = 3.96mV/10µs
- When REFERENCE_SLEW_RATE = 1, Vref slew rate = 6.60mV/10µs

The default value of REFERENCE_SLEW_RATE is 0.

When V_{OUT} is changed by adjusting V_{ref}, the actual V_{OUT} slew rate is affected not only by the V_{ref} slew rate, but also by the output capacitor, load current and loop response speed.

6.3.5 Error Amplifier

The TPS61371 has a transconductance amplifier and compares the feedback voltage with the internal voltage reference (or the internal soft-start voltage during start-up phase). The transconductance of the error amplifier is

175µA/V typically. The loop compensation components are placed between the COMP terminal and ground to optimize the loop stability and response speed.

6.3.6 Bootstrap Voltage (BST)

The TPS61371 has an integrated bootstrap regulator and requires a small ceramic capacitor between the BST and SW pin to provide the gate drive voltage for the high-side FET. The recommended value for this ceramic capacitor is between 20nF to 200nF.

6.3.7 Load Disconnect

The TPS61371 provides a load disconnect function, which completely disconnects the output from the input during shutdown or fault conditions.

6.3.8 Output Discharge

The TPS61371 provides a resistive path to quickly discharge output when the EN pin is logic low or the CONVERTER_EN bit is set to 0 or trigger VIN_UVLO. With this function, the VOUT is connected to ground through an internal resistor, preventing the output from “floating” or entering into an undetermined state. The output discharge function makes the power on and off sequencing smooth. Pay attention to the output discharge function if use this device in applications such as power multiplexing, because the output discharge circuitry creates a constant current path between the multiplexer output and the ground.

Output discharge is controlled by the two bits designated DISCHARGE_VOUT. Output discharge can be disabled or enabled with two different discharge resistors. The default DISCHARGE_VOUT bits are 0b00, which means the discharge function is disabled. Please refer to the DISCHARGE_VOUT bits in Table 7-3 for detailed I^2C settings.

Four output discharge delay times are available, controlled by the DISCHARGE DELAY TIME bits in the CONTROL register.

- When DISCHARGE DELAY TIME = 00, delay time = 50µs
- When DISCHARGE DELAY TIME = 01, delay time = 150µs
- When DISCHARGE DELAY TIME = 10, delay time = 100µs
- When DISCHARGE DELAY TIME = 11, delay time = 200µs

The default value of DISCHARGE DELAY TIME is 00.

6.3.9 Overvoltage Protection

The TPS61371 provides latching FB overvoltage protection. If the FB pin voltage exceeds 1.25 × V_{REF} (typical), the TPS61371 stops switching after a deglitch time (2µs typical), until EN logic or VIN_UVLO is reset.

The latching FB overvoltage protection detection is blocked when changing the output from a high target to a low target by I^2C.

The TPS61371 also provides a latching fixed overvoltage protection. If the output voltage is detected above the overvoltage protection threshold (typically 17.3V), the TPS61371 stops switching immediately (no deglitch time) until EN logic or VIN_UVLO is reset. This function prevents the devices against the overvoltage and secures the circuits connected with the output of excessive overvoltage.

6.3.10 Thermal Shutdown

A thermal shutdown is implemented to prevent the damage due to the excessive heat and power dissipation. Typically, the thermal shutdown occurs at the junction temperature exceeding 150°C (typical). When the thermal shutdown is triggered, the device stops switching and recovers when the junction temperature falls below 130°C (typical).

6.3.11 Start-Up

The TPS61371 implements the soft-start function to reduce the inrush current during start-up. The TPS61371 begins soft start when the EN pin is pulled high. There are two phases for the start-up procedure:

- When V_{OUT} is below 120% V_{IN}, the output voltage ramps up with the switching frequency of 535kHz (typical).
- When V_{OUT} exceeds 120% V_{IN}, the switching frequency changes to 1.5MHz typically and ramps up the output voltage to the setpoint.

6.3.12 Short Protection

The TPS61371 provides latching output short protection. After the 135µs duration of current limit is triggered and the V_{OUT} is pulled below 105% V_{IN}, the TPS61371 immediately stops switching until EN logic or VIN_UVLO is reset. See Figure 6-1.

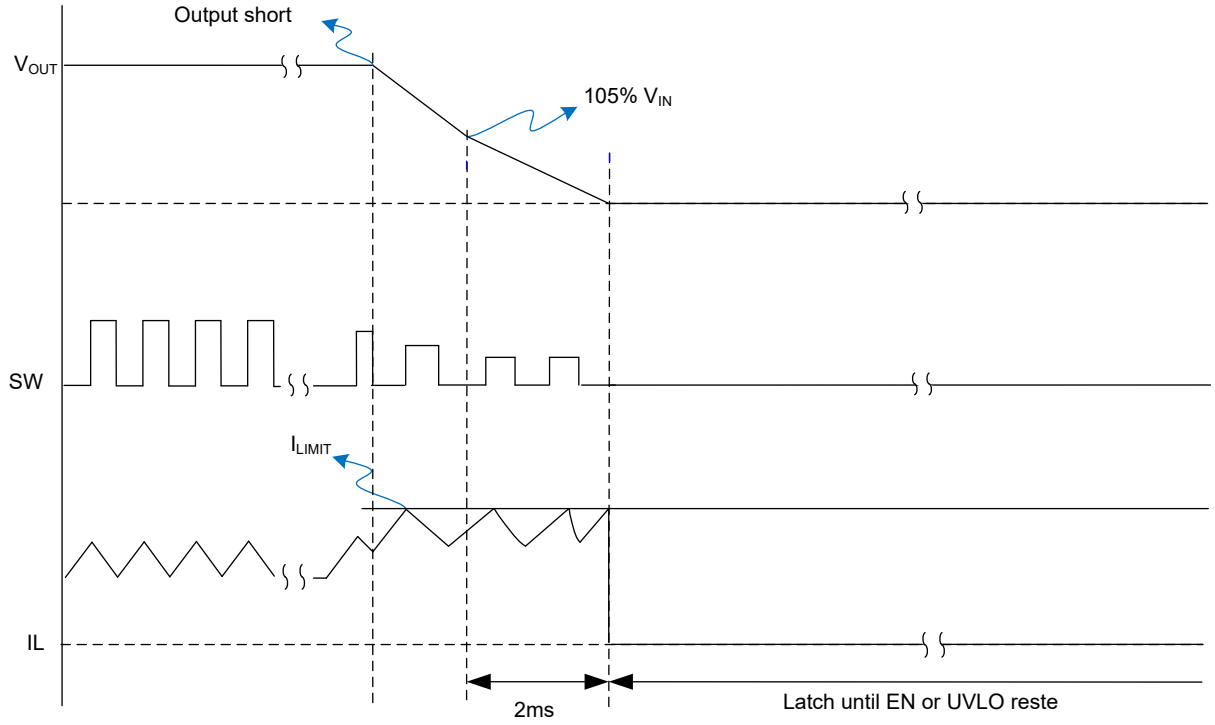


Figure 6-1. Short Protection Behavior

6.4 Device Functional Modes

6.4.1 Operation

In light load condition, the TPS61371 can be configured at auto PFM or forced PWM. At auto PFM operation, the switching frequency is lowered at light load and features higher efficiency, while for forced PWM operation, the frequency keeps constant across the whole load range.

6.4.2 Auto PFM Mode

The TPS61371 integrates a power-save mode with pulse frequency modulation (PFM) at light load (set the mode pin low logic and set the FPWM bit = 0). The device skips the switching cycles and regulates the output voltage at a higher threshold (typically 101.6% × V_{OUT_NORM}). Figure 6-2 shows the working principle of the PFM operation. The auto PFM mode reduces the switching losses and improves efficiency at light load condition by reducing the average switching frequency.

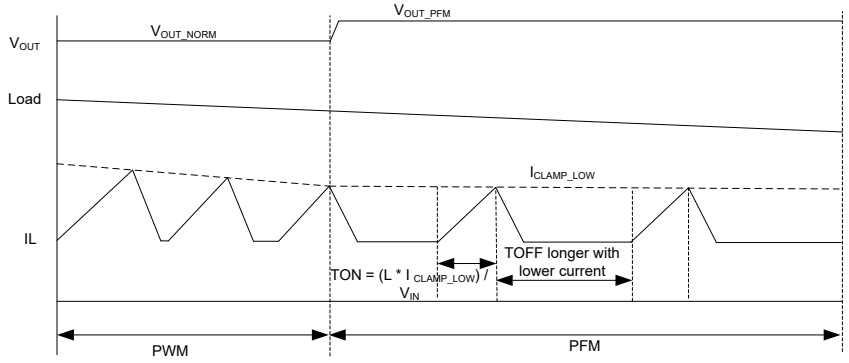


Figure 6-2. Auto PFM Operation Behavior

6.4.3 Forced PWM Mode

In forced PWM mode, the TPS61371 keeps the switching frequency constant across the whole load range. When the load current decreases, the output of the internal error amplifier decreases as well to lower the inductor peak current and delivers less power. The high-side FET is not turned off even if the current through the FET goes negative to keep the switching frequency be the same as that of the heavy load.

6.4.4 Mode Selectable

There is a MODE pin to configure the TPS61371 into two different operation modes. The device works in forced PWM mode when mode pin is high. When the MODE pin is pulled to low, the work mode depends on the FPWM bit in the CONTROL register. See also the FPWM bit in Table 7-3 for detailed I^2C settings.

6.5 Programming

6.5.1 Serial Interface Description

I^2C is a 2-wire serial interface developed by Philips Semiconductor, now NXP Semiconductors (see *NXP Semiconductors, UM10204 – I^2C-Bus Specification and User Manual*). The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I^2C-compatible devices connect to the I^2C bus through open-drain I/O pins, SDA, and SCL. A controller device, typically a microcontroller or a digital signal processor, controls the bus. The controller is responsible for generating the SCL signal and device addresses. The controller also generates specific conditions that indicate the START and STOP of data transfer. A target device receives and transmits data on the bus under control of the controller device.

The device works as a target and supports the following data transfer modes, as defined in the I^2C-Bus Specification:

- Standard-mode (100Kbps)
- Fast-mode (400Kbps)
- Fast-mode Plus (1Mbps)

The interface adds flexibility to the power supply design, enabling most functions to be programmed to new values, depending on the instantaneous application requirements. Register contents remain intact as long as supply voltage remains above $V_{IT+(POR)}$.

The data transfer protocol for standard and fast modes is exactly the same, therefore, the protocol is referred to as F/S-mode in this document. The device supports 7-bit addressing; 10-bit addressing and general call address are not supported. The device 7-bit address is programmable by ADDR pin.

To make sure that the I^2C function in the device is correctly reset, TI recommends that the I^2C controller initiates a STOP condition on the I^2C bus after the initial power up of SDA and SCL pullup voltages.

6.5.2 Standard-, Fast-, and Fast-Mode Plus Protocol

The controller initiates a data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 6-3. All I^2C-compatible devices recognize a start condition.

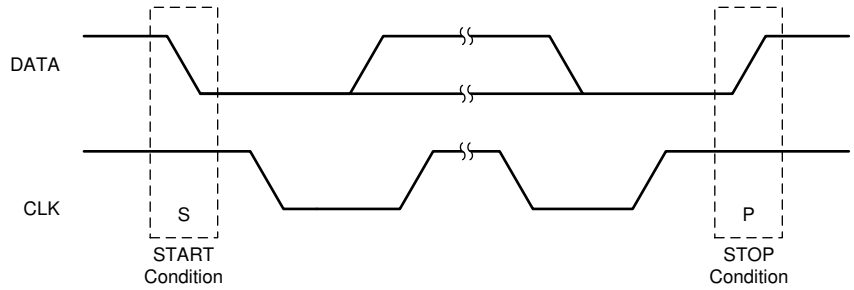


Figure 6-3. START and STOP Conditions

The controller then generates the SCL pulses and transmits the 7-bit address and the read/write direction bit, R/W, on the SDA line. During all transmissions, the controller makes sure that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 6-4). All devices recognize the address sent by the controller and compare to the internal fixed addresses. Only the target device with a matching address generates an acknowledge (see Figure 6-5) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the controller knows that communication link with a target has been established.

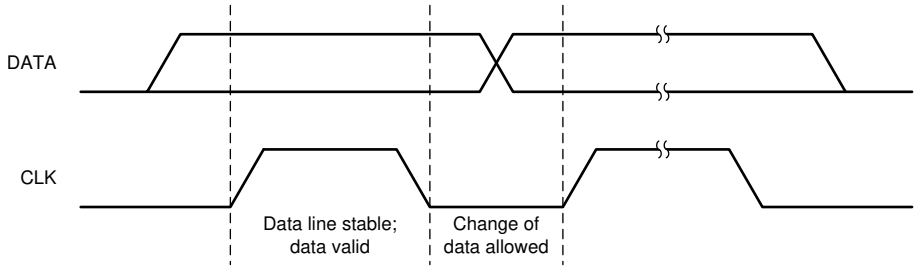


Figure 6-4. Bit Transfer on the Serial Interface

The controller generates further SCL cycles to either transmit data to the target (R/W bit 1) or receive data from the target (R/W bit 0). In either case, the receiver must acknowledge the data sent by the transmitter. An acknowledge signal can either be generated by the controller or by the target, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the controller generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 6-3). This low level to high level transition on the SDA line when the SCL is at high releases the bus and stops the communication link with the addressed target. All I^2C-compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released and the devices wait for a start condition followed by a matching address.

Attempting to read data from register addresses not listed in this section results in 00h being read out.

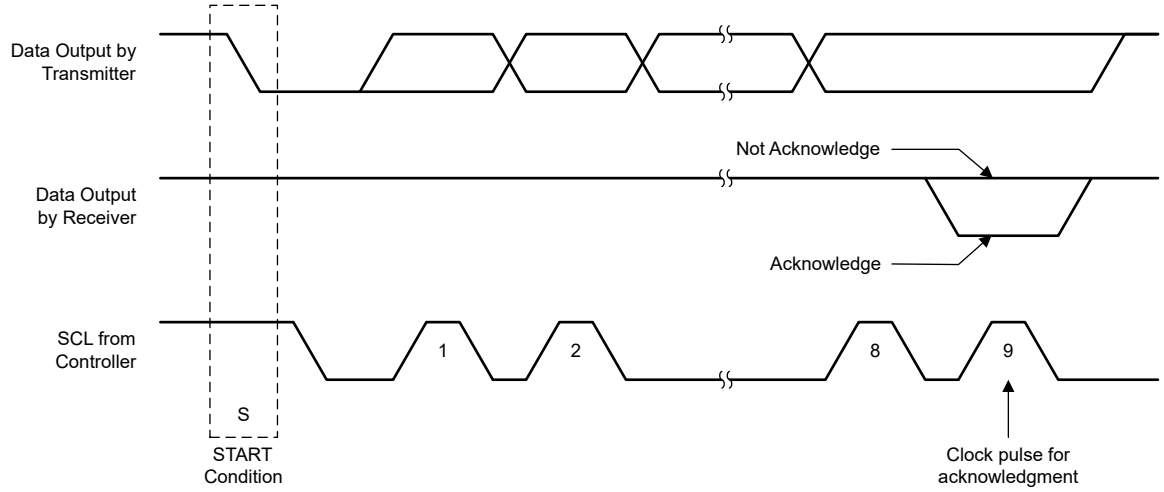


Figure 6-5. Acknowledge on the I²C Bus

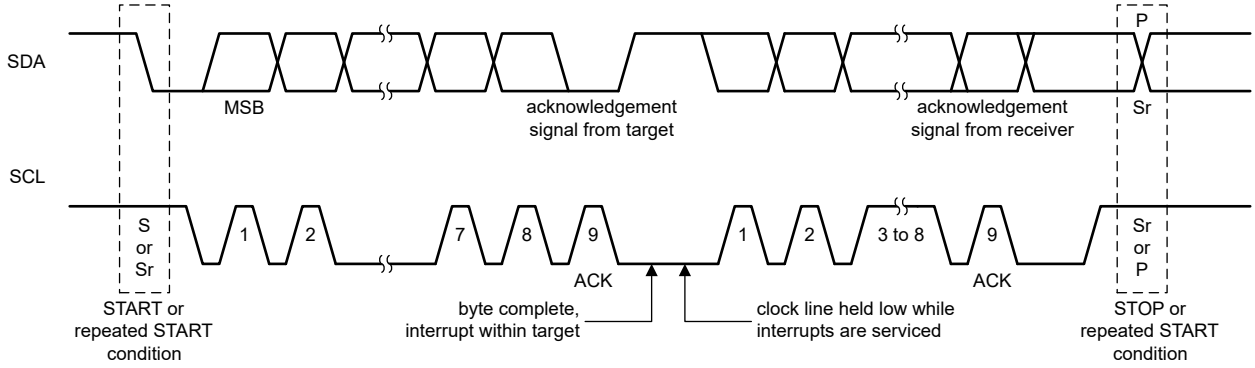


Figure 6-6. Bus Protocol

6.5.3 I²C Update Sequence

A single update requires the following:

- A start condition
- A valid I²C target address
- A register address
- A data byte

To acknowledge the receipt of each byte, the device pulls the SDA line low during the high period of a single clock pulse. The device performs an update on the falling edge of the acknowledge signal that follows the last byte.

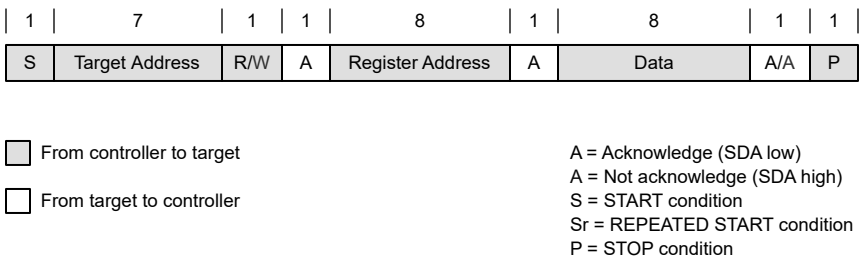


Figure 6-7. "Write" Data Transfer Format in Standard, Fast, and Fast-Plus Modes

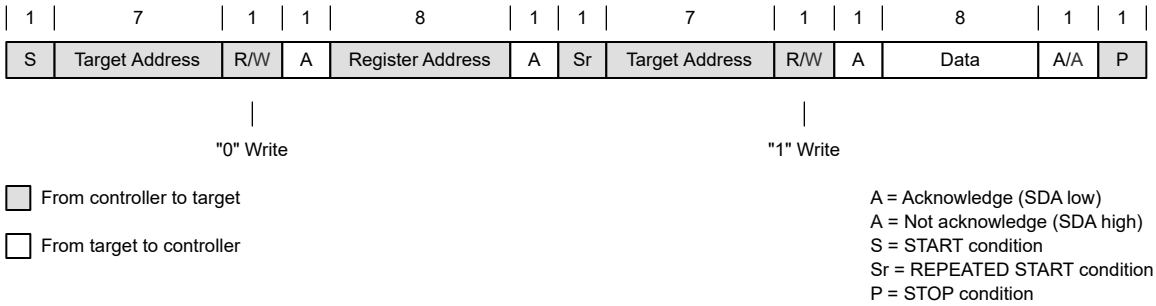


Figure 6-8. “Read” Data Transfer Format in Standard, Fast, and Fast-Plus Modes

6.5.4 I²C Target Address

6.5.4.1 I²C Target Address Description

By setting the ADDR pin to three different states: high, floating, or low, three I²C target addresses of the TPS61371 can be configured: 0x72, 0x73 or 0x74. Table 6-2 shows the detailed ADDR pin states and the corresponding I²C target address.

Table 6-2. I²C Target Addresses

ADDR PIN STATES	ADDR PIN VOLTAGE	I2C TARGET ADDRESS
High	1.2V to 5.5V	0x72
Floating		0x73
Low	GND to 0.4V	0x74

7 Register Map

7.1 Register Description

7.1.1 Register Map

Table 7-1. Register Map

ADDRESS	ACRONYM	REGISTER NAME	SECTION
0x01	CONTROL	Control Register	Go
0x02	VOUT	VOUT Register	Go

7.1.2 Register CONTROL (Register address: 0x01; Default: 0x01)

Return to Register Map

Table 7-2. Register CONTROL Format

7	6	5	4	3	2	1	0
NIL[1:0]	FPWM	REFERENCE SLEW RATE	DISCHARGE DELAY TIME		DISCHARGE_VOUT		CONVERTER_EN
R	R/W	R/W	R/W		R/W		R/W

LEGEND: R/W = Read/Write; R = Read only

Table 7-3. Register CONTROL Field Descriptions

Bit	Field	Type	Reset	Description
7	NIL[1:0]	R	0b00	Not used. During write operations data for these bits are ignored. During read operations 0 is returned
6	FPWM	R/W	0b0	Set device work mode ('OR'ed with MODE-pin) 0: Auto PFM mode if MODE pin is logic low. 1: Forced PWM mode if MODE pin is logic low. If MODE pin is high, the device always works in Forced PWM mode
5	REFERENCE SLEW RATE	R/W	0b0	Vref slew rate 0: Slew Rate 0, 3.96mV/10µs 1: Slew Rate 1, 6.60mV/10µs
4:3	DISCHARGE DELAY TIME	R/W	0b00	Delay time of VOUT discharge 00: 50µs 01: 100µs 10: 150µs 11: 200µs
2:1	DISCHARGE _VOUT	R/W	0b00	Set the VOUT discharge resistance 00: DISABLE 01: 100Ω 10 or 11: 300Ω
0	CONVERTER_EN	R/W	0b1	Enable converter ('AND'ed with EN-pin) 0: DISABLE 1: ENABLE

7.1.3 Register VOUT (Register address: 0x02; Default: 0x36)

Return to Register Map

Table 7-4. Register VOUT Format

7	6	5	4	3	2	1	0
VO_Falling discharge	Vref[6:0]						
R/W	R/W						

LEGEND: R/W = Read/Write; R = Read only

Table 7-5. Register VOUT Field Descriptions

Bit	Field	Type	Reset	Description
7	VO_Falling discharge	R/W	0b0	VO_Falling discharge set bit. 0: DISABLE 1: ENABLE (discharge resistor 100Ω)
6:0	Vref[6:0]	R/W	0x36	These bits set the reference voltage Reference voltage = 0.324V + Vref[6:0] × 0.005V

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS61371 is a synchronous boost converter. The following design procedure can be used to select component values for the TPS61371. This section presents a simplified discussion of the design process.

8.2 Typical Application

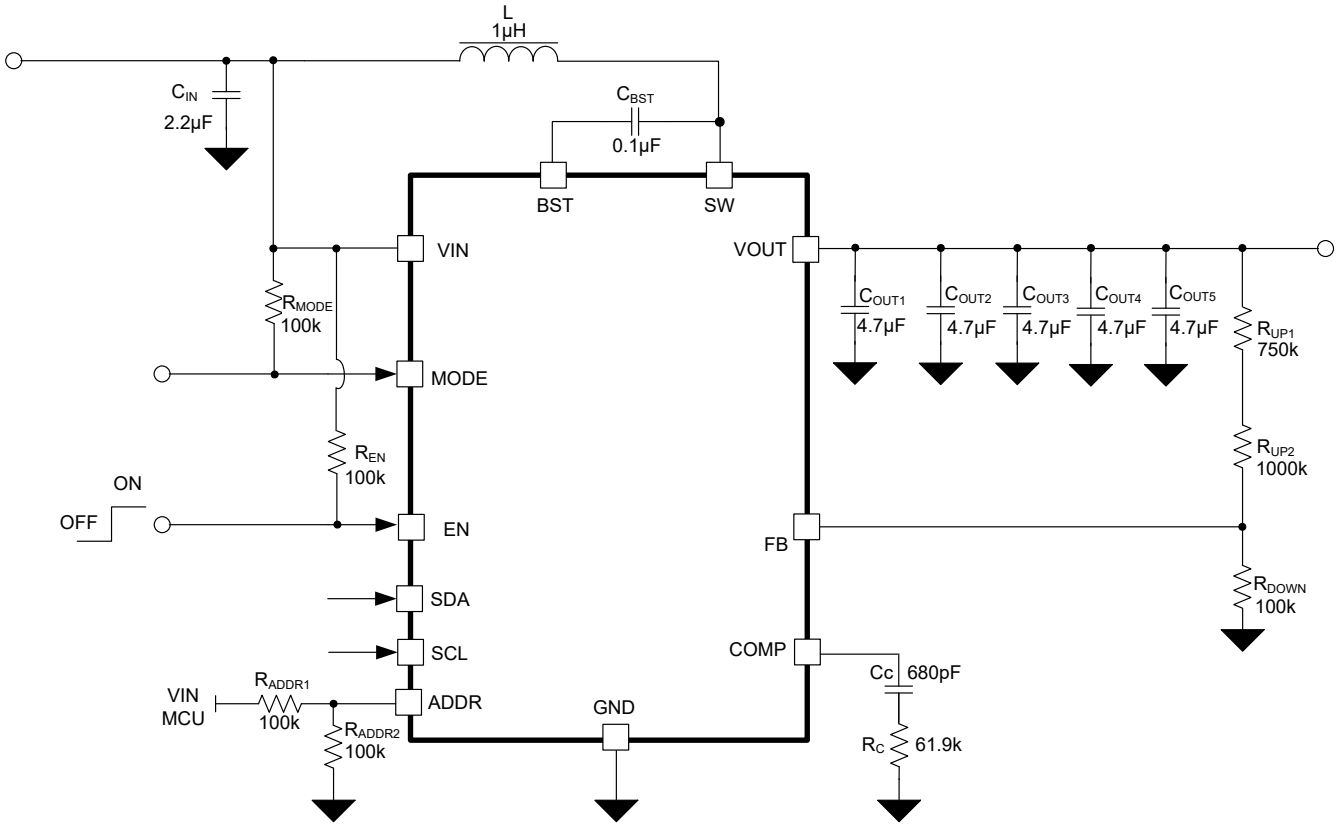


Figure 8-1. TPS61371 11V Output With Load Disconnect Schematic

8.2.1 Design Requirements

For this design example, use Table 8-1 as the design parameters.

Table 8-1. Design Parameters

PARAMETER	VALUE
Input voltage range	3V to 5V
Output voltage	11V
Output ripple voltage	± 3%
Output current	0.6A
Operating frequency	1.5MHz

8.2.2 Detailed Design Procedure

8.2.2.1 Setting the Output Voltage

The output voltage of the TPS61371 is externally adjustable using a resistor divider network. Use Equation 1 to calculate the relationship between the output voltage and the resistor divider.

where

- V_{OUT} is the output voltage
- R_{UP} is the top divider resistor
- R_{DOWN} is the bottom divider resistor

For the best accuracy, TI recommends R_{DOWN} to be around 100kΩ to ensure that the current following through R_{DOWN} is at least 100 times larger than FB pin leakage current. Changing R_{DOWN} toward the lower value increases the robustness against noise injection. Changing R_{DOWN} toward the higher values reduces the quiescent current for achieving higher efficiency at the light load currents.

8.2.2.2 Selecting the Inductor

A boost converter normally requires two main passive components for storing the energy during power conversion: an inductor and an output capacitor. The inductor affects the steady state efficiency (including the ripple and efficiency) as well as the transient behavior and loop stability, which makes the inductor to be the most critical component in application.

When selecting the inductor, as well as the inductance, the other parameters of importance are:

- The maximum current rating (consider RMS and peak current)
- The series resistance
- Operating temperature

Choosing the inductor ripple current with the low ripple percentage of the average inductor current results in a larger inductance value, maximizes the potential output current of the converter, and minimizes EMI. The larger ripple results in a smaller inductance value and a physically smaller inductor, which improves transient response, but results in potentially higher EMI.

The rule in choosing the inductor is to make sure the inductor ripple current (ΔI_L) is a certain percentage of the average current. Then use Equation 2, Equation 3, and Equation 4 to calculate the inductance:

$$\Delta I_L = \frac{V_{IN} \times D}{L \times f_{SW}} \tag{2}$$

$$\Delta I_{L\_R} = Ripple\,\% \times \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN}} \tag{3}$$

$$L = \frac{1}{Ripple\,\%} \times \frac{\eta \times V_{IN}}{V_{OUT} \times I_{OUT}} \times \frac{V_{IN} \times D}{f_{SW}} \tag{4}$$

where

- Δ_{IL} is the peak-peak inductor current ripple
- V_{IN} is the input voltage
- D is the duty cycle
- L is the inductor
- f_{SW} is the switching frequency
- Ripple% is the ripple ration versus the DC current
- V_{OUT} is the output voltage
- I_{OUT} is the output current
- η is the efficiency

The current flowing through the inductor is the inductor ripple current plus the average input current. During power up, load faults, or transient load conditions, the inductor current can increase above the peak inductor current calculated.

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches the saturation level, the inductance can decrease 20% to 35% from the value at 0A bias current depending on how the inductor vendor defines saturation. When selecting an inductor, make sure the rated current, especially the saturation current, is larger than the peak current during the operation.

The inductor peak current varies as a function of the load, the switching frequency, and the input and output voltages and can be calculated by Equation 5 and Equation 6.

$$I_{PEAK} = I_{IN} + \frac{1}{2} \times \Delta I_L \quad (5)$$

where

- I_{PEAK} is the peak current of the inductor
- I_{IN} is the input average current
- ΔI_L is the ripple current of the inductor

The input DC current is determined by the output voltage, the output current, and efficiency can be calculated by:

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (6)$$

where

- I_{IN} is the input current of the inductor
- V_{OUT} is the output voltage
- V_{IN} is the input voltage
- η is the efficiency

While the inductor ripple current depends on the inductance, the frequency, the input voltage, and duty cycle calculated by Equation 2, replace Equation 2, Equation 6 into Equation 5 to calculate the inductor peak current:

$$I_{PEAK} = \frac{I_{OUT}}{(1-D) \times \eta} + \frac{1}{2} \times \frac{V_{IN} \times D}{L \times f_{SW}} \quad (7)$$

where

- I_{PEAK} is the peak current of the inductor
- I_{OUT} is the output current
- D is the duty cycle
- η is the efficiency
- V_{IN} is the input voltage
- L is the inductor
- f_{SW} is the switching frequency

The heat rating current (RMS) is calculated by Equation 8:

$$I_{L\_RMS} = \sqrt{I_{IN}^{2} + \frac{1}{12}(\Delta I_L)^2} \quad (8)$$

where

- I_{L_RMS} is the RMS current of the inductor
- I_{IN} is the input current of the inductor
- ΔI_L is the ripple current of the inductor

Make sure that the peak current does not exceed the inductor saturation current and the RMS current is not over the temperature related rating current of the inductors.

For a given physical inductor size, increasing inductance typically results in an inductor with lower saturation current. The total losses of the coil consists of the DC resistance (DCR) loss and the following frequency dependent loss:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)

For a certain inductor, the larger current ripple (smaller inductor) generates the higher DC and frequency-dependent loss. An inductor with lower DCR is basically recommended for higher efficiency. However, there is typically a tradeoff between the loss and footprint.

The following inductor series in Table 8-2 from the different suppliers are recommended.

Table 8-2. Recommended Inductors for TPS61371

PART NUMBER	L (µH)	DCR TYP (mΩ) TYP.	SATURATION CURRENT / TYP.	SIZE (L × W × H mm)	VENDOR(1)
PIJT3225FE-1R0MSR	1	40	4.4	3.2 × 2.5 × 0.65	Cyntec
XAL4020-222ME	2.2	35	5.6	4 × 4 × 2	Coilcraft
DFE322512F-2R2M=P2	2.2	66	2.6	3.2 × 2.5 × 1.2	Murata
DFE322520FD-4R7M#	4.7	98	3.4	3.2 × 2.5 × 2.0	Murata

(1) See the *Third-Party Products Disclaimer*.

8.2.2.3 Selecting the Output Capacitors

The output capacitor is mainly selected to meet the requirements at load transient or steady state. Then the loop is compensated for the output capacitor selected. The output ripple voltage is related to the equivalent series resistance (ESR) of the capacitor and the capacitance. Assuming a capacitor with zero ESR, use Equation 9 to calculate the minimum capacitance needed for a given ripple:

$$C_{OUT} = \frac{I_{OUT} \times (V_{OUT} - V_{IN})}{f_{SW} \times \Delta V \times V_{OUT}} \quad (9)$$

where

- C_{OUT} is the output capacitor
- I_{OUT} is the output current
- V_{OUT} is the output voltage
- V_{IN} is the input voltage
- Δ_V is the output voltage ripple required
- f_{SW} is the switching frequency

Use Equation 10 to calculate the additional output ripple component caused by ESR:

$$\Delta V_{ESR} = I_{OUT} \times R_{ESR} \quad (10)$$

where

- ΔV_{ESR} is the output voltage ripple caused by ESR
- R_{ESR} is the resistor in series with the output capacitor

For the ceramic capacitor, the ESR ripple can be neglected. However, for the tantalum or electrolytic capacitors, the ESR ripple must be considered if used.

Care must be taken when evaluating the rating of a ceramic capacitor under the DC bias. Ceramic capacitors can derate by as much as 70% of the capacitance at the rated voltage. Therefore, enough margins on the voltage rating must be considered to make sure adequate capacitance at the required output voltage.

Table 8-3. Recommended Output Capacitor for TPS61371

PART NUMBER	C (µF)	PIECES	DESCRIPTION	SIZE	VENDOR(1)
GRM188R61E106MA73D	10	3	X5R, 0603, 25V, ±20% tolerance	0603	Murata

(1) See the *Third-Party Products Disclaimer*.

8.2.2.4 Selecting the Input Capacitors

Multilayer ceramic capacitors are an excellent choice for the input decoupling of the step-up converter as multilayer ceramic capacitors have extremely low ESR and are available in small footprints. Input capacitors must be located as close as possible to the device.

Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the V_{IN} pin. This ringing can couple to the output and be mistaken as loop instability or can even damage the part. Place additional "bulk" capacitance (electrolytic or tantalum) in this circumstance, between C_{IN} and the power source lead, to reduce ringing that can occur between the inductance of the power source leads and C_{IN}.

8.2.2.5 Loop Stability and Compensation

8.2.2.5.1 Small Signal Model

The TPS61371 uses the peak current with adaptive off-time control topology. With the inductor current information sensed, the small-signal model of the power stage reduces from a two-pole system, created by L and C_{OUT}, to a single-pole system, created by R_{OUT} and C_{OUT}. An external loop compensation network connecting to the COMP pin of TPS61371 is added to optimize the loop stability and the response time, a resistor R_C, capacitor C_C, and C_P shown in Figure 8-2 comprises the loop compensation network.

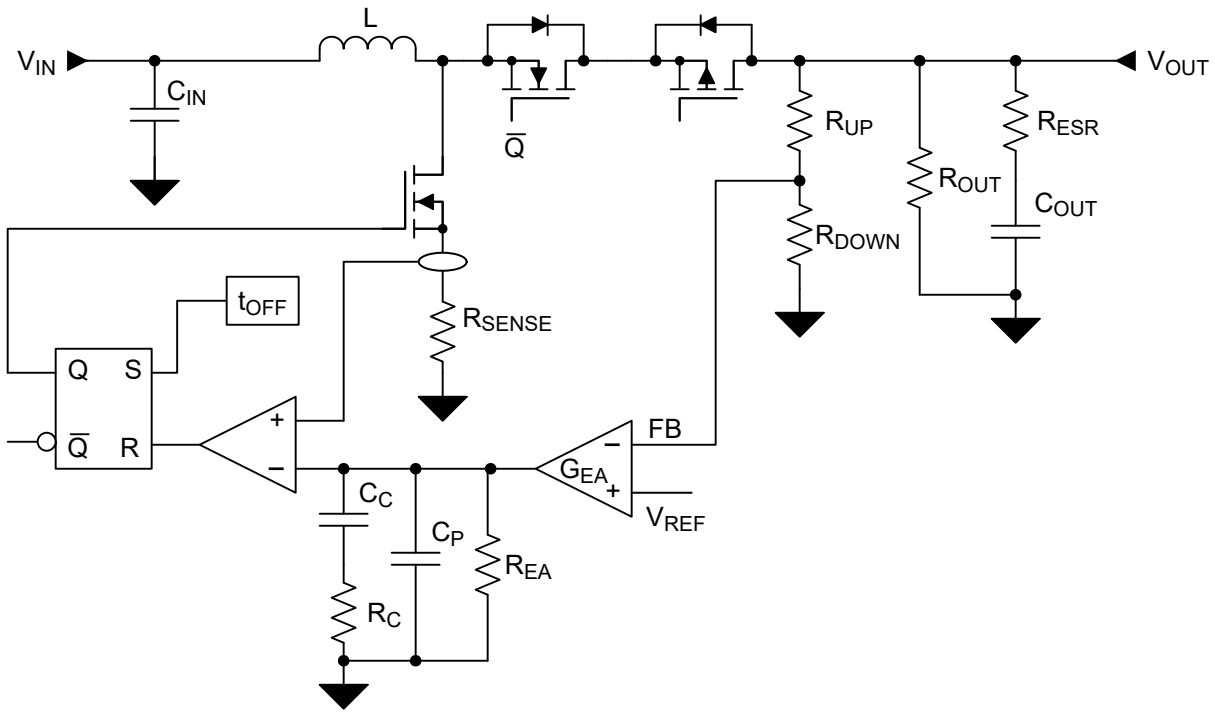


Figure 8-2. TPS61371 Control Equivalent Circuitry Model

The small signal of power stage is:

$$G_{PS}\left(S\right) = \frac{R_{OUT} \times (1 - D)}{2 \times R_{SENSE}} \times \frac{\left(1 + \frac{S}{2 \times \pi \times f_{ESR}}\right)\left(1 - \frac{S}{2 \times \pi \times f_{RHP}}\right)}{1 + \frac{S}{2 \times \pi \times f_P}} \quad (11)$$

where

- D is the duty cycle
- R_{OUT} is the output load resistor
- R_{SENSE} is the equivalent internal current sense resistor, which is typically 0.2Ω of TPS61371

The single pole of the power stage is:

$$f_P = \frac{2}{2\pi \times R_{OUT} \times C_{OUT}} \quad (12)$$

where

- C_{OUT} is the output capacitance, for a boost converter having multiple, identical output capacitors in parallel, simply combine the capacitors with the equivalent capacitance

The zero created by the ESR of the output capacitor is:

$$f_{ESR} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \quad (13)$$

where

- R_{ESR} is the equivalent resistance in series of the output capacitor

The right-hand plane zero is:

$$f_{RHP} = \frac{R_{OUT} \times (1 - D)^2}{2\pi \times L} \quad (14)$$

where

- D is the duty cycle
- R_{OUT} is the output load resistor
- L is the inductance

The TPS61371 COMP pin is the output of the internal trans-conductance amplifier.

Equation 15 shows the equation for feedback resistor network and the error amplifier.

$$H_{EA}\left(S\right) = G_{EA} \times R_{EA} \times \frac{R_{DOWN}}{R_{UP} + R_{DOWN}} \times \frac{1 + \frac{S}{2 \times \pi \times f_Z}}{\left(1 + \frac{S}{2 \times \pi \times f_{P1}}\right) \times \left(1 + \frac{S}{2 \times \pi \times f_{P2}}\right)} \quad (15)$$

where

- R_{EA} is the output impedance of the error amplifier R_{EA} = 500MΩ. G_{EA} is the transconductance of the error amplifier, G_{EA} = 175μS.
- f_{P1}, f_{P2} is the pole frequency of the compensation
- f_Z is the zero frequency of the compensation network

$$f_{P1} = \frac{1}{2\pi \times R_{EA} \times C_C} \quad (16)$$

where

- C_C is the zero capacitor compensation

$$f_{P2} = \frac{1}{2\pi \times R_C \times C_P} \quad (17)$$

where

- C_P is the pole capacitor compensation
- R_C is the resistor of the compensation network

$$f_Z = \frac{1}{2\pi \times R_C \times C_C} \quad (18)$$

8.2.2.6 Loop Compensation Design Steps

With the small signal models coming out, the next step is to calculate the compensation network parameters with the given inductor and output capacitance.

1. **Set the Crossover Frequency, f_C .**
   - The first step is to set the loop crossover frequency, f_C. The higher crossover frequency, the faster the loop response is. The loop gain crossing over no higher than the lower of either 1/10 of the switching frequency, f_{SW}, or 1/5 of the RHPZ frequency, f_{RHPZ} is generally accepted. Then calculate the loop compensation network values of R_c, C_c, and C_p in the following sections.
2. **Set the Compensation Resistor, R_C .**
   - By placing f_Z below f_C, for frequencies above f_C, R_C | | R_{EA} approximately = R_C, so R_C × G_{EA} sets the compensation gain. Setting the compensation gain, $K_{COMP\text{-}dB}$, at f_Z, results in the total loop gain, $T_{(s)}$ = $G_{PS(s)}$ × $H_{EA(s)}$ × He(s) being zero at f_C.
   - Therefore, to approximate a single-pole rolloff up to f_{P2}, rearrange Equation 19 to solve for RC so that the compensation gain, K_{EA}, at f_C is the negative of the gain, K_{PS}, read at frequency f_C for the power stage bode plot or more simply:

$$K_{EA}\left(S\right) = 20 \times \log\left(G_{EA} \times R_C \times \frac{R_{DOWN}}{R_{UP} + R_{DOWN}}\right) = -K_{PS}\left(f_C\right) \quad (19)$$

where

- K_{EA} is gain of the error amplifier network
- K_{PS} is the gain of the power stage
- G_{EA} is the transconductance of the amplifier, the typical value of G_{EA} = 175μA / V

3. **Set the compensation zero capacitor, C_C .**
   - Place the compensation zero at the power stage pole position of R_{OUT}, C_{OUT} to get:

$$f_Z = \frac{1}{2\pi \times R_C \times C_C} \quad (20)$$

   - Set f_Z = f_P, and get:

$$C_C = \frac{R_{OUT} \times C_{OUT}}{2 \times R_C} \quad (21)$$

4. **Set the compensation pole capacitor, C_P .**
   - Place the compensation pole at the zero produced by the R_{ESR} and the C_{OUT}. Canceling unhelpful effects of the ESR zero is useful.

$$f_{P2} = \frac{1}{2\pi \times R_C \times C_P} \quad (22)$$

$$f_{ESR} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \quad (23)$$

   - Set f_{P2} = f_{ESR}, and get:

$$C_P = \frac{R_{ESR} \times C_{OUT}}{R_C} \quad (24)$$

   - If the calculated value of C_P is less than 10pF, the value can be neglected.

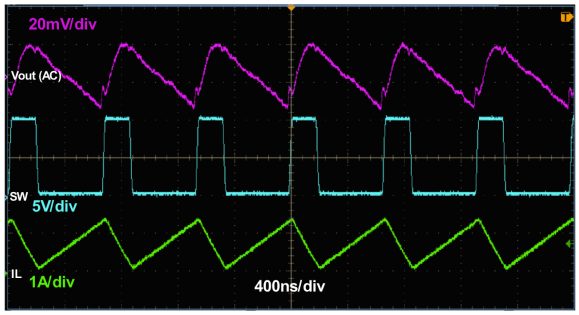
   Designing the loop for greater than 45° of phase margin and greater than 6dB gain margin eliminates output voltage ringing during the line and load transient. The R_C = 61.9kΩ , C_C = 680pF for this design example.

8.2.2.7 Selecting the Bootstrap Capacitor

The bootstrap capacitor between the BST and SW pin supplies the gate current to charge the high-side FET device gate during the turn-on of each cycle and also supplies charge for the bootstrap capacitor. The recommended value of the bootstrap capacitor is 20nF to 200nF. C_{BST} must be a good quality, low-ESR ceramic capacitor located at the pins of the device to minimize potentially damaging voltage transients caused by trace inductance. A value of 100nF is selected for this design example.

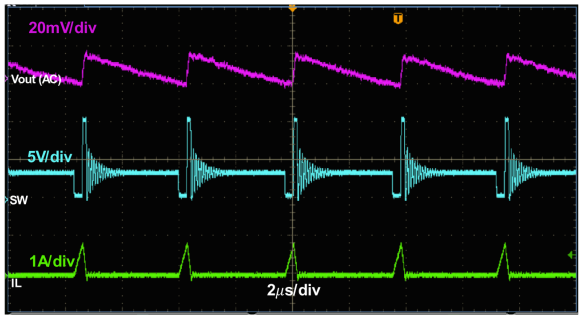
8.2.3 Application Curves

Typical condition V_{IN} = 3V to 5V, V_{OUT} = 11V, temperature = 25°C, unless otherwise noted



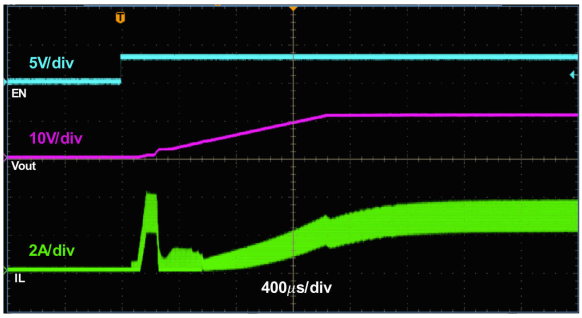
V_{IN} = 3.3V V_{OUT} = 11V Mode = Auto PFM
L = 1µH C_{OUT} = 3 × 10µF

Figure 8-3. Steady-State at 200mA Load



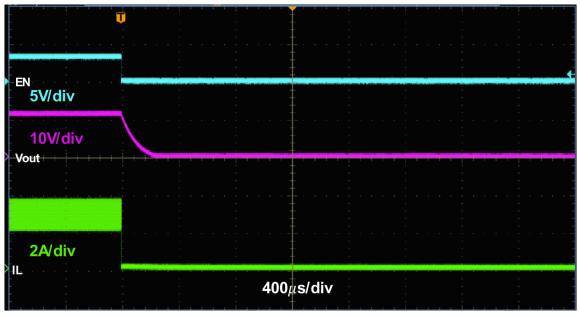
V_{IN} = 3.3V V_{OUT} = 11V Mode = Auto PFM
L = 1µH C_{OUT} = 3 × 10µF

Figure 8-4. Steady-State at 10mA Load



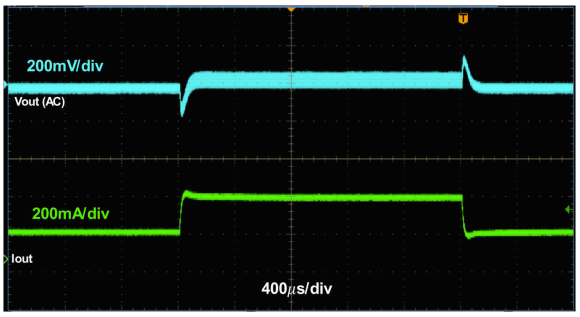
V_{IN} = 3.3V V_{OUT} = 11V Mode = Auto PFM
L = 1µH C_{OUT} = 3 × 10µF

Figure 8-5. Start-Up by EN, Load = 16Ω



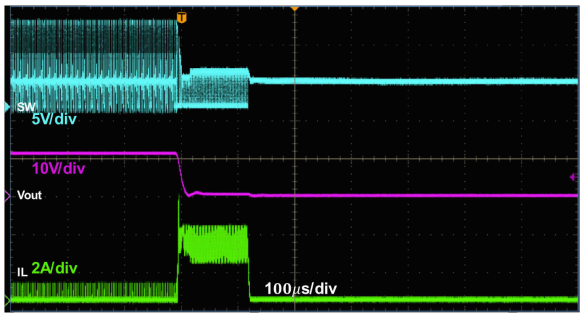
V_{IN} = 3.3V V_{OUT} = 11V Mode = Auto PFM
L = 1µH C_{OUT} = 3 × 10µF

Figure 8-6. Shutdown by EN, Load = 12.5Ω



V_{IN} = 3.3V V_{OUT} = 11V Mode = Auto PFM
L = 1µH C_{OUT} = 3 × 10µF

Figure 8-7. Load Transient, 200mA to 400mA, 100mA / µs



V_{IN} = 3.3V V_{OUT} = 11V Mode = Auto PFM
L = 1µH C_{OUT} = 3 × 10µF

Figure 8-8. Shorted Output

8.3 Power Supply Recommendations

The devices are designed to operate from an input voltage supply ranging from 2.7V to 5.5V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS61371, the bulk capacitance can be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47µF is a typical choice.

8.4 Layout

8.4.1 Layout Guidelines

The basic PCB board layout requires a separation of sensitive signal and power paths. If the layout is not carefully done, the regulator can suffer from the instability or noise problems.

The following checklist is suggested to get good performance for a well-designed board:

1. Minimize the high current path from output of chip, the output capacitor to the GND of chip. This loop contains high di / dt switching currents (nano seconds per ampere) and easy to transduce the high frequency noise.
2. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize inter plane coupling.
3. Use a combination of bulk capacitors and smaller ceramic capacitors with low series resistance for the input and output capacitors. Place the smaller capacitors closer to the IC to provide a low impedance path for decoupling the noise.
4. The ground area near the IC must provide adequate heat dissipating area. Connect the wide power bus (for example, V_{OUT}, SW, GND) to the large area of copper, or to the bottom or internal layer ground plane, using vias for enhanced thermal dissipation.
5. Place the input capacitor being close to the V_{IN} pin and the PGND pin to reduce the input supply ripple.
6. Place the noise sensitive network like the feedback and compensation being far away from the SW trace.
7. Use a separate ground trace to connect the feedback and the loop compensation circuitry. Connect this ground trace to the main power ground at a single point to minimize circulating currents.

8.4.2 Layout Example

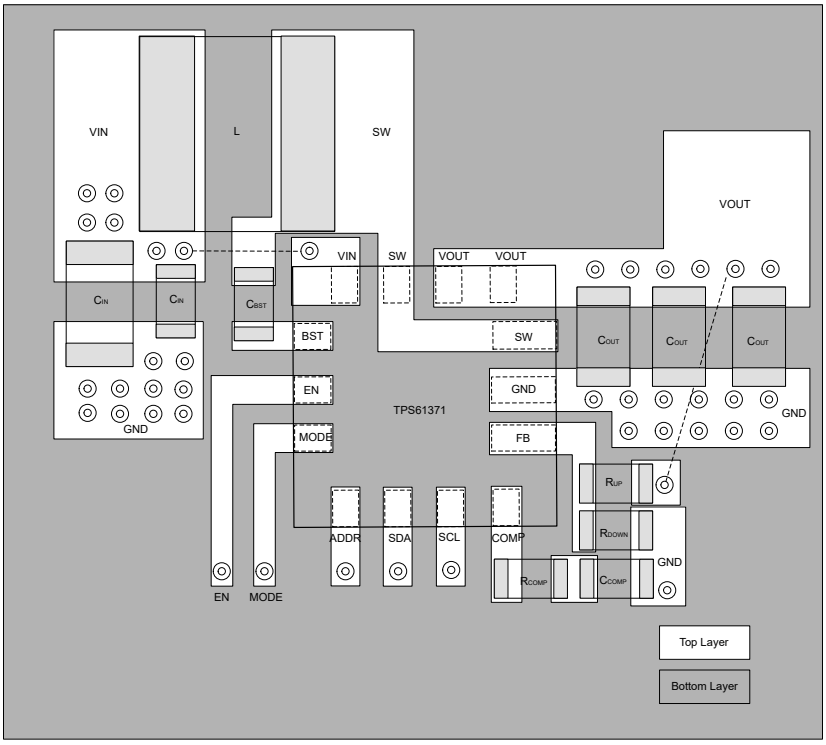


Figure 8-9. Recommended Layout

8.4.2.1 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component.

The following are two basic approaches for enhancing thermal performance:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB

As power demand in portable designs is more and more important, designers must figure the best trade-off between efficiency, power dissipation and design size. Due to integration and miniaturization, junction temperature can increase significantly which can lead to bad application behaviors (that is, premature thermal shutdown or worst case reduce device reliability). Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design. Keep the device operating junction temperature (T_J) below 125°C.

9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

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9.3 Support Resources

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

DATE	REVISION	NOTES
April 2026	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS61371VARR	Active	Production	WQFN-HR (VAR) | 14	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-	1371

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

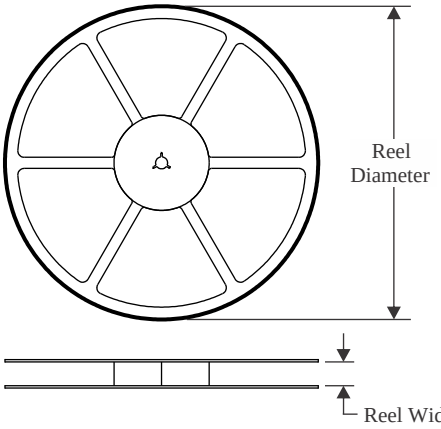
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

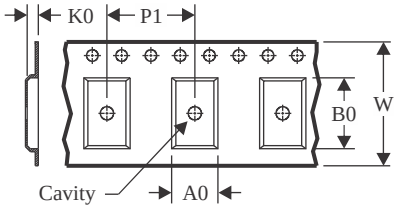
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

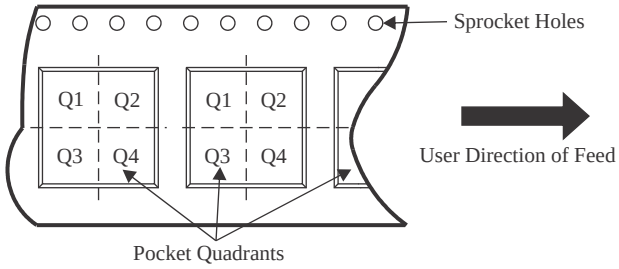


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

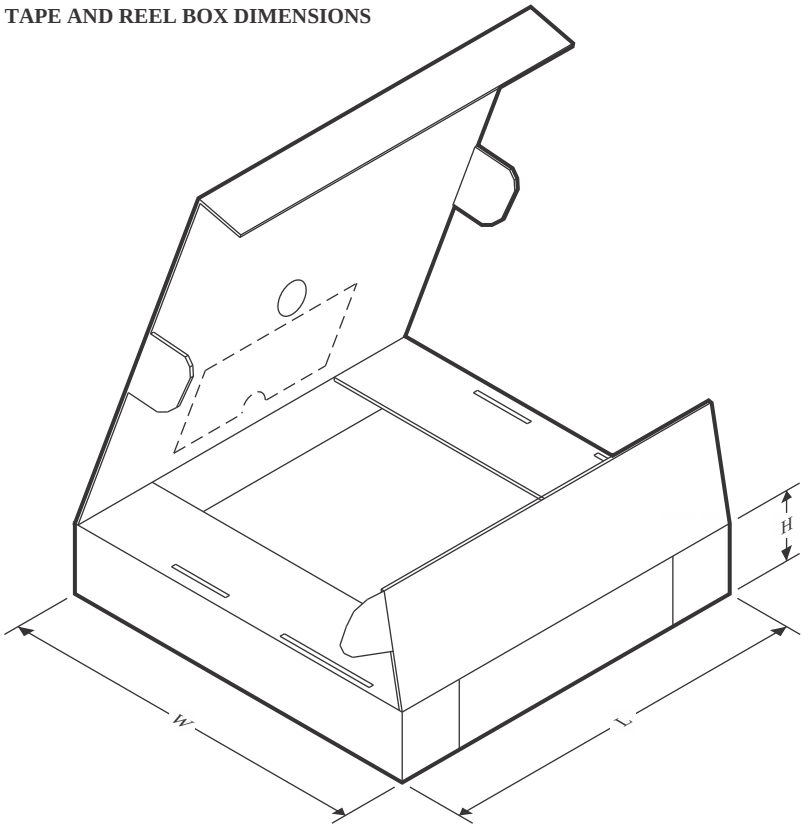
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61371VARR	WQFN-HR	VAR	14	3000	180.0	8.4	2.8	2.8	1.0	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

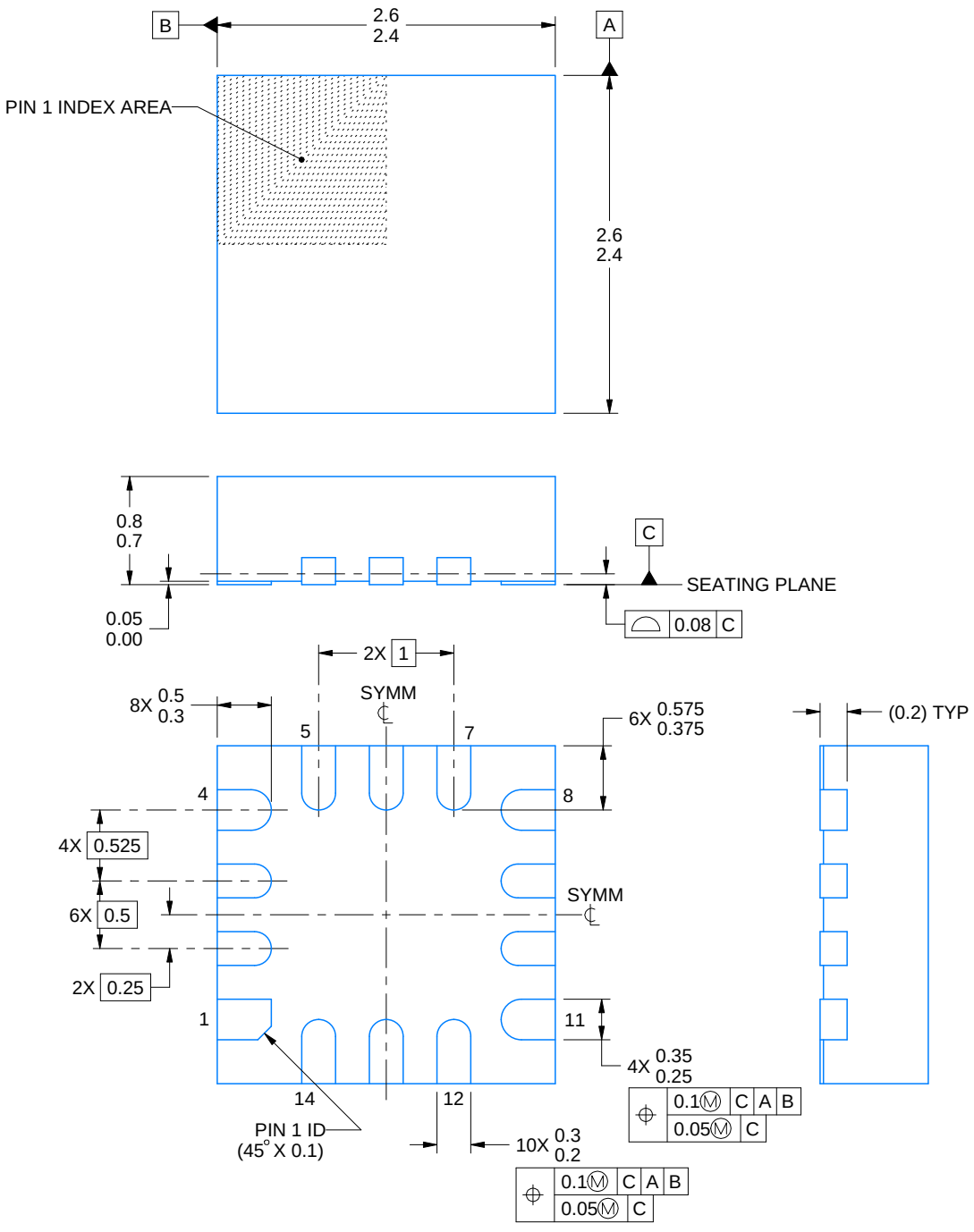
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61371VARR	WQFN-HR	VAR	14	3000	210.0	185.0	35.0

VAR0014A

PACKAGE OUTLINE

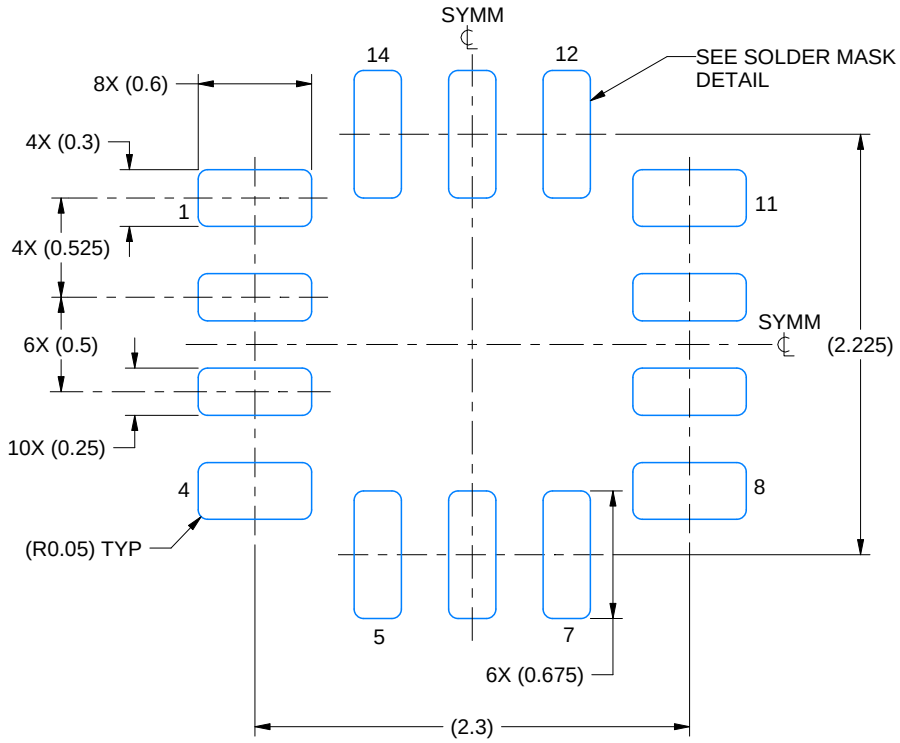
WQFN-HR - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

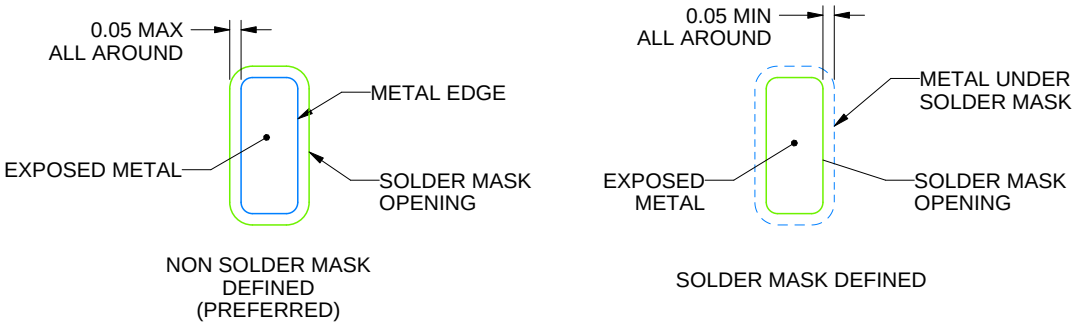


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



SOLDER MASK DETAILS

4231113/A 08/2024

NOTES: (continued)

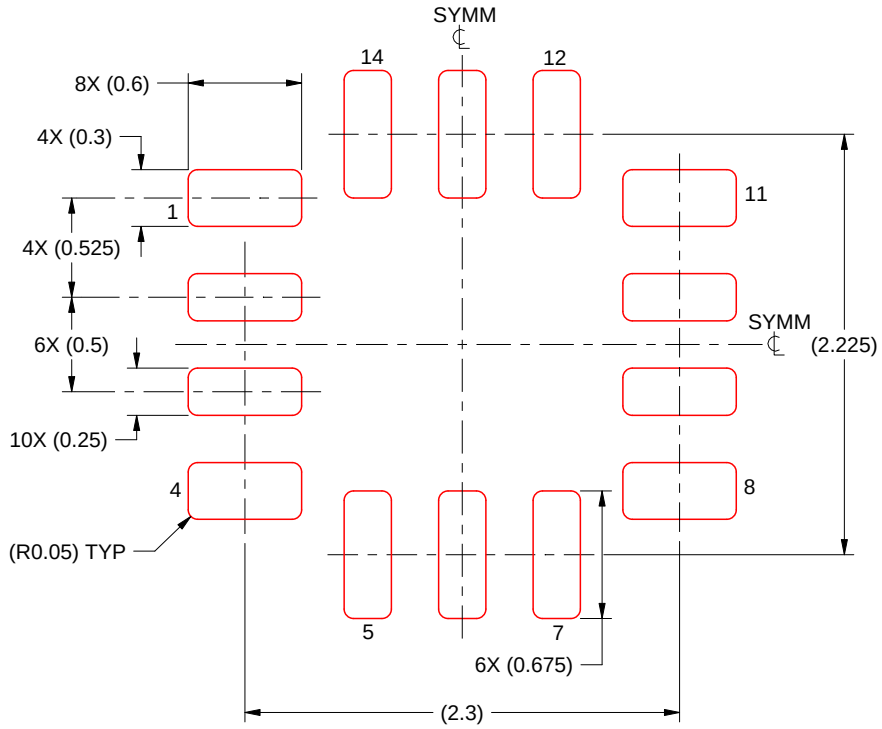
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

VAR0014A

WQFN-HR - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 25X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025