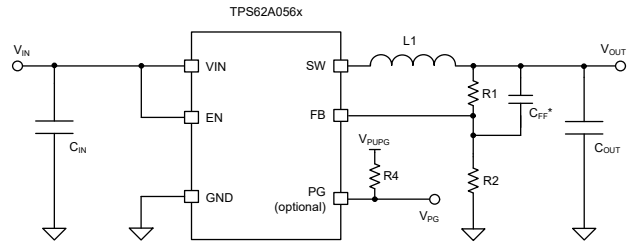
TPS62A0569x 2A, High-Efficiency, Synchronous Buck Converters in SOT-563 Package

1 Features

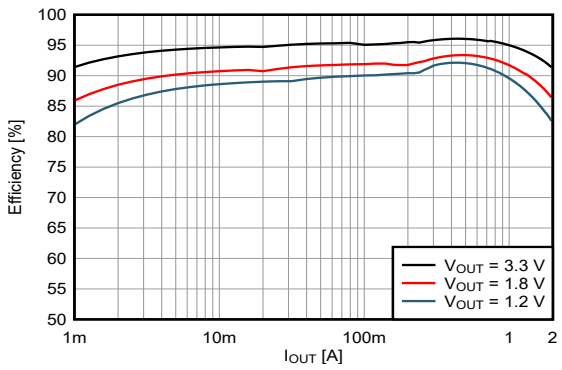
- 2.5V to 5.5V input voltage range
- 2A Power Save Mode (PSM) and Forced Pulse Width Modulation (FPWM) version
- Pin-to-pin compatible with the TLV6256x DRL family
- 0.6V to V_{IN} adjustable output voltage range
- 100mΩ/70mΩ low R_{DSON} switches
- < 23µA quiescent current
- 2% feedback accuracy including temperature effects
- 100% mode operation
- 2.4MHz switching frequency
- Power-good output pin (optional)
- Short-circuit protection (HICCUP)
- Internal soft start-up
- Active fast output discharge (switch with current limit)
- Thermal shutdown protection

2 Applications

- Set top box, TV applications
- IP network camera, Multi-function printer
- Wireless router, solid state drive
- Battery-powered applications
- General purpose point-of-load supply



Typical Application



Efficiency vs Output Current at $5V_{IN}$ (TPS62A0569)

3 Description

The TPS62A0569x family of devices are synchronous step-down buck DC/DC converters optimized for high efficiency and compact design size. The devices integrate switches capable of delivering an output current up to 2A. At medium to heavy loads, the devices operate in peak current mode pulse width modulation (PWM) with approximately 2.4MHz switching frequency. At light load, the devices automatically enter power save mode (PSM) to maintain high efficiency over the entire load current range. In shutdown, the current consumption is minimized for increased application shelf life. The TPS62A0569A variant of this device family operates in forced PWM across the whole load current range.

The TPS62A0569 devices provide an adjustable output voltage through an external resistor divider. An internal soft-start circuit limits the inrush current during start-up. Essential features like overcurrent protection, thermal shutdown protection, and power good (optional) are built-in. The devices are available in SOT563 package.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS62A0568x	DRL (SOT-563, 6)(3)	1.60mm × 1.60mm
	DDC (SOT-23, 5)(3)	2.90mm × 2.80mm
TPS62A0569x	DRL (SOT-563, 6)	1.60mm × 1.60mm
	DDC (SOT-23, 5)(3)	2.90mm × 2.80mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) Preview information (not Production Data).

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4 Device Comparison Table

ORDERABLE PART NUMBER	MODE	PIN 6	OUTPUT CURRENT	NUMBER OF PINS
TPS62A0568DRLR(1)	PSM	NC(2)	1A	6
TPS62A0568ADRLR(1)	FPWM			
TPS62A0568PDRLR(1)	PSM	PG		
TPS62A0568APDRLR(1)	FPWM			
TPS62A0569DRLR(1)	PSM	NC(2)	2A	
TPS62A0569ADRLR	FPWM			
TPS62A0569PDRLR	PSM	PG		
TPS62A0569APDRLR(1)	FPWM			
TPS62A0568DDC(1)	PSM	NA	1A	5
TPS62A0568ADDC(1)	FPWM			
TPS62A0569DDC(1)	PSM		2A	
TPS62A0569ADDC(1)	FPWM			

(1) Preview information (not Production Data).
(2) NC can float, connect to GND or connect to VOUT.

5 Pin Configuration and Functions

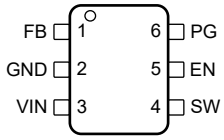


Figure 5-1. 6-Pin DRL SOT563 Package with PG (Top View)

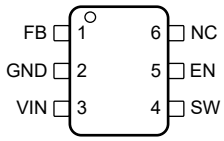


Figure 5-2. 6-Pin DRL SOT563 Package compatible with OUT/VOS (Top View)

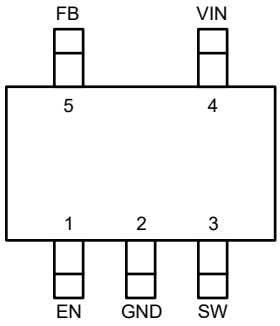


Figure 5-3. Preview of 5-Pin DDC SOT23 Package (Top View)

Table 5-1. Pin Functions

Name	Pin Number		Type[1]	Description
	SOT563	SOT23		
EN	5	1	I	Device enable logic input. Logic high enables the device. Logic low disables the device and turns the device into shutdown. Do not leave the pin floating.
FB	1	5	I	Feedback pin for the internal control loop. Connect this pin to an external feedback divider.
GND	2	2	G	Ground pin.
PG[2], NC[3]	6	n/a	O/NC	This pin is different for the TPS62A056x and TPS62A056x**P**. The P-version has the power-good open-drain output on this pin with a pullup resistor connected to any voltage less than 5.5V. Unused the pin must float or connect to GND. The non P-version can have this pin also connected to the positive connection of the output capacitor.
SW	4	3	O	Switch pin connected to the internal FET switches and inductor terminal. Connect the inductor of the output filter to this pin.
VIN	3	4	I	Input voltage pin. Connect the input capacitor as close as possible between V_{IN} and GND.

(1) I = Input, O = Output, G = Ground, NC = not connected.
(2) TPS62A056xP (P-version), compatible with devices which have a power-good signal on this pin.
(3) TPS62A056x (non P-version), compatible with devices which have this pin connected to the output voltage.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Pin voltage(2)	VIN, EN, PG	–0.3	6.5	V
	SW, DC	–0.3	V_{IN} + 0.3	V
	SW, transient for less than 10 ns while switching	–3.0	10	V
	FB	–0.3	3	V
Operating junction temperature	T_J	–40	150	°C
Storage temperature	T_{stg}	–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to the network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage range		2.5		5.5	V
V_{OUT}	Output voltage range		0.6		V_{IN}	V
I_{OUT}	Output current range	TPS62A0569			2	A
L	Effective inductance		0.4	1.0	2.5	µH
C_{OUT}	Effective output capacitance		10 (1)		90	µF
I_{PG}	Power Good input current capability		0		1	mA
T_J	Operating junction temperature		–40		125 (2)	°C

(1) 5µF minimum effective capacitance (capacitor value corrected by de-rating) are possible under conditions outlined in the section *Output Filter Design*.
(2) Lifetime is reduced when operating continuously at a junction temperature > 105°C.

6.4 Thermal Information

THERMAL METRIC[1]		TPS62A0569x DRL 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	157.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	92.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	45.0	°C/W

(1) For more information about traditional and new thermal metrics, see the S emiconductor and IC Package Thermal Metrics application note.

6.5 Electrical Characteristics

T_J = –40°C to +125°C, V_{IN} = 2.5V to 5.5V. Typical values are at T_J = 25°C and V_{IN} = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
$I_{Q(VIN)}$	VIN quiescent current	Non-switching, V_{EN} = High, V_{FB} = 610mV		23		µA
$I_{SD(VIN)}$	VIN shutdown supply current	V_{EN} = Low; MAX value at 125°C		0.01	2	µA
$V_{UVLO(R)}$	VIN UVLO rising threshold	V_{IN} rising	2.3	2.4	2.5	V
$V_{UVLO(H)}$	VIN UVLO hysteresis	V_{IN} falling		0.12		V
ENABLE						
$V_{EN(R)}$	EN voltage rising threshold	EN rising, enable switching	0.9			V
$V_{EN(F)}$	EN voltage falling threshold	EN falling, disable switching			0.35	V
$V_{EN(LKG)}$	EN Input leakage current	V_{EN} = 5V		0.1		nA
REFERENCE VOLTAGE						
V_{FB}	FB voltage	PWM mode, 25°C	588	600	612	mV
$I_{FB(LKG)}$	FB input leakage current	V_{FB} = 0.6V		0.13		nA
SWITCHING FREQUENCY						
$f_{SW(FCCM)}$	Average switching frequency, PWM versions	V_{IN} = 5V, V_{OUT} = 1.8V		2400		kHz
f_{SW}	Average switching frequency, PSM versions	V_{IN} = 5V, V_{OUT} = 1.8V	0	2400[1]		kHz
STARTUP						
	Internal fixed soft-start time	From EN = High to V_{FB} = 0.56V		0.6		ms
POWER STAGE						
$R_{DSON(HS)}$	High-side MOSFET on-resistance	V_{IN} = 5V		100		mΩ
$R_{DSON(LS)}$	Low-side MOSFET on-resistance	V_{IN} = 5V		70		mΩ
OVERCURRENT PROTECTION						
$I_{HS(OC)}$	High-side peak current limit	TPS62A0569	2.3	3.4		A
POWER GOOD						
V_{PGTH}	Power-good (PG) threshold	PG low, FB falling		93.5		%
V_{PGTH}	PG threshold	PG high, FB rising		96		%
$I_{PG(LKG)}$	PG pin Leakage current when open drain output is high	V_{PG} = 5V			100	nA
	PG pin output low-level voltage	I_{PG} = 1mA			200	mV
OUTPUT DISCHARGE						
	Output discharge current on SW pin	V_{IN} = 3V, V_{OUT} = 2.0V		68		mA
THERMAL SHUTDOWN						
$T_{J(SD)}$	Thermal shutdown threshold	Temperature rising		165		°C

T_J = –40°C to +125°C, V_{IN} = 2.5V to 5.5V. Typical values are at T_J = 25°C and V_{IN} = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{J(HYS)}$	Thermal shutdown hysteresis			20		°C

(1) The frequency can be significantly higher and lower than the typical frequency. The frequency is determined by the conditions the device operates in. Maintaining V_{OUT} has the highest priority and can influence switching frequency. In the range between power save mode and pulse width modulation mode there is no constant frequency but a spectral mix with components up to 5MHz.

6.6 Typical Characteristics

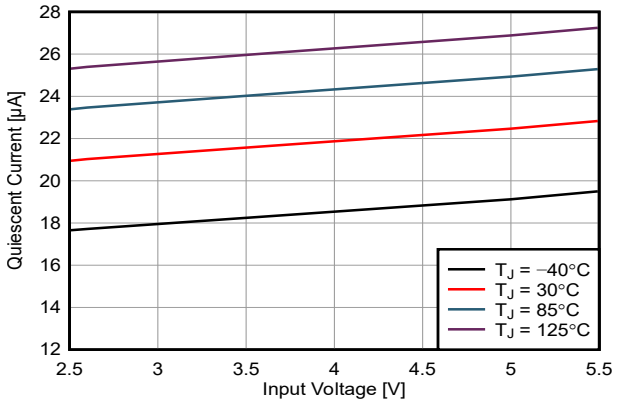


Figure 6-1. Quiescent Current vs Input Voltage (PSM operation only)

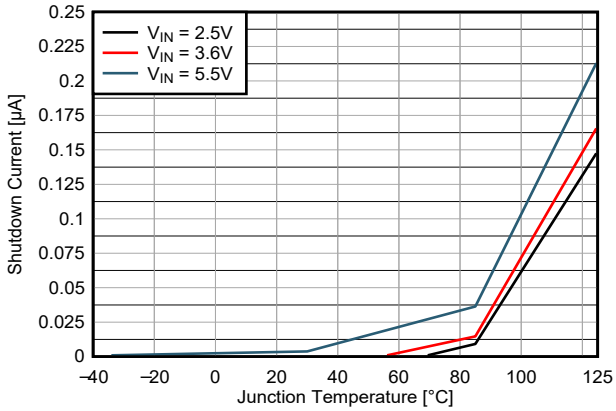


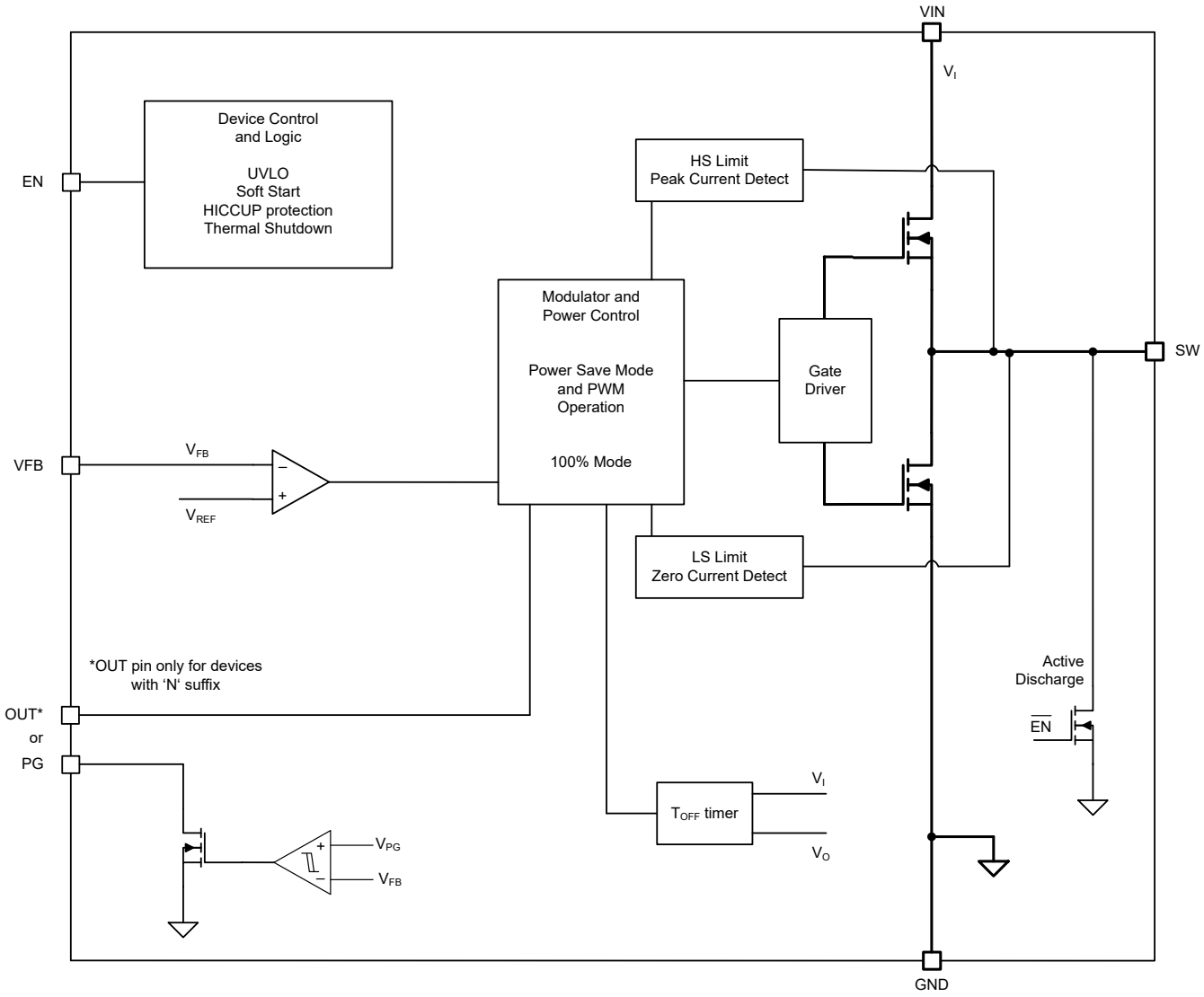
Figure 6-2. Shutdown Current vs Junction Temperature

7 Detailed Description

7.1 Overview

The TPS62A0569 is a high-efficiency synchronous step-down converter. The device operates with an adaptive off time with a peak current control scheme. The device operates typically at 2.4MHz frequency pulse width modulation (PWM) at moderate to heavy load currents. Based on the V_{IN}/V_{OUT} ratio, a simple circuit sets the required off time for the low-side MOSFET, making the switching frequency relatively constant regardless of the variation of the input voltage, output voltage, and load current.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power Save Mode

The device automatically enters power save mode to improve efficiency at light load when the inductor current becomes discontinuous. In power save mode, the converter reduces the switching frequency and minimizes current consumption. In power save mode, the output voltage rises slightly above the nominal output voltage. This effect is minimized by increasing the output capacitor or adding a feedforward capacitor.

7.3.2 100% Duty Cycle Low Dropout Operation

The device offers low input-to-output voltage difference by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on and the low-side MOSFET is switched off. The minimum input voltage to maintain output regulation, depending on the load current and output voltage, is calculated as:

$$V_{IN(MIN)} = V_{OUT} + I_{OUT} \times (R_{DS(ON)} + R_L) \quad (1)$$

where

- $R_{DS(ON)}$ = High-side FET on-resistance
- R_L = Inductor ohmic resistance (DCR)

7.3.3 Soft Start

After enabling the device, internal soft-start circuitry ramps up the output voltage, which reaches the nominal output voltage during start-up time, avoiding excessive inrush current and creating a smooth voltage rise slope. Internal soft-start circuitry also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance.

The TPS62A0569 is able to start into a prebiased output capacitor. The converter starts with the applied bias voltage and ramps the output voltage to the nominal value.

7.3.4 Switch Current Limit and Short-Circuit Protection (HICCUP)

The switch current limit prevents the device from high inductor current and drawing excessive current from the battery or input rail. Due to internal propagation delay, the AC peak current can exceed the static current limit during that time. Excessive current can occur with a shorted or saturated inductor, an overload or shorted output circuit condition. If the inductor current reaches the threshold I_{LIM}, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current with an adaptive off time.

When this switch current limit is triggered 32 times, the device stops switching to protect the output. The device then automatically starts a new start-up after a typical delay time of 100µs has passed. This is named HICCUP short-circuit protection. The device repeats this mode until the high load condition disappears. HICCUP protection is also enabled during the start-up.

7.3.5 Undervoltage Lockout

To avoid misoperation of the device at low input voltages, an undervoltage lockout (UVLO) is implemented, which shuts down the device at voltages lower than V_{UVLO}. A blanking time of t_{UVLO} avoids inadvertently triggering UVLO from noise. If the undervoltage condition still persists after the blanking then UVLO becomes effective.

7.3.6 Thermal Shutdown

The device goes into thermal shutdown and stops switching when the junction temperature exceeds $T_{J(SD)}$. When the device temperature falls below the threshold by $T_{J(HYS)}$, the device returns to normal operation automatically.

7.4 Device Functional Modes

7.4.1 Enable and Disable

The device is enabled by setting the EN input to a logic High. Accordingly, a logic Low disables the device. If the device is enabled, the internal power stage starts switching and regulates the output voltage to the set point voltage. The EN input must be terminated and not be left floating.

7.4.2 Power Good

The TPS62A0569xP versions have a built-in power-good (PG) feature to indicate whether the output voltage has reached the target and the device is ready. The PG signal can be used for start-up sequencing of multiple rails. The PG pin is an open-drain output that requires a pullup resistor to any voltage up to the recommended

input voltage level. PG is low when the device is turned off due to EN, UVLO (undervoltage lockout), or thermal shutdown. VIN must remain present for the PG pin to stay low. If not used, the power-good can be tie to GND or left open. The PG indicator has a de-glitch to avoid the signal indicating glitches or transient responses from the loop. The TPS62A0569x without P have no power good pin. In these versions the pin is an NC which can be left floating, or be connected to GND or V_{OUT}.

Table 7-1. Power-Good indicator Functional Table

Logic Signals				PG Status
V_I	EN Pin	Thermal Shutdown	V_O	
V_I > UVLO	HIGH	NO	V_O on target	High Impedance
			V_O < target	LOW
		YES	x	LOW
	LOW	x	x	LOW
V_I < 1.8V	x	x	x	Undefined

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

8.2 Typical Application

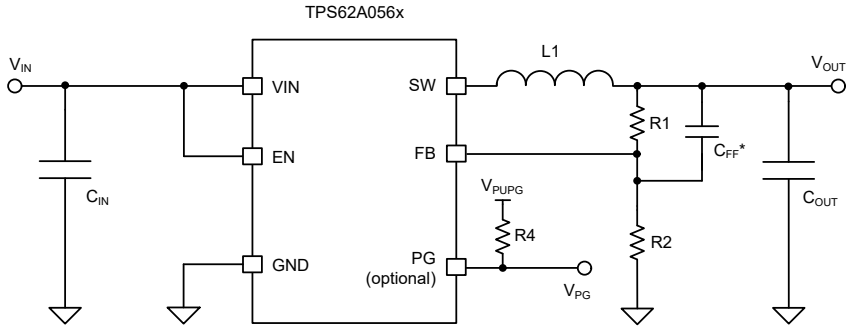


Figure 8-1. TPS62A056x Typical Application Circuit

*C_{FF} is optional, PG is NC on some devices

8.3 Design Requirements

For this design example, use the parameters listed in Table 8-1 as the input parameters

Table 8-1. Design Parameters

Design Parameter	Example Value
Input voltage (V_{IN})	2.5V to 5.5V
Output voltage (V_{OUT})	1.8V
Maximum output current (I_{OUT})	1.0A, 2.0A

Table 8-2 lists the components used for the example.

Table 8-2. List of Components

Reference	Description	Manufacturer (1)
C_{IN}	4.7µF, Ceramic Capacitor, 10V, X7R, size 0805, GRM21BR71A475KA73L	Murata
C_{OUT}	22µF, Ceramic Capacitor, 10V, X7R, size 0805, GRM21BZ71A226KE15L	Murata
L1	1µH, Power Inductor, DFE252012F-1R0M (1A) / XGL3520-102MEC (2A)	Murata / Coilcraft
R1, R2	Chip resistor, 1%, size 0603	Std.
C_{FF}	Optional, up to 120pF if needed	Std.

(1) See the *Third-Party Products Disclaimer*.

8.4 Detailed Design Procedure

8.4.1 Setting the Output Voltage

The output voltage is set by an external resistor divider according to Equation 2.

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right) = R2 \times \left(\frac{V_{OUT}}{0.6\,V} - 1\right) \quad (2)$$

R2 must not be higher than 100kΩ to provide acceptable noise sensitivity.

8.4.2 Input and Output Capacitor Selection

The architecture of the TPS62A0569 allows use of tiny ceramic-type output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are thus recommended. To keep resistance up to high frequencies and to achieve narrow capacitance variation with temperature, TI recommends to use X7R or X6S dielectric.

The input capacitor is the low impedance energy source for the converter that helps provide stable operation. TI recommends a low-ESR multilayer ceramic capacitor for best filtering. For the values see table Recommended Operating Conditions.

The TPS62A0569 is designed to operate with a variety of output capacitor and inductor combinations which are outlined in Matrix of Output Voltage, Capacitor and Inductor Combinations With TPS62A0569x. The tolerated effective inductor and capacitor values are also outlined in table Recommended Operating Conditions. Other combinations are possible but then a Bode plot must be performed to verify phase reserve with the given inductor, output capacitor and feed forward capacitor for best stability. This also valid when components with derating different from the BOM in this datasheet are used.

The feedforward capacitor improves the load transient response and can have a positive impact on the phase reserve in combination with larger output capacitors. With smaller output capacitors phase reserve can be reduced. The optimum value is typically between 10pF and 120pF when using R2 = 100kΩ. With different value for R2 the C_{FF} range needs to be recalculated. The application note Feedforward Capacitor to Improve Stability and Bandwidth discusses this topic in detail.

8.4.3 Output Filter Design

The inductor and output capacitor together provide a low-pass filter. The following tables show possible output capacitor and inductor pair values per output voltage. Checked cells represent combinations that are proven for stability by simulation and lab test. Two plus signs (++) mean this combination of capacitor and inductor values works very stable for the listed V_{OUT} range and can be used without change in the target application. One plus sign (+) means this combination of capacitor and inductor values works stable on the reference board (TPS62A0569x Evaluation Module) but can require adaptation to the target application. Check this capacitor and inductor combination more thoroughly in combination with the application and provide layout or BOM options by adding an unpopulated spare C_{OUT} location. Other combinations can also be suitable for specific target applications and can be used once validated for stability including measuring a Bode plot.

Table 8-3. Matrix of Output Voltage, Capacitor and Inductor Combinations With TPS62A0569x

V_{OUT} [V]	L [µH](1)	C_{OUT} [µF](2)			
		10	22	2 × 22	4 × 22
0.6 ≦ V_{OUT} < 1.2	0.47	+	++	++	++
	1		++	++	++
	2.2		++	++	++
1.2 ≦ V_{OUT} < 1.8	0.47	+	++	++	+(3)
	1		++	++	+(3)
	2.2		++	++	+(3)

Table 8-3. Matrix of Output Voltage, Capacitor and Inductor Combinations With TPS62A0569x (continued)

V_{OUT} [V]	L [µH](1)	C_{OUT} [µF](2)			
		10	22	2 × 22	4 × 22
1.8 ≦ V_{OUT}	0.47	+ (C_{FF} = 0)	++	++	+(3)
	1	+ (C_{FF} = 0)	++(4)	+	+(3)
	2.2		+	+	+(3)

(1) Inductor tolerance and current de-rating comparable to the device families in the BOM are included in the recommendation.
(2) Capacitance tolerance and bias voltage de-rating is included in this recommendation based on the device families from the BOM. Capacitors from different manufacturers or with different form factor can have more derating. Then larger values need to be considered.
(3) Very stable operating condition with strong transient resilience. Voltage drop with large transients is minimized. One '+' is shown here because gain bandwidth is reduced with this setting so time required for V_{OUT} to return to target after large transients is extended.
(4) Evaluation module configuration.

8.5 Application Curves

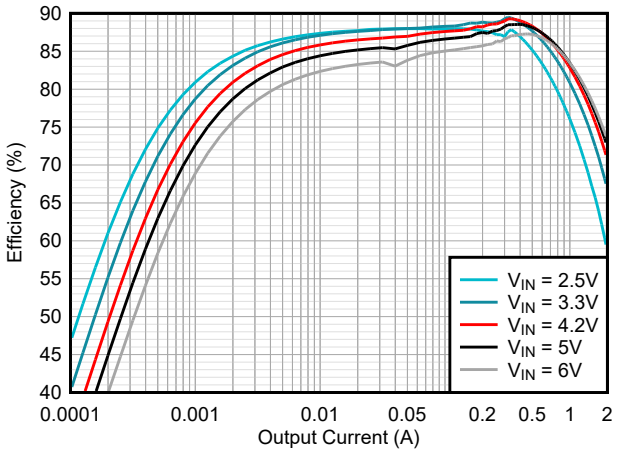


Figure 8-2. 0.6V Output Efficiency

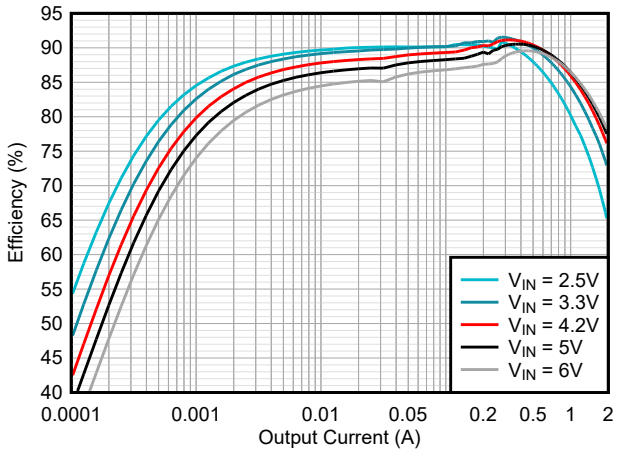


Figure 8-3. 0.9V Output Efficiency

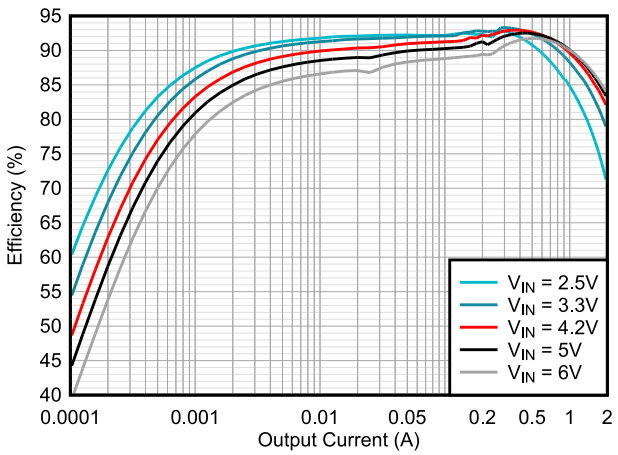


Figure 8-4. 1.2V Output Efficiency

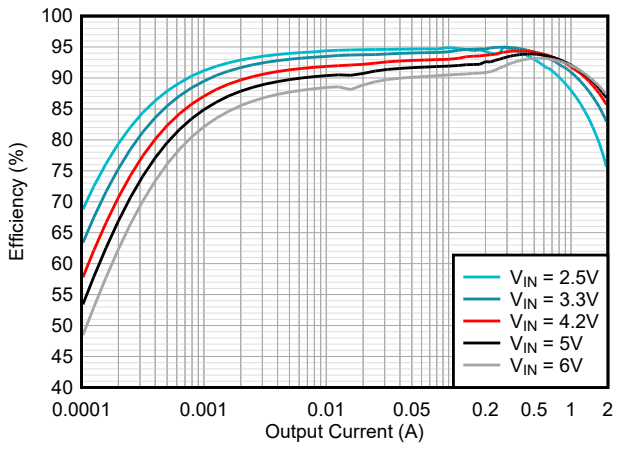


Figure 8-5. 1.8V Output Efficiency

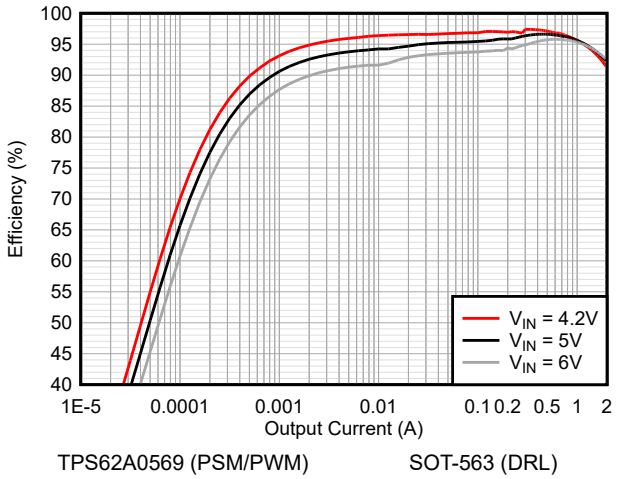


Figure 8-6. 3.3V Output Efficiency

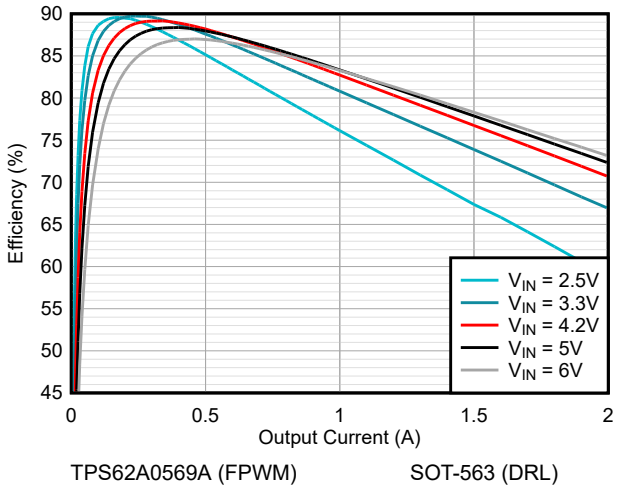
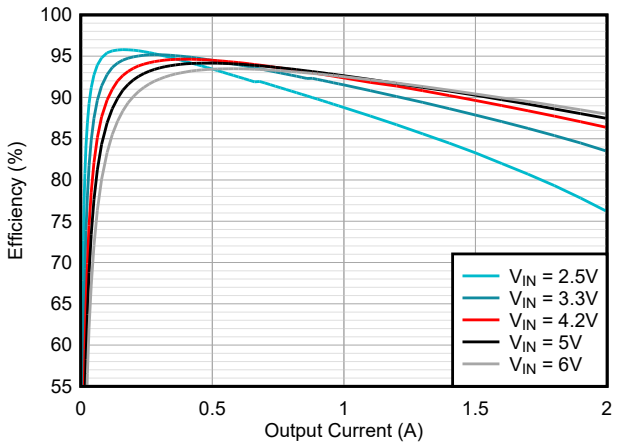
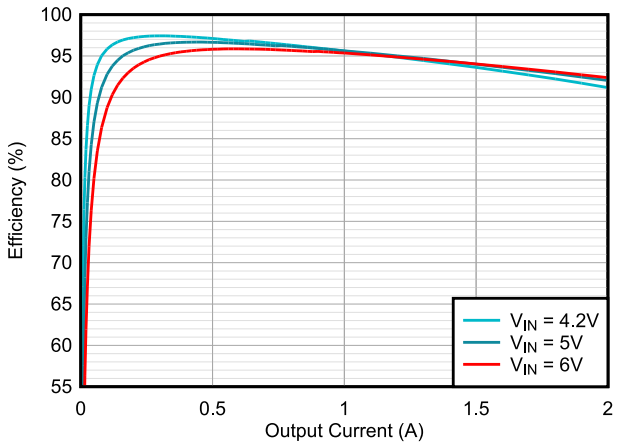


Figure 8-7. 0.6V Output Efficiency



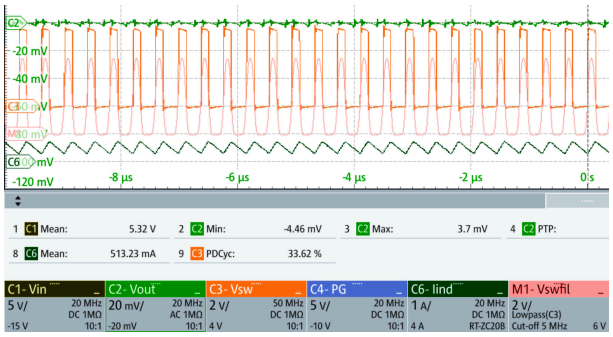
TPS62A0569A (FPWM) SOT-563 (DRL)

Figure 8-8. 1.8V Output Efficiency



TPS62A0569A (FPWM) SOT-563 (DRL)

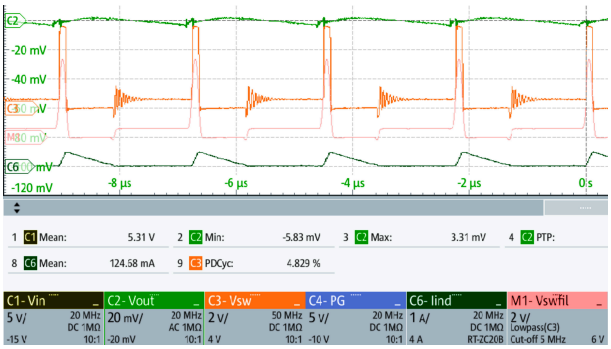
Figure 8-9. 3.3V Output Efficiency



TPS62A0569x Auto PSM and forced PWM versions

V_{IN} = 5.5V, V_{OUT} = 1.8V, I_{OUT} = 500mA

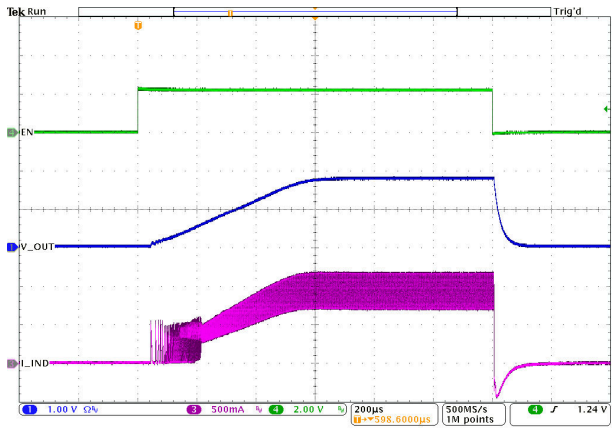
Figure 8-10. PWM Operation



TPS62A0569 (Auto PSM version)

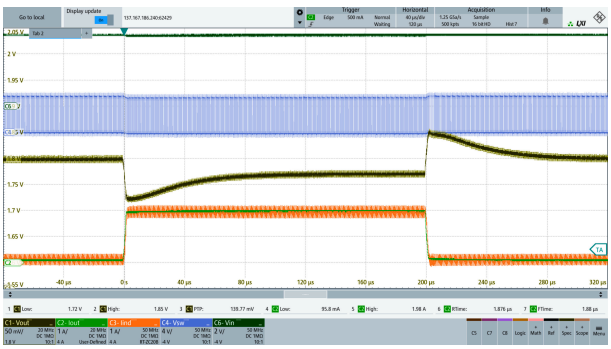
V_{IN} = 5.5V, V_{OUT} = 1.8V, I_{OUT} = 100mA

Figure 8-11. Power Save Mode Operation



I_{OUT} = 1A

Figure 8-12. Start-Up With Load



TPS62A0569A (forced PWM)

V_{IN} = 5.5V, V_{OUT} = 1.8V, I_{OUT} = 0.1A to 2A With 1A/µs

Figure 8-13. Load Transient

8.6 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 2.5V to 5.5V. Make sure that the input power supply has a sufficient current rating for the application.

8.7 Layout

8.7.1 Layout Guidelines

The printed-circuit-board (PCB) layout is an important step to maintain the high performance of the TPS62A056x device family.

- Place the input and output capacitors and the inductor as close as possible to the IC. This action keeps the power traces short. Routing these power traces direct and wide results in low trace resistance and low parasitic inductance.
- Connect the low side of the input and output capacitors properly to the GND pin to avoid a ground potential shift.
- The sense traces connected to FB is a signal trace. Take special care to avoid noise being induced. Keep these traces away from SW nodes.
- Use a common ground. GND layers can be used for shielding.

See Figure 8-14 for the recommended PCB layout.

8.7.2 Layout Example

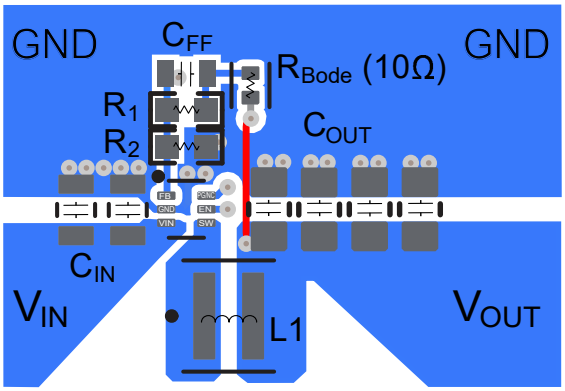


Figure 8-14. TPS62A0569 (SOT563) PCB Layout Recommendation

9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

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TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS62A0569ADRLR	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	-	BARE COPPER	Level-1-260C-UNLIM	-40 to 125	1XH
TPS62A0569PDRLR	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	-	BARE COPPER	Level-1-260C-UNLIM	-40 to 125	1ZK

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

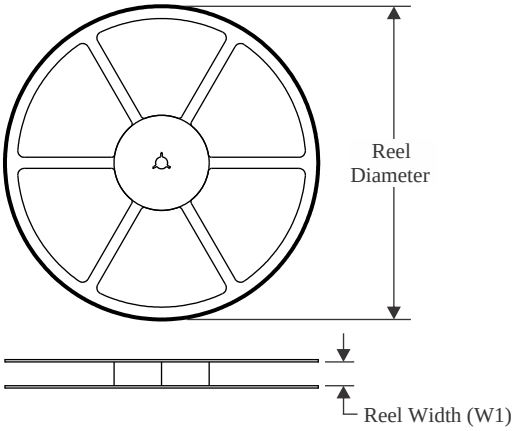
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

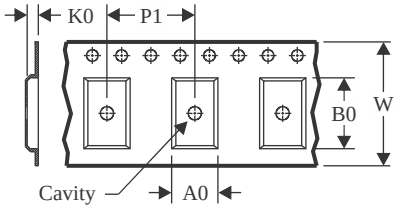
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

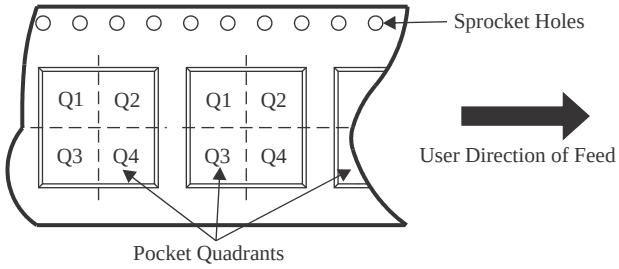


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

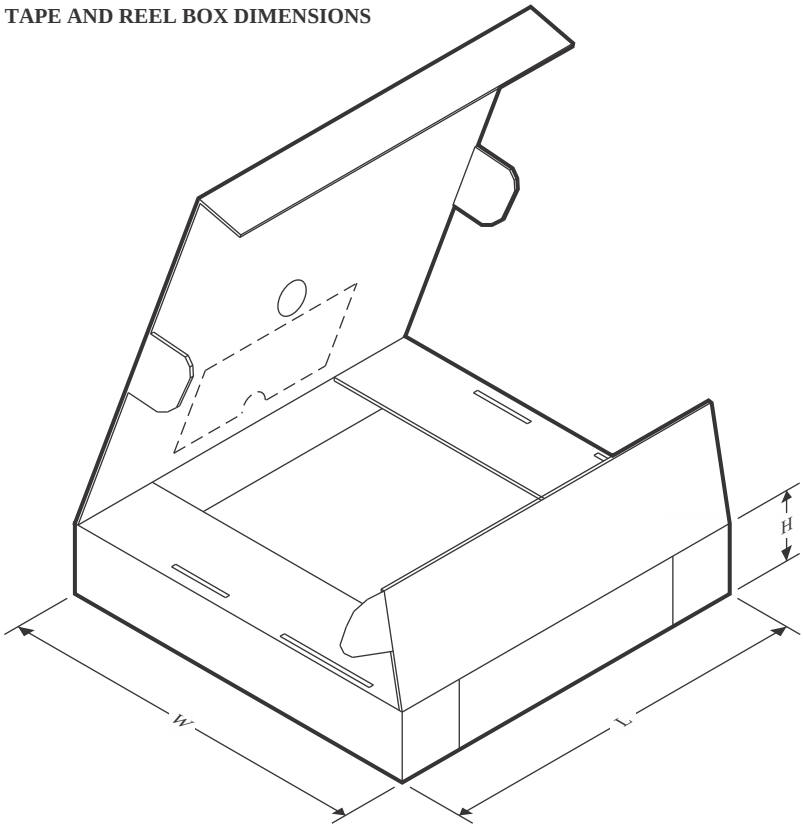
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62A0569ADRLR	SOT-5X3	DRL	6	4000	180.0	8.4	1.8	1.8	0.75	4.0	8.0	Q3
TPS62A0569PDRLR	SOT-5X3	DRL	6	4000	180.0	8.4	1.8	1.8	0.75	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

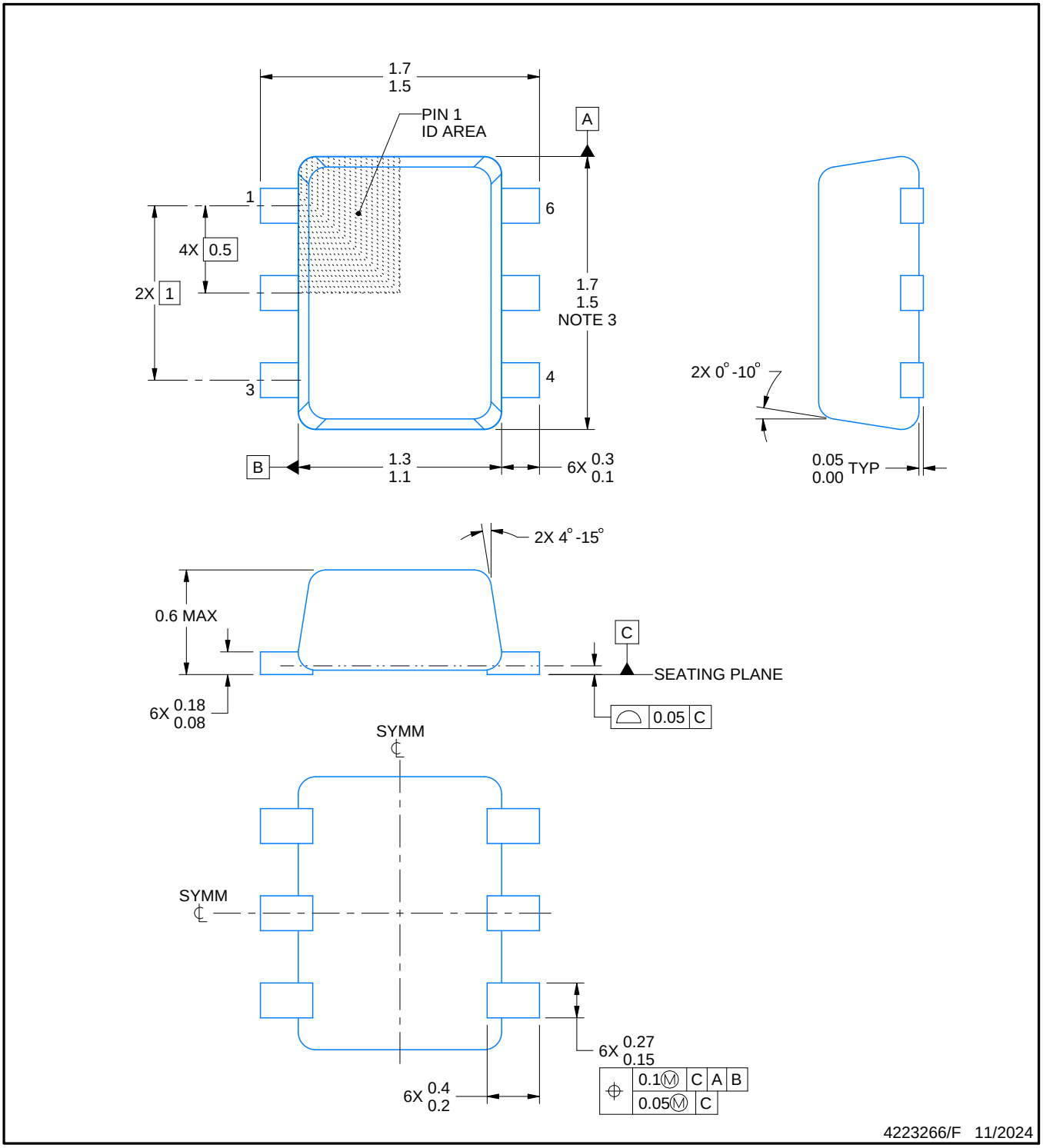
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62A0569ADRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
TPS62A0569PDRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0

PACKAGE OUTLINE

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



NOTES:

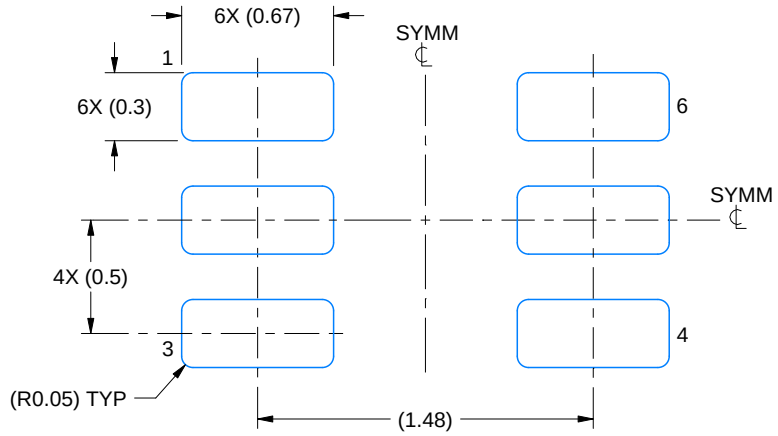
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

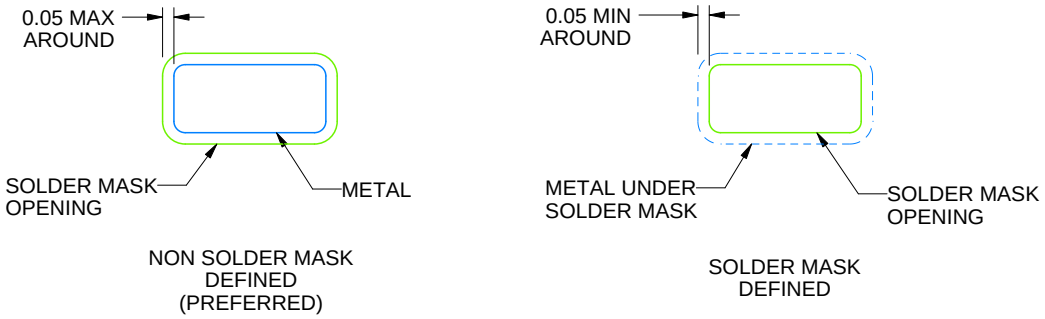
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4223266/F 11/2024

NOTES: (continued)

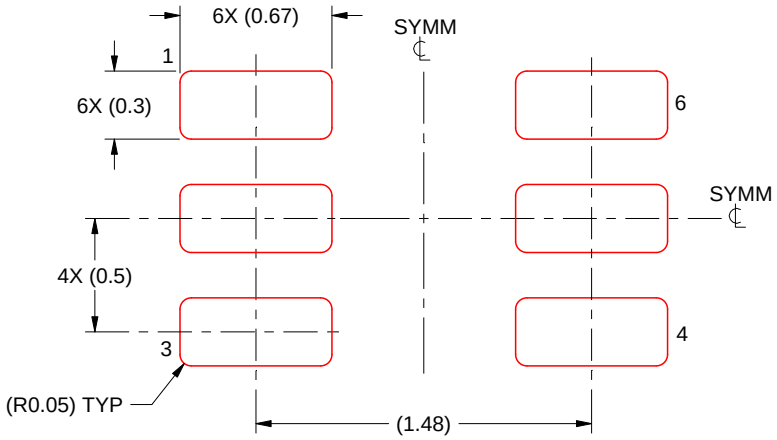
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025