TRIPLE BUCK POWER MANAGEMENT IC

Check for Samples: TPS65232

FEATURES

- **Wide Input Supply Voltage Range (10.8 V - 22 V)**
- **One Adjustable PWM Buck Controller**
  - **10.8-V - 22-V Input Voltage Range**
  - **3.3-V - 6.1-V Output Voltage Range**
  - **500-kHz Switching Frequency**
  - **Type III Compensation**
  - **Programmable Current Limit**
- **Two Adjustable Step-Down Converter With Integrated Switching FETs:**
  - **4.75-V - 5.5-V Input**
  - **0.9-V-3.3-V Output Voltage Range**
  - **3-A Output Current**
  - **1-MHz Switching Frequency**
  - **Type III Compensation**
- **Pull-Up Current Sources on Buck Enable Pins for Accurate Start-Up Timing Control with Preset Default**
- **Over Current Protection on All Rails**
- **Thermal Shutdown to Protect Device During Excessive Power Dissipation**
- **Thermally Enhanced Package for Efficient Heat Management (48-pin HTSSOP or 6-mm x 6-mm 40-Pin QFN)**

APPLICATIONS

- **xDSL and Cable Modems**
- **Wireless Access Points**
- **STB, DTV, DVD and Home Gateway**

DESCRIPTION/ORDERING INFORMATION

The TPS65232 provides one PWM buck controller, two adjustable, synchronous buck regulators. The SMPS have integrated switching FETs for optimized power efficiency and reduced external component count. All power blocks have thermal and over current/short circuit protection. The TPS65232 startup timing can be controlled through buck enable pins. The buck controller and buck converters have internal pole/zero pairs to help stabilizing the system with minimum external components.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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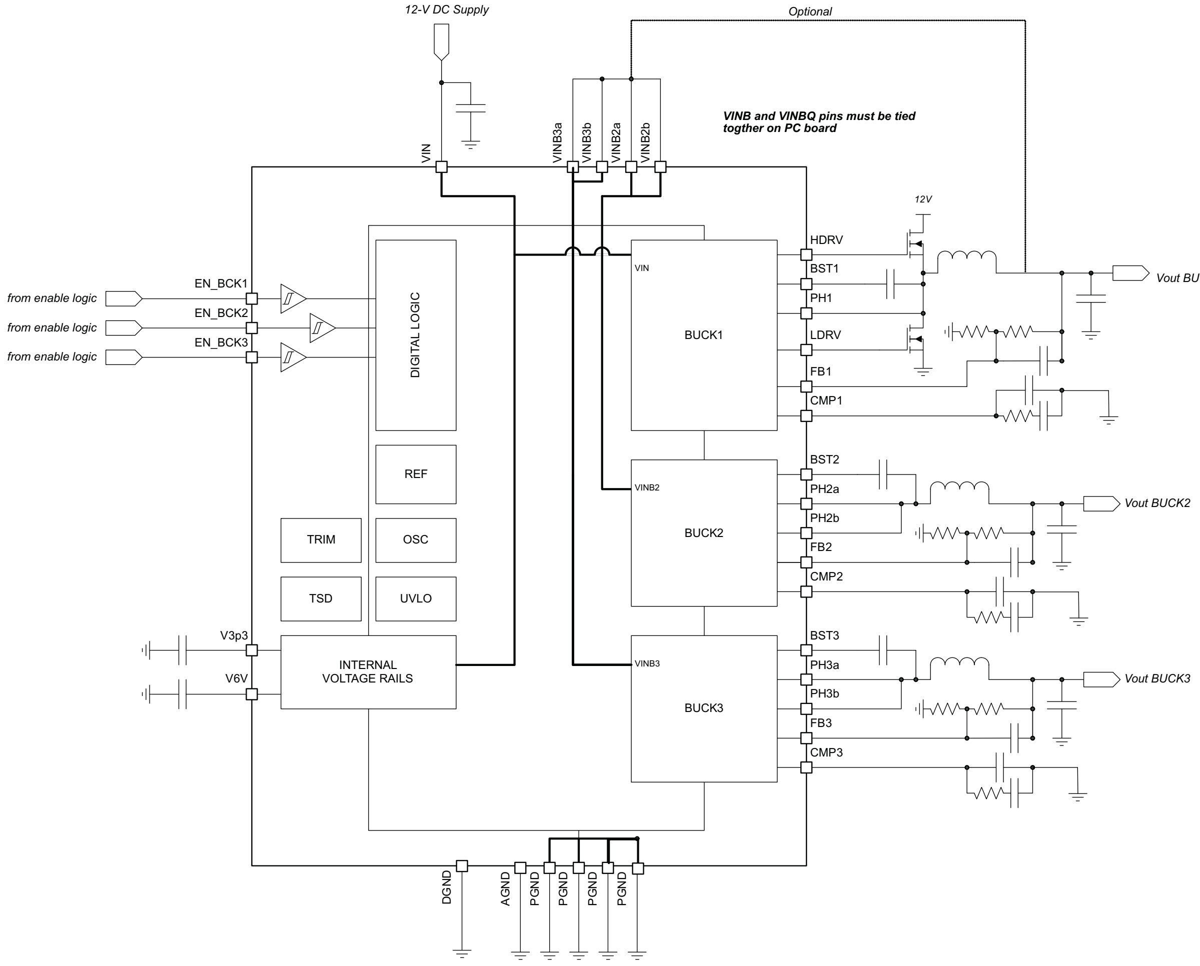
FUNCTIONAL BLOCK DIAGRAM


12-V DC Supply
Optional
VIN
VINB3a
VINB3b
VINB2a
VINB2b
VINB and VINBQ pins must be tied togther on PC board
12V
HDRV
BST1
PH1
LDRV
FB1
CMP1
Vout BUCK1
VIN
BUCK1
EN_BCK1
EN_BCK2
EN_BCK3
from enable logic
from enable logic
from enable logic
DIGITAL LOGIC
REF
TRIM
OSC
TSD
UVLO
V3p3
V6V
INTERNAL VOLTAGE RAILS
VINB2
BUCK2
BST2
PH2a
PH2b
FB2
CMP2
Vout BUCK2
VINB3
BUCK3
BST3
PH3a
PH3b
FB3
CMP3
Vout BUCK3
DGND
AGND
PGND
PGND
PGND
PGND

ORDERING INFORMATION(1)

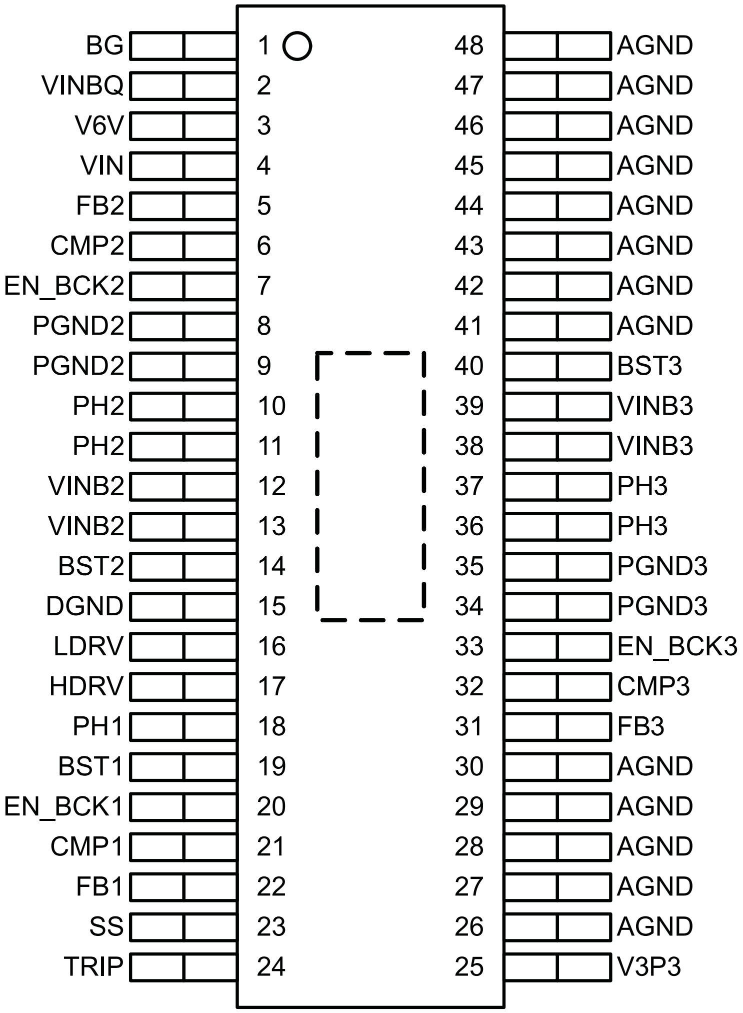
T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 85°C	48-pin (HTSSOP) - DCA	Reel of 2000	TPS65232A2DCAR	TPS65232
	40-pin (QFN) - RHA	Reel of 2500	TPS65232A0RHAR	TPS65232

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

PIN OUT (DCA)

DCA PACKAGE
(TOP VIEW)

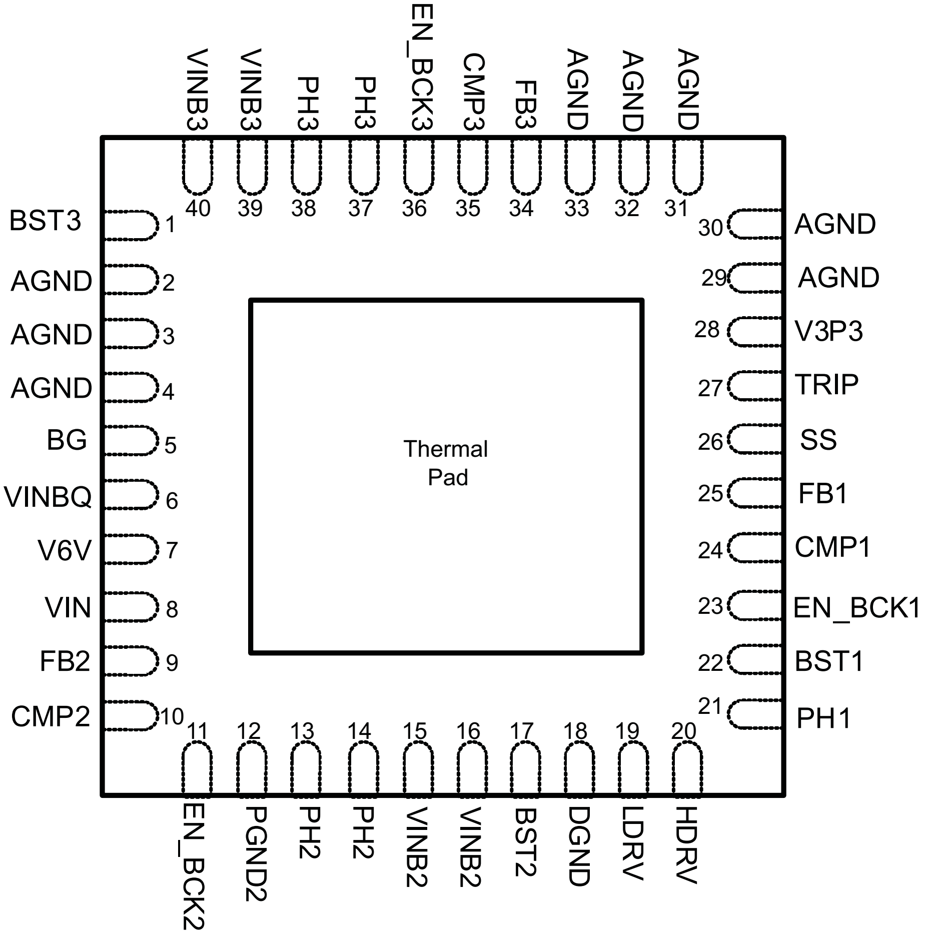

BG 1 48 AGND
VINBQ 2 47 AGND
V6V 3 46 AGND
VIN 4 45 AGND
FB2 5 44 AGND
CMP2 6 43 AGND
EN_BCK2 7 42 AGND
PGND2 8 41 AGND
PGND2 9 40 BST3
PH2 10 39 VINB3
PH2 11 38 VINB3
VINB2 12 37 PH3
VINB2 13 36 PH3
BST2 14 35 PGND3
DGND 15 34 PGND3
LDRV 16 33 EN_BCK3
HDRV 17 32 CMP3
PH1 18 31 FB3
BST1 19 30 AGND
EN_BCK1 20 29 AGND
CMP1 21 28 AGND
FB1 22 27 AGND
SS 23 26 AGND
TRIP 24 25 V3P3

TERMINAL FUNCTIONS (DCA)

NAME	NO.	I/O	DESCRIPTION
BG	1	I	Reference filter pin
VINBQ	2	I	Reference supply for BUCK2 and BUCK3
V6V	3	I	Filter pin for internal voltage regulator (6 V)
VIN	4	I	Input supply for BUCK1 and support circuitry
FB2	5	I	Feedback pin (BUCK2)
CMP2	6	I	Regulator Compensation (BUCK2)
EN_BCK2	7	I	Enable pin for BUCK2, active high
PGND2	8, 9		Power ground BUCK2
PH2	10, 11	O	Switching pin (BUCK2)
VINB2	12, 13		Input supply for BUCK2 (must be tied to VINB3, VINBQ)
BST2	14	I	Bootstrap input (BUCK2)
DGND	15		Digital ground
LDRV	16	O	Low-side gate drive output (PWM controller)
HDRV	17	O	High-side gate drive output (PWM controller)
PH1	18	O	Switching pin (BUCK1)
BST1	19	I	Bootstrap input (BUCK1)
EN_BCK1	20	I	Enable pin for BUCK1, active high
CMP1	21	I	Regulator compensation (PWM controller)
FB1	22	I	Feedback pin (PWM controller)
SS	23	I	External capacitor for soft start
TRIP	24	I	BUCK1 over current trip point set-up
V3P3	25	I	Filter pin for internal voltage regulator (3.3 V)
AGND	26, 27, 28, 29, 30, 41, 42, 43, 44, 45, 46, 47, 48		Analog ground
FB3	31	I	Feedback pin (BUCK3)
CMP3	32	I	Regulator compensation (BUCK3)
EN_BCK3	33	I	Enable pin for BUCK3, active high
PGND3	34, 35		Power ground BUCK3
PH3	36, 37	O	Switching pin (BUCK3)
VINB3	38, 39	I	Input supply for BUCK3 (must be tied to VINB2, VINBQ)
BST3	40	I	Bootstrap input (BUCK3)

PIN OUT (RHA)

RHA PACKAGE
(TOP VIEW)


VINB3 40
VINB3 39
PH3 38
PH3 37
EN_BCK3 36
CMP3 35
FB3 34
AGND 33
AGND 32
AGND 31
BST3 1
AGND 2
AGND 3
AGND 4
BG 5
VINBQ 6
V6V 7
VIN 8
FB2 9
CMP2 10
30 AGND
29 AGND
28 V3P3
27 TRIP
26 SS
25 FB1
24 CMP1
23 EN_BCK1
22 BST1
21 PH1
Thermal Pad
11 EN_BCK2
12 PGND2
13 PH2
14 PH2
15 VINB2
16 VINB2
17 BST2
18 DGND
19 LDRV
20 HDRV

TERMINAL FUNCTIONS (RHA)

NAME	NO.	I/O	DESCRIPTION
BG	5	I	Reference filter pin
VINBQ	6	I	Reference supply for BUCK2 and BUCK3
V6V	7	I	Filter pin for internal voltage regulator (6 V)
VIN	8	I	Input supply for BUCK1 and support circuitry
FB2	9	I	Feedback pin (BUCK2)
CMP2	10	I	Regulator compensation (BUCK2)
EN_BCK2	11	I	Enable pin for BUCK2, active high
PGND2	12		Power ground BUCK2
PH2	13, 14	O	Switching pin (BUCK2)
VINB2	15, 16		Input supply for BUCK2 (must be tied to VINB3, VINBQ)
BST2	17	I	Bootstrap input (BUCK2)
DGND	18		Digital ground
LDRV	19	O	Low-side gate drive output (PWM controller)
HDRV	20	O	High-side gate drive output (PWM controller)
PH1	21	O	Switching pin (BUCK1)
BST1	22	I	Bootstrap input (BUCK1)
EN_BCK1	23	I	Enable pin for BUCK1, active high
CMP1	24	I	Regulator compensation (PWM controller)
FB1	25	I	Feedback pin (PWM controller)
SS	26	I	External capacitor for soft start
TRIP	27	I	BUCK1 over current trip point set-up
V3P3	28	I	Filter pin for internal voltage regulator (3.3 V)
AGND	2, 3, 4, 29, 30, 31, 32, 33		Analog ground
FB3	34	I	Feedback pin (BUCK3)
CMP3	35	I	Regulator Compensation (BUCK3)
EN_BCK3	36	I	Enable pin for BUCK3, active high
PH3	37, 38	O	Switching pin (BUCK3)
VINB3	39, 40	I	Input supply for BUCK3 (must be tied to VINB2, VINBQ)
BST3	1	I	Bootstrap input (BUCK3)

ABSOLUTE MAXIMUM RATINGS(1) (2)

over operating free-air temperature range (unless otherwise noted)

	Input voltage range at VIN		–0.3 to 25	V
	Input voltage range at VINB, VINBQ		–0.3 to 7.0	V
	Voltage range at EN_BCK1, EN_BCK2, EN_BCK3		–0.3 to 3.6	V
	Voltage on HDRV, BST1		–0.3 to 31	V
	Voltage on PH1		–0.3 to 24	V
	Voltage on FB1, CMP1, FB2, CMP2, FB3, CMP3		–0.3 to 3.6	V
	Voltage on PH2, PH3, LDRV		–0.3 to 7.0	V
	Voltage on BST2, BST3		–0.3 to 15	V
	Output current at BUCK2, BUCK3		3.8	A
	Peak output current		Internally limited	
	ESD rating	Human body model (HBM)	2k	V
		Charged device model (CDM)	500	
θ_{JA}	Thermal resistance – Junction to ambient(3)	TSSOP	25	°C/W
		QFN	18.1	
	Continuous total power dissipation 55°C(3) no thermal warning	TSSOP	2.6	W
		QFN	2.5	
T_J	Operating virtual junction temperature range		0 to 150	°C
T_A	Operating ambient temperature range		0 to 85	°C
T_{STG}	Storage temperature range		–65 to 150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

(3) Using JEDEC 51-5 (High K) board. This is based on standard 48DCA package, 4 layers, top/bottom layer: 2 oz Cu, inner layer: 1 oz Cu. Board size: 114.3 x 76.2 mm (4.5 x 3 inches), board thickness: 1.6 mm (0.0629 inch).

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
	Input voltage range at VIN	10.8	12	22	V
	Input voltage range at VINB	4.75		6.1	
	Voltage range, EN_BCK1, EN_BCK2, EN_BCK3	0		3.3	V
T_A	Ambient operating temperature	0		50	°C

ELECTRICAL CHARACTERISTICS

VIN = 12 V ±5%, VINB2, VINB3 = 5 V ±5%, T_J = 0°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE						
VIN	Input supply voltage		10.8	12	22	V
UVLO VIN	UVLO threshold – VIN (main supply)	VIN rising			10.8	V
		VIN falling	4.7			
UVLO VINB	UVLO threshold – VINB (BUCK2/BUCK3 supply)	VINB rising			4.75	V
		VINB falling	4.25			
INPUT CURRENT						
I_{CCQ}	Input supply current	All regulators/USB switches disabled			4	mA
BUCK ENABLE INPUTS (EN_BCK1,2,3)						
VEN	Enable threshold			1.2		V
VEN_{HYS}	Enable voltage hysteresis			100		mV
I_{PULLUP}	Pull-up current	t_{EN} = 0.2 ms/nF		6		µA
R_D	Discharge resistor				1	kΩ
t_D	Discharge time	Power-up		5		ms
PWM CONTROLLER (BUCK1)						
V_{OUT}	Output voltage range(1)		3.3		6.1	V
V_{FB}	Feedback voltage		–2%	0.804	2%	V
LDRV HDRV	High and low side drive voltage	No load		6		V
R_ON_{LDRV}	Low side ON resistance			8		Ω
R_OFF_{LDRV}	Low side OFF resistance			1		Ω
R_ON_{HDRV}	High side ON resistance			20		Ω
R_OFF_{HDRV}	High side OFF resistance			1		Ω
d	Duty cycle(2)		20		80	%
A_{MOD}	Modulator gain			12		
f_{SW}	Switching frequency			500		kHz
I_{TRIP}	Current source for setting OCP trip point	T_A = 25°C		10		µA
TC_{TRIP}	Temperature coefficient of I_{TRIP}			3700		ppm/°C
R_{TRIP}	Current-limit setting resistor		80		250	kW
C_{OUT}	Output capacitance		22(3)			µF
L	Nominal inductance	Recommended		4.7		µH
BUCK2						
V_{OUT}	Output voltage range(1)		0.9		3.3	V
V_{FB}	Feedback voltage		– 2%	0.804	2%	V

(1) Output voltage range is limited by the minimum and maximum duty cycle. V_{OUT}(min) ~ d(min) x V_{INPUT} and V_{OUT}(max) ~ d(max) x V_{INPUT}.
(2) Performance outside these limits is not guaranteed.
(3) Absolute value. User should make allowances for tolerance and variations due to component selection.

ELECTRICAL CHARACTERISTICS (continued)

VIN = 12 V ±5%, VINB2, VINB3 = 5 V ±5%, T_J = 0°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OUT}	Output current				3000	mA
η	Efficiency	I_O = 2 A, V_{OUT} = 3.3V		95		%
$R_{DS(ON)}$	Low-side MOSFET On resistance	VIN12V = 12 V		32		mΩ
	High-side MOSFET On resistance			36		
I_{LIMIT}	Switch current limit			5		A
	Current limit accuracy		–30		30	%
$V_{LINEREG}$	Line regulation - DC ΔVOUT/ΔVINB	VINB = 4.75 V - 6.1 V, I_{OUT} = 1 A			1	%
$V_{LOADREG}$	Load regulation - DC ΔVOUT/ΔIOUT	I_{OUT} = 10 – 90% $I_{OUT,MAX}$		0.5		%/A
V_{OUTTOL}	DC set tolerance	Feedback resistor tolerance not included	–2		2	%
d	Duty cycle(2)		15		85	%
A_{MOD}	Modulator gain			5		
f_{SW}	Switching frequency			1		MHz
C_{OUT}	Output capacitance		10(3)	47		µF
ESR	Capacitor ESR				50	mΩ
L	Nominal inductance			2.2		µH
BUCK3						
V_{OUT}	Output voltage range(4)		0.9		3.3	V
V_{FB}	Feedback voltage		–2%	0.804	2%	V
I_{OUT}	Output current				3	A
η	Efficiency	I_O = 2 A, V_{OUT} = 1.2 V		86		%
$R_{DS(ON)}$	Low-side MOSFET On resistance	VIN12V = 12 V		32		mΩ
	High-side MOSFET On resistance			36		
I_{LIMIT}	Switch current limit			5		A
	Current limit accuracy		–30		30	%
$V_{LINEREG}$	Line regulation - DC ΔVOUT/ΔVINB	VINB = 4.75 V - 6.1 V, I_{OUT} = 1000 mA			1	%
$V_{LOADREG}$	Load regulation - DC ΔVOUT/ΔIOUT	I_{OUT} = 10 – 90% $I_{OUT,MAX}$		0.5		%/A
V_{OUTTOL}	DC Set Tolerance	Feedback resistor tolerance not included	–2		2	%
d	Duty cycle(5)		15		85	%
A_{MOD}	Modulator gain			5		
f_{SW}	Switching frequency			1		MHz
C_{OUT}	Output capacitance		10			µF
ESR	Capacitor ESR				50	mΩ
L	Nominal inductance			2.2		µH

(4) Output voltage range is limited by the minimum and maximum duty cycle. V_{OUT}(min) ~ d(min) x V_{INPUT} and V_{OUT}(max) ~ d(max) x V_{INPUT}.

(5) Performance outside these limits is not guaranteed.

ELECTRICAL CHARACTERISTICS (continued)

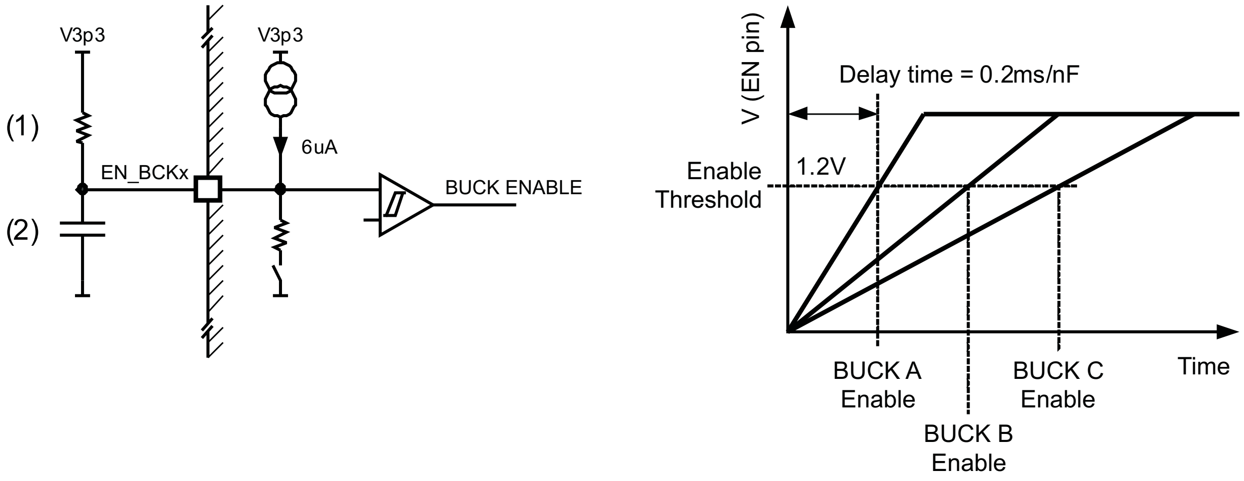
VIN = 12 V ±5%, VINB2, VINB3 = 5 V ±5%, T_J = 0°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SOFT START (BUCK1, 2, and 3)						
I_{SS}	Soft start current source			2		μA
$V_{SS,\ MAX}$	Soft start ramp voltage	Ramp end		0.8		V
C_{SS}	Soft start capacitor	t_{SS} = 0.4 ms/nF	2	3.3	4.7	nF
SSDONE_BK	Deglitch time			2.5		ms
SSDONE_DCH	SS discharge time			500		μs
THERMAL SHUTDOWN						
T_{hot}	Thermal warning			120		°C
T_{trip}	Thermal s/d trip point			160		°C
T_{hyst}	Thermal s/d hysteresis			20		°C

POWER-UP SEQUENCING

ON/OFF control and power sequencing of the three buck regulators is controlled through EN_BCK1, EN_BCK2, and EN_BCK3 enable pins. Each pin is internally connected to a 6-μA constant-current source and monitored by a comparator with Schmitt trigger input with defined threshold. Connecting EN_BCKn pin to ground disables BUCKn and connecting EN_BCKn to V3p3 will enable the respective buck without delay. If more than one buck enable pin is connected to V3p3 the default startup sequence is BUCK1, BUCK2, BUCK3 and the minimum startup delay between rails is the soft-start time (typical 1.5 ms) plus 1 ms.

To create a startup-sequence different from the default, capacitors are connected between the EN_BUCKn pins and ground. At power-up the capacitors are first discharged and then charged to V3p3 level by internal current sources (6 μA typical) creating a constant-slope voltage ramp. A regulator is enabled when its EN pin voltage crosses the enable threshold (typical 1.2 V). A delay of 0.2 ms is generated for each 1-nF of capacitance connected to the enable pin. If two enable pins are pulled high while the third regulator is starting up, the default sequence will be applied to enable the remaining two regulators. To override default power-up sequence it is recommended that delay times differ by more than the soft-start time (typical 1.3 ms) plus 1 ms.



(1) Connect EN_BCKx pin to V3P3 to follow the default power-up sequence or
(2) Connect a capacitor from EN_BCKx to GND to generate a custom power-up sequence.

Figure 1. Customizing the Power-Up Sequence

OVER CURRENT PROTECTION

Over current protection (OCP) for BUCK1 is achieved by comparing the drain-to-source voltage of the low-side MOSFET to a set-point voltage, which is defined by both the internal current source, ITRIP, and the external resistor connected between the TRIP pin and ground. Over current threshold is calculated as follows:

$$I_{LIM} = \frac{R_{TRIP} \bullet I_{TRIP}}{10 \bullet R_{DS(ON)}} \tag{1}$$

ITRIP has a typical value of 10 μA at 25°C and a temperature coefficient of 3700 ppm/°C to compensate the temperature dependency of the MOS $R_{DS(ON)}$. The TPS65232 supports cycle-by-cycle over current limiting control which means that the controller compares the drain-to-source voltage of the low-side FET to the set-point voltage once per switching cycle and blanks out the next switching cycle if an over-current condition is detected. If in the following cycle over current condition is detected again, the controller blanks out 2, then 4, 8, and up to 16 cycles before turning on the high-side driver again. In an over current condition the current to the load exceeds the current to the output capacitor thus the output voltage will drop, and eventually cross the under voltage protection threshold and shut down the BUCK controller. Buck 2 and 3 show a similar mode of operation. All converters operate in “hiccup mode”: Once an over-current is sensed, the controller shuts off the converter for a given time and then tries to start again. If the overload has been removed, the converter will ramp up and operate normally. If this is not the case, the converter will see another over-current event and shuts down again repeating the cycle until the failure is cleared.

SOFT START

Soft start for all three BUCKs is controlled by a single capacitor connected to the SS pin and an internal current source. When one of the BUCKs is enabled, the SS capacitor is pre-charged to the output voltage divided by the feed-back ratio before the internal SS current source starts charging the external capacitor. The output voltage of the BUCK ramps up as the SS pin voltage increased from its pre-charged value to 0.8 V. The soft start time is calculated from the SS supply current (ISS) and the capacitor value and has a typical value of 0.4 ms/nF or 1.3 ms for a 3.3-nF capacitor connected to the SS pin. Before the next rail is enabled, the SS cap is discharged and the SS cycle starts over again.

UNDER VOLTAGE LOCKOUT (UVLO)

TPS65232 monitors VIN and VINB pin voltages and will disable one or more power paths depending on the current use condition:

- If VIN drops below 4.7 V, BUCK1, 2, and 3 are disabled.
- If VINB drops below 4.25 V and either BUCK2 or BUCK3 are enabled, all three output rails are disabled.

UVLO state is not latched and the system recovers as soon as the input voltage rises above its respective threshold. All three BUCK_ENx pins are discharged and remain discharged during UVLO to ensure proper power sequencing when the system recovers.

THERMAL SHUTDOWN (TSD)

TPS65232 monitors junction temperature and will disable the power path (BUCK1-3) if junction temperature rises above the specified trip point. All three BUCK_ENx pins are discharged and remain discharged during TSD to ensure proper power sequencing when the system recovers.

LOOP COMPENSATION

All three BUCKs are voltage mode converters designed to be stable with ceramic capacitors. Refer to Component Selection Procedure section for calculating feedback components.

3.3-V REGULATOR

The TPS65232 has a built-in 3.3-V regulator for powering internal circuitry. The 3.3-V rail can also be used for enabling the BUCK regulators and/or the USB switches, but is not intended for supplying any other external circuitry.

6-V REGULATOR

The TPS65232 has a built-in 6-V regulator for powering internal circuitry.

THERMAL MANAGEMENT AND SAFE OPERATING AREA

Total power dissipation inside TPS65232 is limited not to exceed the maximum allowable junction temperature of 150°C. The maximum allowable power dissipation is a function of the thermal resistance of the package (θ_{JA}) and ambient temperature. θ_{JA} itself is highly dependent on board layout. The maximum allowable power inside the IC for operation at maximum ambient temperature without exceeding the temperature warning flag using the JEDEC High-K board is calculated as follows.

$$\Delta T = \theta_{JA} \bullet P \tag{2}$$

For TSSOP:

$$P_{MAX} = \frac{T_{MAX} - T_{ambient}}{\theta_{JA}} = \frac{120°\text{C} - 55°\text{C}}{25°\text{C/W}} \approx 2.6\ \text{W} \tag{3}$$

For QFN:

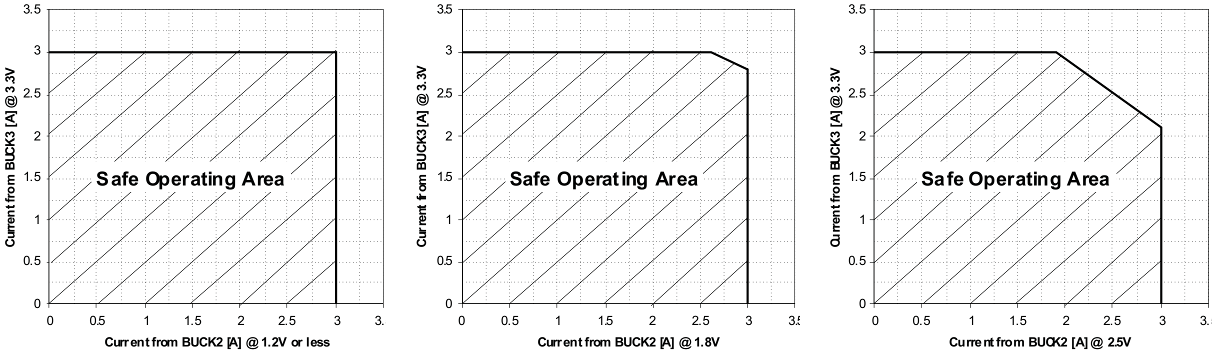
$$P_{MAX} = \frac{T_{MAX} - T_{ambient}}{\theta_{JA}} = \frac{120°\text{C} - 75°\text{C}}{18.1°\text{C/W}} \approx 2.5\ \text{W} \tag{4}$$

For different PCB layout arrangements the thermal resistance (θ_{JA}) will change as the following table shows.

BOARD TYPE	STACK-UP	θ_{JA}
8" x 10" FR4 PCB, four layers	1.5-oz Cu, 60% Cu coverage top layer, 80% Cu coverage bottom layer, no airflow 0.5-oz 30% Cu coverage inner layers	29
8” x 10” FR4 PCB, two layers	1-oz Cu, 20% Cu coverage top layer, 90% Cu coverage bottom layer, no airflow	44

A minimum of two layers of 1-oz Cu with 20% Cu coverage on the top and 90% coverage on the bottom and the use of thermal vias to connect the thermal pad to the bottom layer is recommended. Note that the maximum allowable power inside the device will depend on the board layout. For recommendations on board layout for thermal management using TPS65232 consult your TI field application engineer.

In the example shown above the maximum allowable power dissipation for the IC has been calculated. This figure includes all heat sources inside the device including the power dissipated in BUCK1, BUCK2, BUCK3 and all supporting circuitry. Power dissipated in BUCK1 and all supporting circuitry is approximately 0.4 W and almost independent of the application. Power dissipated in BUCK2 and BUCK3 depends on the output voltage, output current, and efficiency of the switching converters. The following examples of safe operating area assume 90% efficiency for BUCK2 and BUCK3, 3.3-V output from BUCK3 and 1.2-V, 1.8-V, and 2.5-V output from BUCK2, respectively.



For any voltage / current comination inside the shaded area, the dissipated power inside the chip is below the allowable maximum. The examples assume $T_{ambient}$ < 60°C, η = 90% and θ_{JA} < 44°C/W.

Figure 2. Examples of Thermal Safe Operating Area for V(BUCK3) = 3.3 V and V(BUCK1) = 1.2 V, 1.8 V and 2.5 V, Respectively

COMPONENT SELECTION PROCEDURE

The following example illustrates the design procedure for selecting external components for the three buck converters. The example focuses on BUCK1 but the procedure can be directly applied to BUCK2 and BUCK3 as well. The design goal parameters are given in the table below. A list of symbol definitions is found at the end of this section. For this example the schematic in Figure 3 will be used.

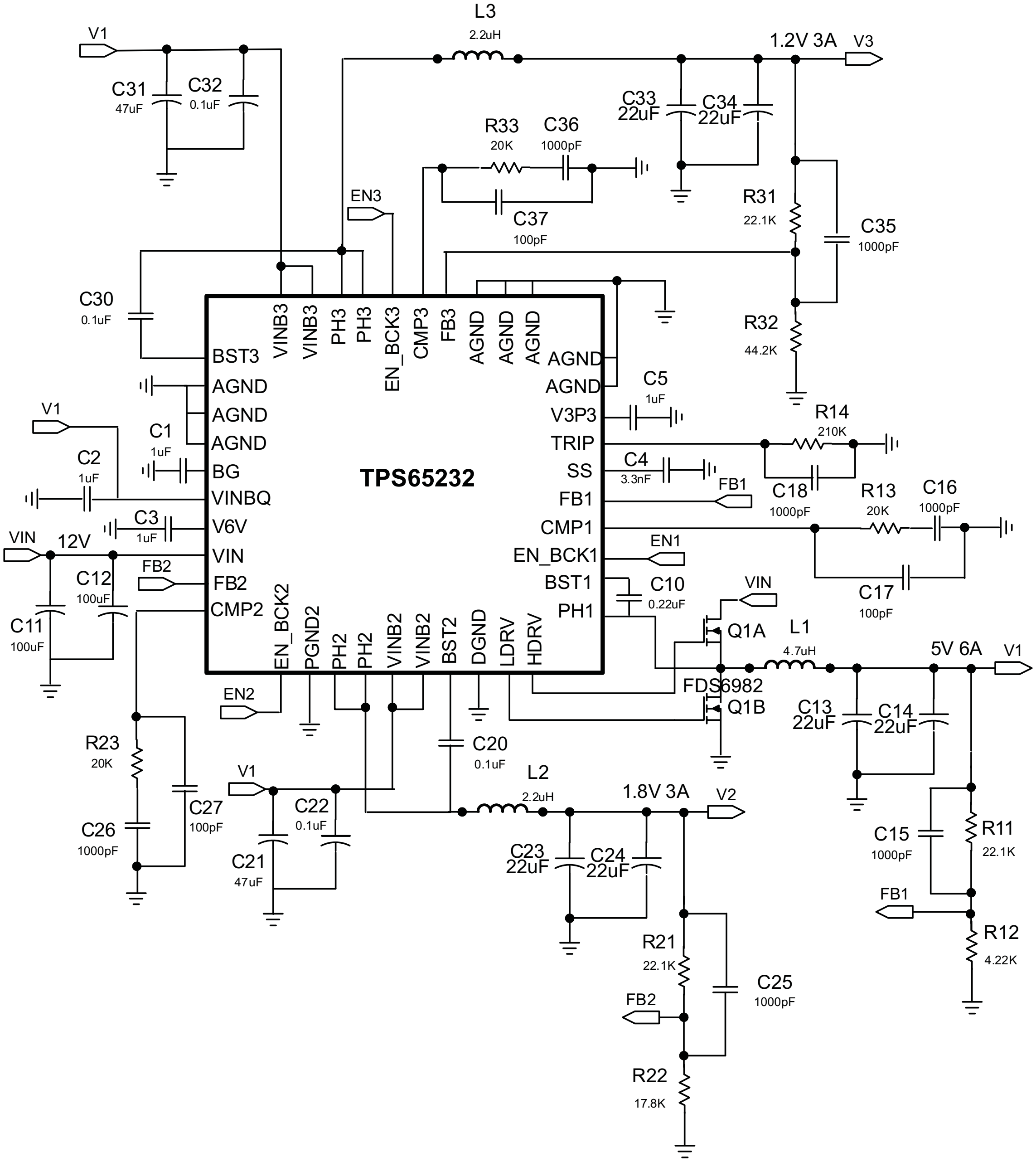

TPS65232
V1
C31 47uF
C32 0.1uF
L3 2.2uH
1.2V 3A
V3
C33 22uF
C34 22uF
R33 20K
C36 1000pF
C37 100pF
EN3
R31 22.1K
C35 1000pF
R32 44.2K
C30 0.1uF
VINB3
VINB3
PH3
PH3
EN_BCK3
CMP3
FB3
AGND
AGND
AGND
BST3
AGND
AGND
AGND
BG
VINBQ
V6V
VIN
FB2
CMP2
AGND
AGND
V3P3
TRIP
SS
FB1
CMP1
EN_BCK1
BST1
PH1
C5 1uF
R14 210K
C4 3.3nF
C18 1000pF
R13 20K
C16 1000pF
C17 100pF
EN1
C10 0.22uF
VIN
Q1A
L1 4.7uH
5V 6A
V1
FDS6982
Q1B
C13 22uF
C14 22uF
C1 1uF
C2 1uF
C3 1uF
VIN 12V
C12 100uF
C11 100uF
FB2
EN_BCK2
PGND2
PH2
PH2
VINB2
VINB2
BST2
DGND
LDRV
HDRV
EN2
R23 20K
C27 100pF
C26 1000pF
V1
C21 47uF
C22 0.1uF
C20 0.1uF
L2 2.2uH
1.8V 3A
V2
C23 22uF
C24 22uF
R21 22.1K
FB2
C25 1000pF
R22 17.8K
C15 1000pF
R11 22.1K
FB1
R12 4.22K

Figure 3. Sample Schematic for TPS65232

BUCK1 DESIGN GUIDELINE

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input supply voltage		10.8	12	13.2	V
$V_{IN\ RIPPLE}$	Input voltage ripple	$I_{OUT,\ BUCK1}$ = 6 A			75	mV
V_{OUT}	Output voltage		4.75	5	5.25	V
	Line regulation	V_{IN} = 10.8 V to 13.2 V		25		mV
	Load regulation	$I_{OUT,\ BUCK1}$ = 0 A to 6 A		25		mV
$V_{OUT\ RIPPLE}$	Output ripple	$I_{OUT,\ BUCK1}$ = 6 A			75	mV
V_{TRANS}	Transient deviation	$I_{OUT,\ BUCK1}$ = 1.5 A to 3 A		50		mV
I_{OUT}	Output current	V_{IN} = 10.8 V to 13.2 V	0		6	A
f_{SW}	Switching frequency			500		kHz

INDUCTOR SELECTION (L1)

The inductor is typically sized for < 30% peak-to-peak ripple current (I_{RIPPLE}). Given this target ripple current, the required inductor size is calculated by Equation 5.

$$L = \frac{V_{IN(MAX)} - V_{OUT}}{0.3 \bullet I_{OUT}} \bullet \frac{V_{OUT}}{V_{IN(MAX)}} \bullet \frac{1}{f_{SW}} \tag{5}$$

Solving Equation 5 with $V_{IN(MAX)}$ = 13.2 V, an inductor value of 3.5 µH is obtained. A standard value of 4.7 µH is selected, resulting in 1.25-A peak-to-peak ripple. The RMS current through the inductor is approximated by Equation 6.

$$I_{L(RMS)} = \sqrt{\left(I_{L(avg)}{}^{2} + \frac{1}{12}\left(I_{RIPPLE}\right)^{2}\right)} = \sqrt{\left(I_{OUT}\right)^{2} + \frac{1}{12}\left(I_{RIPPLE}\right)^{2}} \tag{6}$$

Using Equation 6, the maximum RMS current in the inductor is about 6.01 A.

OUTPUT CAPACITOR SELECTION (C13, C14)

The selection of the output capacitor is typically driven by the output load transient response requirement.

Equation 7 and Equation 8 estimate the output capacitance required for a given output voltage transient deviation.

$$C_{OUT(MIN)} = \frac{I_{TRAN(MAX)}{}^{2} \bullet L}{\left(V_{IN(MIN)} - V_{OUT}\right) \bullet V_{TRAN}} \quad \text{when } V_{IN(MIN)} < 2 \bullet V_{OUT} \tag{7}$$

$$C_{OUT(MIN)} = \frac{I_{TRAN(MAX)}{}^{2} \bullet L}{V_{OUT} \bullet V_{TRAN}} \quad \text{when } V_{IN(MIN)} > 2 \bullet V_{OUT} \tag{8}$$

For this example, Equation 8 is used in calculating the minimum output capacitance.

Based on a 1.5-A load transient with a maximum 50-mV deviation, a minimum of 42-µF output capacitance is required. We choose two 22-µF capacitors in parallel for a total capacitance of 44 µF.

The output ripple is divided into two components. The first is the ripple generated by the inductor ripple current flowing through the output capacitor’s capacitance, and the second is the voltage generated by the ripple current flowing in the output capacitor’s ESR. The maximum allowable ESR is then determined by the maximum ripple voltage and is approximated by Equation 9.

$$ESR_{MAX} = \frac{V_{RIPPLE(total)} - V_{RIPPLE(cap)}}{I_{RIPPLE}} = \frac{V_{RIPPLE(total)} - \left(\frac{I_{RIPPLE}}{C_{OUT} \bullet f_{SW}}\right)}{I_{RIPPLE}} \tag{9}$$

Based on 44-µF of capacitance, 1.25-A ripple current, 500-kHz switching frequency and a design goal of 75-mV ripple voltage, we calculate a capacitive ripple component of 56 mV and an maximum ESR of 15 mΩ. Two 1210, 47-µF, 10-V X5R ceramic capacitors are selected to provide significantly less than 15-mΩ of ESR.

PEAK CURRENT RATING OF THE INDUCTOR

With output capacitance known, it is now possible to calculate the charging current during start-up and determine the minimum saturation current rating of the inductor. The start-up charging current is approximated by Equation 10.

$$I_{CHARGE} = \frac{V_{OUT} \bullet C_{OUT}}{T_{SS}} \tag{10}$$

Using the TPS65232's recommended 1.3-ms soft-start time, C_{OUT} = 44 µF and V_{OUT} = 5 V, I_{CHARGE} is found to be 169 mA. The peak current rating of the inductor is now found by Equation 11.

$$I_{L(PEAK)} = I_{OUT(MAX)} + \frac{1}{2} I_{RIPPLE} + I_{CHARGE} \tag{11}$$

For this example an inductor with a peak current rating of 6.79 A is required.

INPUT CAPACITOR SELECTION (C11, C12)

The input voltage ripple is divided between capacitance and ESR. For this design, $V_{RIPPLE(CAP)}$ = 50 mV and $V_{RIPPLE(ESR)}$ = 25 mV. The minimum capacitance and maximum ESR are estimated by Equation 12 and Equation 13.

$$C_{IN(MIN)} = \frac{I_{LOAD} \bullet V_{OUT}}{V_{RIPPLE(cap)} \bullet V_{IN} \bullet f_{SW}} \tag{12}$$

$$ESR_{MAX} = \frac{V_{RIPPLE(ESR)}}{I_{LOAD} + \frac{1}{2} I_{RIPPLE}} \tag{13}$$

For this design, C_{IN} > 100 µF and ESR < 3.7 mΩ. The RMS current in the output capacitors is estimated by Equation 14.

$$I_{RMS(CIN)} = I_{IN(RMS)} - I_{IN(avg)} = \sqrt{\left((I_{OUT})^2 + \frac{1}{12}(I_{RIPPLE})^2\right) \bullet \frac{V_{OUT}}{V_{IN}}} - \frac{V_{OUT} \bullet I_{OUT}}{V_{IN}} \tag{14}$$

With V_{IN} = $V_{IN(MAX)}$, the input capacitors must support a ripple current of 1.4-A RMS. The two 1210, 47-µF X5R ceramic capacitors with about 5-mΩ ESR and 2-A RMS current rating are selected. It is important to check the DC bias voltage de-rating curves to ensure the capacitors provide sufficient capacitance at the working voltage.

BOOTSTRAP CAPACITOR (C10)

To ensure proper charging of the high-side MOSFET gate, limit the ripple voltage on the bootstrap capacitor to < 5% of the minimum gate drive voltage.

$$C_{BOOST} = \frac{20 \bullet Q_{GS,\,HSD}}{V_{IN(MIN)}} \tag{15}$$

Based on the FDS6982 MOSFET with a maximum total gate charge of 12 nC, calculate a minimum of 22-nF of capacitance. A standard value of 220 nF is selected.

SHORT CIRCUIT PROTECTION (R14, C18) (BUCK1 ONLY)

The TPS65232 uses the forward drop across the low-side MOSFET during the OFF time to measure the inductor current. The voltage drop across the low-side MOSFET is given by Equation 16.

$$V_{DS} = I_{L(PEAK)} \bullet R_{DSON,\,LSD} \tag{16}$$

When V_{IN} = 10.8 V to 13.2 V, I_{PEAK} = 7.4 A. Using the FDS6982 MOSFET with a $R_{DSON,MAX}$ at T_J = 25°C of 20 mΩ we calculate the peak voltage drop to be 148 mV. Solving Equation 1 for R_{TRIP} and using I_{TRIP} = 10 µA:

$$R14 = R_{TRIP} = R_{DS(ON)} \bullet I_{LIM} \bullet 10^6 \tag{17}$$

We calculate a trip resistor value of 210 kΩ. Place a 1-nF capacitor parallel to R14. Please note that typical FET $R_{DS(ON)}$ is specified at 10 mΩ. Since we used $R_{DSON,MAX}$, for setting the current limit, the actual current flowing through the inductor with a nominal FET can be higher than the peak current of 7.4 A before the current limit kicks in. Make sure that the chosen inductor has the correct peak current capabilities.

FEEDBACK LOOP DESIGN

TPS65232 loop compensation looks like a type-II compensation network because an internal zero-pole pair can provide additional phase boost to stabilize this voltage mode control DC/DC controller. The internal zero is located at 45 kHz and the pole is located at 240 kHz. Ideally, the best cross-over frequency is around 1/10th of the switching frequency.

FEEDBACK DIVIDER (R11, R12)

Select R11 between 10 kΩ and 100 kΩ. For this design select 22.1 kΩ. Next, R12 Is selected to produce the desired output voltage when V_{FB} = 0.8 V using the following formula:

$$R12 = \frac{V_{FB} \bullet R11}{V_{OUT} - V_{FB}} \tag{18}$$

V_{FB} = 0.8 V and R11 = 22.1 KΩ for V_{OUT} = 5.0 V, R12 = 4.22 kΩ.

Error Amplifier Pole-Zero Selection

The design guidelines for TPS65232 Buck1 loop compensation are as follows:

1. Place a compensation zero at 8 kHz to boost the phase margin at the anticipated cross-over frequency.
2. Set the value of R and C of this to zero: C16 = 1000 pF and R13 = 20 kΩ.
3. Add an additional pole by making C17 = 100 pF. This pole is used to attenuate high frequency noise.
4. If V_{IN} is 20 V - 24 V, make C17 = 200 pF.

BUCK2 DESIGN GUIDELINE

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input supply voltage		4.75	5	6	V
$V_{IN\ RIPPLE}$	Input voltage ripple	$I_{OUT,\ BUCK1}$ = 3 A			75	mV
V_{OUT}	Output voltage			1.8		V
	Line regulation	V_{IN} = 3 V to 6 V		18		mV
	Load regulation	$I_{OUT,\ BUCK1}$ = 0 A to 3 A		18		mV
$V_{OUT\ RIPPLE}$	Output ripple	$I_{OUT,\ BUCK1}$ = 3 A			36	mV
V_{TRANS}	Transient deviation	$I_{OUT,\ BUCK1}$ = 1.5 A to 3 A		50		mV
I_{OUT}	Output current	V_{IN} = 3 V to 6 V	0		3	A
f_{SW}	Switching frequency			1000		kHz

INDUCTOR SELECTION (L2)

The inductor is typically sized for < 30% peak-to-peak ripple current (I_{RIPPLE}). Given this target ripple current, the required inductor size is calculated by Equation 5.

$$L = \frac{V_{IN(MAX)} - V_{OUT}}{0.3 \bullet I_{OUT}} \bullet \frac{V_{OUT}}{V_{IN(MAX)}} \bullet \frac{1}{f_{SW}} \tag{19}$$

Solving Equation 19 with $V_{IN(MAX)}$ = 6 V, an inductor value of 1.4 µH is obtained. A standard value of 2.2 µH is selected, resulting in 0.37-A peak-to-peak ripple. The RMS current through the inductor is approximated by Equation 6.

$$I_{L(RMS)} = \sqrt{\left(I_{L(avg)}{}^{2} + \frac{1}{12}(I_{RIPPLE})^{2}\right)} = \sqrt{(I_{OUT})^{2} + \frac{1}{12}(I_{RIPPLE})^{2}} \tag{20}$$

Using Equation 20, the maximum RMS current in the inductor is about 3.002 A.

OUTPUT CAPACITOR SELECTION (C23, C24)

The selection of the output capacitor is typically driven by the output load transient response requirement.

Equation 21 and Equation 22 estimate the output capacitance required for a given output voltage transient deviation.

$$C_{OUT(MIN)} = \frac{I_{TRAN(MAX)}^{2} \bullet L}{(V_{IN(MIN)} - V_{OUT}) \bullet V_{TRAN}} \quad \text{when } V_{IN(MIN)} < 2 \bullet V_{OUT} \tag{21}$$

$$C_{OUT(MIN)} = \frac{I_{TRAN(MAX)}^{2} \bullet L}{V_{OUT} \bullet V_{TRAN}} \quad \text{when } V_{IN(MIN)} > 2 \bullet V_{OUT} \tag{22}$$

For this example, Equation 22 is used in calculating the minimum output capacitance.

Based on a 1-A load transient with a maximum 54-mV deviation, a minimum of 26-μF output capacitance is required. We choose two 22-μF capacitors in parallel for a total capacitance of 44 μF.

The output ripple is divided into two components. The first is the ripple generated by the inductor ripple current flowing through the output capacitor's capacitance, and the second is the voltage generated by the ripple current flowing in the output capacitor's ESR. The maximum allowable ESR is then determined by the maximum ripple voltage and is approximated by Equation 23.

$$ESR_{MAX} = \frac{V_{RIPPLE(total)} - V_{RIPPLE(cap)}}{I_{RIPPLE}} = \frac{V_{RIPPLE(total)} - \left(\frac{I_{RIPPLE}}{C_{OUT} \bullet f_{SW}}\right)}{I_{RIPPLE}} \tag{23}$$

Based on 44-μF of capacitance, 0.37-A ripple current, 1-MHz switching frequency and a design goal of 36-mV ripple voltage, we calculate a maximum ESR of 76 mΩ. Two 1210, 22-μF, 10-V X5R ceramic capacitors are selected to provide significantly less than 76-mΩ of ESR.

PEAK CURRENT RATING OF THE INDUCTOR

With output capacitance known, it is now possible to calculate the charging current during start-up and determine the minimum saturation current rating of the inductor. The start-up charging current is approximated by Equation 24.

$$I_{CHARGE} = \frac{V_{OUT} \bullet C_{OUT}}{T_{SS}} \tag{24}$$

Using the common start time (1 ms), C_{OUT} = 44 μF and V_{OUT} = 1.8 V, I_{CHARGE} is found to be 79 mA. The peak current rating of the inductor is now found by Equation 25.

$$I_{L(PEAK)} = I_{OUT(MAX)} + \frac{1}{2} I_{RIPPLE} + I_{CHARGE} \tag{25}$$

For this example an inductor with a peak current rating of 3.264 A is required.

INPUT CAPACITOR SELECTION (C21, C22)

The input voltage ripple is divided between capacitance and ESR. For this design, $V_{RIPPLE(CAP)}$ = 50 mV and $V_{RIPPLE(ESR)}$ = 25 mV. The minimum capacitance and maximum ESR are estimated by Equation 26 and Equation 27.

$$C_{IN(MIN)} = \frac{I_{LOAD} \bullet V_{OUT}}{V_{RIPPLE(cap)} \bullet V_{IN} \bullet f_{SW}} \tag{26}$$

$$ESR_{MAX} = \frac{V_{RIPPLE(ESR)}}{I_{LOAD} + \frac{1}{2} I_{RIPPLE}} \tag{27}$$

For this design, C_{IN} > 32 μF and ESR < 7.8 mΩ. The RMS current in the output capacitors is estimated by Equation 28.

$$I_{RMS(CIN)} = I_{IN(RMS)} - I_{IN(avg)} = \sqrt{\left((I_{OUT})^2 + \frac{1}{12}(I_{RIPPLE})^2\right) \bullet \frac{V_{OUT}}{V_{IN}}} - \frac{V_{OUT} \bullet I_{OUT}}{V_{IN}} \tag{28}$$

With $V_{IN} = V_{IN(TYP)}$, the input capacitors must support a ripple current of 0.58-A RMS. The two 1210, 47-µF X5R ceramic capacitors with about 5-mΩ ESR and 2-A RMS current rating are selected. It is important to check the DC bias voltage de-rating curves to ensure the capacitors provide sufficient capacitance at the working voltage.

BOOTSTRAP CAPACITOR (C20)

A standard value of 100 nF is selected.

SHORT CIRCUIT PROTECTION

Current limits for BUCK2 are internally set to 5 A.

FEEDBACK LOOP DESIGN

TPS65232 loop compensation looks like a type-II compensation network because an internal zero-pole pair can provide additional phase boost to stabilize this voltage mode control DC/DC controller. The internal zero is located at 45 kHz and the pole is located at 240 kHz. Ideally, the best cross-over frequency is around 1/10th of the switching frequency.

FEEDBACK DIVIDER (R21, R22)

Select R21 between 10 kΩ and 100 kΩ. For this design select 22.1 kΩ. Next, R22 Is selected to produce the desired output voltage when V_{FB} = 0.8 V using the following formula:

$$R22 = \frac{V_{FB} \bullet R21}{V_{OUT} - V_{FB}} \tag{29}$$

V_{FB} = 0.8 V and R21 = 22.1 KΩ for V_{OUT} = 1.8 V, R22 = 17.8 kΩ.

Error Amplifier Pole-Zero Selection

The design guidelines for TPS65232 BUCK2 loop compensation are as follows:

1. Place a compensation zero at 8 kHz to boost the phase margin at the anticipated cross-over frequency.
2. Set the value of R and C of this to zero: C26 = 1000 pF and R23 = 20 kΩ.
3. Add an additional pole by making C27 = 100 pF. This pole is used to attenuate high frequency noise.

BUCK3 DESIGN GUIDELINE

Both BUCK2 and BUCK3 have the same internal structure. Thus, BUCK2's design guideline can be applied to BUCK3's design directly.

OTHER COMPONENTS

A 1-µF ceramic capacitor should be connected as close as possible to the following pins:

- BG: Bandgap reference
- VIN: Bypass capacitor
- V6V: Internal 6-V supply
- V3P3: Internal 3.3-V supply

SIX RAIL POWER SYSTEM

The following example illustrates two TPS65232 ICs can provide six power rails and the low output voltage rail is capable of delivering 10-A load current with high efficiency.

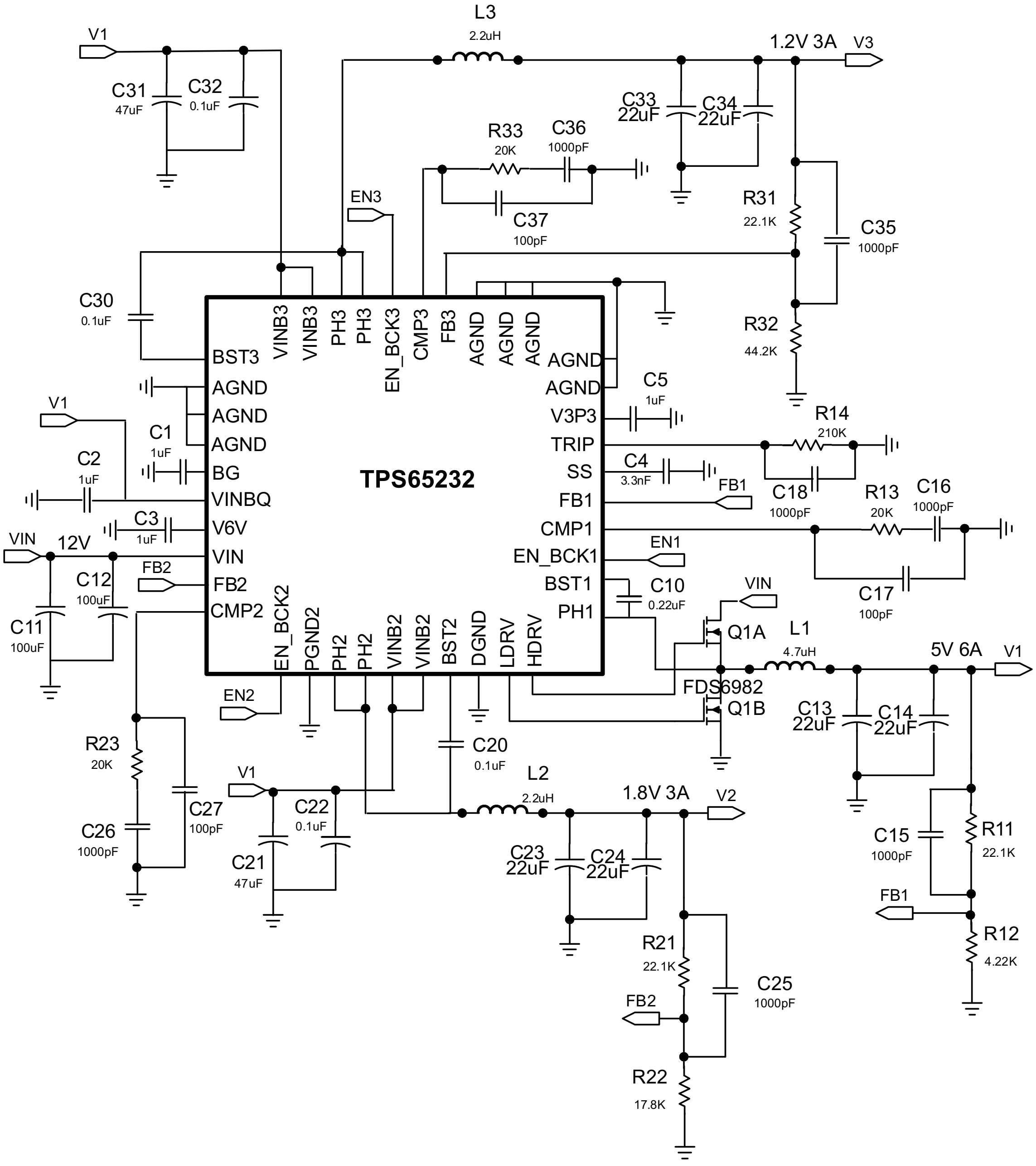

V1
L3
2.2uH
1.2V 3A
V3
C31
47uF
C32
0.1uF
C33
22uF
C34
22uF
R33
20K
C36
1000pF
EN3
C37
100pF
R31
22.1K
C35
1000pF
C30
0.1uF
R32
44.2K
VINB3
VINB3
PH3
PH3
EN_BCK3
CMP3
FB3
AGND
AGND
AGND
BST3
AGND
AGND
AGND
BG
VINBQ
V6V
VIN
FB2
CMP2
AGND
AGND
V3P3
TRIP
SS
FB1
CMP1
EN_BCK1
BST1
PH1
TPS65232
EN_BCK2
PGND2
PH2
PH2
VINB2
VINB2
BST2
DGND
LDRV
HDRV
V1
C1
1uF
C2
1uF
C3
1uF
VIN
12V
C12
100uF
FB2
C11
100uF
C5
1uF
R14
210K
C4
3.3nF
FB1
C18
1000pF
R13
20K
C16
1000pF
EN1
C10
0.22uF
C17
100pF
VIN
Q1A
L1
4.7uH
5V 6A
V1
FDS6982
Q1B
C13
22uF
C14
22uF
EN2
R23
20K
C20
0.1uF
L2
2.2uH
1.8V 3A
V2
V1
C22
0.1uF
C27
100pF
C26
1000pF
C21
47uF
C23
22uF
C24
22uF
C15
1000pF
R11
22.1K
FB1
R12
4.22K
R21
22.1K
FB2
C25
1000pF
R22
17.8K

Figure 4. Six Rail Power System Part I: 5 V, 1.8 V and 1.2 V

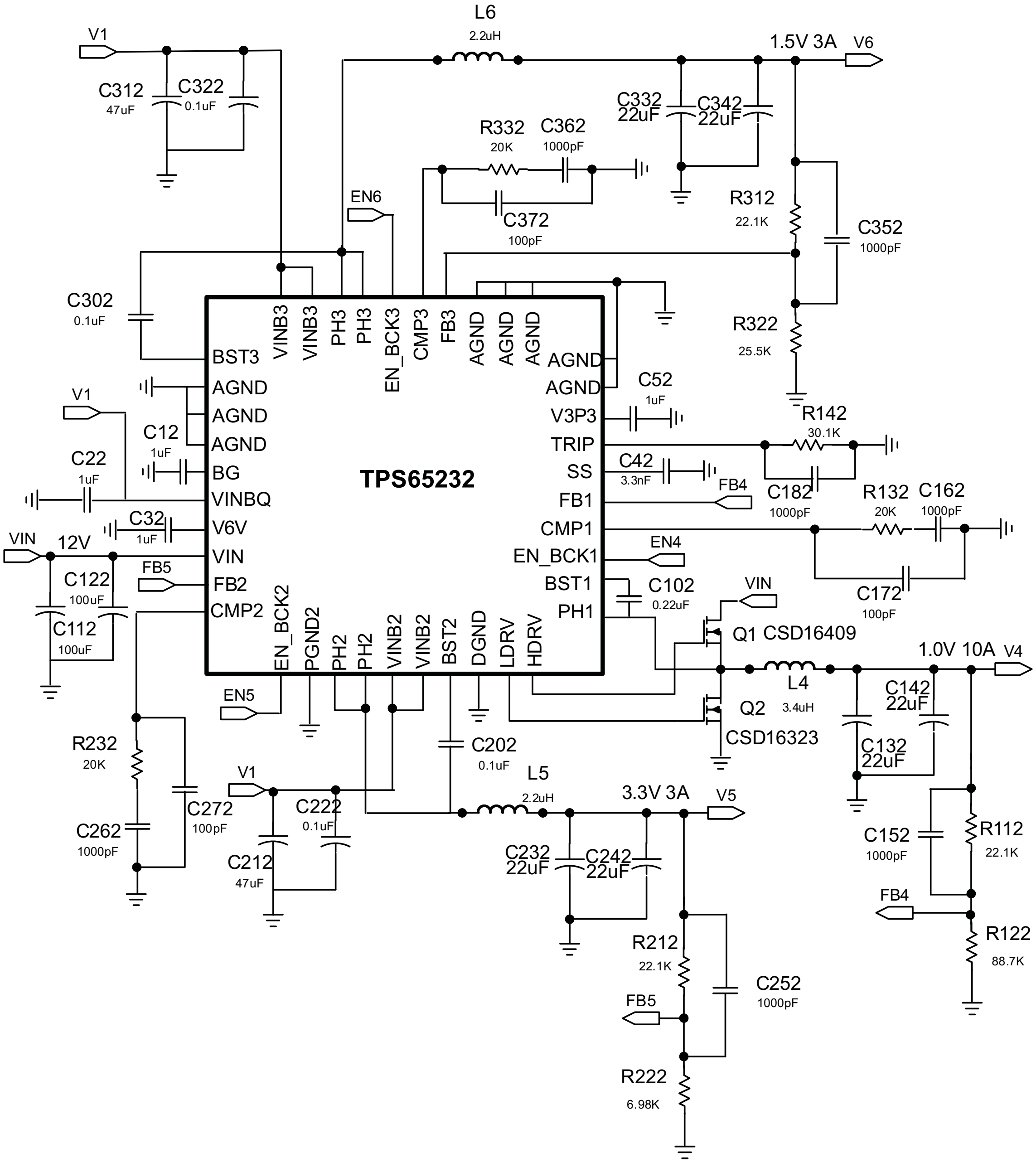

V1
C312
47uF
C322
0.1uF
L6
2.2uH
1.5V 3A
V6
C332
22uF
C342
22uF
R332
20K
C362
1000pF
C372
100pF
EN6
R312
22.1K
C352
1000pF
C302
0.1uF
R322
25.5K
VINB3
VINB3
PH3
PH3
EN_BCK3
CMP3
FB3
AGND
AGND
AGND
BST3
AGND
AGND
AGND
BG
VINBQ
V6V
VIN
FB2
CMP2
TPS65232
AGND
AGND
V3P3
TRIP
SS
FB1
CMP1
EN_BCK1
BST1
PH1
V1
C12
1uF
C22
1uF
C32
1uF
VIN
12V
C122
100uF
C112
100uF
FB5
C52
1uF
R142
30.1K
C42
3.3nF
FB4
C182
1000pF
R132
20K
C162
1000pF
EN4
C102
0.22uF
C172
100pF
VIN
Q1 CSD16409
1.0V 10A
V4
L4
3.4uH
Q2
CSD16323
C142
22uF
C132
22uF
EN_BCK2
PGND2
PH2
PH2
VINB2
VINB2
BST2
DGND
LDRV
HDRV
EN5
R232
20K
C262
1000pF
C272
100pF
V1
C222
0.1uF
C212
47uF
C202
0.1uF
L5
2.2uH
3.3V 3A
V5
C232
22uF
C242
22uF
C152
1000pF
R112
22.1K
FB4
R122
88.7K
R212
22.1K
FB5
C252
1000pF
R222
6.98K

Figure 5. Six Rail Power System Part II: 3.3 V, 1.5 V and 1 V

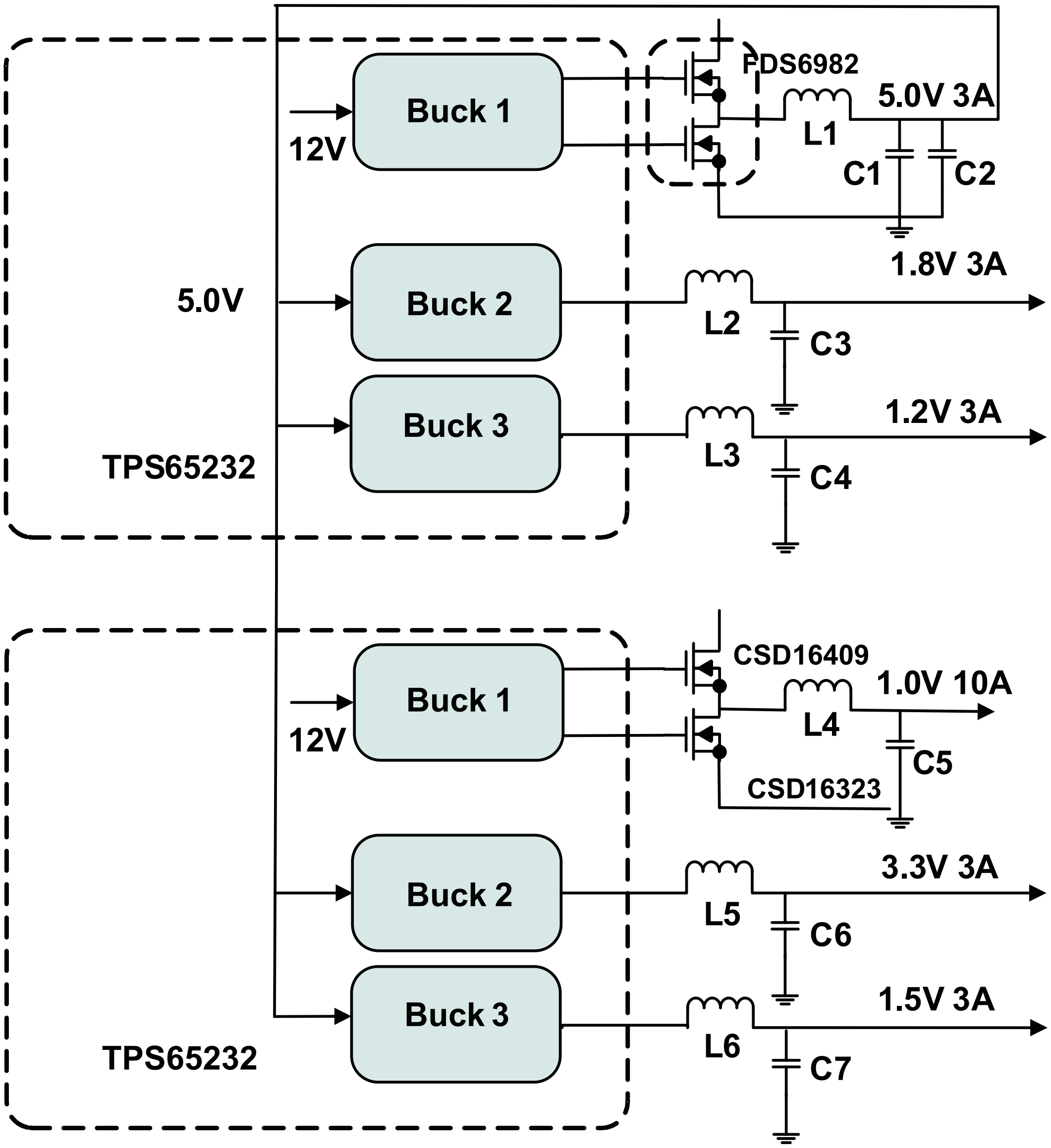

FDS6982
5.0V 3A
Buck 1
12V
L1
C1
C2
5.0V
Buck 2
1.8V 3A
L2
C3
Buck 3
1.2V 3A
L3
C4
TPS65232
CSD16409
Buck 1
1.0V 10A
12V
L4
C5
CSD16323
Buck 2
3.3V 3A
L5
C6
Buck 3
1.5V 3A
L6
C7
TPS65232

Figure 6. Six Rail Power System Block Diagram

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS65232A0RHA	Active	Production	VQFN (RHA) | 40	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	0 to 85	TPS 65232 A0
TPS65232A0RHA.B	Active	Production	VQFN (RHA) | 40	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	0 to 85	TPS 65232 A0
TPS65232A0RHAR	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 85	TPS 65232
TPS65232A0RHAR.B	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 85	TPS 65232
TPS65232A2DCA	Active	Production	HTSSOP (DCA) | 48	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	0 to 85	TPS65232 A2
TPS65232A2DCA.B	Active	Production	HTSSOP (DCA) | 48	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	0 to 85	TPS65232 A2
TPS65232A2DCAR	Active	Production	HTSSOP (DCA) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 85	TPS65232 A2
TPS65232A2DCAR.B	Active	Production	HTSSOP (DCA) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 85	TPS65232 A2

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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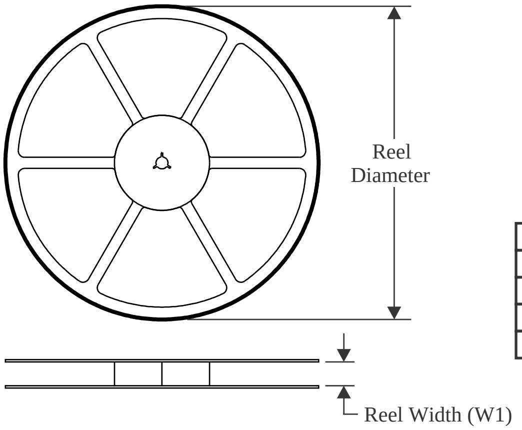
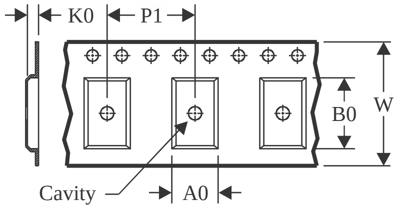
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

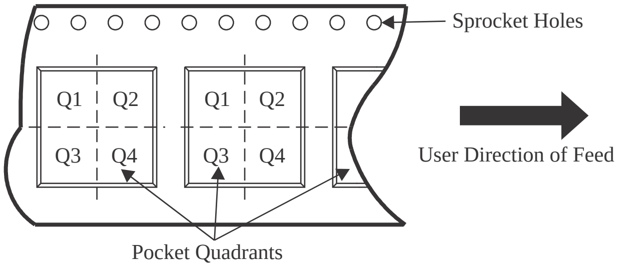

Reel
Diameter
Reel Width (W1)

TAPE DIMENSIONS


K0
P1
B0
W
Cavity
A0

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

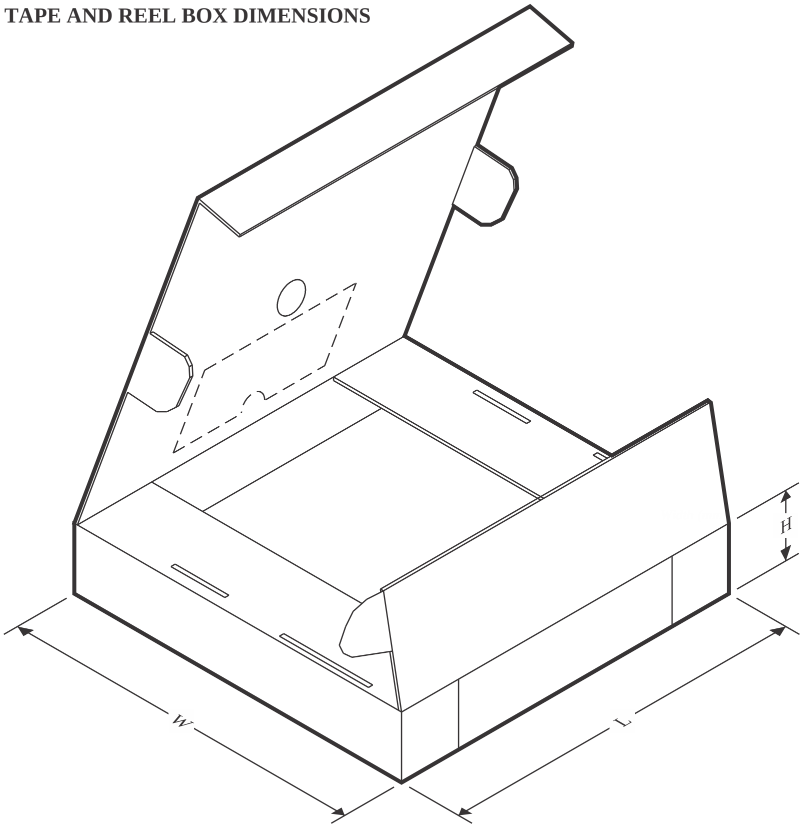
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


Sprocket Holes
Q1
Q2
Q3
Q4
Q1
Q2
Q3
Q4
User Direction of Feed
Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65232A0RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65232A2DCAR	HTSSOP	DCA	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1

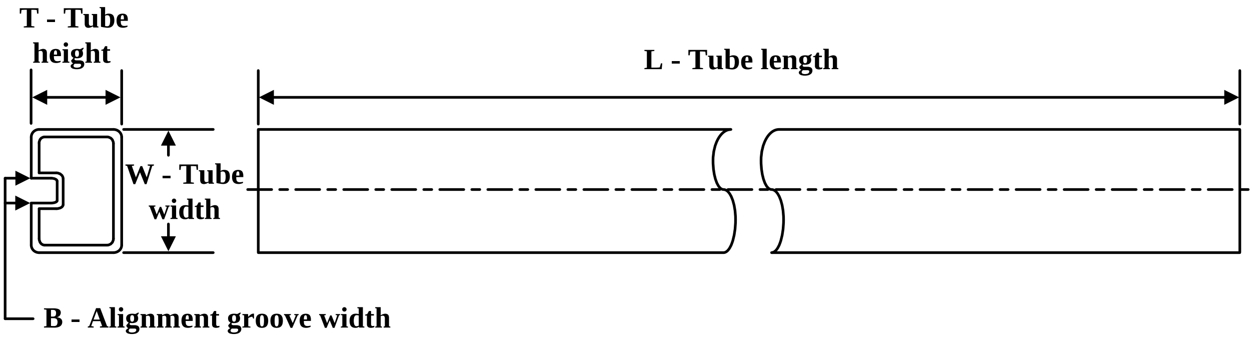
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65232A0RHAR	VQFN	RHA	40	2500	353.0	353.0	32.0
TPS65232A2DCAR	HTSSOP	DCA	48	2000	350.0	350.0	43.0

TUBE


T - Tube height
L - Tube length
W - Tube width
B - Alignment groove width

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS65232A0RHA	RHA	VQFN	40	50	381	7.92	2286	0
TPS65232A0RHA.B	RHA	VQFN	40	50	381	7.92	2286	0
TPS65232A2DCA	DCA	HTSSOP	48	40	530	11.89	3600	4.9
TPS65232A2DCA.B	DCA	HTSSOP	48	40	530	11.89	3600	4.9

GENERIC PACKAGE VIEW

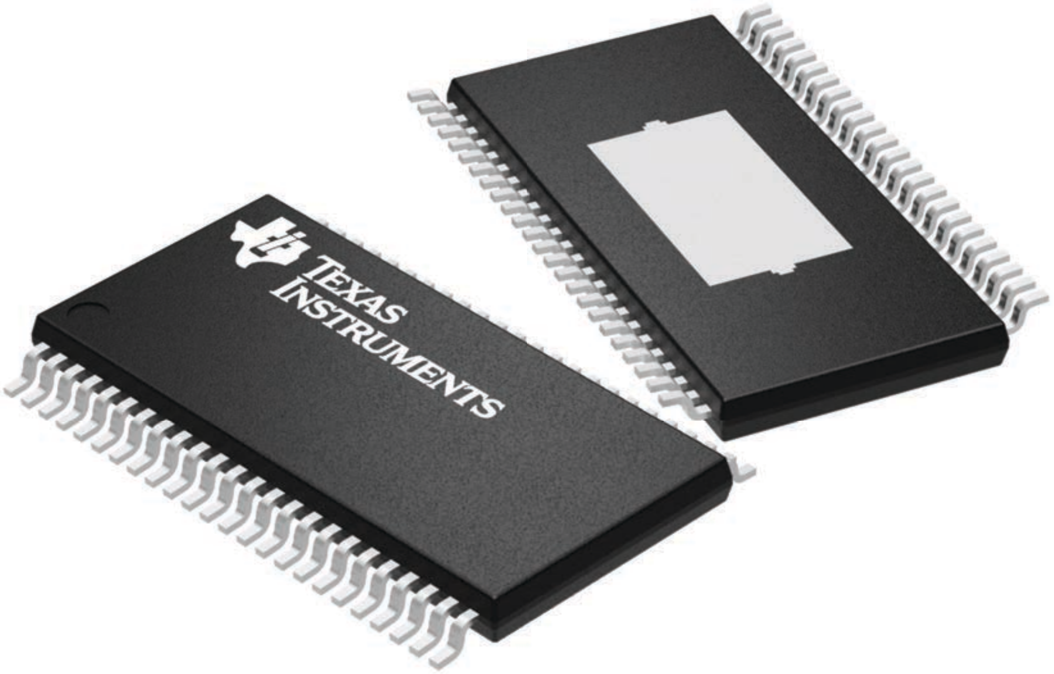
DCA 48

HTSSOP - 1.2 mm max height

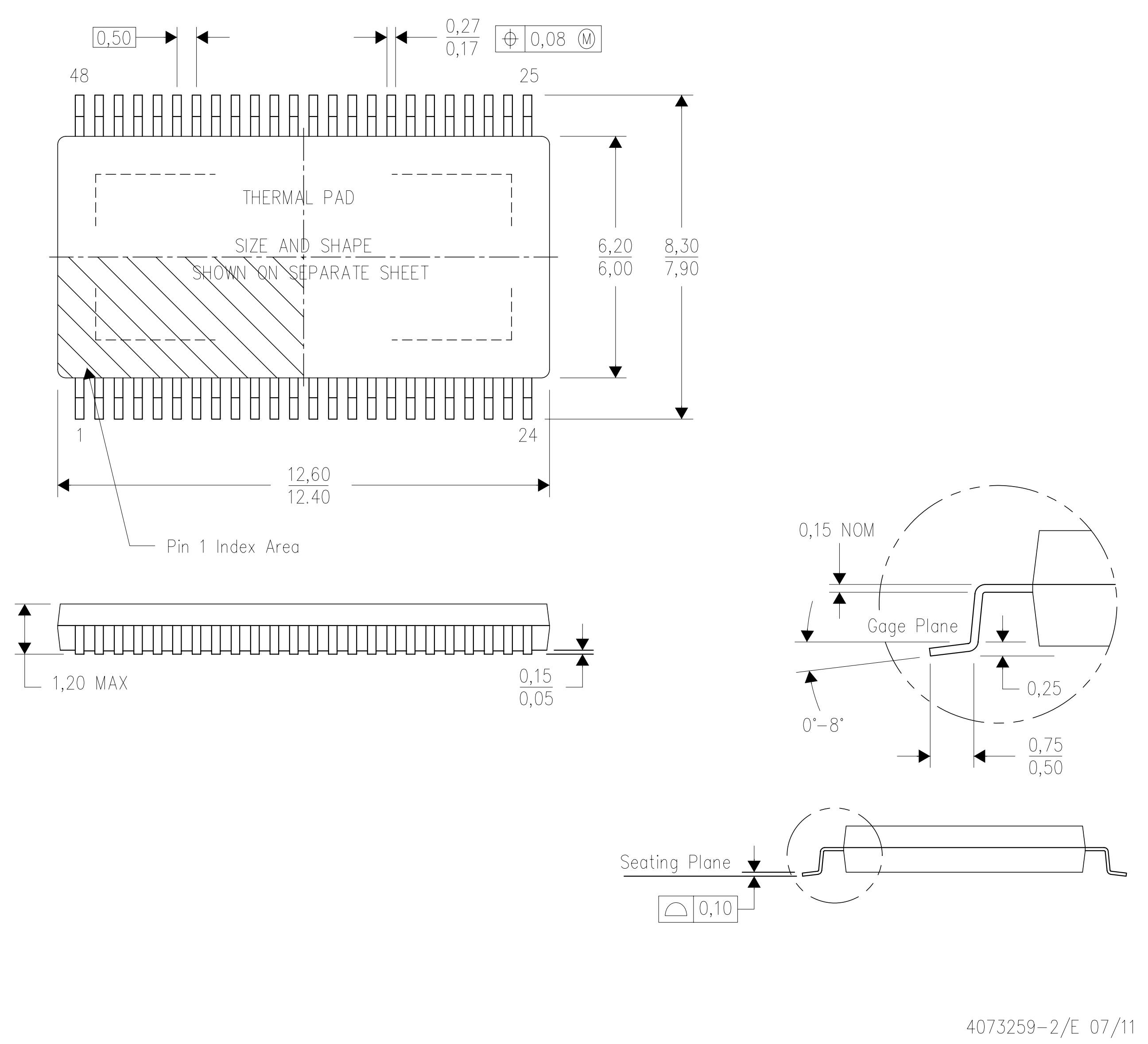
12.5 x 6.1, 0.5 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



DCA (R-PDSO-G48) PowerPAD™ PLASTIC SMALL-OUTLINE


0,50
0,27
0,17
⌖ 0,08 Ⓜ
48
25
THERMAL PAD
SIZE AND SHAPE
SHOWN ON SEPARATE SHEET
6,20
6,00
8,30
7,90
1
24
12,60
12.40
Pin 1 Index Area
0,15 NOM
Gage Plane
0,25
0°–8°
0,75
0,50
1,20 MAX
0,15
0,05
Seating Plane
0,10
4073259-2/E 07/11

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

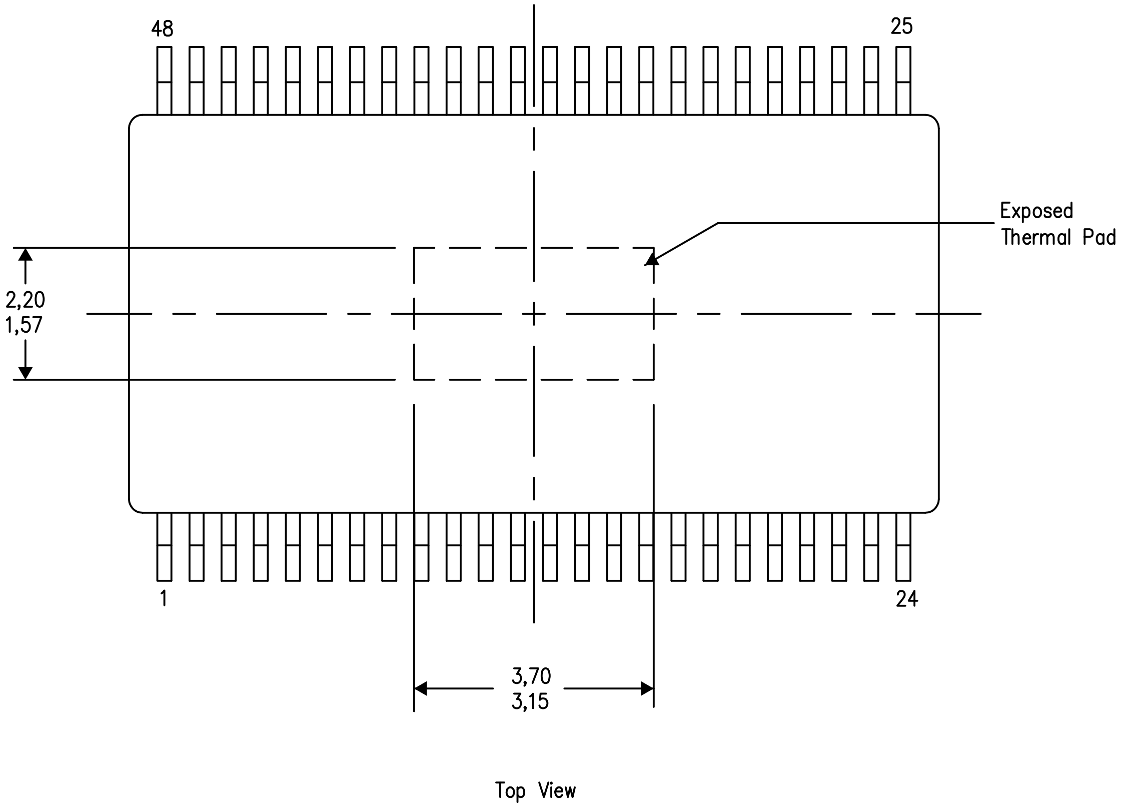
DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



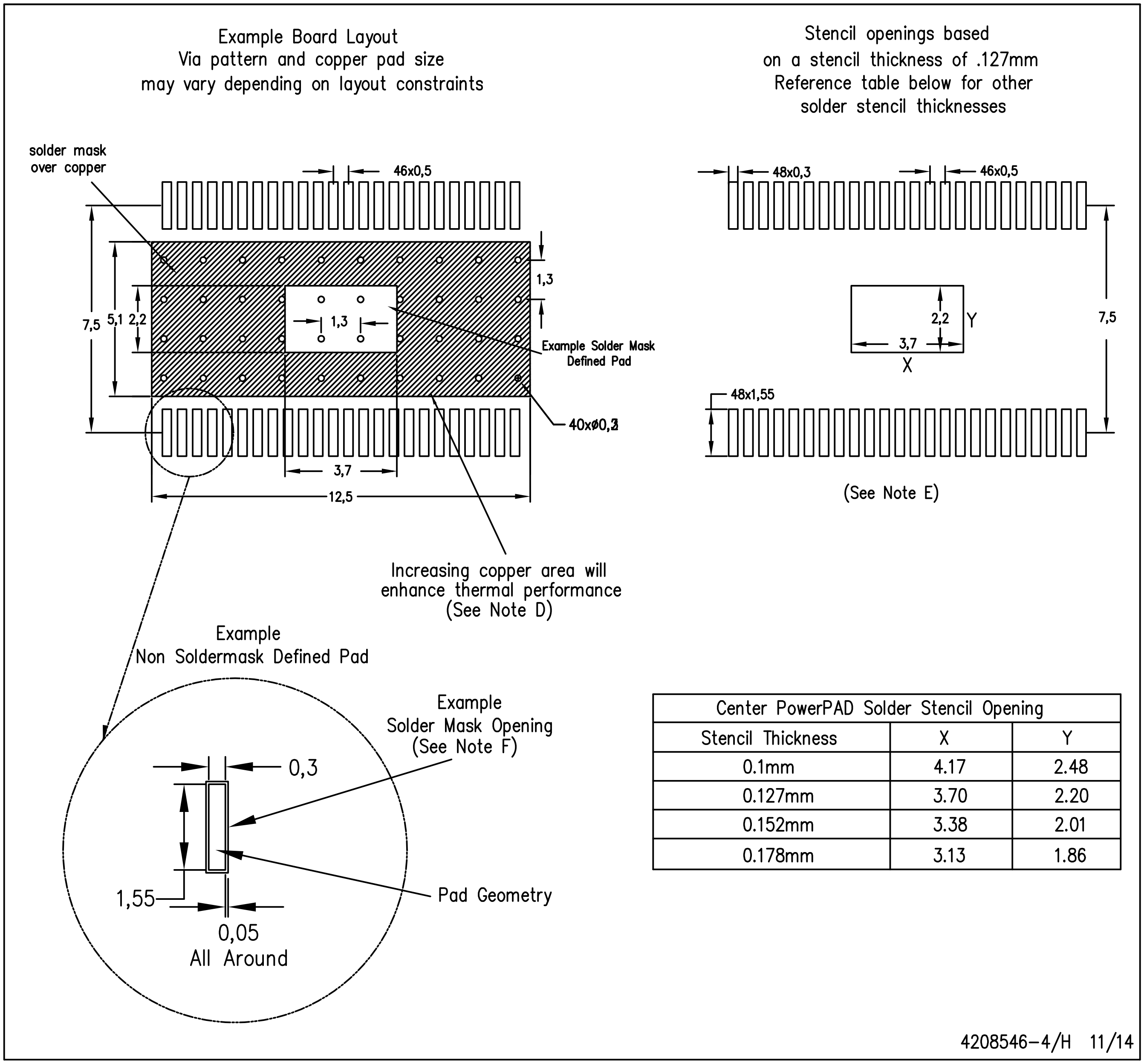
Exposed Thermal Pad Dimensions

4206320–5/S 11/14

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments.

DCA (R-PDSO-G48) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE


Example Board Layout
Via pattern and copper pad size
may vary depending on layout constraints
solder mask
over copper
46x0,5
1,3
1,3
7,5
5,1
2,2
Example Solder Mask
Defined Pad
40xø0,3
3,7
12,5
Increasing copper area will
enhance thermal performance
(See Note D)
Example
Non Soldermask Defined Pad
Example
Solder Mask Opening
(See Note F)
0,3
1,55
0,05
All Around
Pad Geometry
Stencil openings based
on a stencil thickness of .127mm
Reference table below for other
solder stencil thicknesses
48x0,3
46x0,5
2,2
Y
3,7
X
7,5
48x1,55
(See Note E)

Center PowerPAD Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	4.17	2.48
0.127mm	3.70	2.20
0.152mm	3.38	2.01
0.178mm	3.13	1.86

4208546-4/H 11/14

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

GENERIC PACKAGE VIEW

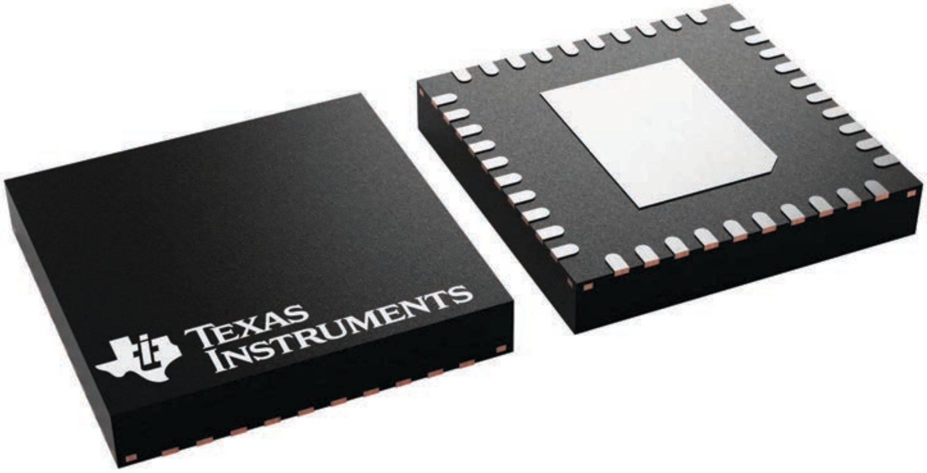
RHA 40

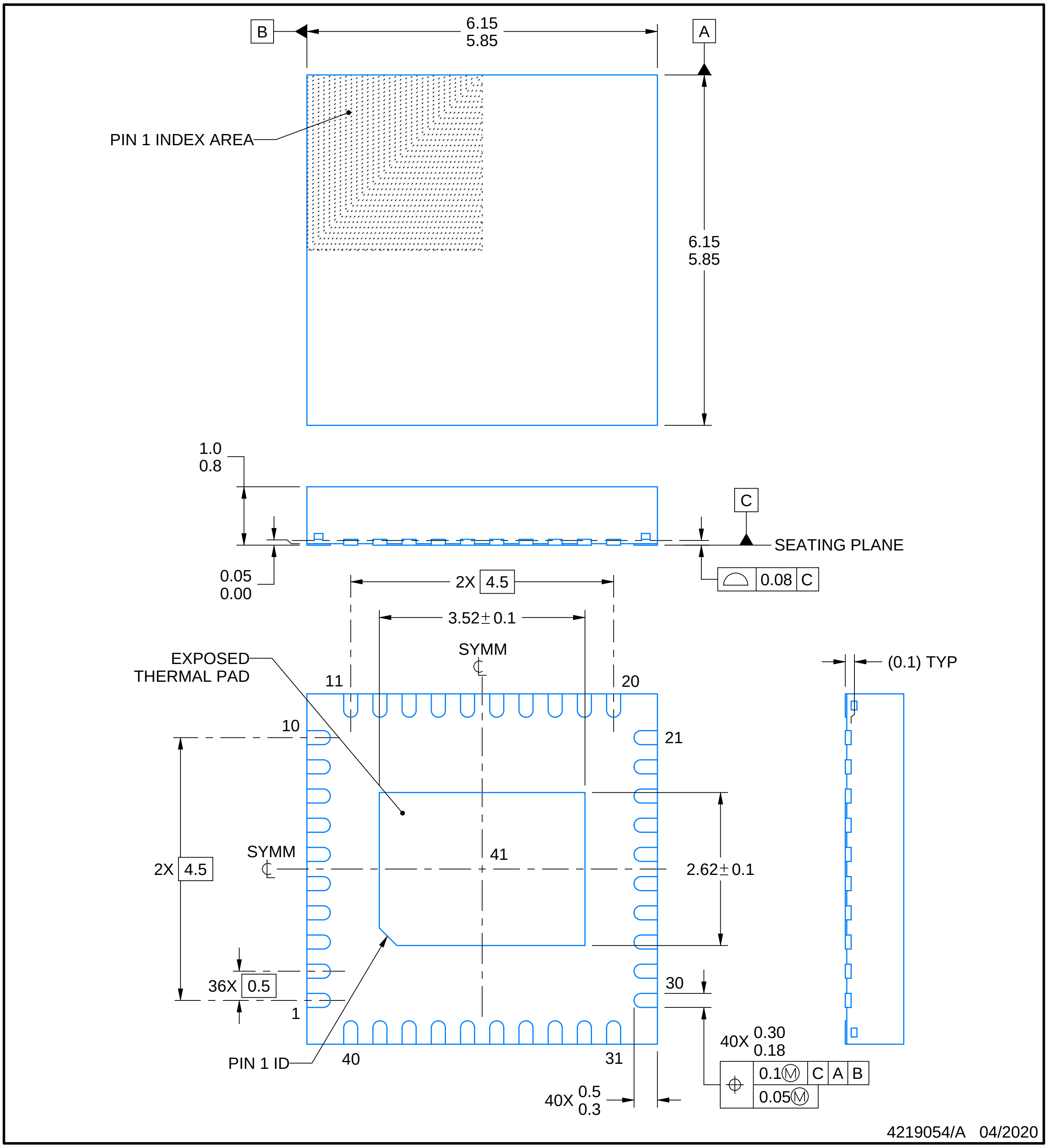
VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

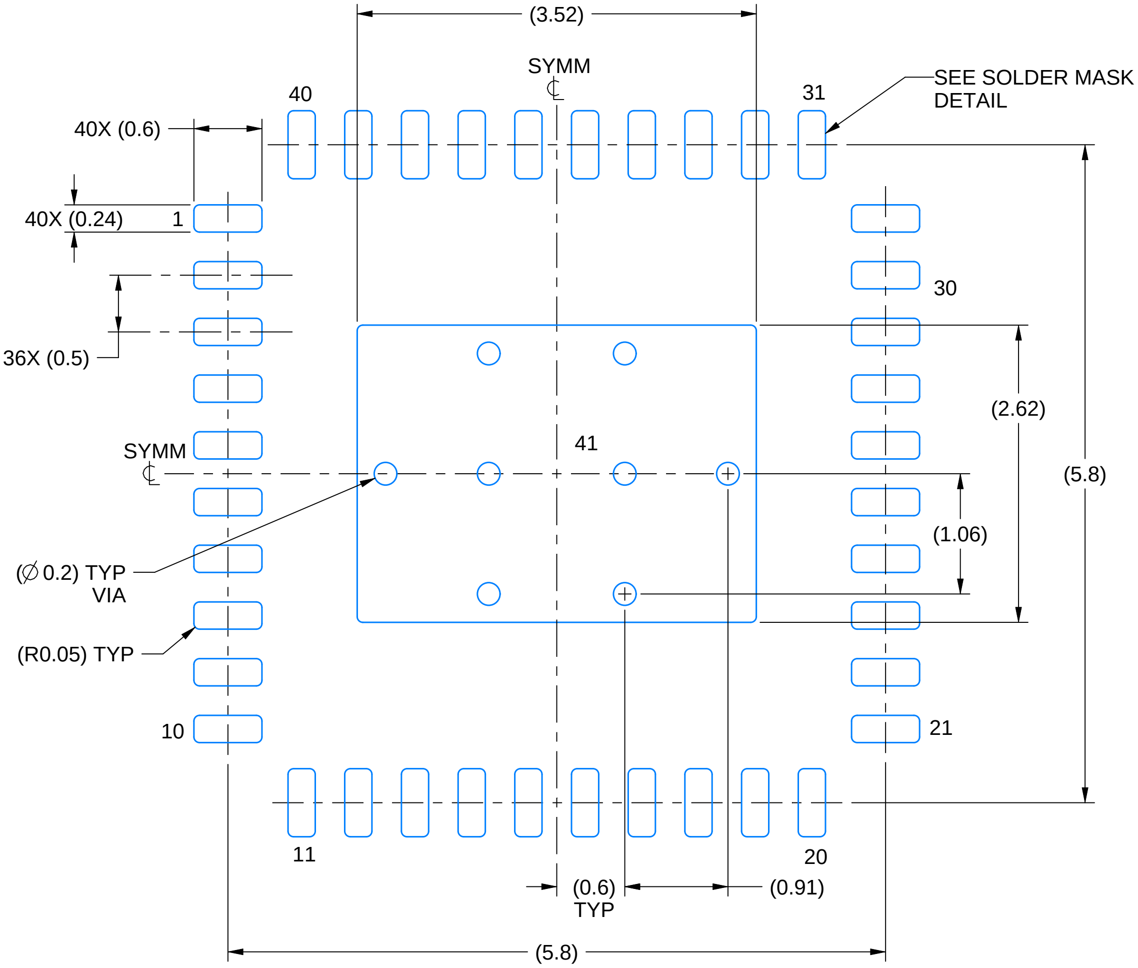
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



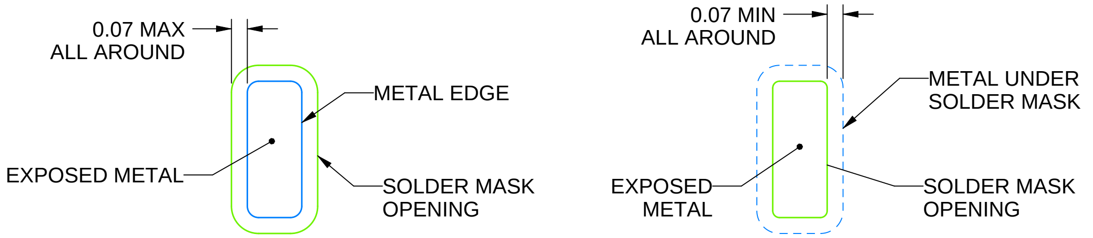

B
6.15
5.85
A
PIN 1 INDEX AREA
6.15
5.85
1.0
0.8
C
SEATING PLANE
0.05
0.00
0.08 C
2X 4.5
3.52±0.1
SYMM
EXPOSED THERMAL PAD
11
20
(0.1) TYP
10
21
2X 4.5
SYMM
41
2.62±0.1
36X 0.5
30
1
PIN 1 ID
40
31
40X 0.30
0.18
0.1Ⓜ C A B
0.05Ⓜ
40X 0.5
0.3
4219054/A 04/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.


(3.52)
SYMM
℄
40
31
SEE SOLDER MASK DETAIL
40X (0.6)
40X (0.24)
1
36X (0.5)
30
(2.62)
(5.8)
SYMM
℄
41
(1.06)
(∅0.2) TYP VIA
(R0.05) TYP
10
21
11
20
(0.6) TYP
(0.91)
(5.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X


0.07 MAX ALL AROUND
METAL EDGE
EXPOSED METAL
SOLDER MASK OPENING
0.07 MIN ALL AROUND
METAL UNDER SOLDER MASK
EXPOSED METAL
SOLDER MASK OPENING

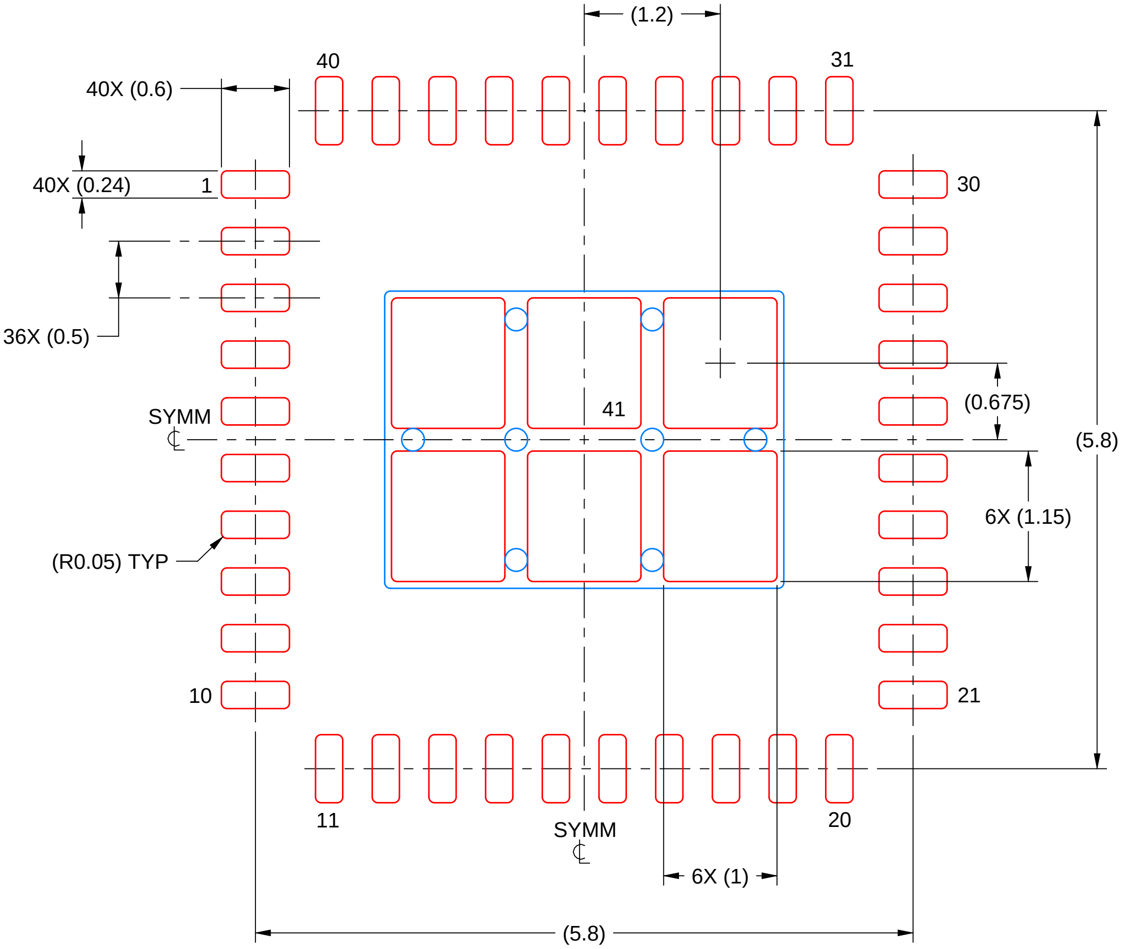
NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.


(1.2)
40
31
40X (0.6)
40X (0.24)
1
30
36X (0.5)
41
(0.675)
SYMM
℄
(5.8)
6X (1.15)
(R0.05) TYP
10
21
11
20
SYMM
℄
6X (1)
(5.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 41
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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