TPS736xx-EP Cap-Free, NMOS, 400mA, Low-Dropout Regulators With Reverse Current Protection

1 Features

- Controlled baseline:
  - One assembly
  - One test site
  - One fabrication site
- Extended temperature performance: –55°C to +125°C
- Enhanced diminishing manufacturing sources (DMS) support
- Enhanced product-change notification
- Qualification pedigree[1]
- Stable with no output capacitor or any value or type of capacitor
- Input voltage range: 1.7V to 5.5V
- Ultra-low dropout voltage: 75mV typical
- Excellent load transient response (With or without optional output capacitor)
- New NMOS topology delivers low reverse leakage current
- Low noise:
  $30\mu V_{RMS}$ typical (10Hz to 100kHz)
- Initial accuracy: 0.5%
- 1% Overall accuracy over line, load, and temperature
- Less than 1µA max I_Q in shutdown mode
- Thermal shutdown and specified min/max current limit protection
- Available in multiple output voltage versions:
  - Fixed outputs: 1.2V to 3.3V
  - Adjustable output: 1.2V to 5.5V
  - Custom outputs available

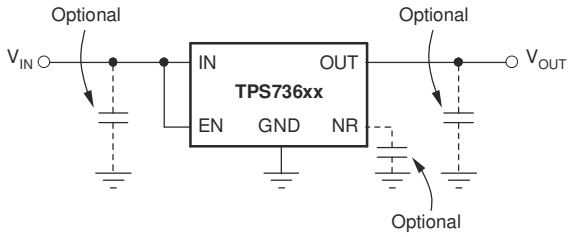
2 Applications

- Portable-, Battery-Powered Equipment
- Post-Regulation for Switching Supplies
- Noise-Sensitive Circuitry Such as VCOs
- Point of Load Regulation for DSPs, FPGAs, ASICs, and Microprocessors

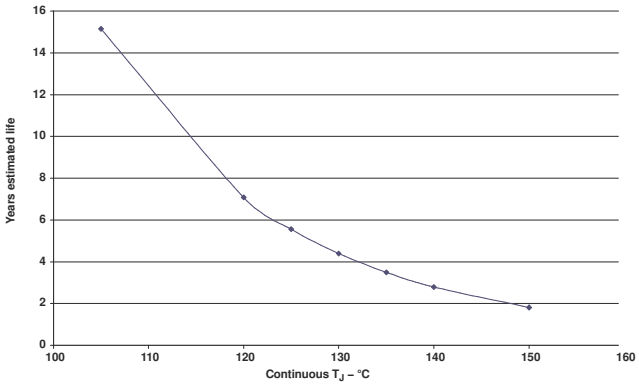
3 Description

The TPS736xx-EP family of low-dropout (LDO) linear voltage regulators uses a new topology—an NMOS pass element in a voltage-follower configuration. This topology is stable using output capacitors with low ESR and allows operation without a capacitor. This family also provides high reverse blockage (low reverse current) and ground-pin current that is nearly constant over all values of output current.

The TPS736xx-EP uses an advanced BiCMOS process to yield high precision while delivering low dropout voltages and low ground-pin current. Current consumption, when not enabled, is under 1µA and ideal for portable applications. The low output noise ($30\mu V_{RMS}$ with 0.1µF C_{NR}) is ideal for powering VCOs. These devices are protected by thermal shutdown and foldback current limit.



Typical Application Circuit for Fixed-Voltage Versions



TPS736xxDBVzEP Estimated Device Life at Elevated Temperatures Electromigration Fail Mode ($T_J = T_{JA} \times W + T_A$, Standard JESD 51 conditions)

[1] Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

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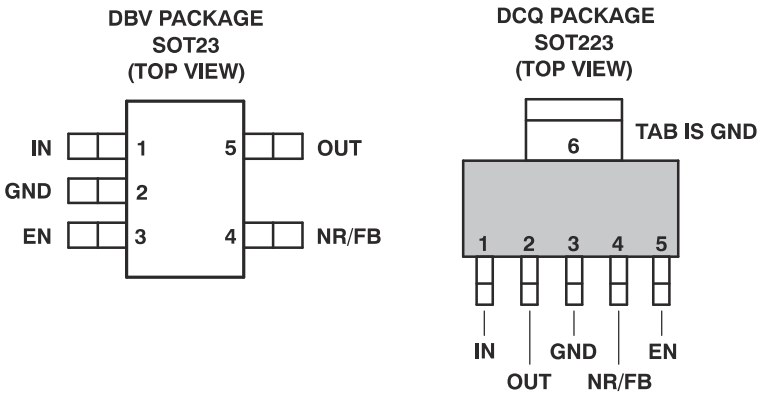
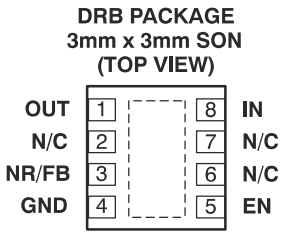
4 Pin Configuration and Functions





N/C - No internal connection

Table 4-1. Pin Functions

NAME	SOT23 (DBV) PIN NO.	SOT223 (DCQ) PIN NO.	3x3 SON (DRB) PIN NO.	DESCRIPTION
IN	1	1	8	Unregulated input supply
GND	2	3, 6	4, Pad	Ground
EN	3	5	5	Enable. Driving EN high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. See the Shutdown section under Applications Information for more details. EN can be connected to IN if not used.
NR	4	4	3	Fixed-voltage versions only. Connecting an external capacitor to this pin bypasses noise generated by the internal bandgap, reducing output noise to low levels.
FB	4	4	3	Feedback. Adjustable-voltage version only. This is the input to the control loop error amplifier and is used to set the output voltage of the device.
OUT	5	2	1	Output of the regulator. There are no output capacitor requirements for stability.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted(1)

			UNIT
V_{IN} range		–0.3 to 6	V
V_{EN} range		–0.3 to 6	V
V_{OUT} range		–0.3 to 5.5	V
Peak output current		Internally limited	
Output short-circuit duration		Indefinite	
Continuous total power dissipation		See Dissipation Ratings Table	
Junction temperature range, T_J		–55 to 150	°C
Storage temperature range		–65 to 150	°C
ESD rating	Human-body model - HBM	2	kV
	Charged-device model - CDM	500	V

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the Electrical Characteristics is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

5.2 Power Dissipation Ratings

see (1)

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = 25°C	$T_A \le 25°C$ POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
Low-K(2)	DBV	64°C/W	255°C/W	3.9 mW/°C	392 mW	216 mW	157 mW
High-K(3)	DBV	64°C/W	180°C/W	5.6 mW/°C	556 mW	306 mW	222 mW
Low-K(2)	DCQ	15°C/W	53°C/W	18.9 mW/°C	1887 mW	1038 mW	755 mW
High-K(3)	DCQ	15°C/W	45°C/W	22.2 mW/°C	2222 mW	1222 mW	889 mW
High-K(3) (4)	DRB	1.2°C/W	40°C/W	25.0 mW/°C	2500 mW	1375 mW	1000 mW

(1) See the Thermal Protection section for more information related to thermal design.
(2) The JEDEC Low-K (1s) board design used to derive this data was a 3 in × 3 in, two-layer board with 2 oz copper traces on top of the board.
(3) The JEDEC High-K (2s2p) board design used to derive this data was a 3 in × 3 in, multilayer board with 1 oz internal power and ground planes, and 2-oz copper traces on the top and bottom of the board.
(4) Based on preliminary thermal simulations.

5.3 Electrical Characteristics

over operating temperature range (T_A = –55°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V(1), I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF (unless otherwise noted). Typical values are at T_J = 25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range(1) (4)			1.7		5.5	V
V_{FB}	Internal reference (TPS73601)		T_J = 25°C	1.198	1.2	1.21	V
V_{OUT}	Output voltage range (TPS73601)			V_{FB}		5.5 – V_{DO}	V
	Accuracy(1)	Nominal	T_J = 25°C	–0.5%		0.5%	
		Over V_{IN}, I_{OUT}, and T	V_{OUT} + 0.5 V ≤ V_{IN} ≤ 5.5 V, 10 mA ≤ I_{OUT} ≤ 400 mA	–1%	±0.5%	1%	
$\Delta V_{OUT}\%/\Delta V_{IN}$	Line regulation(1)		$V_{O(nom)}$ + 0.5 V ≤ V_{IN} ≤ 5.5 V		0.01		%/V
$\Delta V_{OUT}\%/\Delta I_{OUT}$	Load regulation		1 mA ≤ I_{OUT} ≤ 400 mA		0.002		%/mA
			10 mA ≤ I_{OUT} ≤ 400 mA		0.0005		
V_{DO}	Dropout voltage(2) (V_{IN} = $V_{OUT(nom)}$ – 0.1 V)		I_{OUT} = 400 mA		75	200	mV
Z_O(DO)	Output impedance in dropout		1.7 V ≤ V_{IN} ≤ V_{OUT} + V_{DO}		0.25		Ω
I_{CL}	Output current limit		V_{OUT} = 0.9 × $V_{OUT(nom)}$	400	650	800	mA
I_{SC}	Short-circuit current		V_{OUT} = 0 V		450		mA
I_{REV}	Reverse leakage current(3) (–I_{IN})		V_{EN} ≤ 0.5 V, 0 V ≤ V_{IN} ≤ V_{OUT}		0.1	15	µA
I_{GND}	Ground-pin current		I_{OUT} = 10 mA (I_Q)		400	550	µA
			I_{OUT} = 400 mA		800	1000	
I_{SHDN}	Shutdown current (I_{GND})		V_{EN} ≤ 0.5 V, V_{OUT} ≤ V_{IN} ≤ 5.5 V		0.02	1	µA
I_{FB}	FB pin current (TPS73601)				0.1	0.45	µA
PSRR	Power-supply rejection ratio (ripple rejection)		f = 100 Hz, I_{OUT} = 400 mA		58		dB
			f = 10 kHz, I_{OUT} = 400 mA		37		
V_N	Output noise voltage BW = 10 Hz to 100 kHz		C_{OUT} = 10 µF, No C_{NR}		27 × V_{OUT}		μV_{RMS}
			C_{OUT} = 10 µF, C_{NR} = 0.01 µF		8.5 × V_{OUT}		
t_{STR}	Startup time		V_{OUT} = 3 V, R_L = 30 Ω, C_{OUT} = 1 µF, C_{NR} = 0.01 µF		600		µs
V_{EN}(HI)	Enable high (enabled)			1.7		V_{IN}	V
V_{EN}(LO)	Enable low (shutdown)			0		0.5	V
I_{EN}(HI)	Enable pin current (enabled)		V_{EN} = 5.5 V		0.02	0.1	µA
T_{SD}	Thermal shutdown temperature		Shutdown, temperature increasing		160		°C
			Reset, temperature decreasing		140		
T_A	Operating ambient temperature			-55		125	°C

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 1.7 V, whichever is greater.
(2) V_{DO} is not measured for the TPS73615 ($V_{OUT(nom)}$ = 1.5 V) since minimum V_{IN} = 1.7 V.
(3) See the *Application and Implementation* section for more information.
(4) For $V_{OUT(nom)}$ < 1.6 V, when V_{IN} ≤ 1.6 V, the output locks to V_{IN} and may result in a damaging over-voltage level on the output. To avoid this situation, disable the device before powering down the V_{IN}.

5.4 Typical Characteristics

for all voltage versions, T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF (unless otherwise noted)

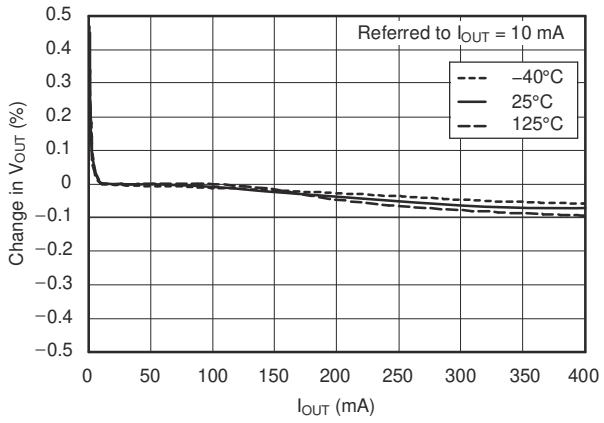


Figure 5-1. Load Regulation

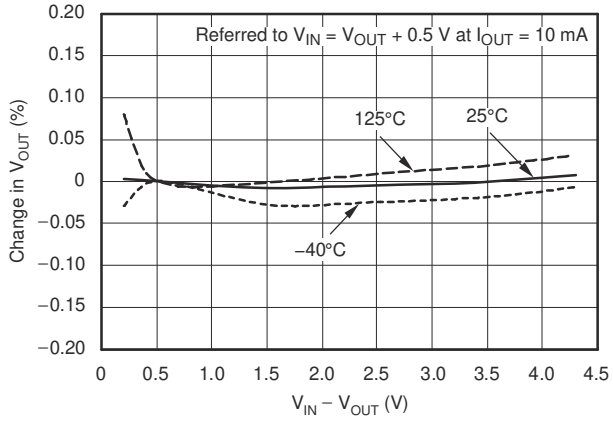


Figure 5-2. Line Regulation

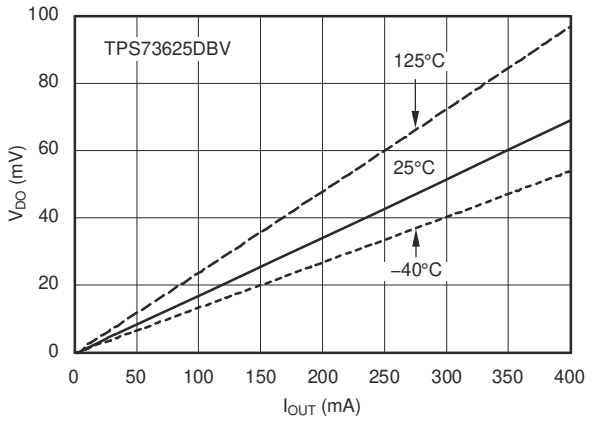


Figure 5-3. Dropout Voltage vs Output Current

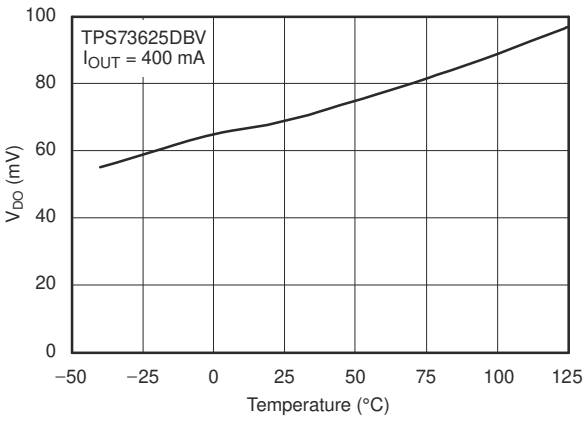


Figure 5-4. Dropout Voltage vs Temperature

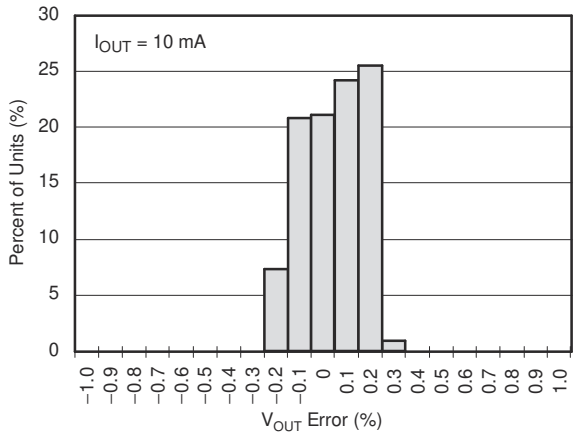


Figure 5-5. Output Voltage Accuracy Histogram

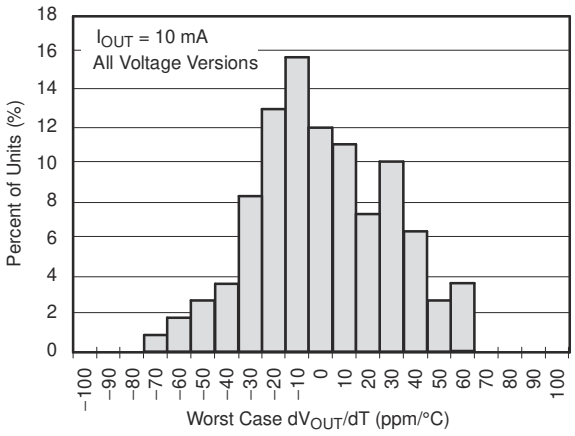


Figure 5-6. Output Voltage Drift Histogram

5.4 Typical Characteristics (continued)

for all voltage versions, T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF (unless otherwise noted)

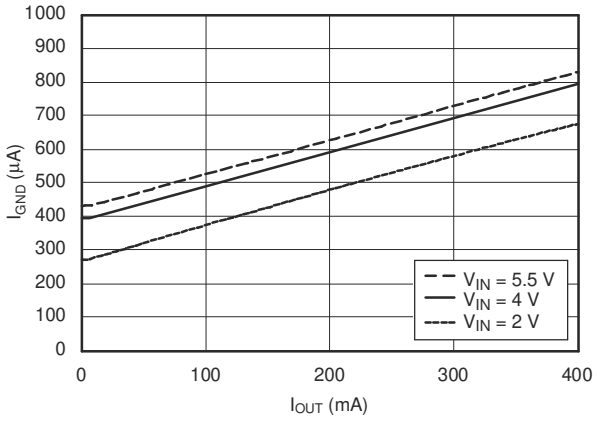


Figure 5-7. Ground Pin Current vs Output Current

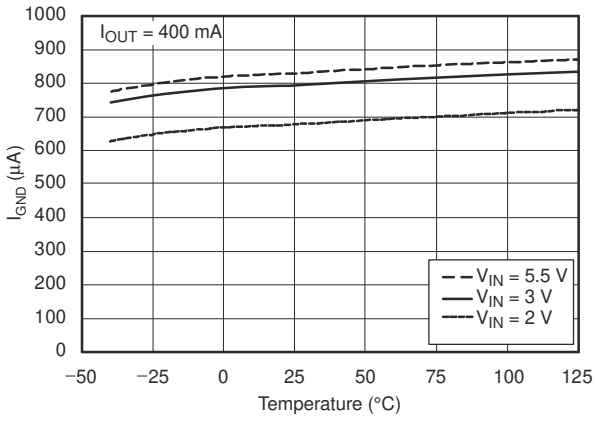


Figure 5-8. Ground Pin Current vs Temperature

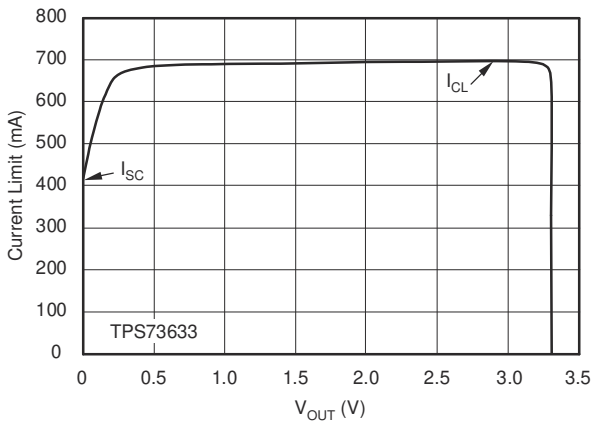


Figure 5-9. Current Limit vs V_{OUT} (Foldback)

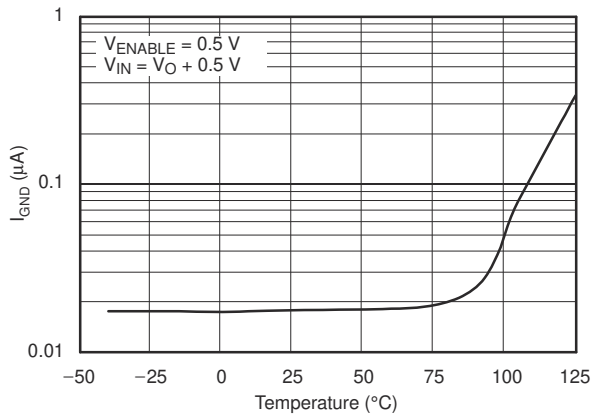


Figure 5-10. Ground Pin Current in Shutdown vs Temperature

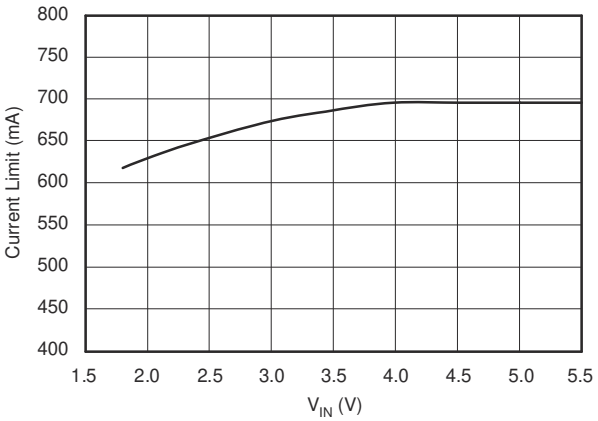


Figure 5-11. Current Limit vs V_{IN}

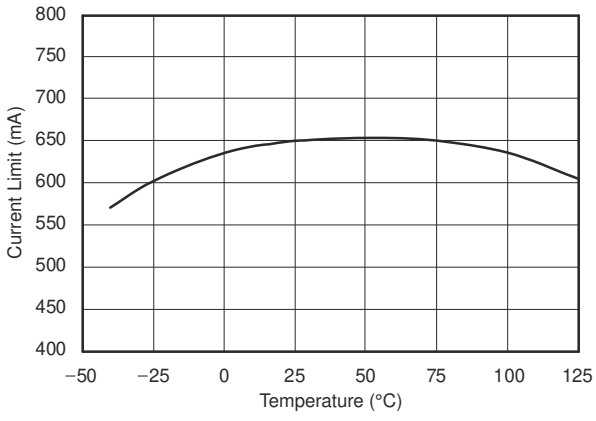


Figure 5-12. Current Limit vs Temperature

5.4 Typical Characteristics (continued)

for all voltage versions, T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF (unless otherwise noted)

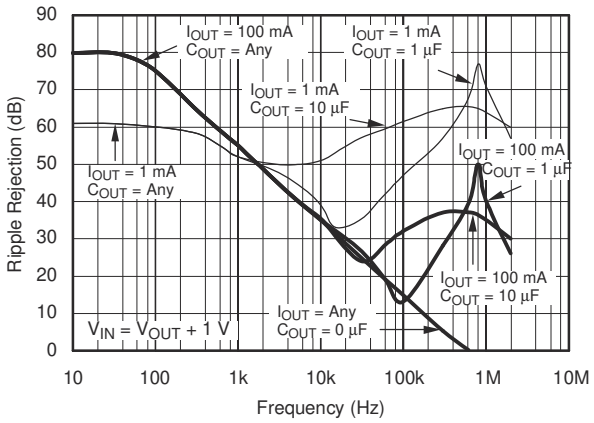


Figure 5-13. PSRR (Ripple Rejection) vs Frequency

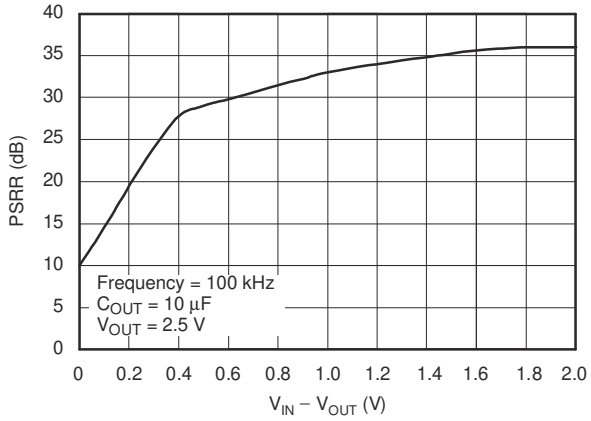


Figure 5-14. PSRR (Ripple Rejection) vs V_{IN} – V_{OUT}

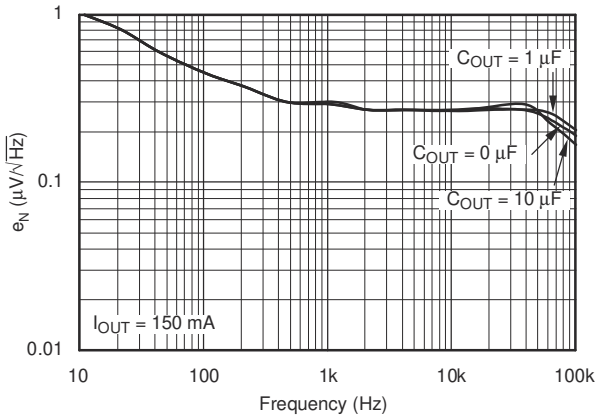


Figure 5-15. Noise Spectral Density C_{NR} = 0 µF

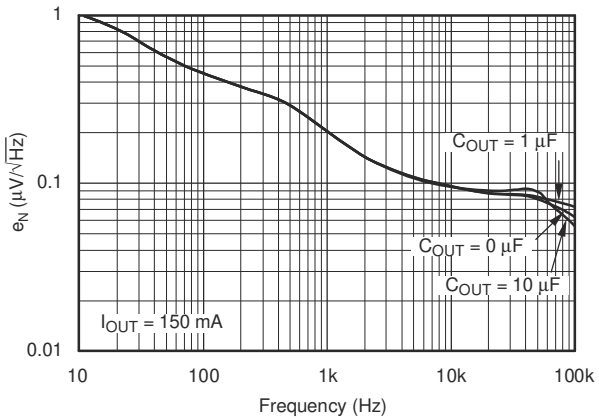


Figure 5-16. Noise Spectral Density C_{NR} = 0.01 µF

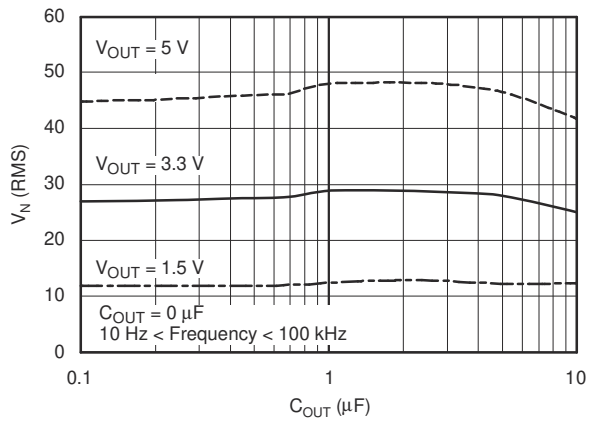


Figure 5-17. RMS Noise Voltage vs C_{OUT}

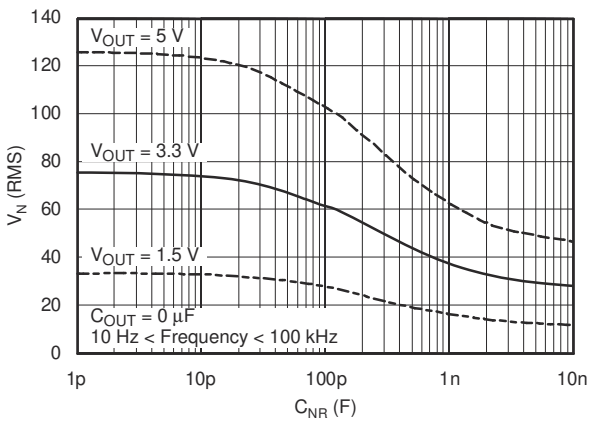


Figure 5-18. RMS Noise Voltage vs C_{NR}

5.4 Typical Characteristics (continued)

for all voltage versions, T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF (unless otherwise noted)

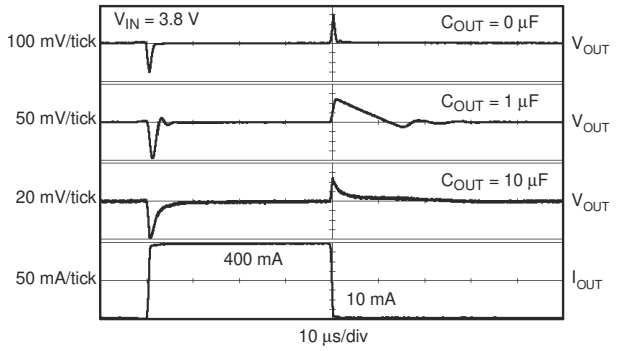


Figure 5-19. TPS73633 Load Transient Response

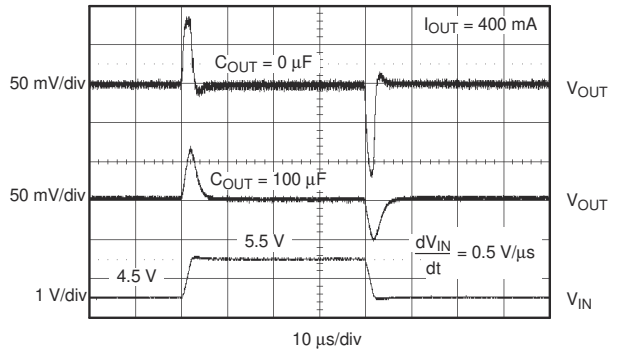


Figure 5-20. TPS73633 Line Transient Response

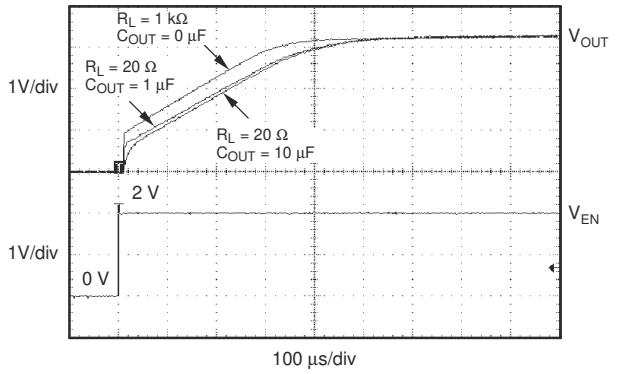


Figure 5-21. TPS73633 Turn-On Response

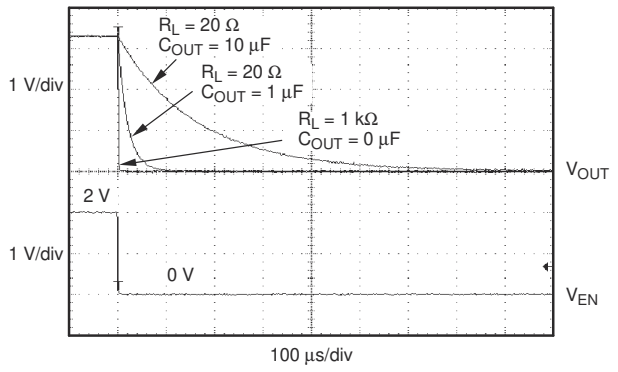


Figure 5-22. TPS73633 Turn-Off Response

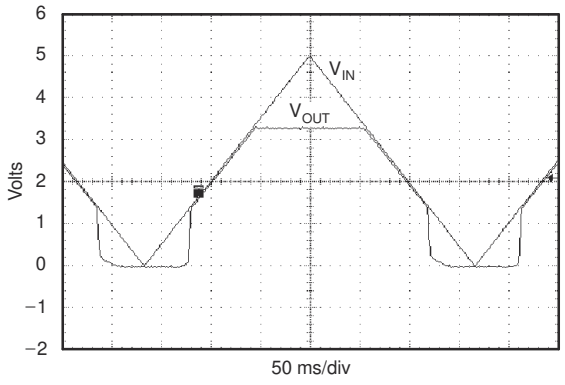


Figure 5-23. TPS73633 Power-Up, Power-Down

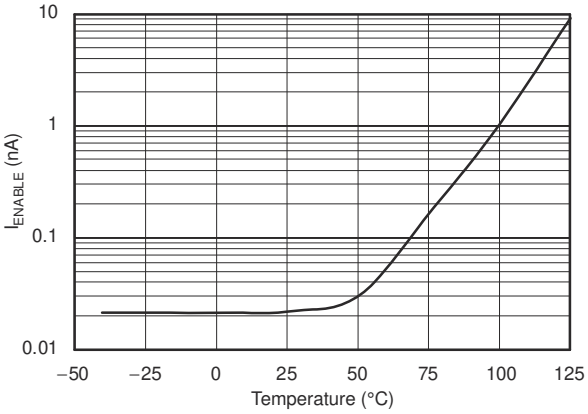


Figure 5-24. I_{ENABLE} vs Temperature

5.4 Typical Characteristics (continued)

for all voltage versions, T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF (unless otherwise noted)

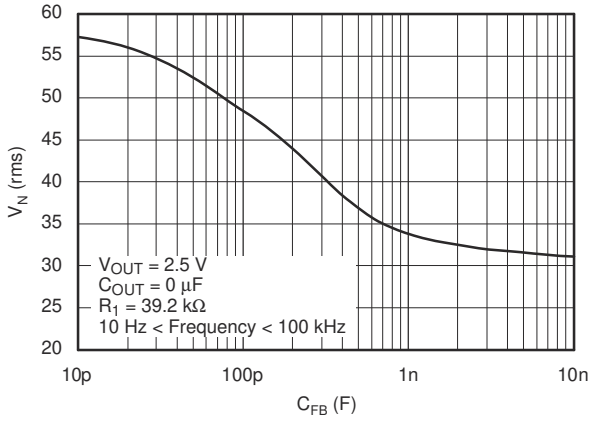


Figure 5-25. TPS73601 RMS Noise Voltage vs C_{ADJ}

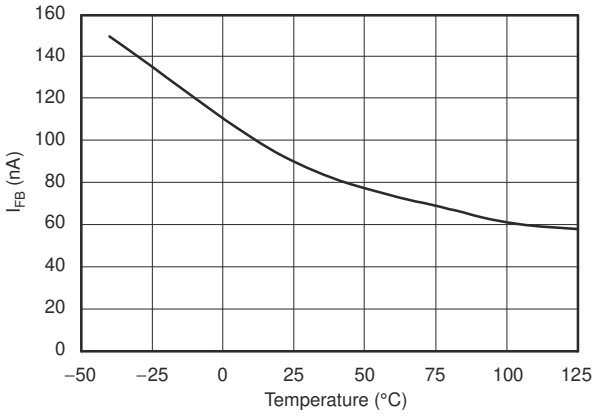


Figure 5-26. TPS73601 I_{FB} vs Temperature

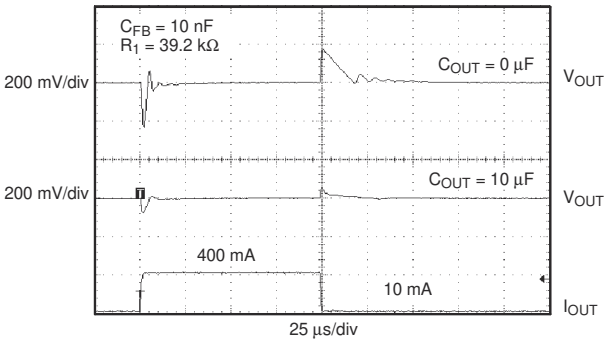


Figure 5-27. TPS73601 Load Transient, Adjustable Version

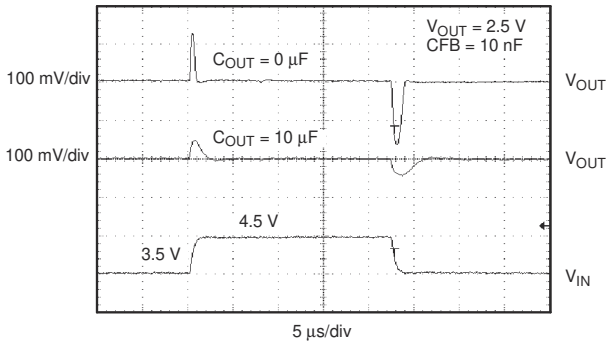


Figure 5-28. TPS73601 Line Transient, Adjustable Version

6 Functional Block Diagrams

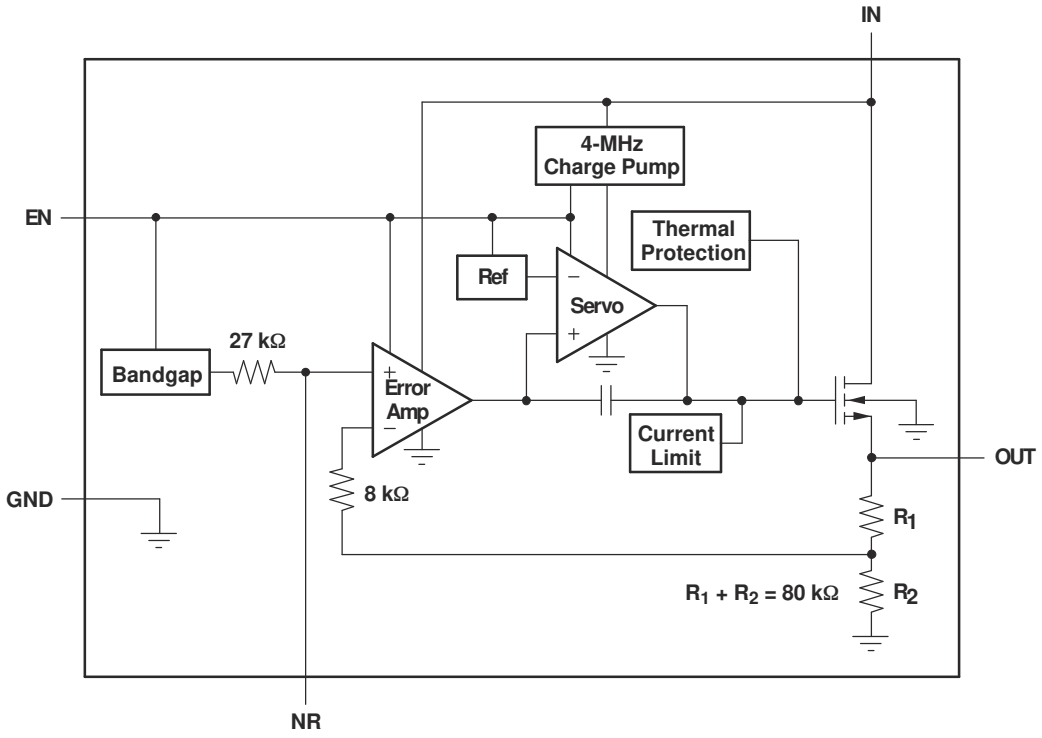
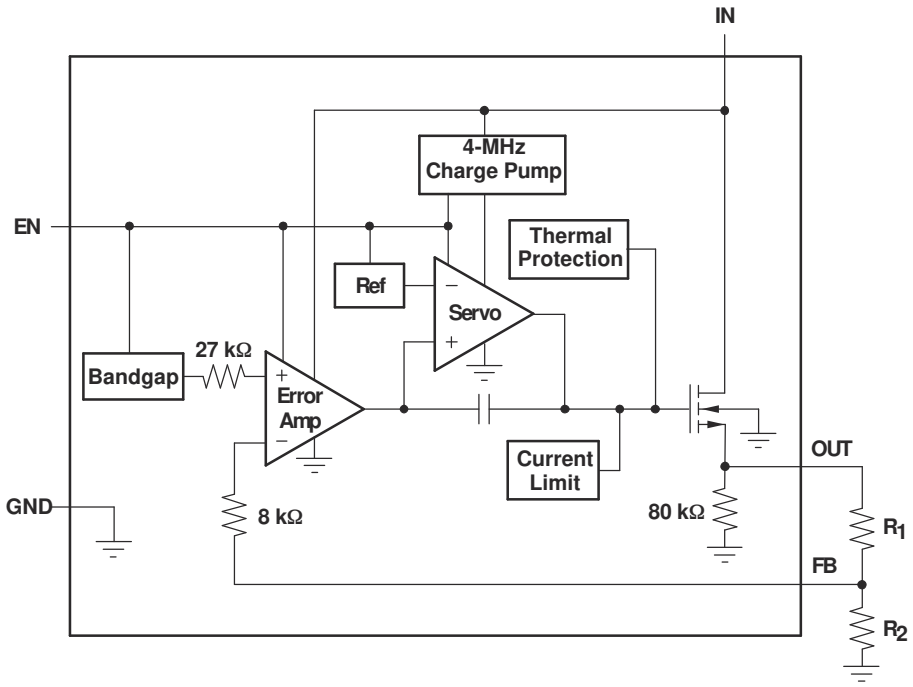


Figure 6-1. Fixed-Voltage Version



Standard 1% Resistor Values for Common Output Voltages

V_O	R_1	R_2
1.2 V	Short	Open
1.5 V	23.2 kΩ	95.3 kΩ
1.8 V	28 kΩ	56.2 kΩ
2.5 V	39.2 kΩ	36.5 kΩ
2.8 V	44.2 kΩ	33.2 kΩ
3 V	46.4 kΩ	30.9 kΩ
3.3 V	52.3 kΩ	30.1 kΩ

NOTE: $V_{OUT} = (R_1 + R_2)/R_2 \times 1.204$; $R_1 || R_2 \cong 19$ kΩ for best accuracy

Figure 6-2. Adjustable-Voltage Version

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TPS736xx-EP belongs to a family of new-generation LDO regulators that use an NMOS pass transistor to achieve ultra-low-dropout performance, reverse current blockage, and freedom from output capacitor constraints. These features, combined with low noise and an enable input, make the TPS736xx-EP ideal for portable applications. This regulator family offers a wide selection of fixed-output voltage versions and an adjustable-output version. All versions have thermal and overcurrent protection, including foldback current limit.

Figure 7-1 shows the basic circuit connections for the fixed-voltage models. Figure 7-2 shows the connections for the adjustable-output version (TPS73601-EP). R_1 and R_2 can be calculated for any output voltage using the formula in Figure 7-2. Sample resistor values for common output voltages are shown in Figure 6-2. For the best accuracy, make the parallel combination of R_1 and R_2 approximately 19 kΩ.

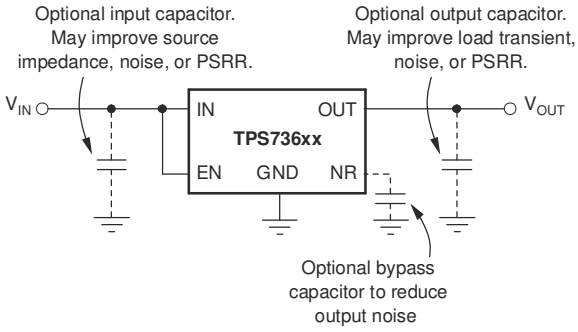


Figure 7-1. Typical Application Circuit for Fixed-Voltage Versions

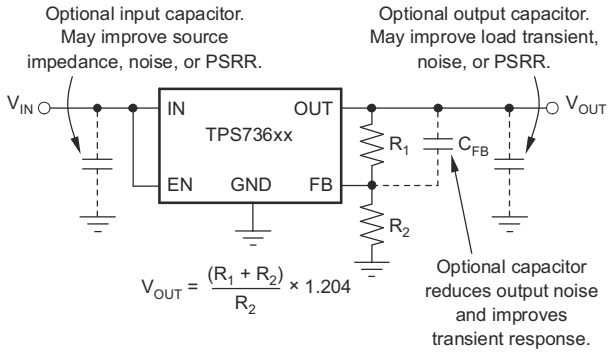


Figure 7-2. Typical Application Circuit for Adjustable-Voltage Versions

7.1.1 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1-µF to 1-µF low ESR capacitor across the input supply near the regulator. This counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or the device is located several inches from the power source.

The TPS736xx-EP does not require an output capacitor for stability and has maximum phase margin with no capacitor. It is designed to be stable for all available types and values of capacitors. In applications where V_{IN} − V_{OUT} < 0.5 V and multiple low ESR capacitors are in parallel, ringing may occur when the product of C_{OUT} and total ESR drops below 50 Ω. Total ESR includes all parasitic resistance, including capacitor ESR and board, socket, and solder-joint resistance. In most applications, the sum of capacitor ESR and trace resistance meets this requirement.

7.1.2 Output Noise

A precision band-gap reference is used to generate the internal reference voltage, V_{REF}. This reference is the dominant noise source within the TPS736xx-EP and it generates approximately 32 μV_{RMS} (10 Hz to 100 kHz) at the reference output (NR). The regulator control loop gains up the reference noise with the same gain as the reference voltage, so that the noise voltage of the regulator is approximately given by:

$$V_N = 32\ \mu V_{RMS} \times \frac{(R_1 + R_2)}{R_2} = 32\ \mu V_{RMS} \times \frac{V_{OUT}}{V_{REF}} \quad (1)$$

Since the value of V_{REF} is 1.2 V, this relationship reduces to:

$$V_N(\mu V_{RMS}) = 27\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \quad (2)$$

for the case of no C_{NR}.

An internal 27-kΩ resistor in series with the noise reduction pin (NR) forms a low-pass filter for the voltage reference when an external noise reduction capacitor, C_{NR}, is connected from NR to ground. For C_{NR} = 10 nF, the total noise in the 10-Hz to 100-kHz bandwidth is reduced by a factor of ~3.2, giving the approximate relationship:

$$V_N(\mu V_{RMS}) = 8.5\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \quad (3)$$

for C_{NR} = 10 nF.

This noise reduction effect is shown as RMS Noise Voltage vs C_{NR} in Figure 5-18.

The TPS73601-EP adjustable version does not have the noise-reduction pin available. However, connecting a feedback capacitor, C_{FB}, from the output to the FB pin reduces output noise and improves load transient performance.

The TPS736xx-EP uses an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the NMOS pass element above V_{OUT}. The charge pump generates ~250 µV of switching noise at ~4 MHz; however, charge-pump noise contribution is negligible at the output of the regulator for most values of I_{OUT} and C_{OUT}.

7.1.3 Board Layout Recommendation to Improve PSRR and Noise Performance

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the

GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

7.1.4 Internal Current Limit

The TPS736xx-EP internal current limit helps protect the regulator during fault conditions. Foldback helps to protect the regulator from damage during output short-circuit conditions by reducing current limit when V_{OUT} drops below 0.5 V. See Figure 5-9 for a graph of I_{OUT} vs V_{OUT}.

7.1.5 Shutdown

The enable (EN) pin is active high and is compatible with standard TTL-CMOS levels. V_{EN} below 0.5 V (max) turns the regulator off and drops the ground-pin current to approximately 10 nA. When shutdown capability is not required, EN can be connected to V_{IN}. When a pullup resistor is used, and operation down to 1.8 V is required, use pullup resistor values below 50 kΩ.

7.1.6 Dropout Voltage

The TPS736xx-EP uses an NMOS pass transistor to achieve extremely low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the NMOS pass device is in its linear region of operation and the input-to-output resistance is the R_{DS-ON} of the NMOS pass element.

For large step changes in load current, the TPS736xx-EP requires a larger voltage drop from V_{IN} to V_{OUT} to avoid degraded transient response. The boundary of this transient dropout region is approximately twice the dc dropout. Values of V_{IN} – V_{OUT} above this line ensure normal transient response.

Operating in the transient dropout region can cause an increase in recovery time. The time required to recover from a load transient is a function of the magnitude of the change in load current rate, the rate of change in load current, and the available headroom (V_{IN} to V_{OUT} voltage drop). Under worst-case conditions [full-scale instantaneous load change with (V_{IN} – V_{OUT}) close to dc dropout levels], the TPS736xx-EP can take a couple of hundred microseconds to return to the specified regulation accuracy.

7.1.7 Transient Response

The low open-loop output impedance provided by the NMOS pass element in a voltage-follower configuration allows operation without an output capacitor for many applications. As with any regulator, the addition of a capacitor (nominal value 1µF) from the output pin to ground reduces undershoot magnitude but increases duration. In the adjustable version, the addition of a capacitor, C_{FB}, from the output to the adjust pin also improves the transient response.

The TPS736xx-EP does not have active pulldown when the output is overvoltage. This allows applications that connect higher voltage sources, such as alternate power supplies, to the output. This also results in an output overshoot of several percent if load current quickly drops to zero when a capacitor is connected to the output. The duration of overshoot can be reduced by adding a load resistor. The overshoot decays at a rate determined by output capacitor C_{OUT} and the internal/external load resistance. The rate of decay is given by:

Fixed-voltage version:

$$dV/dt = \frac{V_{OUT}}{C_{OUT} \times 80\ k\Omega \parallel R_{LOAD}} \quad (4)$$

Adjustable-voltage version:

$$dV/dt = \frac{V_{OUT}}{C_{OUT} \times 80\ k\Omega \parallel (R_1 + R_2) \parallel R_{LOAD}} \quad (5)$$

7.1.8 Reverse Current

The NMOS pass element of the TPS736xx-EP provides inherent protection against current flow from the output of the regulator to the input when the gate of the pass device is pulled low. To ensure that all charge is removed from the gate of the pass element, EN must be driven low before the input voltage is removed. If this is not done, the pass element may be left on due to stored charge on the gate.

After EN is driven low, no bias voltage is needed on any pin for reverse current blocking. Note that reverse current is specified as the current flowing out of the IN pin due to voltage applied on the OUT pin. There is additional current flowing into the OUT pin due to the 80-kΩ internal resistor divider to ground (see Figure 6-1 and Figure 6-2).

For the TPS73601-EP, reverse current may flow when V_{FB} is more than 1 V above V_{IN}.

7.1.9 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This limits the dissipation of the regulator, protecting it from damage due to overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 35°C above the maximum expected ambient condition of the application. This produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS736xx-EP has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS736xx-EP into thermal shutdown degrades reliability.

7.1.10 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are shown in the *Power Dissipation Ratings* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation is equal to the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (6)$$

Power dissipation can be minimized by using the lowest-possible input voltage necessary to ensure the required output voltage.

7.1.11 Package Mounting

Solder-pad footprint recommendations for the TPS736xx-EP are presented in application bulletin *Solder Pad Recommendations for Surface-Mount Devices* (AB-132), available from the TI web site at www.ti.com.

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed in this section.

8.1 Device Support

8.1.1 Device Nomenclature

Table 8-1. Available Options

PRODUCT(1)	DESCRIPTION
TPS736xxMyyyREP	**xx** is normal output voltage (for example, 25 = 2.5 V, 01 = Adjustable(2)). ***yyy*** is package designator. ***z*** is package quantity.

(1) Additional output voltages from 1.25 V to 4.3 V in 100 mV increments are available on a quick-turn basis using innovative factory EEPROM programming. Minimum order quantities apply; contact TI for details and availability.
(2) For fixed 1.2-V operation, tie FB to OUT.

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (February 2009) to Revision D (August 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Deleted *Ordering Information* table	1
• Changed R1 to R2 in denominator of equation is *Typical Application Circuit for Adjustable-Voltage Versions* figure	12

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS73601MDBVREP	NRND	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	PJRM
TPS73601MDBVREP.A	NRND	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	PJRM
TPS73601MDCQREP	NRND	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	PWZM
TPS73601MDCQREP.A	NRND	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	PWZM
TPS73601MDRBREP	NRND	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	PMNM
TPS73601MDRBREP.A	NRND	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	PMNM
TPS73615MDBVREP	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T59
TPS73615MDBVREP.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T59
TPS73618MDBVREP	NRND	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T60
TPS73618MDBVREP.A	NRND	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T60
TPS73625MDBVREP	NRND	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T61
TPS73625MDBVREP.A	NRND	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T61
TPS73630MDBVREP	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T62
TPS73630MDBVREP.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T62
TPS73632MDBVREP	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T63
TPS73632MDBVREP.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T63
TPS73633MDBVREP	NRND	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T64
TPS73633MDBVREP.A	NRND	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T64
V62/06626-01XE	NRND	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	PJRM
V62/06626-01YE	NRND	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	PWZM
V62/06626-01ZE	NRND	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	PMNM
V62/06626-02XE	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T59
V62/06626-03XE	NRND	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T60
V62/06626-04XE	NRND	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T61
V62/06626-05XE	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T62
V62/06626-06XE	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T63
V62/06626-07XE	NRND	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T64

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

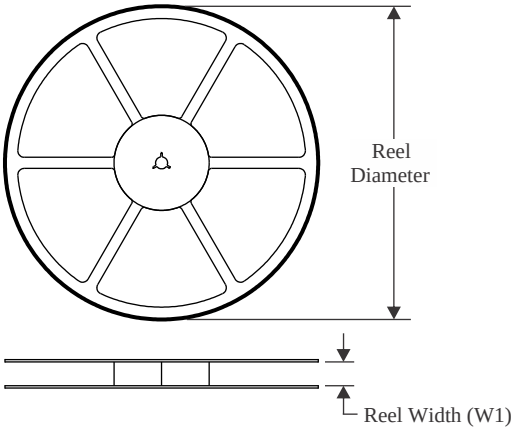
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

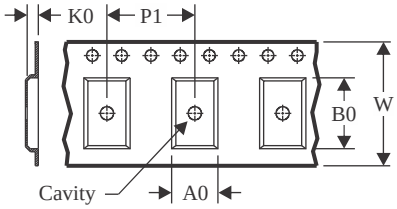
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

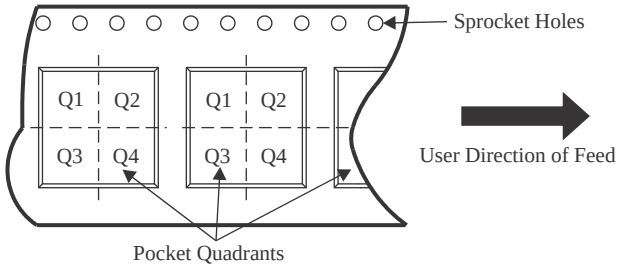


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

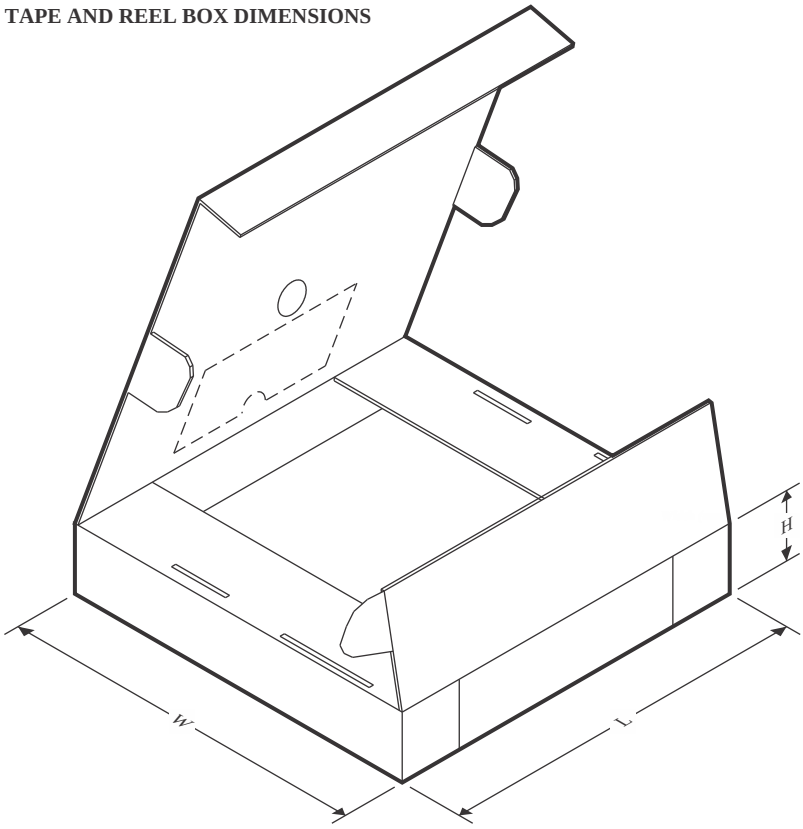
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73601MDBVREP	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73601MDCQREP	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS73601MDRBREP	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TPS73615MDBVREP	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73618MDBVREP	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73625MDBVREP	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73630MDBVREP	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73632MDBVREP	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73633MDBVREP	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

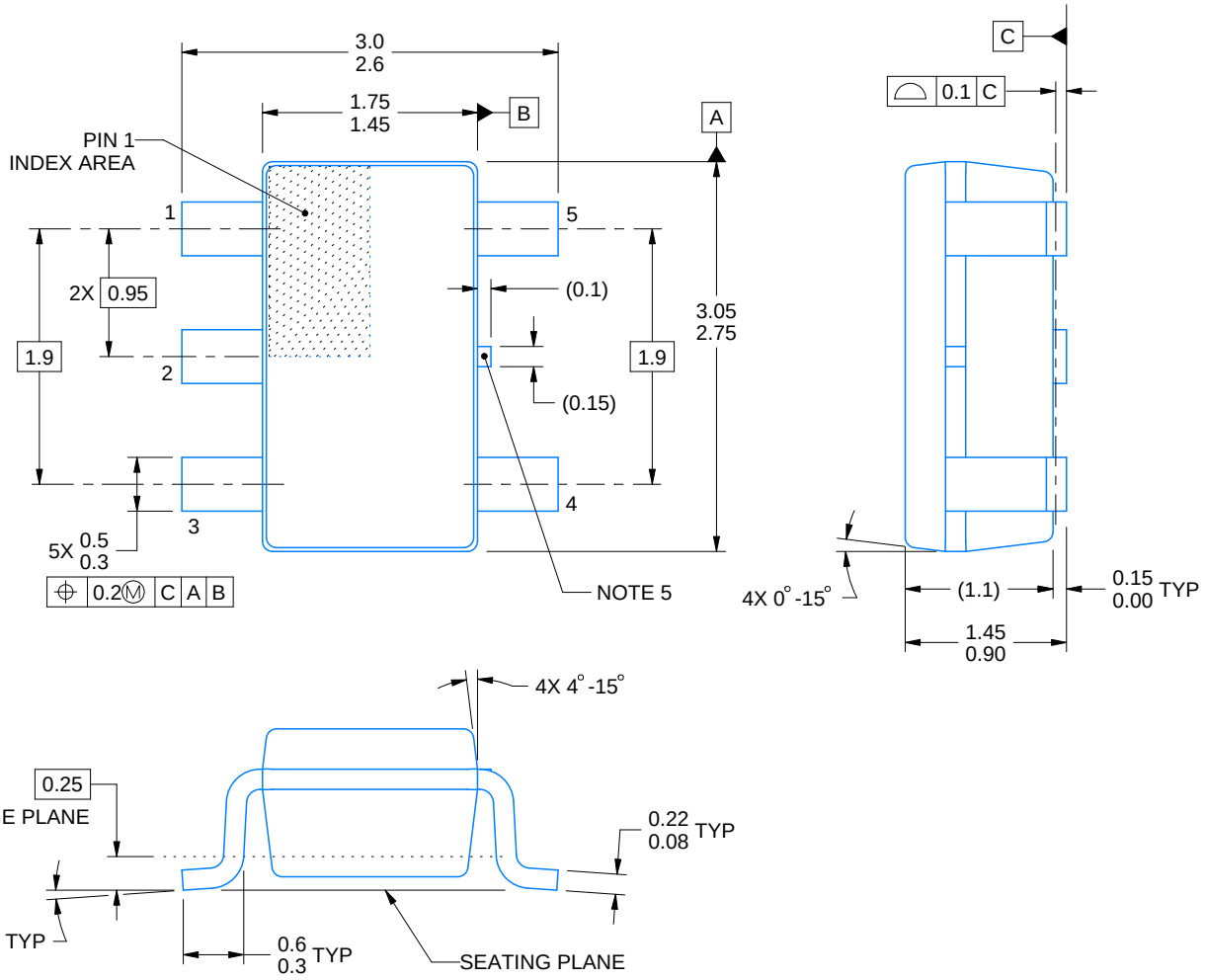
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73601MDBVREP	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS73601MDCQREP	SOT-223	DCQ	6	2500	346.0	346.0	41.0
TPS73601MDRBREP	SON	DRB	8	3000	367.0	367.0	38.0
TPS73615MDBVREP	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS73618MDBVREP	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS73625MDBVREP	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS73630MDBVREP	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS73632MDBVREP	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS73633MDBVREP	SOT-23	DBV	5	3000	200.0	183.0	25.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

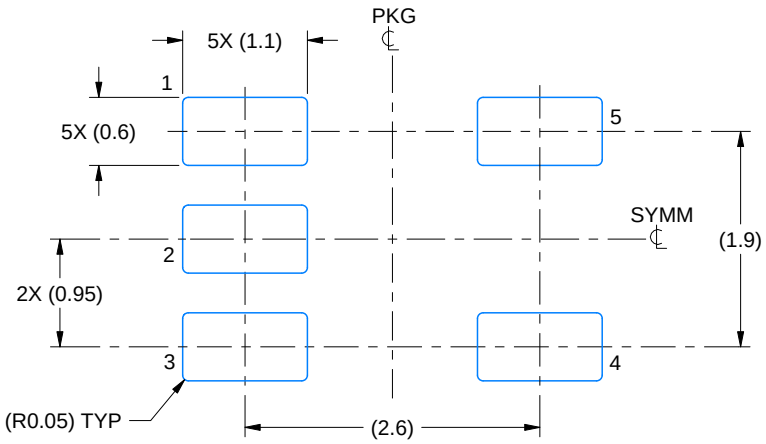
SMALL OUTLINE TRANSISTOR



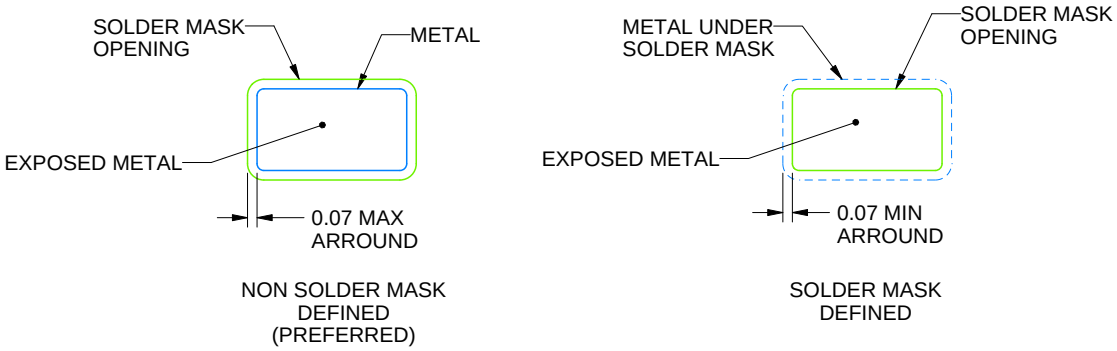
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

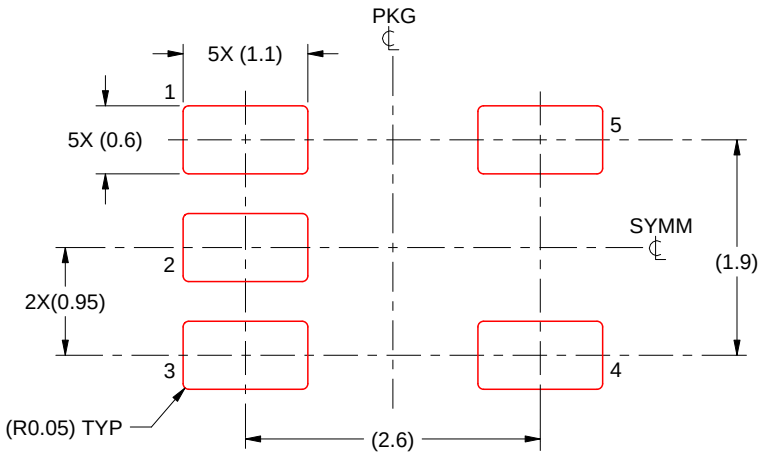


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

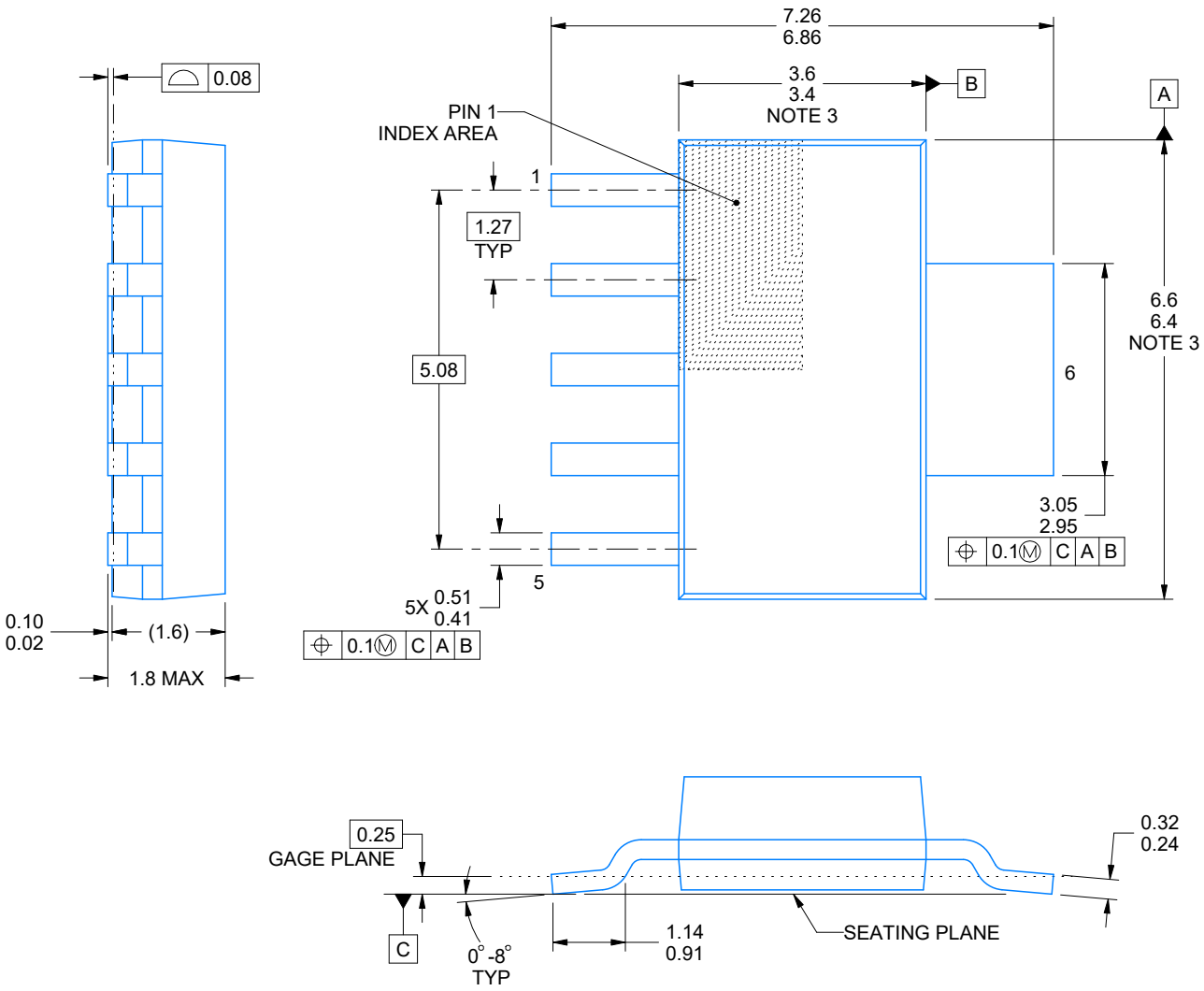
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCQ0006A

SOT - 1.8 mm max height

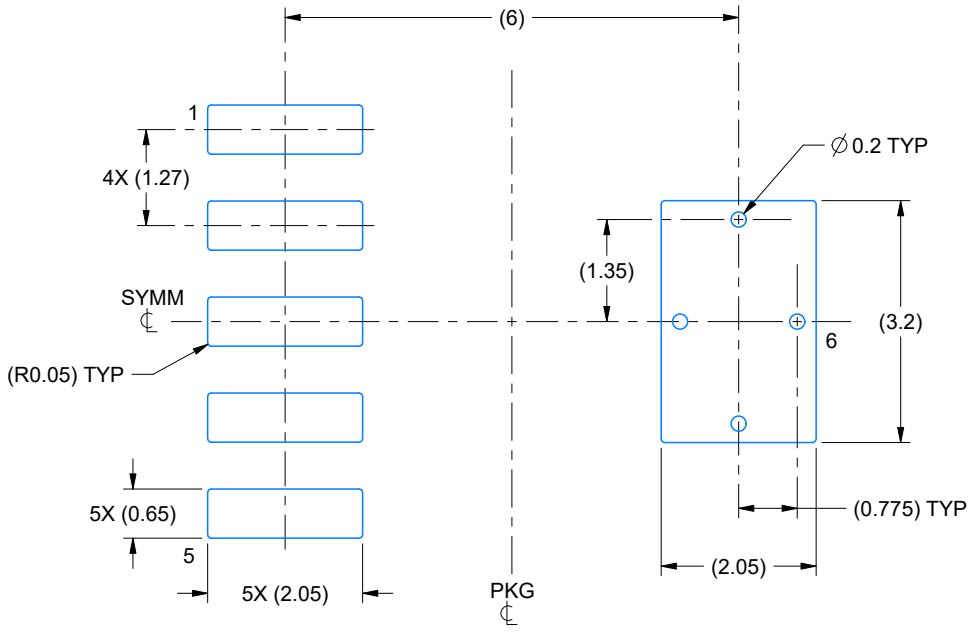
PLASTIC SMALL OUTLINE



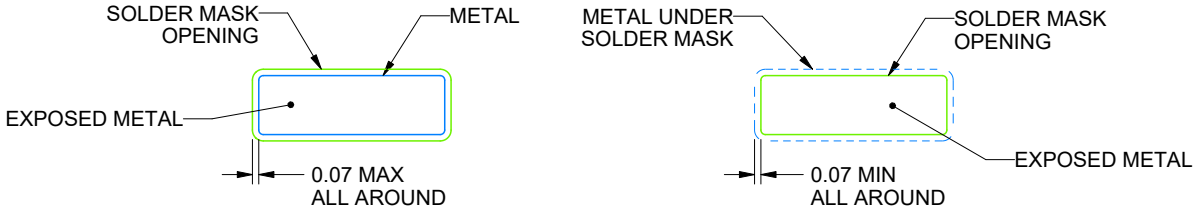
4214845/C 11/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

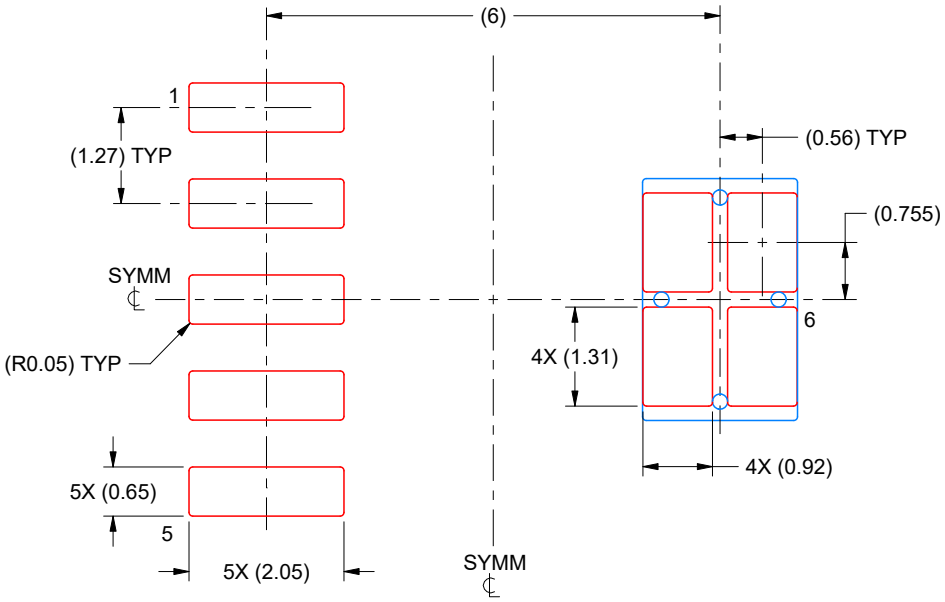


SOLDER MASK DETAILS

4214845/C 11/2021

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214845/C 11/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DRB 8

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

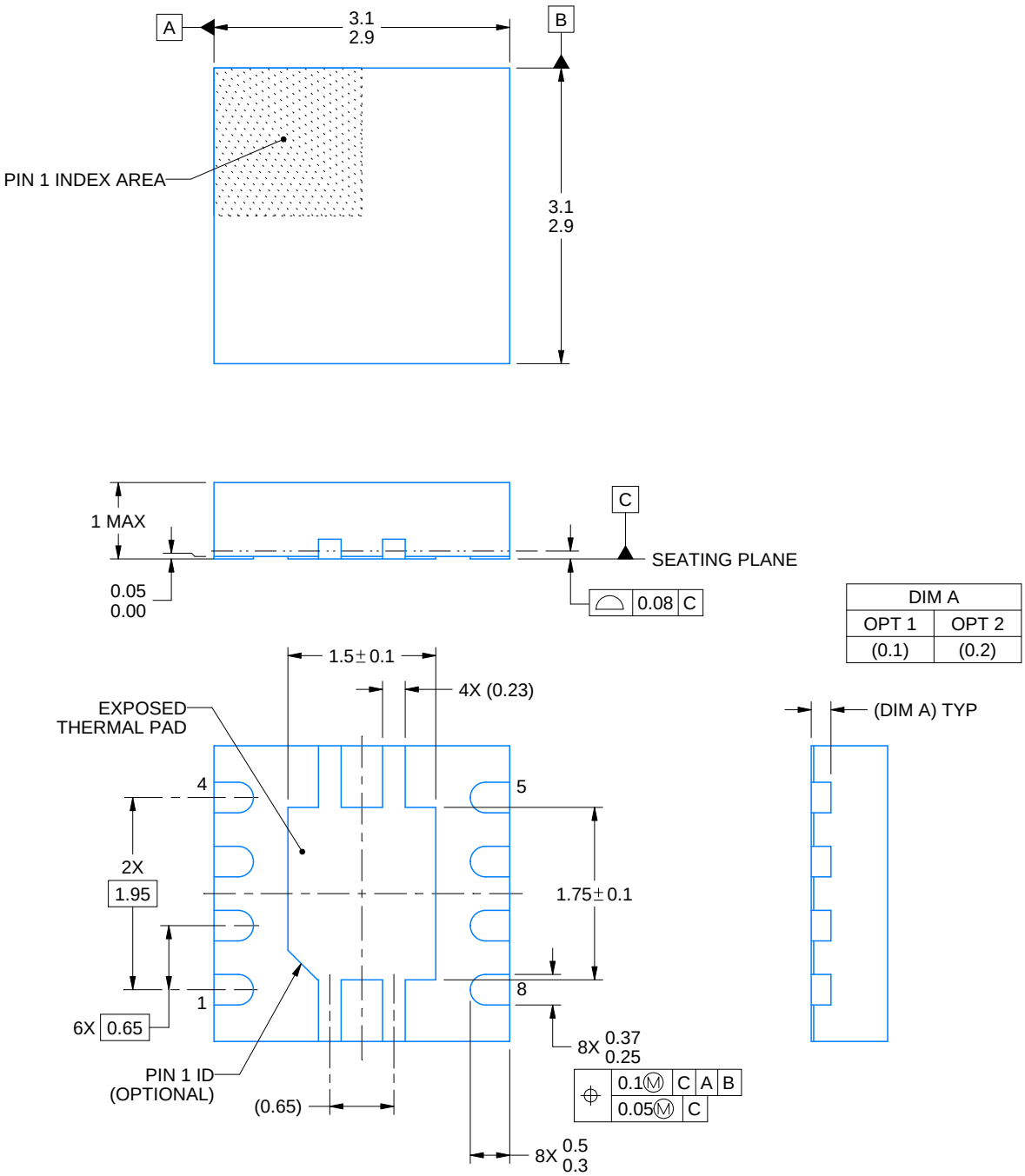
4203482/L

PACKAGE OUTLINE

DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

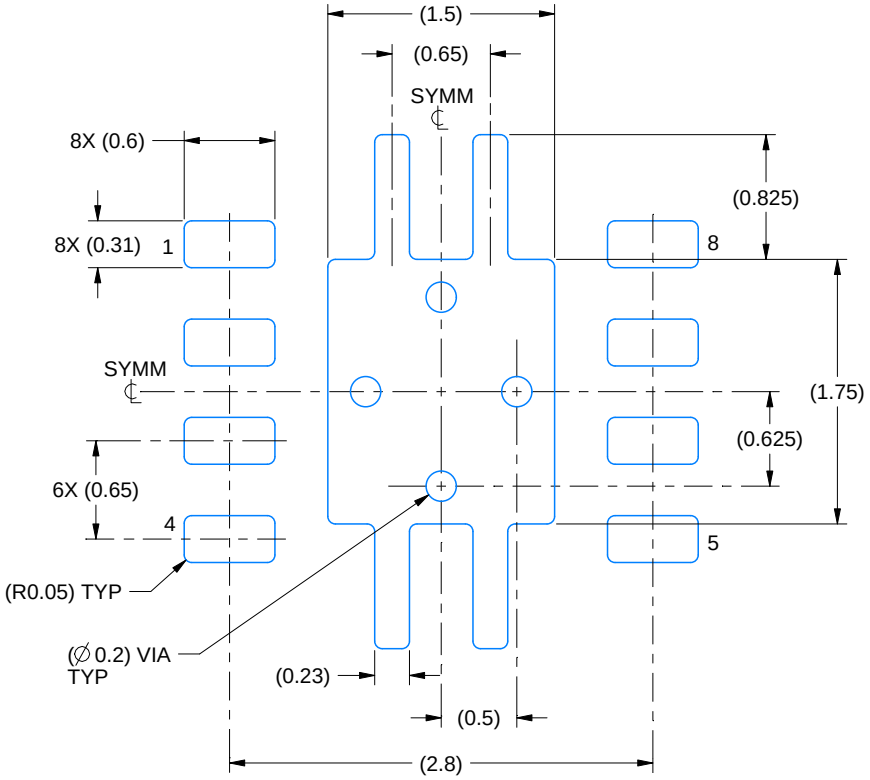
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

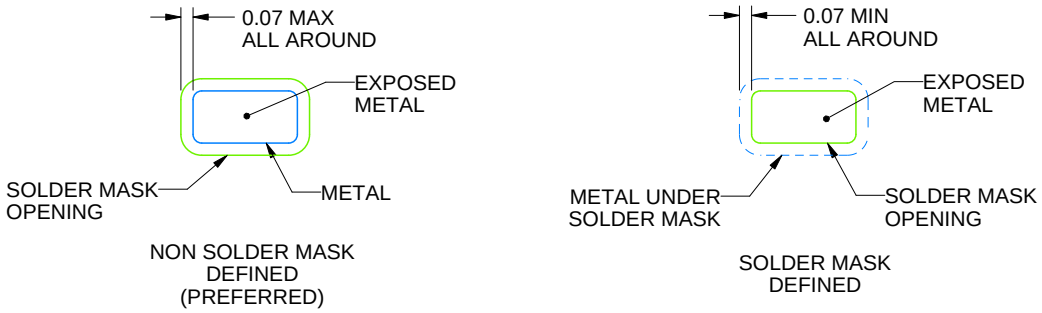
DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

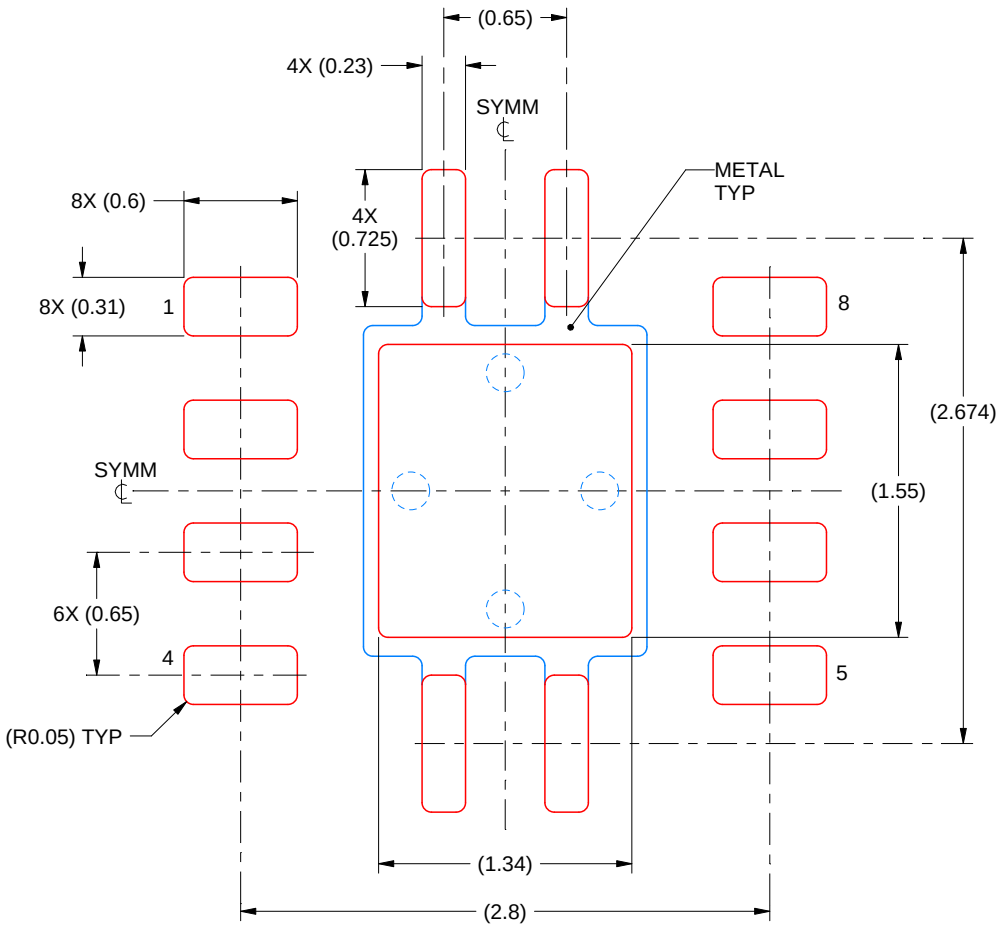


SOLDER MASK DETAILS

4218875/A 01/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218875/A 01/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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