TPS7H3xx4-SP Radiation-Hardened, 14V, 4-Channel Supervisor With Watchdog Timer

1 Features

- Radiation performance:
  - Radiation hardness assurance (RHA) up to a total ionizing dose (TID) of 100krad(Si)
  - Single-event latchup (SEL), single-event burnout (SEB), and single-event gate rupture (SEGR) immune up to linear energy transfer (LET) = 75MeV-cm^2/mg
  - Single-event functional interrupt (SEFI) and single-event transient (SET) characterized up to LET = 75MeV-cm^2/mg
- Wide supply IN voltage range (V_{IN}): 3V to 14V
- Monitor up to 4 voltage rails with high accuracy:
  - TPS7H3024: 2 OV + 2 UV or 2 window with push-pull $\overline{\text{RESETx}}$
  - TPS7H3134: 2 OV + 2 UV or 2 window with open-drain $\overline{\text{RESETx}}$
  - TPS7H3034: 4 UV or 4 OV with push-pull $\overline{\text{RESETx}}$
  - TPS7H3134: 4 UV or 4 OV with open-drain $\overline{\text{RESETx}}$
- Monitor coherent processor execution using the watchdog timer
- Single resistor programmable global delay timer
- Programmable watchdog time-out
- Precision threshold voltage and hysteresis current:
  - V_{TH_SENSEx} of 599.7mV ± 1% across: voltage, temperature, and radiation (TID)
  - I_{HYS_SENSEx} of 24µA ± 3% across: voltage, temperature, and radiation (TID)
- Push-Pull outputs with programmable pull-up voltage from 1.6V to 7V
  - Global $\overline{\text{RESETx}}$ pull-up domain (V_{PULL_UP1})
  - Common PWRGD and $\overline{\text{WDO}}$ pull-up domain (V_{PULL_UP2})
- SR_$\overline{\text{UVLO}}$ input to reset all outputs
  - Can also be used as configurable undervoltage lockout with an external resistor divider
- Available in military (–55°C to 125°C) temperature range

2 Applications

- Satellite electrical power system (EPS)
- Monitoring voltage rails for complex digital processors such as: FPGAs, SoCs, AFEs, and power systems for space applications
- Monitoring of coherent processor execution

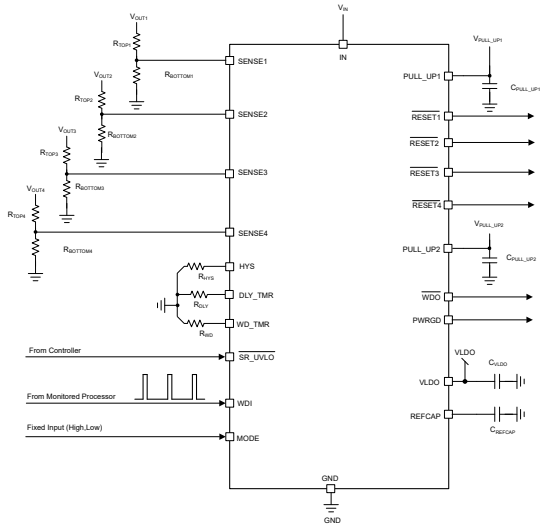
3 Description

The TPS7H3xx4-SP is an integrated, 3V to 14V, four-channel radiation-hardened power-supply supervisor with watchdog. An accurate 599.7mV ± 1% threshold voltage and a 24µA ± 3% hysteresis current provide programmable monitoring voltages. A global programmable delay timer is programmed via a single resistor. Additionally, a PWRGD output is provided to monitor the global power tree status. The device also incorporates a positive edge detection watchdog timer to monitor an external processor for coherent execution. Faults can be detected and mitigated by the external controller, using the SR_$\overline{\text{UVLO}}$ input. The device is offered with push-pull and open-drain outputs types.

Package Information

PART NUMBER(1)	GRADE	PACKAGE(2)
5962R2420601VXC	QMLV-RHA	22-pin ceramic (CFP) 6.21mm × 7.69mm Mass = 415.6mg
5962R2420602VXC(3)		
5962R2420603VXC(3)		
5962R2420604VXC(3)		
TPS7H3024HFT/EM	Engineering sample	
TPS7H3124HFT/EM(3)		
TPS7H3034HFT/EM(3)		
TPS7H3134HFT/EM(3)		

(1) For additional information, see Section 4.
(2) The mass is a nominal value and the body size (length × width) is a nominal value and does not include pins.
(3) Advanced information.



Note: Outputs shown here are push-pull

Typical Application

Table of Contents

4 Device Comparison Table

GENERIC PART NUMBER	OUTPUT TYPE	FUNCTION	RADIATION RATING(1)	GRADE(2)	PACKAGE	ORDERABLE PART NUMBER
TPS7H3024-SP	Push-pull	2 UV + 2 OV (or 2 window)	TID of 100krad(Si) RLAT, DSEE free to 75MeV-cm^2/mg	QMLV-RHA	22-pin CFP HFT	5962R2420601VXC
			None	Engineering model(3)		TPS7H3024HFT/EM
TPS7H3124-SP	Open-drain		TID of 100krad(Si) RLAT, DSEE free to 75MeV-cm^2/mg	QMLV-RHA		5962R2420602VXC(4)
			None	Engineering model(3)		TPS7H3124HFT/EM(4)
TPS7H3034-SP	Push-pull	4 UV or 4 OV	TID of 100krad(Si) RLAT, DSEE free to 75MeV-cm^2/mg	QMLV-RHA		5962R2420603VXC(4)
			None	Engineering model(3)		TPS7H3034HFT/EM(4)
TPS7H3134-SP	Open-drain		TID of 100krad(Si) RLAT, DSEE free to 75MeV-cm^2/mg	QMLV-RHA		5962R2420604VXC(4)
			None	Engineering model(3)		TPS7H3134HFT/EM(4)

(1) TID is total ionizing dose and DSEE is destructive single event effects. Additional information is available in the associated TID reports and SEE reports for each product.
(2) For additional information about part grade, view TI Part Ratings.
(3) These units are intended for engineering evaluation only. The units are processed to a non-compliant flow (such as no burn-in and only 25°C testing). These units are not designed for qualification, production, radiation testing, or flight use. Parts are not specified as to performance over temperature or operating life.
(4) Advanced information.

5 Pin Configuration and Functions

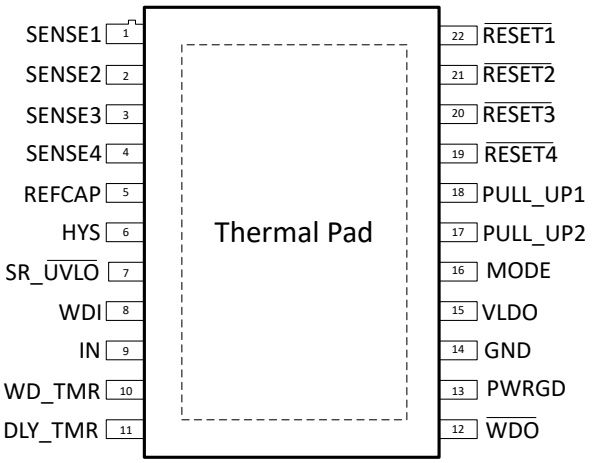


Figure 5-1. TPS7H30x4 HFT Package 22-Pin CFP (Top View)

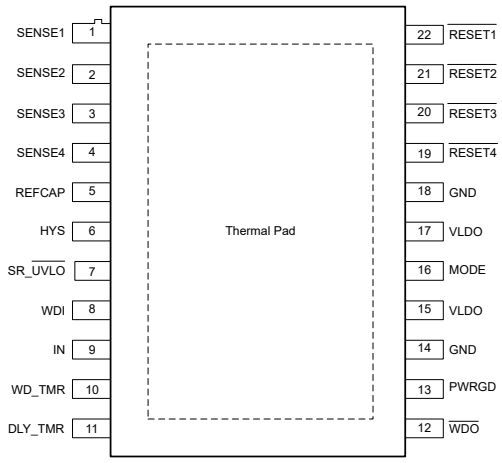


Figure 5-2. TPS7H31x4 HFT Package 22-Pin CFP (Top View)

Table 5-1. Pin Functions

PIN			TYPE[1]	DESCRIPTION
NAME	TPS7H30x4	TPS7H31x4		
SENSE1	1	1	I	The non-inverting input of the comparator used to monitor a desired voltage rail. To set the V_{ON1} and V_{OFF1} voltages, connect an external resistive divider between the rail to be monitored and GND with the middle point tied to SENSE1 pin. A voltage greater than V_{TH_SENSEx} (599.7mV typical) on this pin is considered as a regulated voltage rail (V_{ON1}). The V_{OFF1} is a function of the I_{HYS} current, the resistive divider, and V_{TH_SENSEx} . Refer to Top and Bottom Resistive Divider Design Equations.
SENSE2	2	2	I	The non-inverting input of the comparator used to monitor a desired voltage rail. To set the V_{ON2} and V_{OFF2} voltages, connect an external resistive divider between the rail to be monitored and GND with the middle point tied to SENSE2 pin. A voltage greater than V_{TH_SENSEx} (599.7mV typical) on this pin is considered as a regulated voltage rail (V_{ON2}). The V_{OFF2} is a function of the I_{HYS} current, the resistive divider, and V_{TH_SENSEx} . Refer to Top and Bottom Resistive Divider Design Equations.
SENSE3	3	3	I	The non-inverting input of the comparator used to monitor a desired voltage rail. To set the V_{ON3} and V_{OFF3} voltages, connect an external resistive divider between the rail to be monitored and GND with the middle point tied to SENSE3 pin. A voltage greater than V_{TH_SENSEx} (599.7mV typical) on this pin is considered as a regulated voltage rail (V_{ON2}). The V_{OFF2} is a function of the I_{HYS} current, the resistive divider, and V_{TH_SENSEx} .Refer to Top and Bottom Resistive Divider Design Equations.
SENSE4	4	4	I	The non-inverting input of the comparator used to monitor a desired voltage rail. To set the V_{ON4} and V_{OFF4} voltages, connect an external resistive divider between the rail to be monitored and GND with the middle point tied to SENSE4 pin. A voltage greater than V_{TH_SENSEx} (599.7mV typical) on this pin is considered as a regulated voltage rail (V_{ON4}). The V_{OFF4} is a function of the I_{HYS} current, the resistive divider, and V_{TH_SENSEx} .Refer to Top and Bottom Resistive Divider Design Equations.
REFCAP	5	5	O	1.2V internal reference. This pin requires a 470nF external capacitor to GND. Do not load this pin with any additional external circuitry
HYS	6	6	O	Hysteresis. Connect a 49.9kΩ resistor between this pin and GND, to program the hysteresis current (typically 24µA) at SENSE1 to SENSE4. Users are recommended to use a resistor with a 0.1% or better tolerance.
SR_$\overline{\text{UVLO}}$	7	7	O	System reset and UVLO input. Force this input low to assert all outputs low. A resistor divider from V_{IN} to GND can be used to set the device turn-on level.

Table 5-1. Pin Functions (continued)

PIN			TYPE[1]	DESCRIPTION
NAME	TPS7H30x4	TPS7H31x4		
WDI	8	8	I	Watchdog input. Toggle this signal from low to high to clear the watchdog timer. If this input is toggled low to high before the watchdog timer is expired, the $\overline{\text{WDO}}$ stays high, otherwise is asserted low.
IN	9	9	I	Input supply to the device. Input voltage range is from 3V to 14V. Connect at least a 0.1µF ceramic capacitor as close as possible to the pin.
WD_TMR	10	10	I/O	Watchdog timer. Connect a resistor to GND between 56.2kΩ and 174kΩ to set the watchdog timeout. The delay can be adjusted from 0.52s to 1.5s. Leave this pin floating to deactivate the watchdog timer.
DLY_TMR	11	11	I/O	Delay timer. Connect a resistor to GND between 10.5kΩ and 1.18MΩ to set the out-of-fault delay. The delay can be adjusted from 0.25ms to 25ms. Leave this pin floating for no delay.
$\overline{\text{WDO}}$	12	12	O	Watchdog output. Push-pull or open-drain output. For the push-pull output the V_{OH} level is set by the PULL_UP2 input supply voltage. For the open-drain output an external pull-up to the desired logic level is needed. A 10kΩ pull-up resistor is recommended.
PWRGD	13	13	O	Power Good. This output indicates when all rails (SENSE1 to SENS4) are in regulation. Push-pull or open-drain output. For the push-pull output the V_{OH} level is set by the PULL_UP2 input supply voltage. For the open-drain output an external pull-up to the desired logic level is needed. A 10kΩ pull-up resistor is recommended.
GND	14	14, 18	—	Ground.
VLDO	15	15, 17	O	Output of internal regulator. This pin requires at least a 1µF external ceramic capacitor to GND. This voltage can be used to create positive offset when monitoring negative voltages. For the TPS7H31x4, connect pins 15 and 17 externally through a 10kΩ resistor.The maximum load for this LDO is 5mA. This pin is not protected for over-current events.
MODE	16	16	I	Logical input to control the behavior of the output stage (window or UV + OV). For more details refer to Section 8.3.4. This input must not be dynamically changed. MODE=0 corresponds to 2 UV + 2 OV while MODE=1 corresponds to 2 window.
PULL_UP2	17	—	I	Input supply voltage to program the pull-up voltage for the push-pull outputs on PWRGD and $\overline{\text{WDO}}$. Connect at least a 1µF ceramic capacitor as close as possible to the pin.
PULL_UP1	18	—	I	Input supply voltage to program the global pull-up voltage for the push-pull outputs on $\overline{\text{RESET1}}$ to $\overline{\text{RESET4}}$. Connect at least a 1µF ceramic capacitor as close as possible to the pin.
$\overline{\text{RESET4}}$	19	19	O	Reset 4. $\overline{\text{RESET4}}$ is asserted low when SENSE4 is in a fault. Push-pull or open-drain output. For the push-pull output the V_{OH} level is set by the PULL_UP1 input supply voltage. For the open-drain output an external pull-up to the desired logic level is needed. A 10kΩ pull-up resistor is recommended.
$\overline{\text{RESET3}}$	20	20	O	Reset 3. $\overline{\text{RESET3}}$ is asserted low when SENSE3 is in a fault. Push-pull or open-drain output. For the push-pull output the V_{OH} level is set by the PULL_UP1 input supply voltage. For the open-drain output an external pull-up to the desired logic level is needed. A 10kΩ pull-up resistor is recommended.
$\overline{\text{RESET2}}$	21	21	O	Reset 2. $\overline{\text{RESET2}}$ is asserted low when SENSE2 is in a fault. Push-pull or open-drain output. For the push-pull output the V_{OH} level is set by the PULL_UP1 input supply voltage. For the open-drain output an external pull-up to the desired logic level is needed. A 10kΩ pull-up resistor is recommended.
$\overline{\text{RESET1}}$	22	22	O	Reset 1. $\overline{\text{RESET1}}$ is asserted low when SENSE1 is in a fault. Push-pull or open-drain output. For the push-pull output the V_{OH} level is set by the PULL_UP1 input supply voltage. For the open-drain output an external pull-up to the desired logic level is needed. A 10kΩ pull-up resistor is recommended.
Thermal pad	—	—	—	Internally grounded. It is recommended to connect this metal thermal pad to a large ground plane for effective heat dissipation.

Table 5-1. Pin Functions (continued)

PIN			TYPE[1]	DESCRIPTION
NAME	TPS7H30x4	TPS7H31x4		
Metal lid	Lid	Lid	—	The lid is internally connected to the thermal pad and GND through the seal ring.

(1) I = Input, O = Output, I/O = Input or Output, — = Other

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
Input voltage	IN	–0.3	16	V
	WDI, MODE	–0.3	7.5	
	SENSE1, SENSE2, SENSE3, SENSE4	–0.3	3.6	
	PULL_UP1, PULL_UP2	–0.3	7.5	
	SR_$\overline{\text{UVLO}}$	–0.3	7.5	
	DLY_TMR, WD_TMR	–0.3	3.6	
Output voltage	REFCAP	–0.3	2	V
	VLDO	–0.3	3.6	
	HYS	–0.3	3.6	
	$\overline{\text{RESET1}}$, $\overline{\text{RESET2}}$, $\overline{\text{RESET3}}$, $\overline{\text{RESET4}}$	–0.3	7.5	
	PWRGD, $\overline{\text{WDO}}$	–0.3	7.5	
Output current	$\overline{\text{RESET1}}$, $\overline{\text{RESET2}}$, $\overline{\text{RESET3}}$, $\overline{\text{RESET4}}$	–20	20	mA
	PWRGD, $\overline{\text{WDO}}$	–20	20	
Junction temperature	T_J	–55	150	°C
Storage temperature	T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages values are with respect to GND.

6.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±1000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins (2)	±250	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted) (1)

		MIN	NOM	MAX	UNIT
Input voltage	IN	3		14	V
	WDI, MODE	0		7	
	SENSE1, SENSE2, SENSE3, SENSE4	0		3.5	
	PULL_UP1, PULL_UP2	1.6		7	
	SR_$\overline{\text{UVLO}}$	0		7	
Output voltage	$\overline{\text{RESET1}}$, $\overline{\text{RESET2}}$, $\overline{\text{RESET3}}$, $\overline{\text{RESET4}}$	0		7	V
	PWRGD, $\overline{\text{WDO}}$	0		7	
Output current	$\overline{\text{RESET1}}$, $\overline{\text{RESET2}}$, $\overline{\text{RESET3}}$, $\overline{\text{RESET4}}$	–10		10	mA
	PWRGD, $\overline{\text{WDO}}$	–10		10	
Junction temperature	T_J	–55		125	°C

over operating temperature range (unless otherwise noted) (1)

		MIN	NOM	MAX	UNIT
Input voltage slew rate	SR_{IN}	0.001		10	V/µs

(1) All voltages values are with respect to GND.

6.4 Thermal Information

THERMAL METRIC(1)		TPS7H3xx4-SP HFT (CFP) 22 pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	16.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	8.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	17	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

6.5 Electrical Characteristics

Over 3V ≤ V_{IN} ≤ 14V, R_{DLY_TMR} = 10kΩ, R_{WD_TMR} = 56.2kΩ, V_{PULL_UP1} = 3.3V, V_{PULL_UP2} = 3.3V, over temperature range (T_A= –55°C to 125°C), unless otherwise noted; includes group E radiation testing at T_A = 25°C for QML RHA devices (1) (2)

PARAMETER		TEST CONDITIONS	SUB-GROUP (3)	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGES AND CURRENTS							
I_{Q_IN}	V_{IN} quiescent current	$V_{SR\_\overline{UVLO}}$ > $V_{TH\_SR\_\overline{UVLO}\_RISING\ (MAX)}$	1, 2, 3		1.5	2.5	mA
I_{SD_IN}	V_{IN} shutdown current	$V_{SR\_\overline{UVLO}}$ = 0V	1, 2, 3		1.5	2.1	mA
$UVLO_{RISE}$	V_{IN} rising undervoltage lockout		1, 2, 3	2.73	2.80	2.88	V
$UVLO_{FALL}$	V_{IN} falling udervoltage lockout		1, 2, 3	2.58	2.65	2.72	V
V_{LDO}	Internal linear regulator output voltage	4V ≤ V_{IN} ≤ 14V	1, 2, 3	3.23	3.29	3.37	V
		V_{IN} = 3V	1, 2, 3	98%	99%		× V_{IN}
$VLDO_{I\_MAX}$	VLDO maximum current	3.65V ≤ V_{IN} ≤ 14V, VLDO= 98.5% x $VLDO_{(NOM)}$	1, 2, 3			5	mA
REFCAP	Internal bandgap voltage		1, 2, 3	1.188	1.2	1.212	V
V_{POR_IN}	IN power on reset voltage (4)	1.6V ≤ V_{PULL_UPx} ≤ 7V, V_{OL} ≤ 320mV with $I_{\overline{RESETx}}$ = –1mA	1, 2, 3		1.42	2	V
$V_{POR\_PULL\_UPx}$	PULL_UPx power on reset voltage (5)	V_{IN} = 0V, V_{OL} ≤ 320mV, $I_{\overline{RESETx}}$ = –100µA	1, 2, 3		0.85	1.1	V
V_{HYS}	HYS pin internal voltage	R_{HYS} = 49.9kΩ	1, 2, 3	1.164	1.2	1.236	V
SENSE1 TO SENSE4, SR_UVLO, WDI AND MODE COMPARATOR INPUTS							
V_{TH_SENSEx}	Threshold voltage at SENSEx		1, 2, 3	593.1	599.7	604.9	mV
I_{HYS_SENSEx}	SENSEx hysteresis current	V_{SENSEx} = 700mV	1, 2, 3	23.28	24	24.72	µA
I_{LKG_SENSEx}	Input leakage current at SENSEx	V_{SENSEx} = 500mV	1, 2, 3		1	100	nA

6.5 Electrical Characteristics (continued)

Over 3V ≤ V_{IN} ≤ 14V, R_{DLY_TMR} = 10kΩ, R_{WD_TMR} = 56.2kΩ, V_{PULL_UP1} = 3.3V, V_{PULL_UP2} = 3.3V, over temperature range (T_A= –55°C to 125°C), unless otherwise noted; includes group E radiation testing at T_A = 25°C for QML RHA devices (1) (2)

PARAMETER		TEST CONDITIONS		SUB-GROUP (3)	MIN	TYP	MAX	UNIT
$V_{TH\_SR\_\overline{UVLO}\_RISING}$	Rising threshold voltage at SR_$\overline{UVLO}$			1, 2, 3	580	602	618	mV
$V_{TH\_SR\_\overline{UVLO}\_FALLING}$	Falling threshold voltage at SR_$\overline{UVLO}$			1, 2, 3	475	499	517	
$I_{LKG\_SR\_\overline{UVLO}}$	Input leakage current at SR_$\overline{UVLO}$	$V_{SR\_\overline{UVLO}}$ = 7V		1, 2, 3		2	100	nA
$V_{TH\_WDI\_RISING}$	Rising threshold voltage at WDI			1, 2, 3	578	602	624	mV
$V_{TH\_WDI\_FALLING}$	Falling threshold voltage at WDI			1, 2, 3	473	498	521	mV
I_{LKG_WDI}	Input leakage current at WDI	V_{WDI} = 7V		1, 2, 3		1.4	100	nA
$V_{TH\_MODE\_RISING}$	Rising threshold voltage at MODE			1, 2, 3 7, 8	576	600	623	mV
$V_{TH\_MODE\_FALLING}$	Falling threshold voltage at MODE			1, 2, 3 7, 8	475	498	520	mV
I_{LKG_MODE}	Input leakage current at MODE	V_{MODE} = 7V		1, 2, 3		1	100	nA
$\overline{RESET1}$ TO $\overline{RESET4}$, PWRGD AND $\overline{WDO}$ PUSH PULL OUTPUTS (TPS7H3024 AND TPS7H3034)								
$PULL\_UPx_{LKG}$	PULL_UPx leakage current	V_{PULL_UPx} = 7V, $\overline{RESETx}$= LOW		1, 2, 3		48	100	µA
$V_{OL\_\overline{RESETx}}$	Low-level $\overline{RESETx}$ output voltage	1.6V ≤ V_{PULL_UP1} ≤ 7V	I_{LOAD} = –2mA	1, 2, 3			5%	x V_{PULL_UP1}
			I_{LOAD} = –10mA	1, 2, 3			23%	
$V_{OH\_\overline{RESETx}}$	High-level $\overline{RESETx}$ output voltage	1.6V ≤ V_{PULL_UP1} ≤ 7V	I_{LOAD} = 2mA	1, 2, 3	95%			
			I_{LOAD} = 10mA	1, 2, 3	75%			
V_{OL_PWRGD}	Low-level PWRGD output voltage	1.6V ≤ V_{PULL_UP2} ≤ 7V	I_{LOAD} = –2mA	1, 2, 3			5%	x V_{PULL_UP2}
			I_{LOAD} = –10mA	1, 2, 3			23%	
V_{OH_PWRGD}	High-level PWRGD output voltage	1.6V ≤ V_{PULL_UP2} ≤ 7V	I_{LOAD} = 2mA	1, 2, 3	95%			
			I_{LOAD} = 10mA	1, 2, 3	75%			
$V_{OL\_\overline{WDO}}$	Low-level $\overline{WDO}$ output voltage	1.6V ≤ V_{PULL_UP2} ≤ 7V	I_{LOAD} = –2mA	1, 2, 3			5%	
			I_{LOAD} = –10mA	1, 2, 3			23%	
$V_{OH\_\overline{WDO}}$	High-level $\overline{WDO}$ output voltage	1.6V ≤ V_{PULL_UP2} ≤ 7V	I_{LOAD} = 2mA	1, 2, 3	95%			
			I_{LOAD} = 10mA	1, 2, 3	75%			
$SR_{\overline{RESETx}\_RISE}$	$\overline{RESETx}$ rising output voltage slew rate	10% to 90% of V_{PULL_UP1}, R_{LOAD} = 50kΩ, C_{LOAD} = 100pF	1.6V ≤ V_{PULL_UP1} ≤ 7V	7, 8 9, 10, 11	17	298		V/µs
SR_{PWRGD_RISE}	PWRGD rising output voltage slew rate			7, 8 9, 10, 11	17	298		
$SR_{\overline{WDO}\_RISE}$	$\overline{WDO}$ rising output voltage slew rate			7, 8 9, 10, 11	17	298		
$SR_{\overline{RESETx}\_FALL}$	$\overline{RESETx}$ falling output voltage slew rate	90% to 10% of V_{PULL_UP1}, R_{LOAD} = 50kΩ, C_{LOAD} = 100pF	1.6V ≤ V_{PULL_UP1} ≤ 7V	7, 8 9, 10, 11	44	186		
SR_{PWRGD_FALL}	PWRGD falling output voltage slew rate			7, 8 9, 10, 11	44	186		
$SR_{\overline{WDO}\_FALL}$	$\overline{WDO}$ falling output voltage slew rate			7, 8 9, 10, 11	44	186		

6.5 Electrical Characteristics (continued)

Over 3V ≤ V_{IN} ≤ 14V, R_{DLY_TMR} = 10kΩ, R_{WD_TMR} = 56.2kΩ, V_{PULL_UP1} = 3.3V, V_{PULL_UP2} = 3.3V, over temperature range (T_A= –55°C to 125°C), unless otherwise noted; includes group E radiation testing at T_A = 25°C for QML RHA devices (1) (2)

PARAMETER		TEST CONDITIONS		SUB-GROUP (3)	MIN	TYP	MAX	UNIT
$R_{\overline{RESETx}\_PULL\_UP}$	$\overline{RESET}$ PMOS source output resistance	I_{LOAD} = 2mA	1.6V ≤ V_{PULL_UP1} < 3.3V	1, 2, 3		20	40	Ω
			3.3V ≤ V_{PULL_UP1} ≤ 7V	1, 2, 3		9	20	
$R_{PWRGD\_PULL\_UP}$	PWRGD PMOS source output resistance	I_{LOAD} = 2mA	1.6V ≤ V_{PULL_UP2} < 3.3V	1, 2, 3		20	40	
			3.3V ≤ V_{PULL_UP2} ≤ 7V	1, 2, 3		9	20	
$R_{\overline{WDO}\_PULL\_UP}$	$\overline{WDO}$ PMOS source output resistance	I_{LOAD} = 2mA	1.6V ≤ V_{PULL_UP2} < 3.3V	1, 2, 3		20	40	
			3.3V ≤ V_{PULL_UP2} ≤ 7V	1, 2, 3		9	20	
$R_{\overline{RESETx}\_PULL\_DOWN}$	$\overline{RESET}$ NMOS sink output resistance	I_{LOAD} = –2mA, 1.6V ≤ V_{PULL_UP1} ≤ 7V		1, 2, 3		16	36	
$R_{PWRGD\_PULL\_DOWN}$	PWRGD NMOS sink output resistance	I_{LOAD} = –2mA, 1.6V ≤ V_{PULL_UP1} ≤ 7V		1, 2, 3		16	36	
$R_{\overline{WDO}\_PULL\_DOWN}$	$\overline{WDO}$ NMOS sink output resistance	I_{LOAD} = –2mA, 1.6V ≤ V_{PULL_UP1} ≤ 7V		1, 2, 3		16	36	
RESET1 TO RESET4, PWRGD AND WDO OPEN DRAIN (TPS7H3124 AND TPS7H3134)								
$\overline{RESETx}_{LKG}$	$\overline{RESETx}$ leakage current	$V_{\overline{RESETx}}$ = 7V		1, 2, 3		23	600	nA
$PWRGD_{LKG}$	PWRGD leakage current	V_{PWRGD} = 7V		1, 2, 3		23	600	
$\overline{WDO}_{LKG}$	WDO leakage current	$V_{\overline{WDO}}$ = 7V		1, 2, 3		23	600	
$R_{\overline{RESETx}\_PULL\_DOWN}$	RESET NMOS sink output resistance	I_{LOAD} = –2mA, 1.6V ≤ V_{PULL_UP} ≤ 7V		1, 2, 3		131	200	Ω
$R_{PWRGD\_PULL\_DOWN}$	PWRGD NMOS sink output resistance			1, 2, 3		131	200	
$R_{\overline{WDO}\_PULL\_DOWN}$	$\overline{WDO}$ NMOS sink output resistance			1, 2, 3		131	200	
$V_{OL\_\overline{RESETx}}$	Low level $\overline{RESETx}$ output voltage	1.6V ≤ V_{PULL_UP} ≤ 7V	I_{LOAD} = -2mA	1, 2, 3		0.262	0.4	V
			I_{LOAD} = -10mA	1, 2, 3		1.31	2	
V_{OL_PWRGD}	Low level PWRGD output voltage	1.6V ≤ V_{PULL_UP} ≤ 7V	I_{LOAD} = -2mA	1, 2, 3		0.262	0.4	
			I_{LOAD} = -10mA	1, 2, 3		1.31	2	
$V_{OL\_\overline{WDO}}$	Low level $\overline{WDO}$ output voltage	1.6V ≤ V_{PULL_UP} ≤ 7V	I_{LOAD} = -2mA	1, 2, 3		0.262	0.4	
			I_{LOAD} = -10mA	1, 2, 3		1.31	2	
THERMAL PROTECTION								
T_{SD_ENTER}	Thermal shutdown enter temperature					185		°C
T_{SD_EXIT}	Thermal shutdown exit temperature					171		
DELAY AND WATCHDOG TIMERS								
t_{DLY_TMR}	Delay time	R_{DLY_TMR} = 10.5kΩ		1, 2, 3	0.22	0.26	0.33	ms
		R_{DLY_TMR} = 619kΩ		1, 2, 3	11.3	12.5	13.7	
		R_{DLY_TMR} = 1.18MΩ		1, 2, 3	21.3	23.7	26.2	

6.5 Electrical Characteristics (continued)

Over 3V ≤ V_{IN} ≤ 14V, R_{DLY_TMR} = 10kΩ, R_{WD_TMR} = 56.2kΩ, V_{PULL_UP1} = 3.3V, V_{PULL_UP2} = 3.3V, over temperature range (T_A= –55°C to 125°C), unless otherwise noted; includes group E radiation testing at T_A = 25°C for QML RHA devices (1) (2)

PARAMETER		TEST CONDITIONS	SUB-GROUP (3)	MIN	TYP	MAX	UNIT
t_{WD_TMR}	Watchdog time-out	R_{WD_TMR} = 56.2kΩ	1, 2, 3	0.43	0.52	0.57	s
		R_{WD_TMR} = 118kΩ	1, 2, 3	0.8	1	1.2	
		R_{WD_TMR} = 174kΩ	1, 2, 3	1.34	1.5	1.7	

(1) See the 5962R24206 SMD (standard microcircuit drawing) for additional information on the RHA devices.
(2) All voltage values are with respect to GND.
(3) For subgroup definitions, see Quality Conformance Inspection table.
(4) V_{POR_IN} is the minimum V_{IN} voltage for a controlled output state, when 1.6V ≤ V_{PULL_UPx} ≤ 7V. Below V_{POR_IN}, the output state cannot be determined.
(5) $V_{POR\_PULL\_UPx}$ is the minimum V_{PULL_UPx} voltage for a controlled output state, when V_{IN} ≤ 3V. Below $V_{POR\_PULL\_UPx}$ the output state cannot be determined.

6.6 Timing Requirements

Over 3V ≤ V_{IN} ≤ 14V, R_{DLY_TMR} = 10kΩ, R_{REG_TMR} = 10kΩ, V_{PULL_UP1} = 3.3V, V_{PULL_UP2} = 3.3V, over temperature range (T_A = –55°C to 125°C) unless otherwise noted; includes group E radiation testing at T_A = 25°C for RHA devices (1)

PARAMETER		TEST CONDITIONS		SUB-GROUP (2)	MIN	TYP	MAX	UNIT
$t_{START\_UP\_DLY}$	Start-up delay time (3)	V_{REFCAP} ≥ 1.1V, See Figure 7-1		1, 2, 3		0.3	2.8	ms
$t_{pd\_\overline{RESETx}}$	$\overline{RESET}$ propagation delay	DLY_TMR = Open, See Figure 7-2 and Figure 7-3	TPS7H3024 and TPS7H3034 (push-pull)	1, 2, 3		0.62	4.3	µs
t_{pd_PWRGD}	PWRGD propagation delay	DLY_TMR = Open, See Figure 7-4				0.51	4.3	
$t_{pd\_\overline{RESETx}}$	$\overline{RESET}$ propagation delay	DLY_TMR = Open, See Figure 7-5 and Figure 7-6	TPS7H3124 andTPS7H3134 (open-drain) R_{PULL_UP} = 10kΩ and C_{LOAD} = 100pF	1, 2, 3		2.6	4.9	µs
t_{pd_PWRGD}	PWRGD propagation delay	DLY_TMR = Open, See Figure 7-7				2.6	4.9	
$t_{pd\_SR\_\overline{UVLO}}$	SR_$\overline{UVLO}$ propagation delay	See Figure 7-8		1, 2, 3		0.92	2	µs
t_{pd_WDI}	WDI propagation delay	See Figure 7-9 TPS7H3024 and TPS7H3034 (push-pull)	t_{WD_TMR} = 0.52s	1, 2, 3		23	40	µs
			t_{WD_TMR} = 1s			47	80	
			t_{WD_TMR} = 1.5s			68	116	
t_{pd_WDI}	WDI propagation delay	See Figure 7-10 TPS7H3124 and TPS7H3134 (open-drain) R_{PULL_UP} = 10kΩ and C_{LOAD} = 100pF	t_{WD_TMR} = 0.52s	1, 2, 3		30	48	µs
			t_{WD_TMR} = 1s			54	94	µs
			t_{WD_TMR} = 1.5s			76	131	µs
t_{PW_WDI}	WDI minimum pulse width	See Figure 7-11		4, 5, 6	2			× t_{WD_OSC}
$t_{PW\_SR\_\overline{UVLO}}$	SR_UVLO minimum pulse width for valid reset	See Figure 7-12		4, 5, 6		0.61	1.1	µs
$t_{h\_VENSEx\_FAULT}$	VSENSEx hold time for valid fault detection	C_{LOAD} = 100pF, See Figure 7-13 and Figure 7-14		4, 5, 6		0.56	2.2	µs
$t_{h\_VENSEx\_RISE}$	Rising threshold on VSENSEx hold time	See Figure 7-15 and Figure 7-16		4, 5, 6			3.7	µs

(1) See the 5962R24206 SMD (standard microcircuit drawing) for additional information on the RHA device.
(2) For subgroup definitions, see Quality Conformance Inspection table.
(3) During the power-on, V_{IN} must be at or above $UVLO_{RISE(MAX)}$ for at least $t_{Start\_up\_delay}$ for all internal references to be within specification.

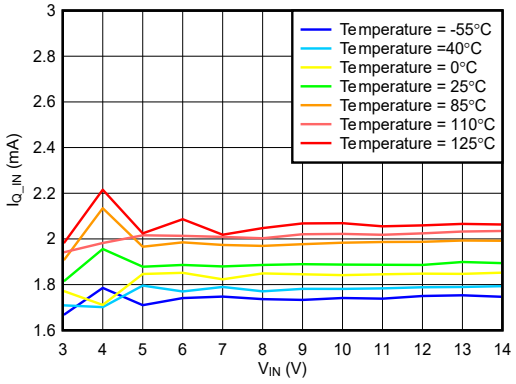
6.7 Quality Conformance Inspection

MIL-STD-883, Method 5005 - Group A

SUBGROUP	DESCRIPTION	TEMP (°C)
1	Static tests at	25
2	Static tests at	125
3	Static tests at	–55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	–55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	–55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	–55

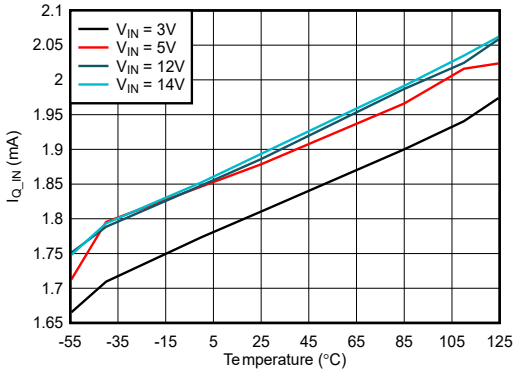
6.8 Typical Characteristics

R_{DLY_TMR} = 10.5kΩ, R_{WD_TMR} = 56.2kΩ, V_{PULL_UP1} = 3.3V, V_{PULL_UP2} = 3.3V, R_{HYS} = 49.9kΩ, MODE = Logic Low, for the TPS7H3024, unless otherwise noted.



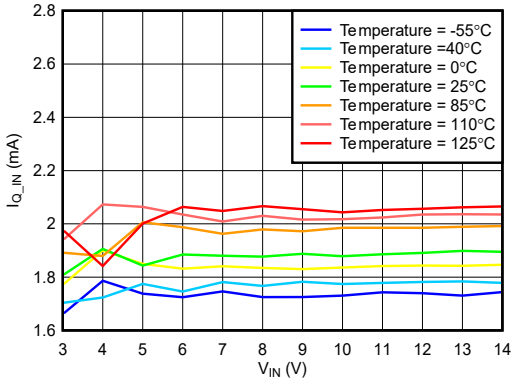
RESETx = Low V_{PULL_UPx} = 7V

Figure 6-1. I_{Q_IN} vs V_{IN} Across Temperature with RESETx = Low



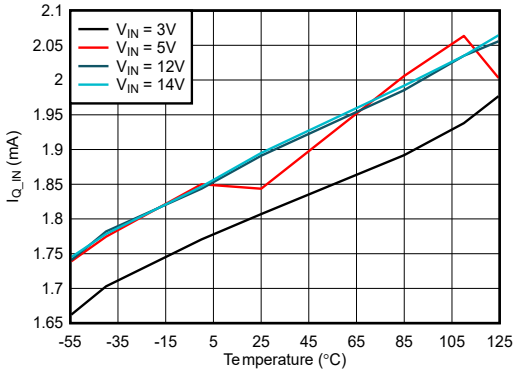
RESETx = Low V_{RESETx} = 7V

Figure 6-2. I_{Q_IN} vs Temperature Across V_{IN} with RESETx = Low



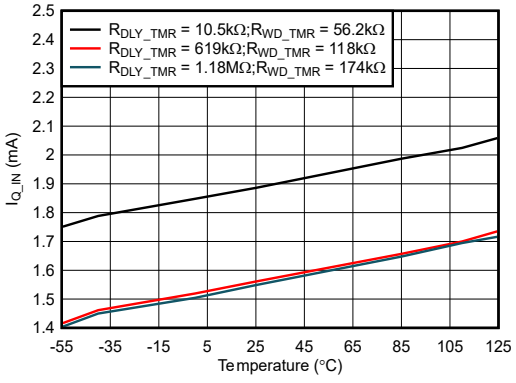
RESETx = High V_{PULL_UPx} = 7V

Figure 6-3. I_{Q_IN} vs V_{IN} Across Temperature with RESETx = High



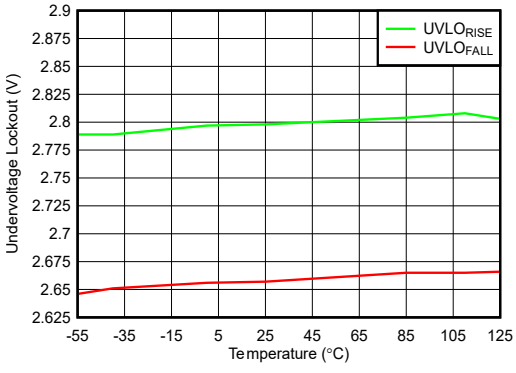
RESETx = High V_{RESETx} = 7V

Figure 6-4. I_{Q_IN} vs Temperature Across V_{IN} with RESETx = High



V_{IN} = 12V RESETx = Low
V_{PULL_UPx} = 7V

Figure 6-5. IQ_IN vs Temperature Across DLY_TMR and WD_TMR Resistance



R_{DLY_TMR} = Floating R_{WD_TMR} = Floating

Figure 6-6. Undervoltage Lockout vs Temperature

6.8 Typical Characteristics (continued)

R_{DLY_TMR} = 10.5kΩ, R_{WD_TMR} = 56.2kΩ, V_{PULL_UP1} = 3.3V, V_{PULL_UP2} = 3.3V, R_{HYS} = 49.9kΩ, MODE = Logic Low, for the TPS7H3024, unless otherwise noted.

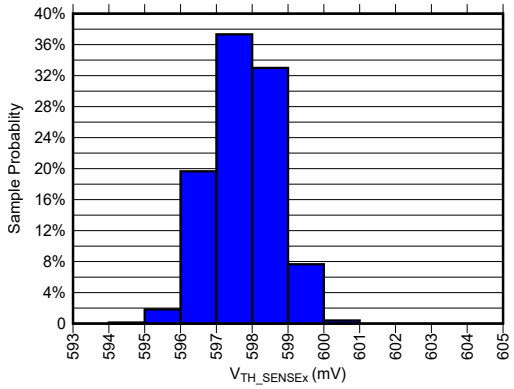


Figure 6-7. V_{TH_SENSEx} Voltage Distribution at Temperature of –55°C

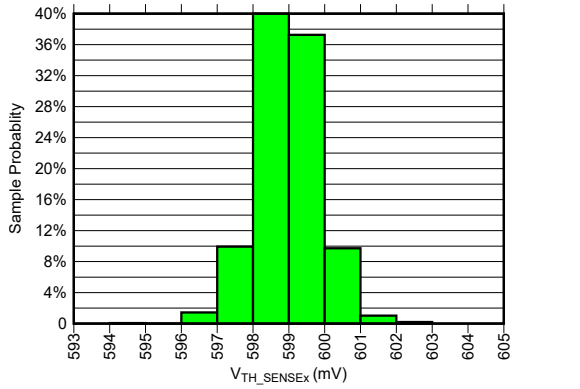


Figure 6-8. V_{TH_SENSEx} Voltage Distribution at Temperature of +25°C

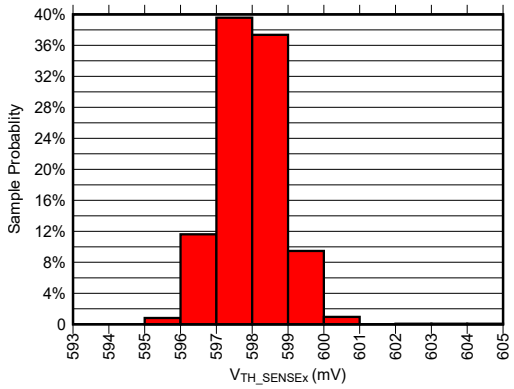


Figure 6-9. V_{TH_SENSEx} Voltage Distribution at Temperature of 125°C

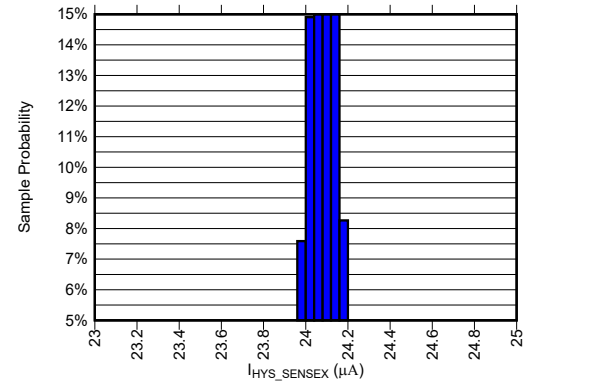


Figure 6-10. I_{HYS_SENSEx} Current Distribution at Temperature of –55°C

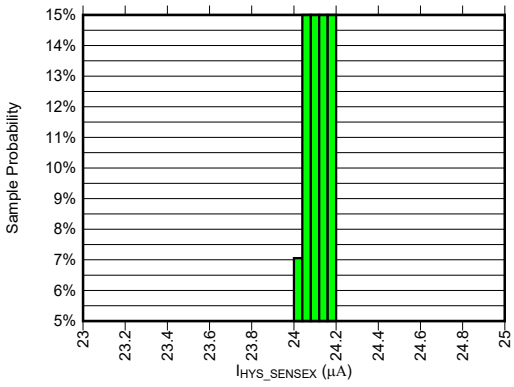


Figure 6-11. I_{HYS_SENSEx} Current Distribution at Temperature of 25°C

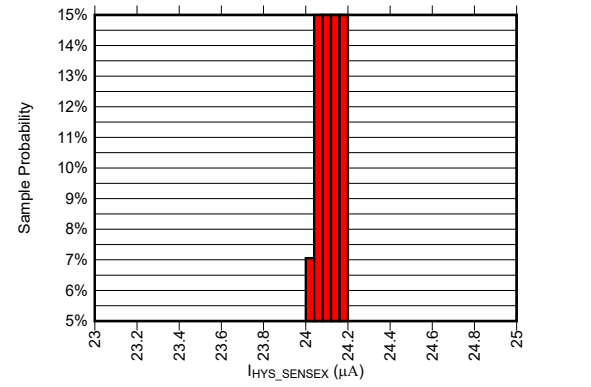
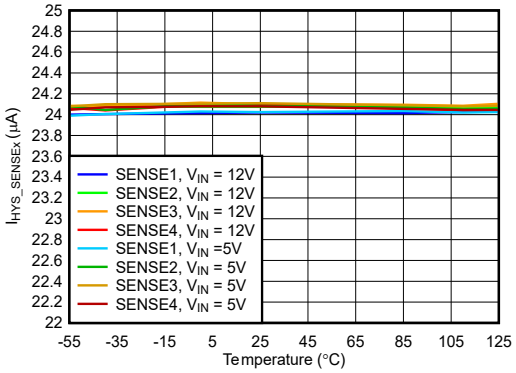


Figure 6-12. I_{HYS_SENSEx} Current Distribution at Temperature of 125°C

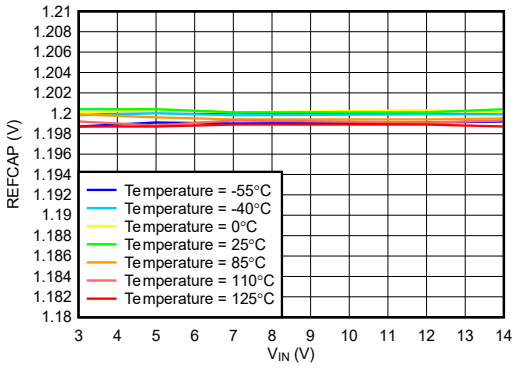
6.8 Typical Characteristics (continued)

R_{DLY_TMR} = 10.5kΩ, R_{WD_TMR} = 56.2kΩ, V_{PULL_UP1} = 3.3V, V_{PULL_UP2} = 3.3V, R_{HYS} = 49.9kΩ, MODE = Logic Low, for the TPS7H3024, unless otherwise noted.



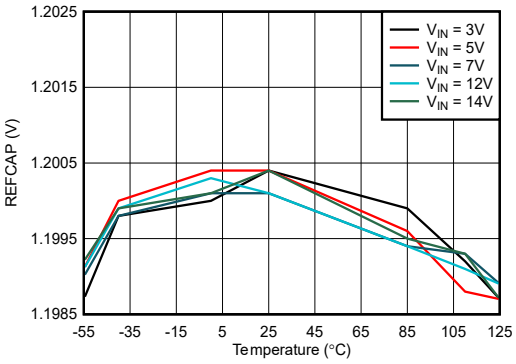
V_{SENSEx} = 700mV R_{DLY_TMR} = Floating
R_{WD_TMR} = Floating

Figure 6-13. I_{HYS_SENSEx} vs Temperature Across V_{IN} and SENSEx Channel



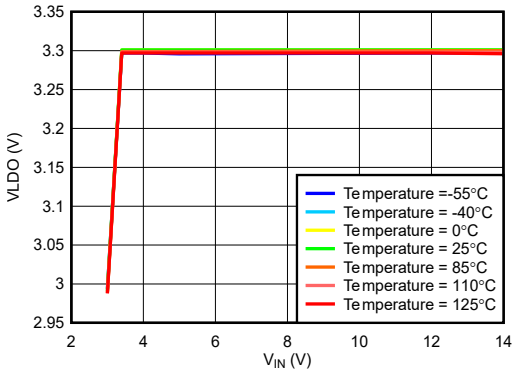
$V_{SR\_\overline{UVLO}}$ = 1V

Figure 6-14. REFCAP vs V_{IN} Across Temperature



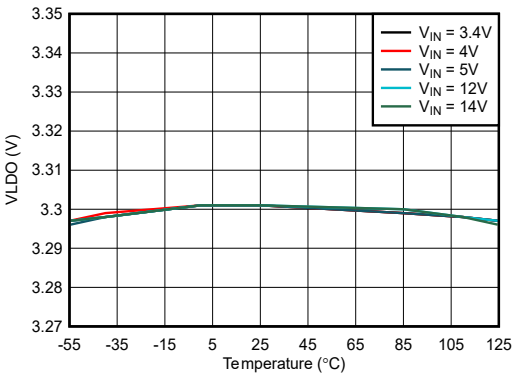
$V_{SR\_\overline{UVLO}}$ = 1V

Figure 6-15. REFCAP vs Temperature Across V_{IN}



R_{DLY_TMR} = Floating R_{WD_TMR} = Floating
MODE = Low $V_{SENSE1,3}$ = 0.3V and
$V_{SENSE2,4}$ = 1V

Figure 6-16. VLDO vs V_{IN} Across Temperature



R_{DLY_TMR} = Floating R_{WD_TMR} = Floating
MODE = Low $V_{SENSE1,3}$ = 0.3V and
$V_{SENSE2,4}$ = 1V

Figure 6-17. VLDO vs Temperature Across V_{IN}

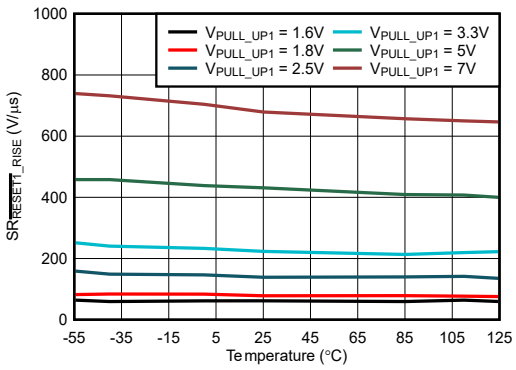


Figure 6-18. $SR_{\overline{RESET1}\_RISE}$ vs Temperature Across V_{PULL_UP1}

6.8 Typical Characteristics (continued)

R_{DLY_TMR} = 10.5kΩ, R_{WD_TMR} = 56.2kΩ, V_{PULL_UP1} = 3.3V, V_{PULL_UP2} = 3.3V, R_{HYS} = 49.9kΩ, MODE = Logic Low, for the TPS7H3024, unless otherwise noted.

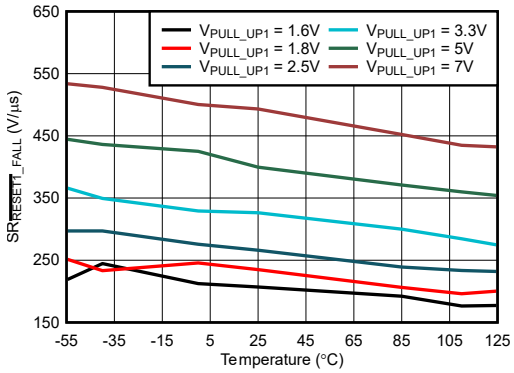


Figure 6-19. SR $\overline{\text{RESET1}}$_FALL vs Temperature Across V_{PULL_UP1}

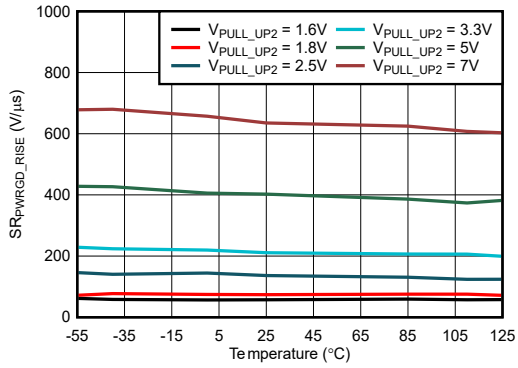


Figure 6-20. SR_{PWRGD_RISE} vs Temperature Across V_{PULL_UP2}

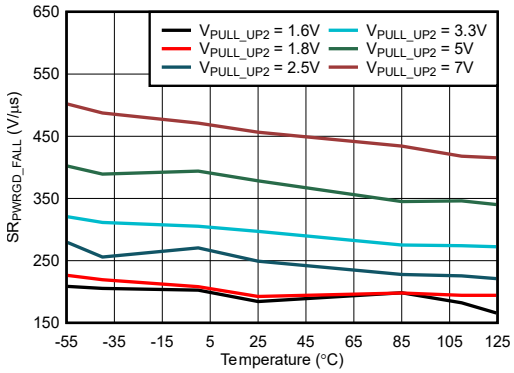


Figure 6-21. SR_{PWRGD_FALL} vs Temperature Across V_{PULL_UP2}

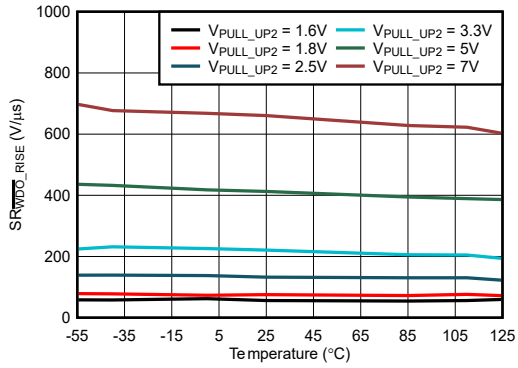


Figure 6-22. SR $\overline{\text{WDO}}$_RISE vs Temperature Across V_{PULL_UP2}

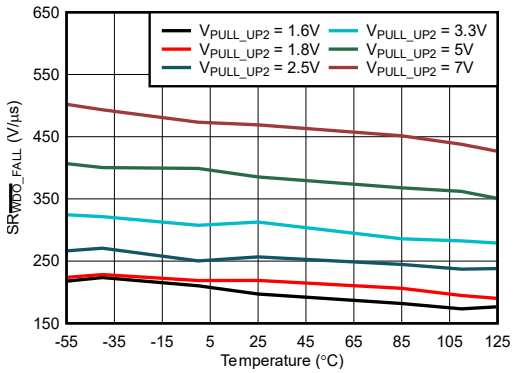


Figure 6-23. SR $\overline{\text{WDO}}$_FALL vs Temperature Across V_{PULL_UP2}

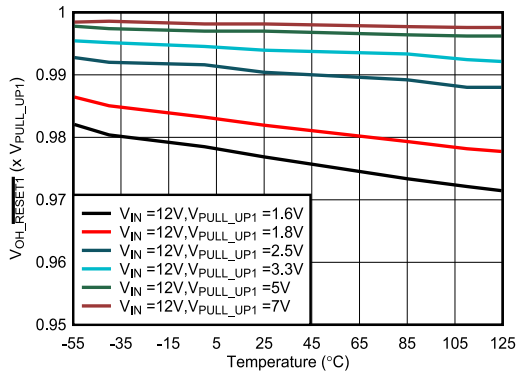


Figure 6-24. $\overline{\text{RESET1}}$ VOH Voltage as Percentage of V_{PULL_UP1} vs Temperature Across V_{PULL_UP1} at I_{LOAD} = 2mA

6.8 Typical Characteristics (continued)

R_{DLY_TMR} = 10.5kΩ, R_{WD_TMR} = 56.2kΩ, V_{PULL_UP1} = 3.3V, V_{PULL_UP2} = 3.3V, R_{HYS} = 49.9kΩ, MODE = Logic Low, for the TPS7H3024, unless otherwise noted.

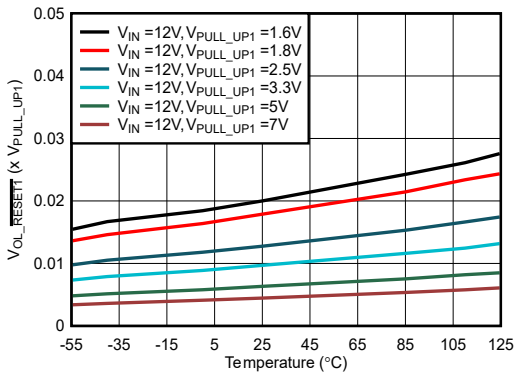


Figure 6-25. $\overline{\text{RESET1}}$ VOL Voltage as Percentage of V_{PULL_UP1} vs Temperature Across V_{PULL_UP1} at I_{LOAD} = 2mA

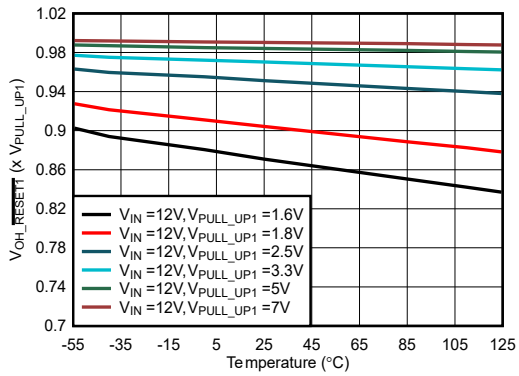


Figure 6-26. $\overline{\text{RESET1}}$ VOH Voltage as Percentage of V_{PULL_UP1} vs Temperature Across V_{PULL_UP1} at I_{LOAD} = 10mA

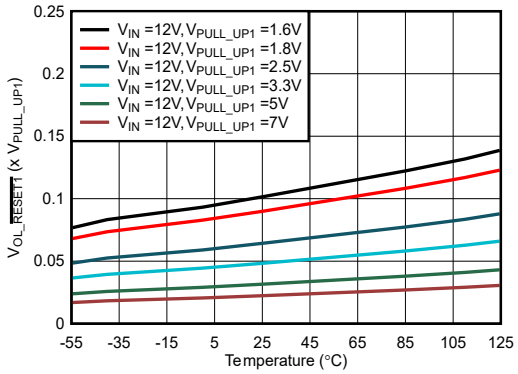


Figure 6-27. $\overline{\text{RESET1}}$ VOL Voltage as Percentage of V_{PULL_UP1} vs Temperature Across V_{PULL_UP1} at I_{LOAD} = 10mA

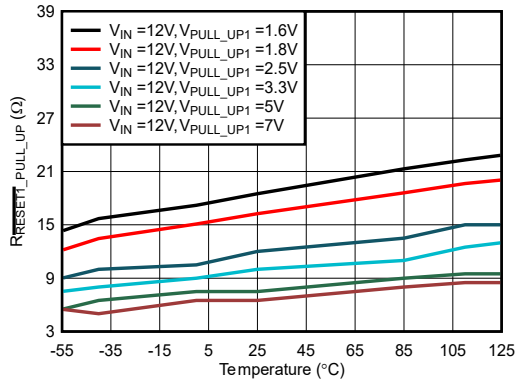


Figure 6-28. $\overline{\text{RESET1}}$ Pull-Up Resistance vs Temperature Across V_{PULL_UP1} at I_{LOAD} = 2mA

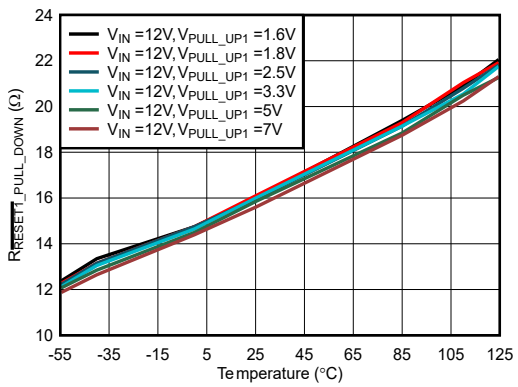


Figure 6-29. $\overline{\text{RESET1}}$ Pull-Down Resistance vs Temperature Across V_{PULL_UP1} at I_{LOAD} = 2mA

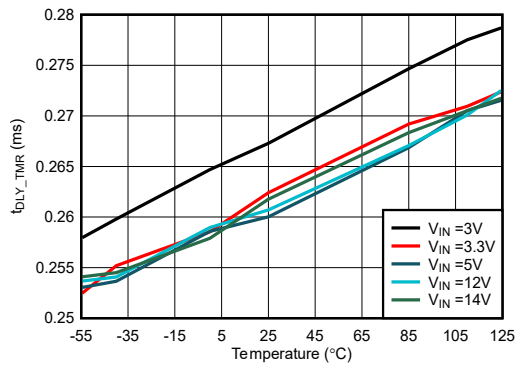


Figure 6-30. Delay Time vs Temperature Across V_{IN} with R_{DLY_TMR} = 10.5kΩ

6.8 Typical Characteristics (continued)

R_{DLY_TMR} = 10.5kΩ, R_{WD_TMR} = 56.2kΩ, V_{PULL_UP1} = 3.3V, V_{PULL_UP2} = 3.3V, R_{HYS} = 49.9kΩ, MODE = Logic Low, for the TPS7H3024, unless otherwise noted.

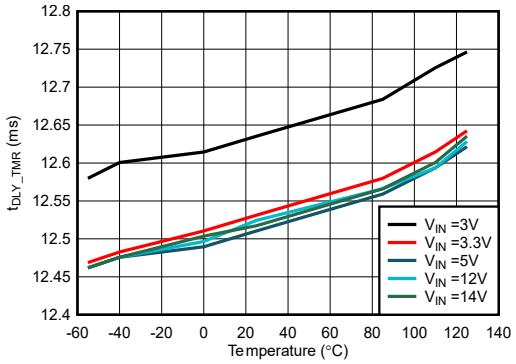


Figure 6-31. Delay Time vs Temperature Across V_{IN} with R_{DLY_TMR} = 619kΩ

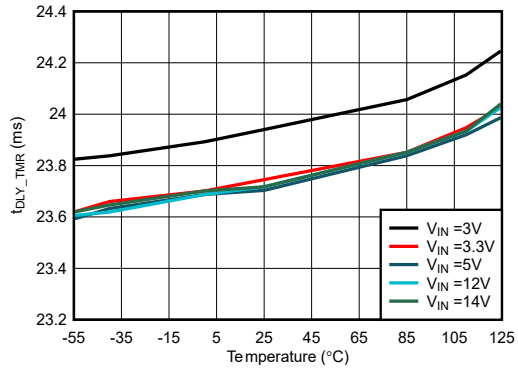
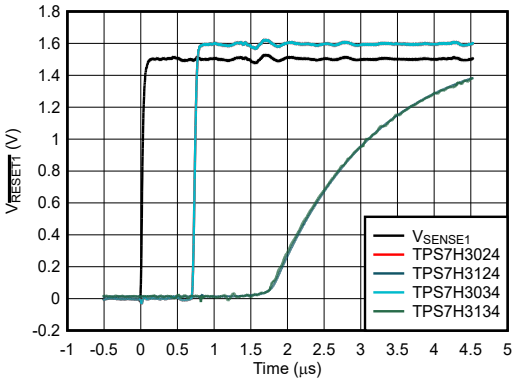


Figure 6-32. Delay Time vs Temperature Across V_{IN} with R_{DLY_TMR} = 1.18MΩ



R_{DLY_TMR} = Floating
MODE = Low

R_{WD_TMR} = Floating
V_{PULL_UPx} = 1.6V

Figure 6-33. Time Domain SENSE1 to RESET1 Propagation Delay for TPS7H3xx4

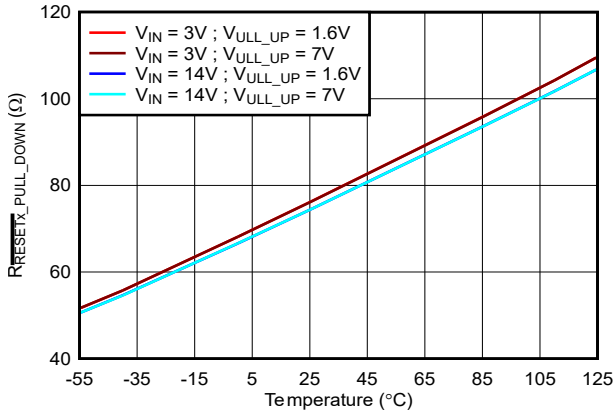


Figure 6-34. $\overline{\text{RESET1}}$ Pull-Down Resistance vs Temperature Across V_{PULL_UP} and V_{IN} at I_{LOAD} = 2mA for the TPS7H3124

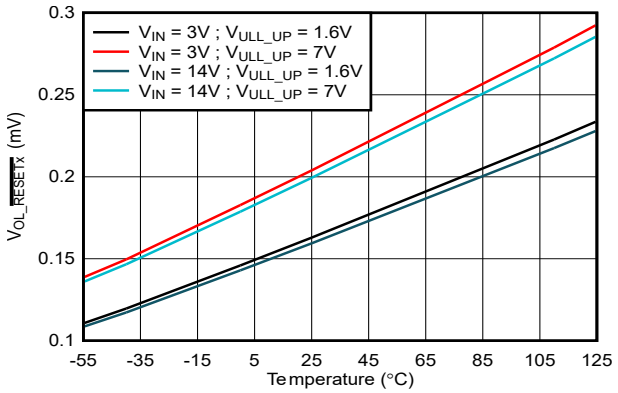


Figure 6-35. $\overline{\text{RESET1}}$ VOL Voltage vs Temperature Across V_{PULL_UP} and V_{IN} at I_{LOAD} = 2mA for the TPS7H3124

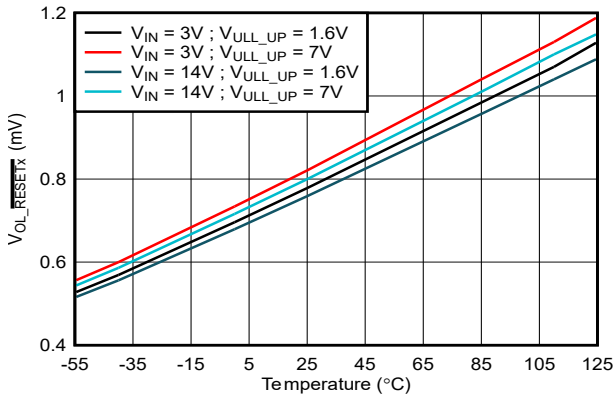
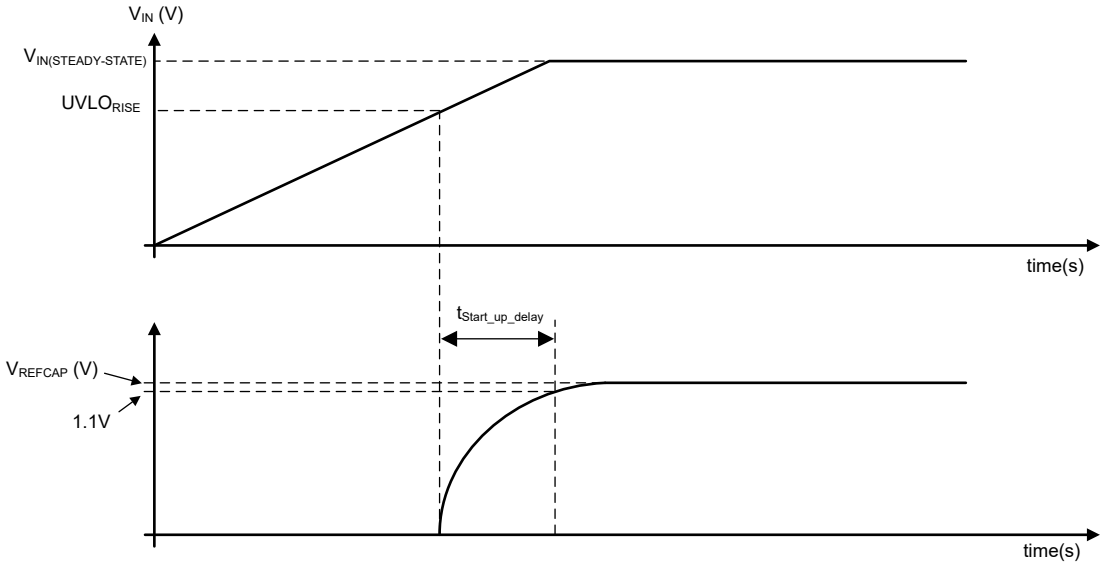


Figure 6-36. $\overline{\text{RESET1}}$ VOL Voltage vs Temperature Across V_{PULL_UP} and V_{IN} at I_{LOAD} = 10mA for the TPS7H3124

7 Parameter Measurement Information

With MODE=0, for all measurements referenced to the PWRGD voltage, the SENSEx voltage is forced in a non-fault state, unless otherwise specified.



A. $V_{IN(STEADY-STATE)}$ is a valid operating voltage from 3V to 14V

Figure 7-1. $t_{Start\_up\_delay}$ Time Measurement

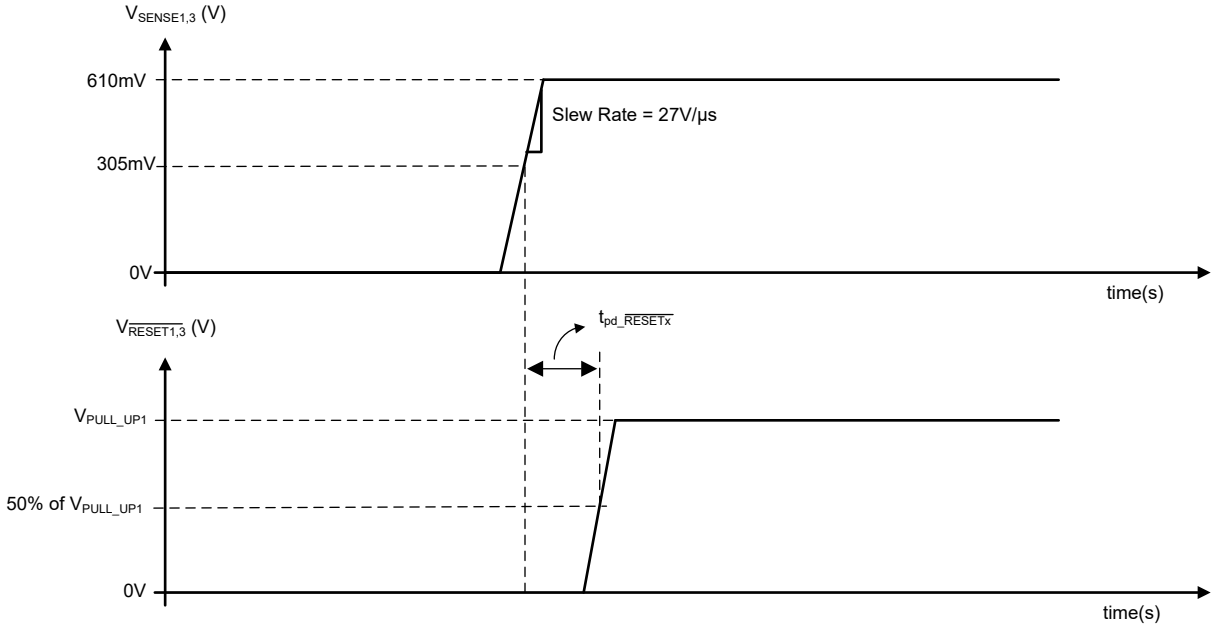
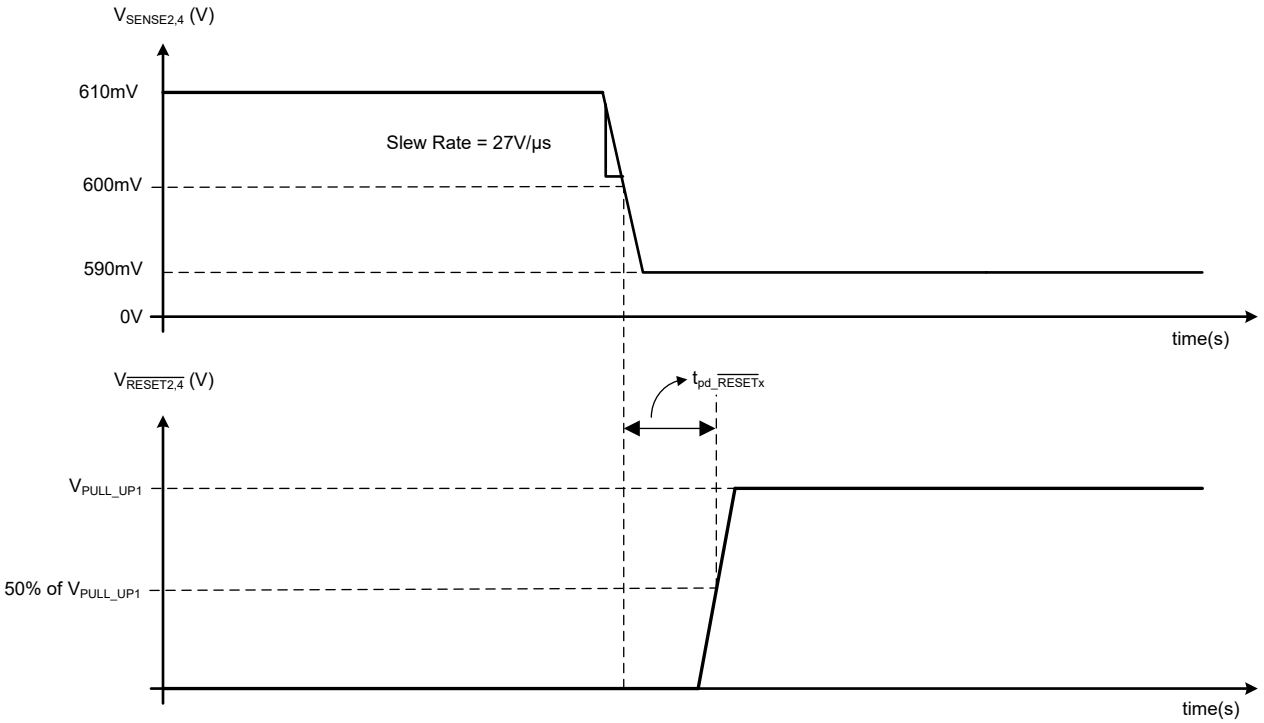
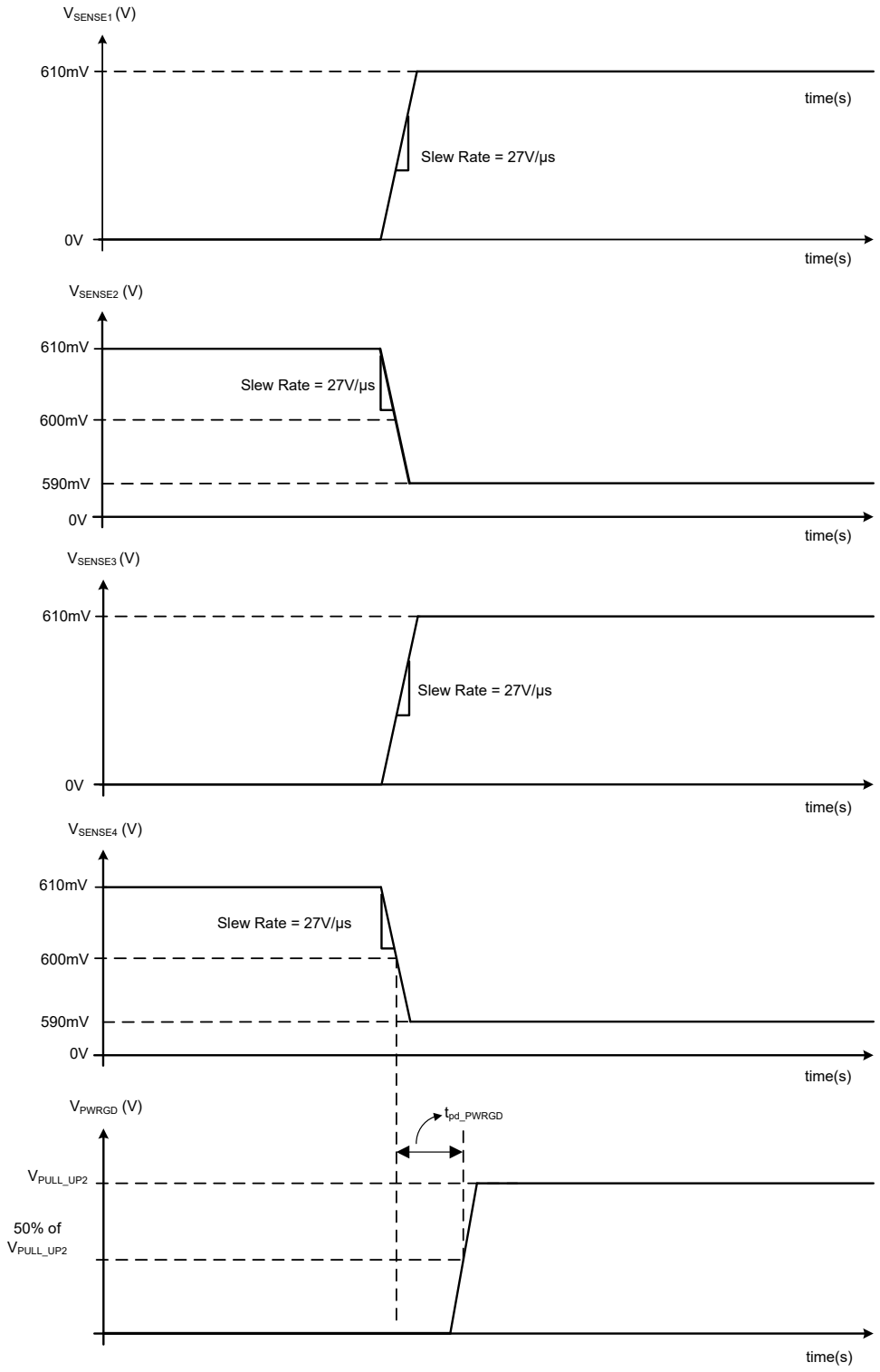


Figure 7-2. $\overline{RESET1}$ and $\overline{RESET3}$ Propagation Delay ($t_{pd\_\overline{RESETx}}$) Time Measurement for TPS7H30x4 (Push-Pull)



A. For $t_{pd\_\overline{RESETx}}$, each SENSEx propagation delay is measured independently.

Figure 7-3. $\overline{RESET2}$and $\overline{RESET4}$ Propagation Delay ($t_{pd\_\overline{RESETx}}$) Time Measurement for TPS7H30x4 (Push-Pull)



A. In the TPS7H3034 with MODE=0, all V_{SENSEx} are ramped up as per $V_{SENSE1,3}$ in this diagram.

Figure 7-4. PWRGD Propagation Delay (t_{pd_PWRGD}) for TPS7H3024 (Push-Pull)

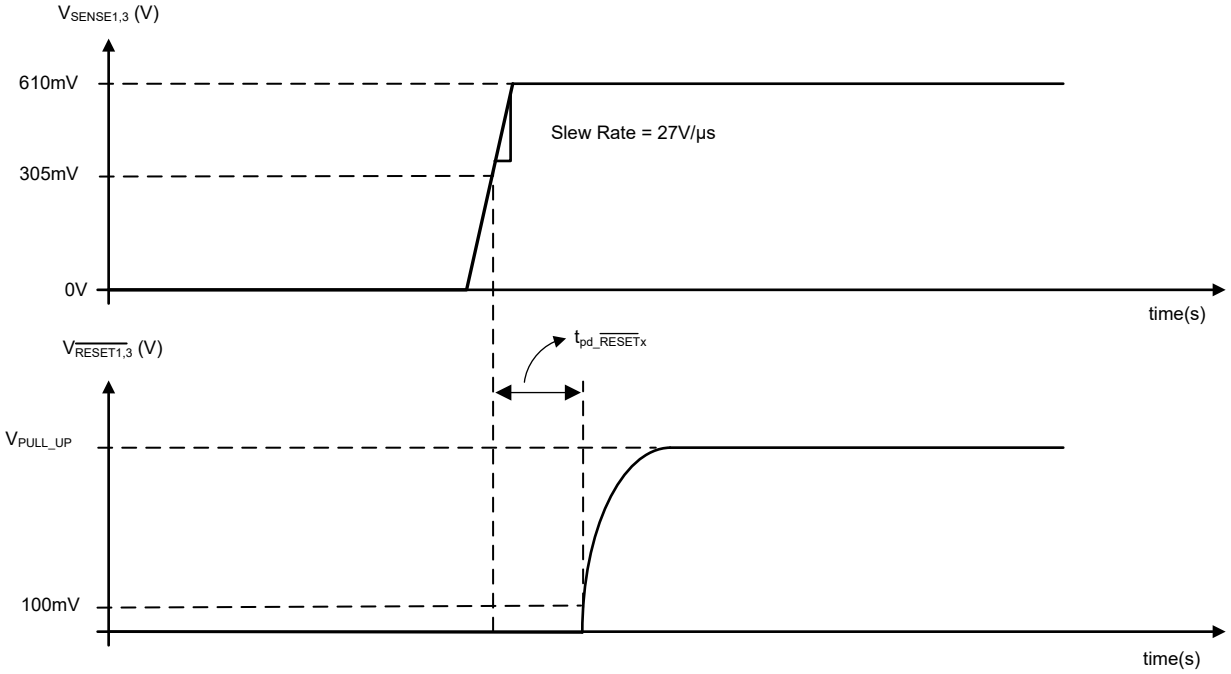


Figure 7-5. $\overline{\text{RESET1}}$ and $\overline{\text{RESET3}}$ Propagation Delay ($t_{pd\_\overline{RESETx}}$) Time Measurement for TPS7H31x4 (Open-Drain)

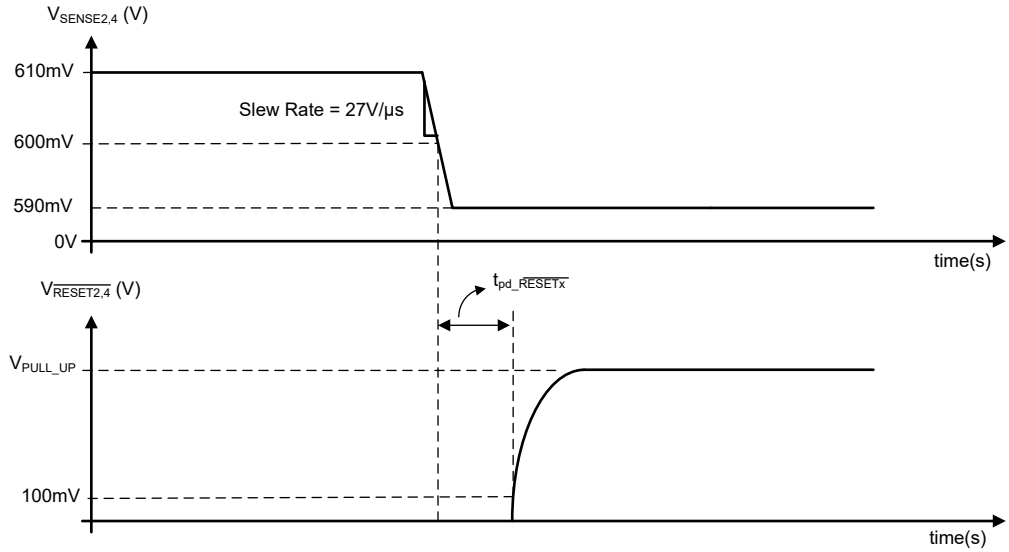
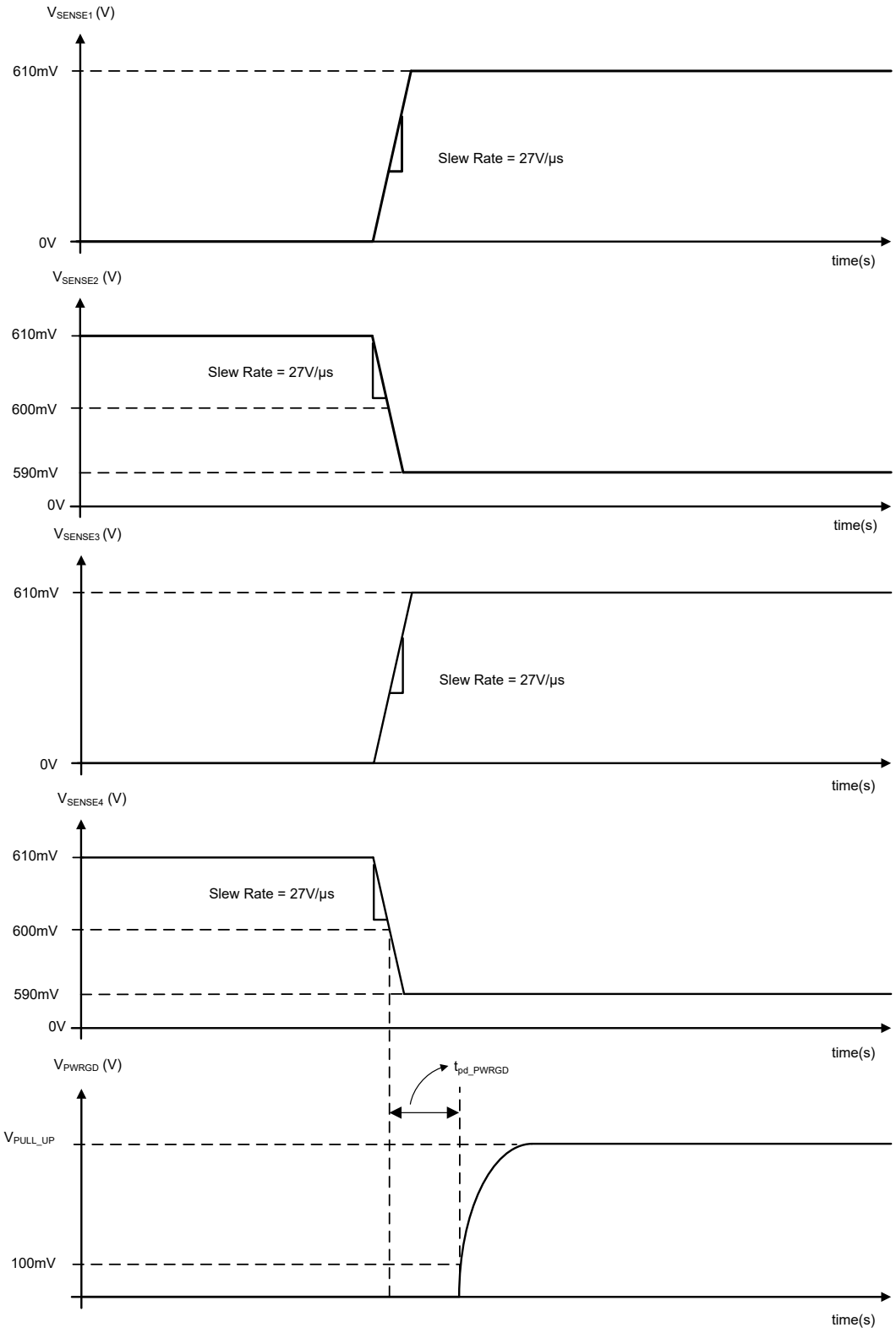


Figure 7-6. $\overline{\text{RESET2}}$ and $\overline{\text{RESET4}}$ Propagation Delay ($t_{pd\_\overline{RESETx}}$) Time Measurement for TPS7H31x4 (Open-Drain)



A. In the TPS7H3134 with MODE=0, all V_{SENSEx} are ramped up as per $V_{SENSE1,3}$ in this diagram.

Figure 7-7. PWRGD Propagation Delay (t_{pd_PWRGD}) for TPS7H3124 (Open-Drain)

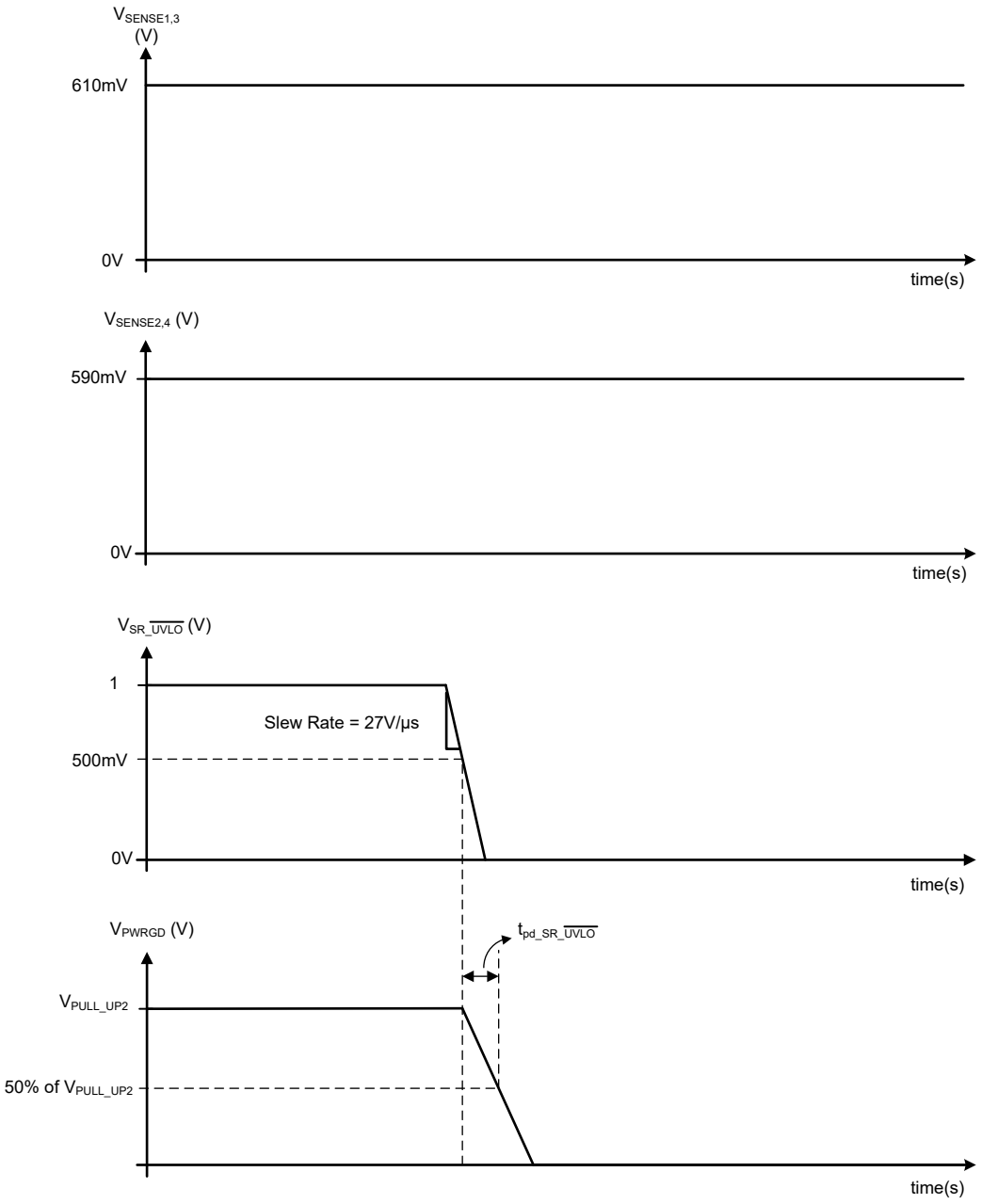
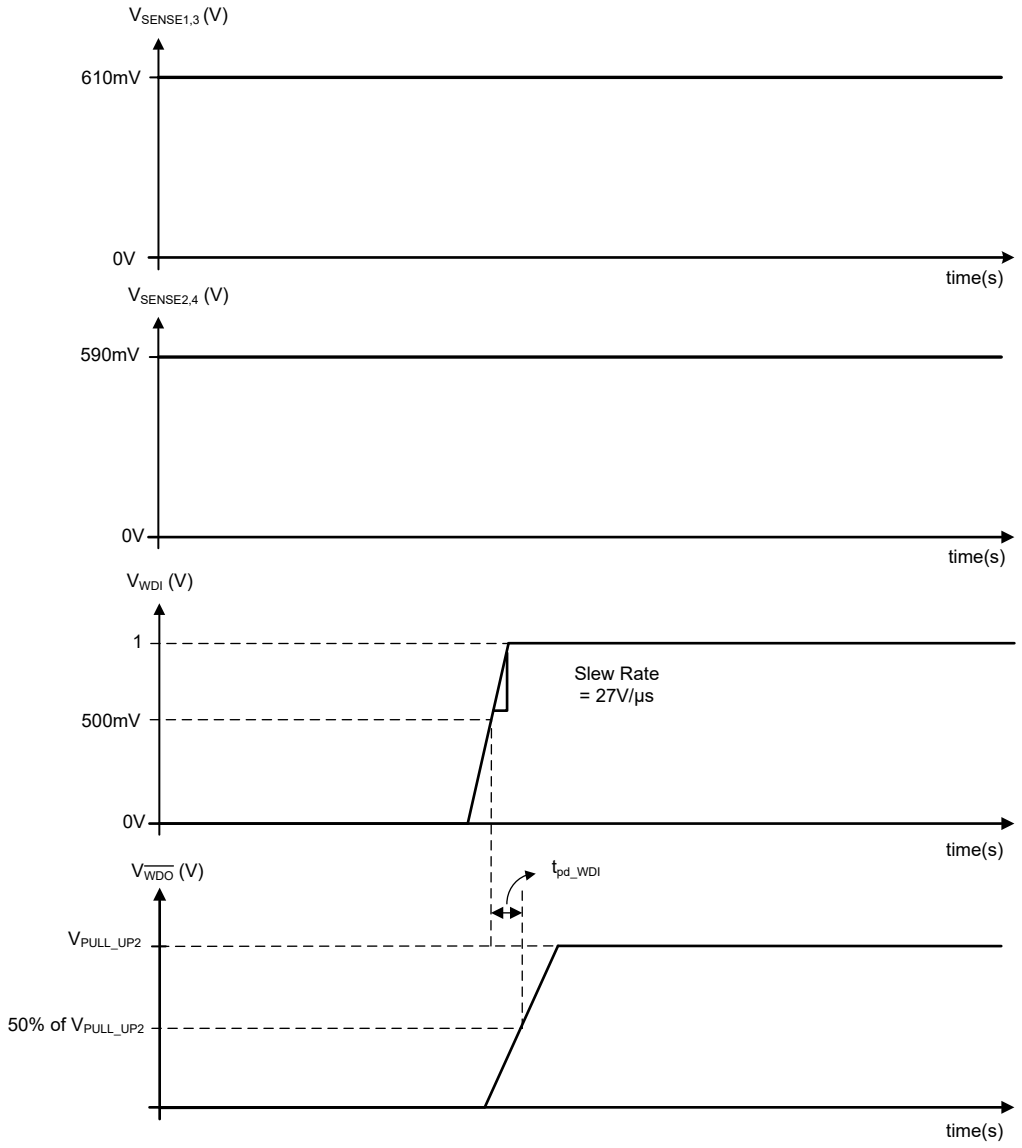
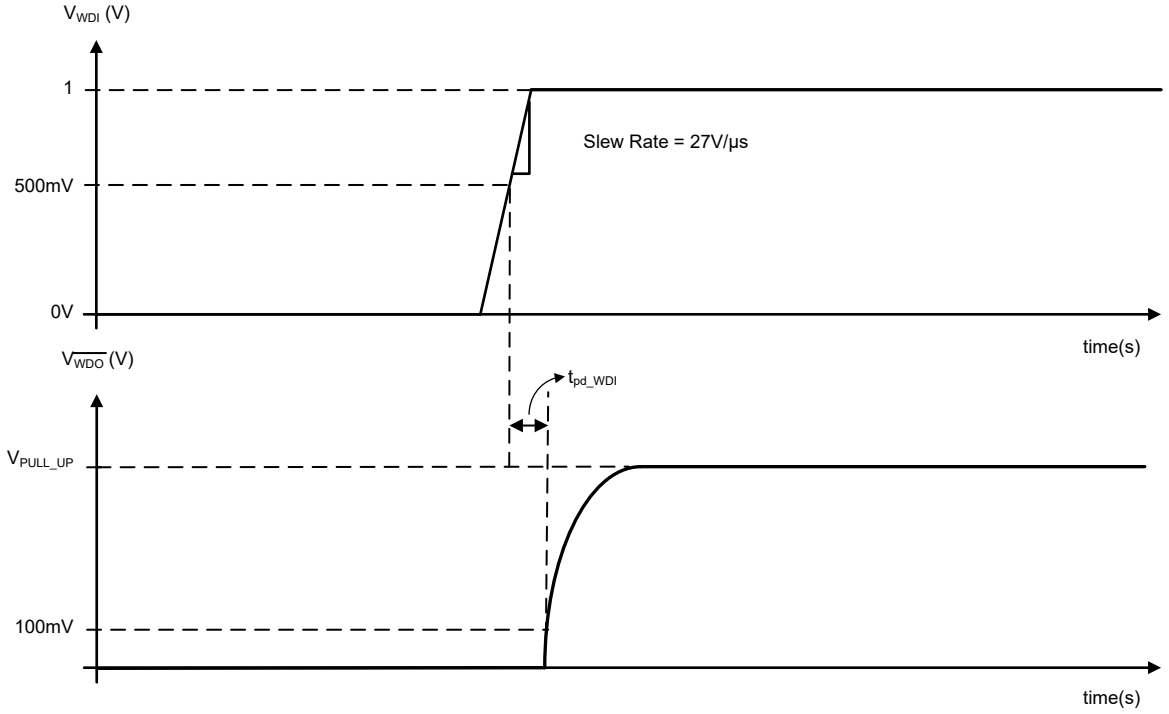


Figure 7-8. SR_$\overline{\text{UVLO}}$ Propagation Delay ($t_{pd\_SR\_\overline{UVLO}}$)



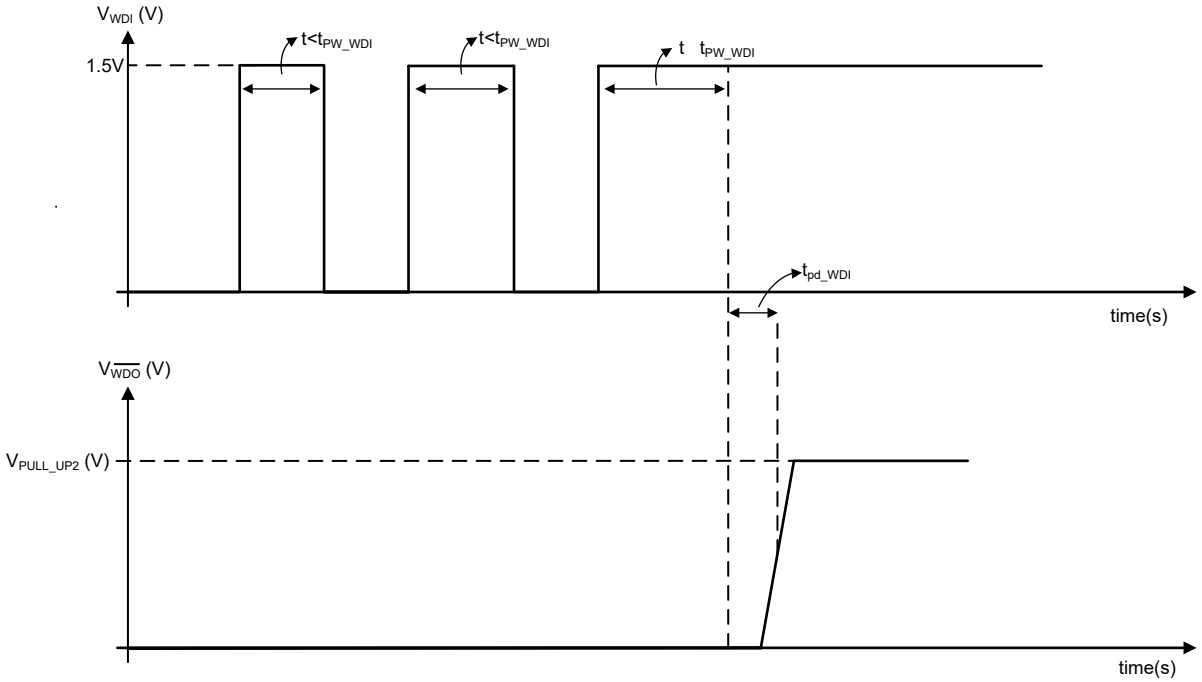
A. With MODE=0 for TPS7H3024. In the TPS7H3034 with MODE=0, all V_{SENSEx} are forced high as per $V_{SENSE1,3}$ in this diagram.

Figure 7-9. WDI Propagation Delay (t_{pd_WDI}) for TPS7H3024 (Push-Pull)



A. In the TPS7H31x4 (open-drain) the WDO is not masked with PWRGD.

Figure 7-10. WDI Propagation Delay (t_{pd_WDI}) for TPS7H31x4 (Open-Drain)



A. With $V_{SENSE1,3}$ = 1.5V; $V_{SENSE2,4}$ = 0V for the TPS7H30x4 (push-pull). In the TPS7H31x4, WDO is not masked by PWRDG.

Figure 7-11. WDI Pulse Width (t_{PW_WDI})

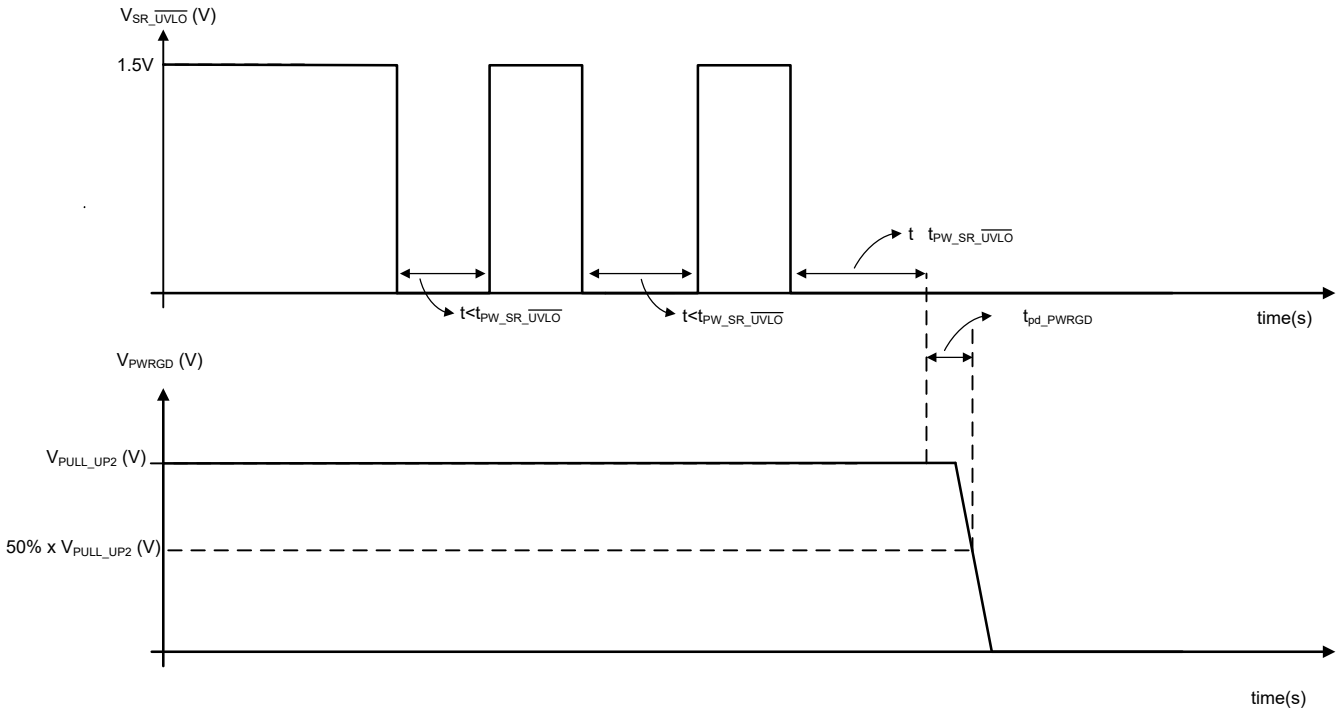
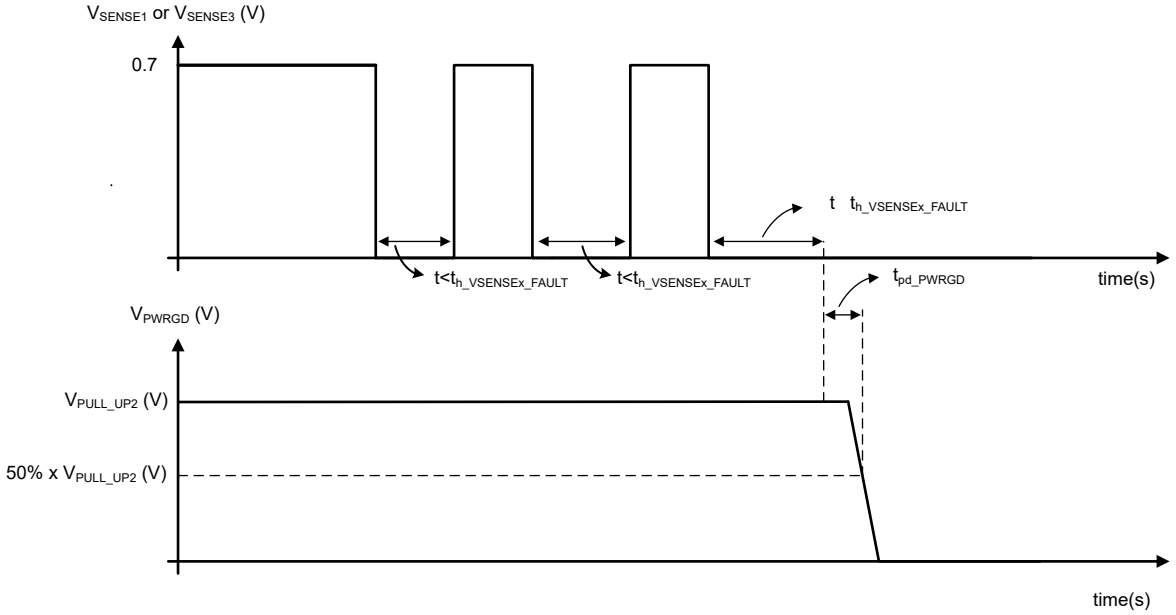
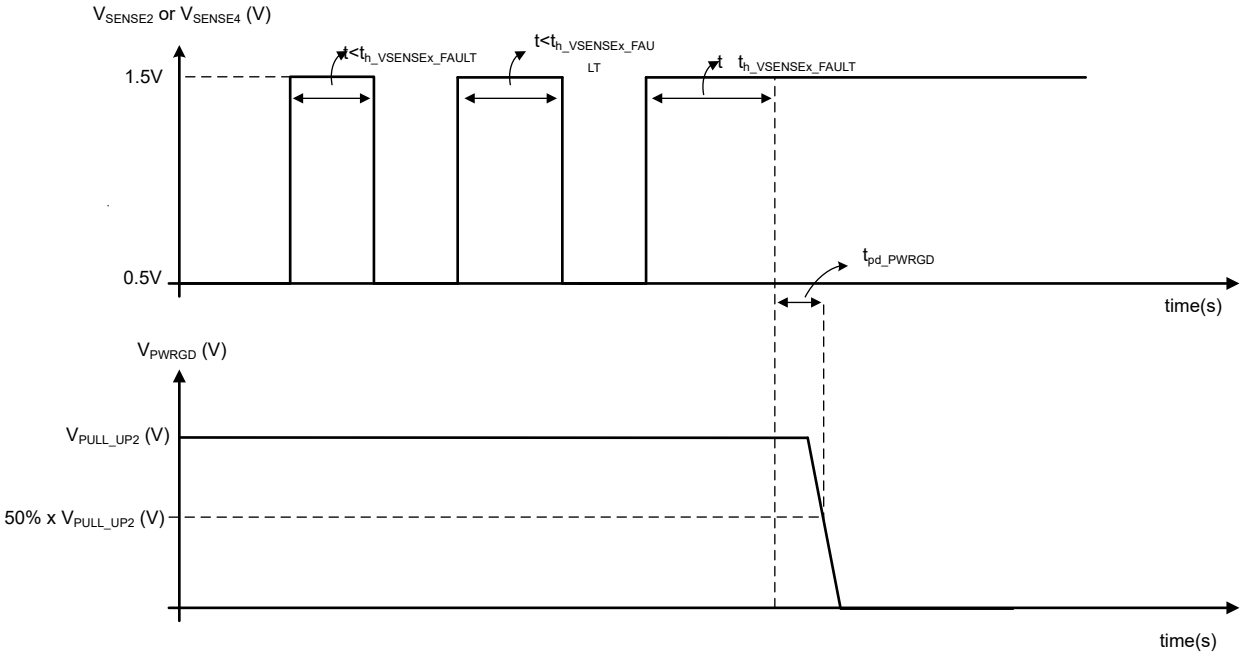


Figure 7-12. SR_$\overline{UVLO}$ Pulse Width ($t_{PW\_SR\_\overline{UVLO}}$)



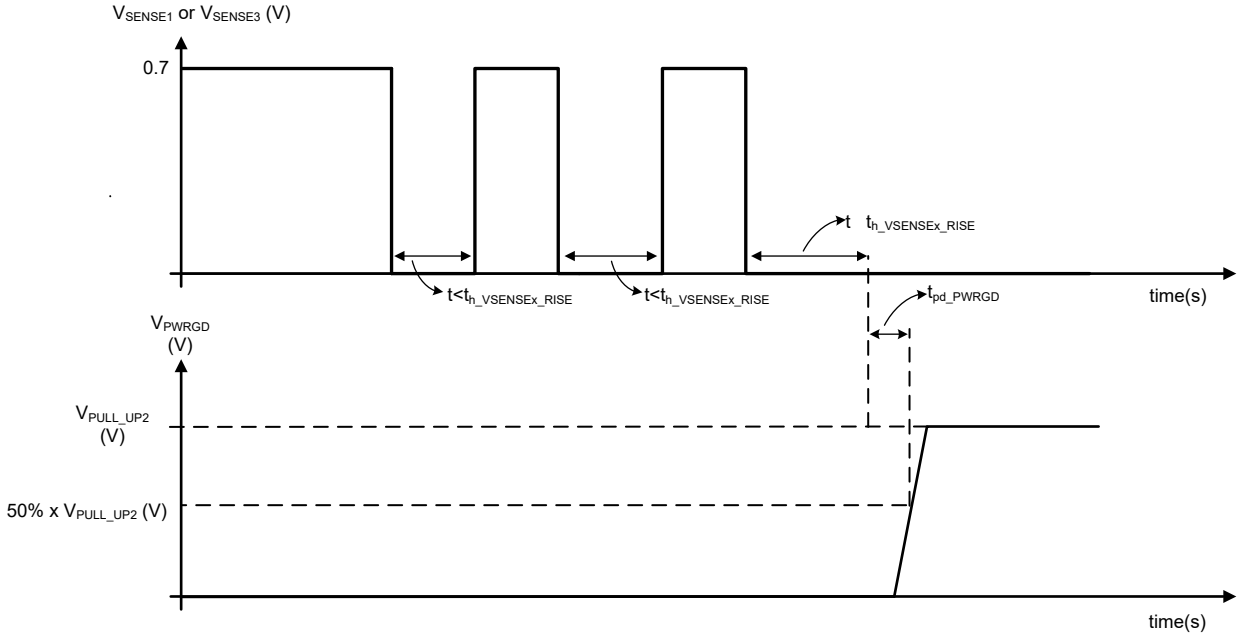
A. For $t_{h\_VSENSEx\_FAULT}$ each SENSEx is measured independently.

Figure 7-13. VSENSE1 and VSENSE3 Hold Time for Valid Fault Detection ($t_{h\_VSENSEx\_FAULT}$)



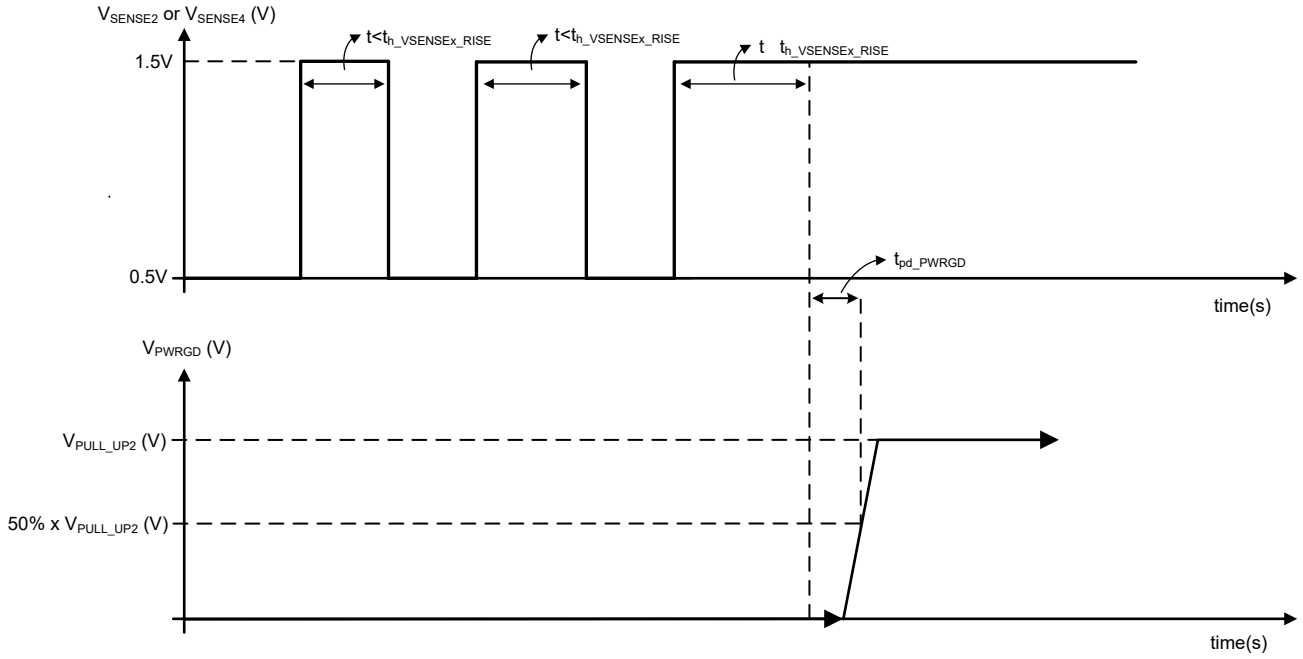
A. For $t_{h\_VSENSEx\_FAULT}$ each SENSEx is measured independently.

Figure 7-14. VSENSE2 and VSENSE4 Hold Time for Valid Fault Detection ($t_{h\_VSENSEx\_FAULT}$)



A. For $t_{h\_VSENSEx\_FAULT}$ each SENSEx is measured independently.

Figure 7-15. VSENSE1 and VSENSE3 Rising Threshold Hold Time ($t_{h\_VENSEx\_RISE}$)



A. For $t_{h\_VSENSEx\_FAULT}$ each SENSEx is measured independently.

Figure 7-16. VSENSE2 and VSENSE4 Rising Threshold Hold Time ($t_{h\_VENSEx\_RISE}$)

8 Detailed Description

8.1 Overview

The TPS7H3xx4 are four-channel, 3V to 14V, voltage supervisors with an integrated watchdog timer for space applications. The active low $\overline{\text{RESETx}}$ outputs readily supports monitoring of devices with disable low inputs. Table 8-1 describe the monitoring capabilities (undervoltage, overvoltage or window) and output types (push-pull or open-drain) for the offered GPNs. The behavior of the front-end is controlled by the logical value of the MODE pin.

Table 8-1. TPS7H3xx4 Functional Modes

GPN	Output Topology	Function	Mode(1) (2) (3)
TPS7H3024	Push-pull	2 UV + 2 OV	0
		2 window	1
TPS7H3124	Open-drain	2 UV + 2 OV	0
		2 window	1
TPS7H3034	Push-pull	4 UV	0
		4 OV	1
TPS7H3134	Open-drain	4 UV	0
		4 OV	1

(1) Mode is an static input, the user most not change the logical value dynamically. Once the device is power-up, the value most not change.
(2) 0 = V_{MODE} < $V_{TH\_MODE\_FALLING(min)}$
(3) 1 = V_{MODE} > $V_{TH\_MODE\_RISING(max)}$

The logic high for the $\overline{\text{RESETx}}$, PWRGD, and $\overline{\text{WDO}}$ is externally controlled using the PULL_UPx input voltage supply. Users are required to connect at least a 1µF capacitor as close to the PULL_UPx pins as possible. The logic high of all the $\overline{\text{RESETx}}$ outputs is programmed via the PULL_UP1 input, while the PWRGD and $\overline{\text{WDO}}$ is programmed via PULL_UP2. The voltage range of the PULL_UPx inputs is from 1.6V to 7V.

For open-drain outputs, the user must pull up the output through a resistor (typically 10kΩ) to the required logic voltage. The maximum pull-up voltage is 7V.

The SENSEx inputs are connected to the non-inverting input of a comparator which is used to classify the monitored voltages as:

1. In regulation.
2. Not in regulation.

For more details on the behavior of the undervoltage and overvoltage comparators refer to Section 8.3.3.3. Each of these inputs feature a threshold level of 599.7mV (typical) with an accuracy of ±1% across voltage, temperature, and radiation (TID). The hysteresis voltage threshold level can be adjusted by the user and determined by the R_{TOPx} resistance and the hysteresis current (I_{HYS_SENSEx}). The I_{HYS_SENSEx} becomes active once the rising voltage at SENSEx exceeds the V_{TH_SENSEx} threshold (typically 599.7mV). I_{HYS} is 24µA with an accuracy of ±3% across voltage, temperature, and radiation (TID). In addition the device offers an output called PWRGD to monitor the status of the power tree (complete system).

Note

For the overvoltage comparators, the $\overline{\text{RESETx}}$ output is logically inverted from the front-end comparator output. Refer to Figure 8-16 and Figure 8-18 for details.

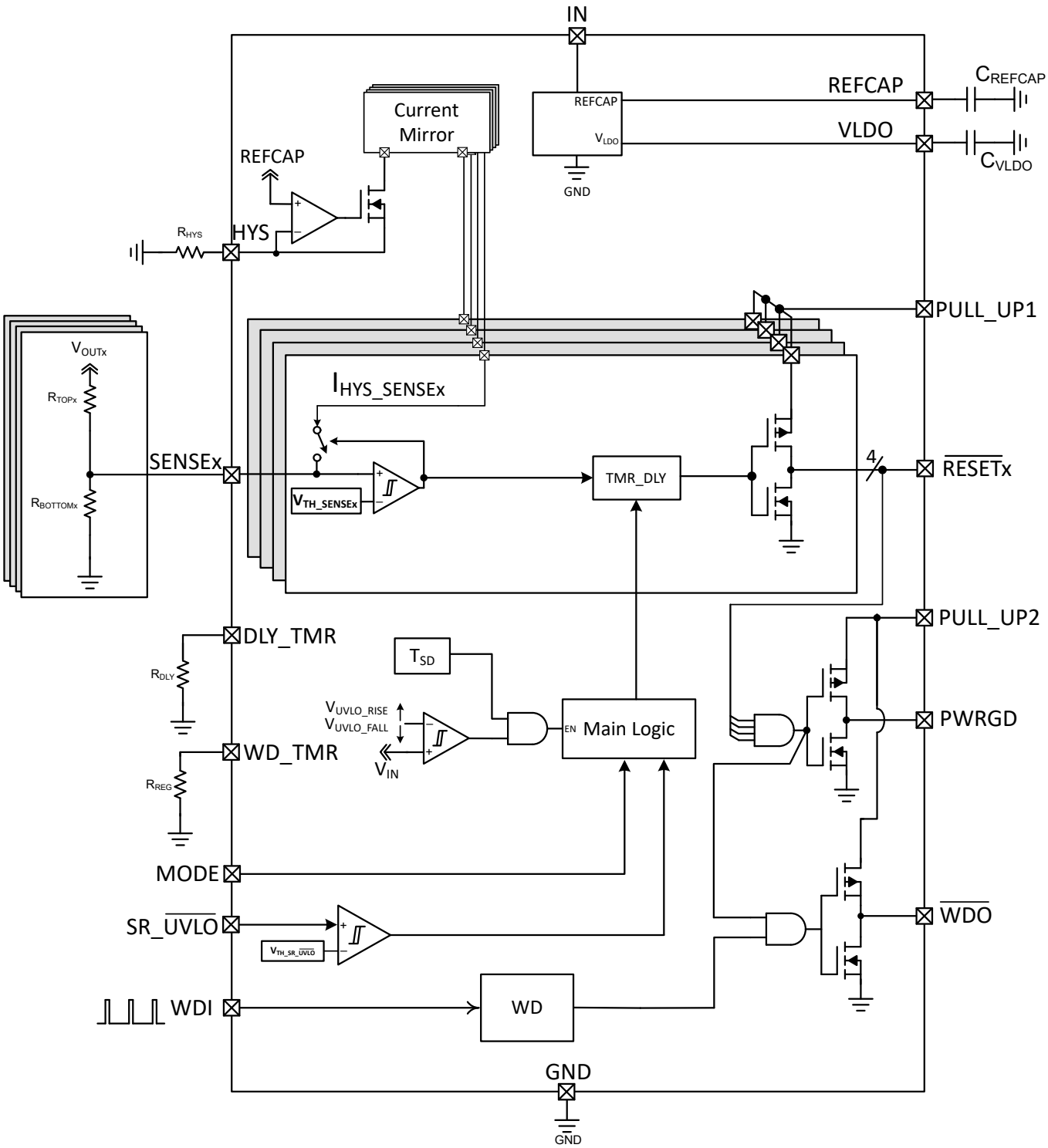
In addition to the voltage supervision, the TPS7H3xx4 incorporates a rising-edge watchdog timer. The watchdog input (WDI) detects rising-edge voltage changes. When the watchdog timer logic detects a rising voltage on the WDI pin, the timer is cleared if the watchdog timer is already active, or starts counting if the pulse is the first detected pulse. With the detection of a rising pulse on the WDI pin, the system has until the programmed time-out (0.5ms to 1.5ms nominally) to clear the timer again. If the timer is cleared before the time-out, the

watchdog output ($\overline{WDO}$) remains high, otherwise WDO is asserted low. Usually the watchdog timer is used to monitor coherent processor execution. Typically a processor induces a rising-edge voltage on the WDI using an output channel and the $\overline{WDO}$ is connected to a non-maskable interrupt. If the processor is stuck, the WDI pin is not toggled, and, consequently the $\overline{WDO}$ goes low to reset the processor to a known state.

The device incorporates two programmable timers:

1. **DLY_TMR**: Sets the out-of-fault delay. Once the monitored voltage changes state, from not in regulation to in regulation, the $\overline{RESET}$x is asserted high once the delay programmed by the user (using the DLY_TMR) is expired. This timer can be programmed from 0.25ms to 25ms, by using a 10.5kΩ to a 1.18MΩ resistor, respectively. This delay is not valid when the input ("monitored voltage") changes state from in regulation to not in regulation to propagate the fault as soon as possible.
2. **WD_TMR**: Sets the time-out for the watchdog timer. When the watchdog input detects a rising voltage on the input (WDI), the monitored process has until the programmed time-out to provide another rising voltage for the output ($\overline{WDO}$) to stay high, otherwise the output goes low.

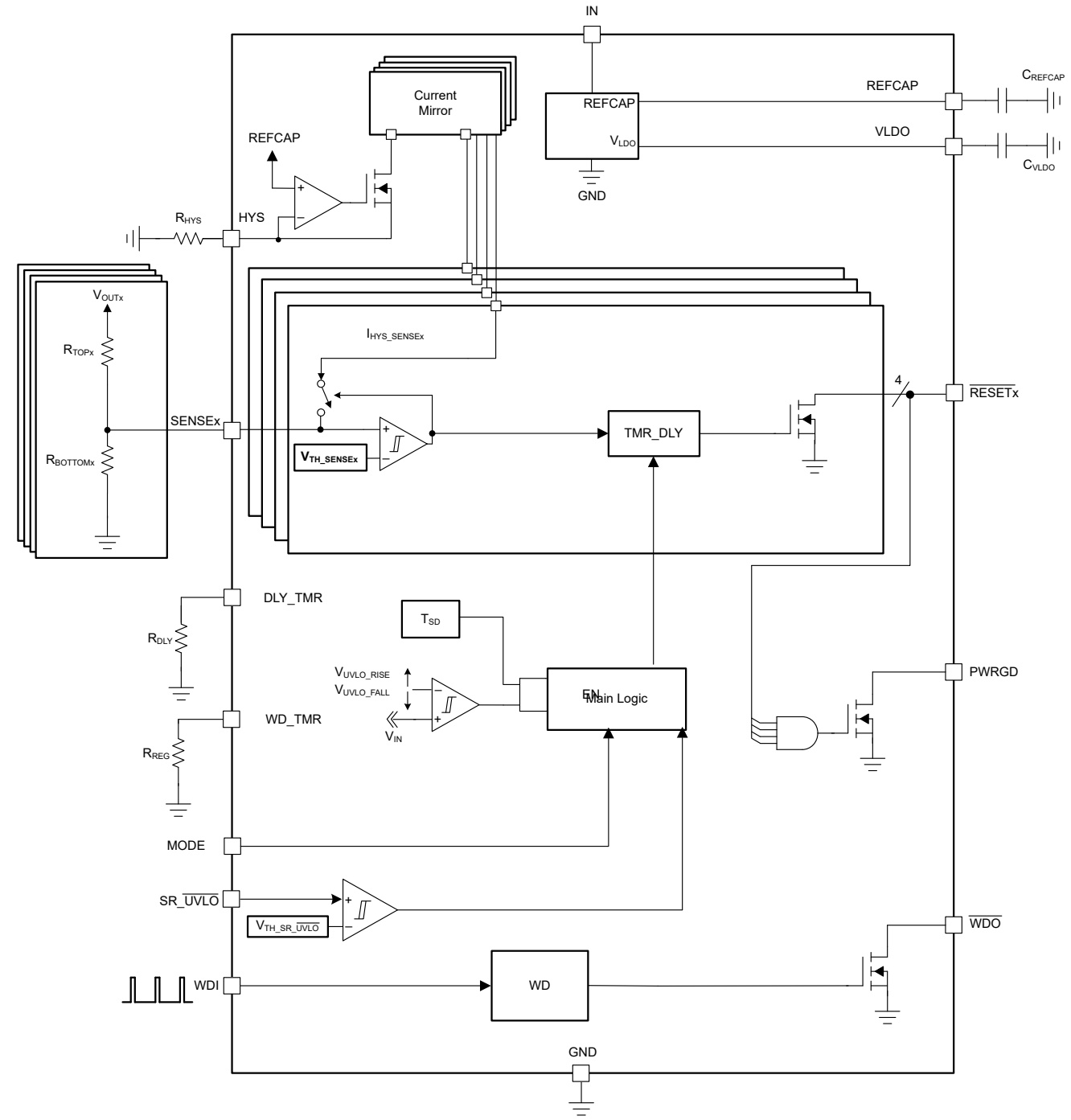
8.2 Functional Block Diagram



A. In the TPS7H3024, the RESET2 and RESET4 output stages are driven logically inverted from the output of the input comparator to detect overvoltage events. This behavior also applies to the TPS7H3034 when MODE=1. For more details refer to Figure 8-16

B. In the TPS7H3024, when MODE=1, the RESET1 and RESET3 outputs are of the window comparator type. For more details refer to Figure 8-11. RESET2 and RESET4 are the overvoltage comparator flags.

Figure 8-1. Block Diagram for the TPS7H30x4 (Push-Pull Outputs)



A. In the TPS7H3124, the RESET2 and RESET4 output stages are driven logically inverted from the output of the input comparator to detect overvoltage events. This behavior also applies to the TPS7H3134 when MODE=1. For more details refer to Figure 8-18

B. In the TPS7H3024, when MODE=1, the RESET1 and RESET3 outputs are of the window comparator type. For more details refer to Figure 8-12. RESET2 and RESET4 are the overvoltage comparator flags.

Figure 8-2. Block Diagram for the TPS7H31x4 (Open-Drain Outputs)

8.3 Feature Description

8.3.1 Input Voltage (IN), VLDO, and REFCAP

During steady state operation, the input voltage of the TPS7H3024 must be from 3V to 14V. A minimum bypass capacitance of 0.1µF is required between V_{IN} and GND. The input bypass capacitors is recommended to be placed as close to the device as possible. The V_{IN} slew rate must be controlled between 10V/µs to 1mV/µs for proper IC operation.

The voltage applied at V_{IN} serves as the input for the internal regulator that generates the VLDO voltage, typically 3.29V. At input voltages less than 3.65, the VLDO regulator can be on dropout. The recommended capacitance for VLDO is 1µF of ceramic type. The VLDO can be loaded up to a maximum of 5mA.

Note

The VLDO output is not protected against short circuit conditions.

During power up, the user is recommended to wait at least 2.8ms ($t_{Start\_up\_delay}$) after V_{IN} > $UVLO_{RISE}$. This is to make sure all internal time constants are surpassed, otherwise the reference can be out of the ± 1% accuracy.

Each device generates an internal 1.2V bandgap reference that is used throughout the various internal control logic blocks. This is the voltage present on the REFCAP pin during steady state operation. This voltage is divided down to produce the reference for the comparator inputs at:

1. SENSEx = 599.7mV (typical)
2. SR_$\overline{UVLO}$ = 602mV (typical) during a rising voltage and 489mV during a falling voltage.
3. WDI = 602mV (typical) during a rising voltage and 498mV during a falling voltage.
4. MODE = 600mV (typical)during a rising voltage and 498mV during a falling voltage.

The V_{TH_SENSEx} reference is measured at the $\overline{RESETx}$ outputs to account for offsets in the error amplifier and maintain regulation within ±1% across voltage, temperature, and radiation TID (up to 100krad in silicon). This tight reference tolerance allows the user to monitor voltage rails with high accuracy.

A 470nF capacitor to GND is required at the REFCAP pin for proper electrical operation as well as to provide robust SET performance of the device.

8.3.1.1 Undervoltage Lockout (V_{POR_IN} < V_{IN} < UVLO)

When the voltage on V_{IN} is less than the UVLO (2.79V typical) voltage, but greater than the power-on reset voltage (V_{POR_IN}, 1.42V typical), the output pins ($\overline{RESETx}$, PWRGD and $\overline{WDO}$) are in a logic low state, regardless of the voltage at the following device input pins:

- SENSEx
- SR_$\overline{UVLO}$
- WDI
- MODE

8.3.1.2 Power-On Reset (V_{IN} < V_{POR_IN})

When the voltage on V_{IN} is lower than the power on reset voltage (V_{POR_IN}), the output signal is undefined and is not to be relied for setting external deices to the correct logic level.

Figure 8-3 shows the $\overline{RESETx}$ outputs relationship to a rising input voltage (V_{IN}). As can be observed, the $\overline{RESETx}$ are undefined when V_{IN} is lower than V_{POR_IN} (typically 1.42V). During this time the outputs can be any value from 0V to V_{IN}.

In this example, the input voltages to all input comparators (SENSEx) are below the V_{TH_SENSEx} (typically 599.7mV). For this reason the $\overline{RESETx}$, PWRGD and $\overline{WDO}$ stays low after V_{IN} rises above $UVLO_{RISE}$ (typically 2.79V).

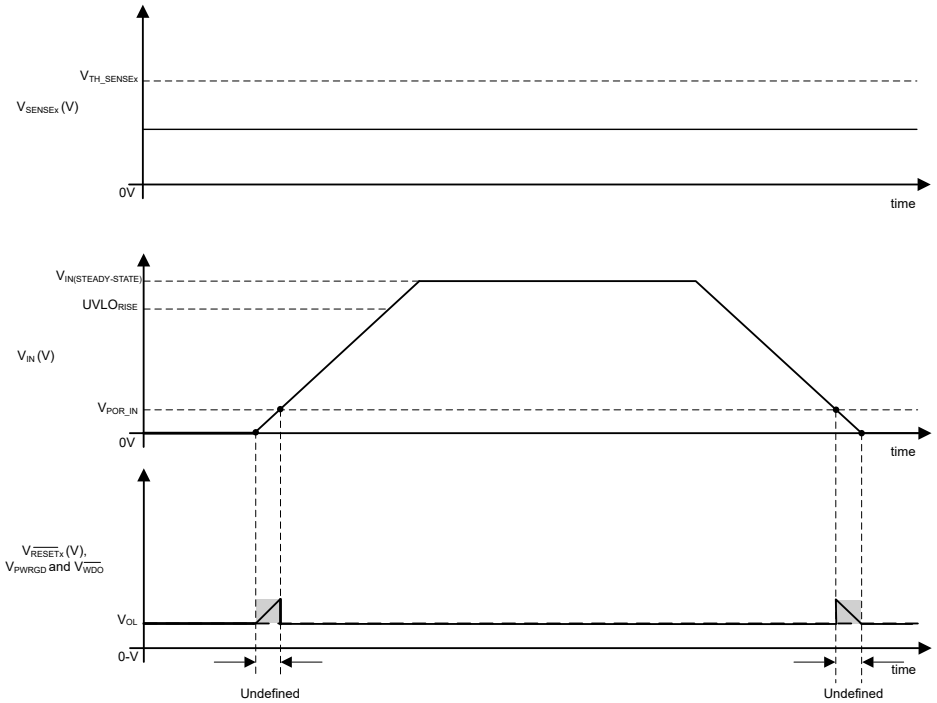


Figure 8-3. Outputs in a Valid Low State After V_{IN} > V_{POR_IN}

A. This figures assumes:
1. A valid external pull-up voltage is connected to the PULL_UPx inputs (1.6V ≤ V_{PULL_UPx} ≤ 7V).
2. $V_{IN(STEADY-SATE)}$ is a valid V_{IN} voltage from 3V to 14V.
3. All inputs are assumed to be of undervoltage (UV) type for this graph.
4. V_{OL} represents: $V_{OL\_\overline{RESETx}}$, V_{OL_PWRGD} and $V_{OL\_\overline{WDO}}$ or the low logic output voltage for all outputs.

8.3.2 SR_$\overline{UVLO}$

The SR_$\overline{UVLO}$ (system reset and undervoltage lockout) input pin allows for an external controller to propagate an external fault by asserting (or force low) all outputs at once. When SR_UVLO is low (< $V_{TH\_SR\_\overline{UVLO}\_FALLING}$) the device enters in shutdown mode and all outputs are forced logical low. As the SR_$\overline{UVLO}$ is the input to an accurate (± 3.17%) comparator with a rising threshold voltage of $V_{TH\_SR\_\overline{UVLO}\_RISING}$ = 602mV, the designer can use the pin to set a external undervoltage lock-out if desired (refer to Figure 8-4). A fixed hysteresis of 103mV is incorporated in the comparator.

Usually the designer knows the voltage at which desired to enable the TPS7H3024. With that information, the resistive divider values can be calculated using Equation 1. Usually the top resistor is fixed to a 10kΩ value, but other values can be used. Using a larger value resistor minimizes power dissipation but can allow noise to couple into the outputs signal due a "weaker" pull-up.

$$R_{BOTTOM\_SR\_\overline{UVLO}} = R_{TOP\_SR\_\overline{UVLO}} \times \frac{V_{TH\_SR\_\overline{UVLO}\_RISING}}{V_{IN\_UVLO\_DESIRED} - V_{TH\_SR\_\overline{UVLO}\_RISING}} \quad (1)$$

where:

- $V_{TH\_SR\_\overline{UVLO}\_RISING}$ is the internal reference during a rising voltage on SR_$\overline{UVLO}$ (602mV typically).
  - Rather than use the typical value the designer can use the centered to minimize the error across voltage, temperature and radiation as shown below:

$$\frac{V_{TH\_SR\_\overline{UVLO}\_RISING(MIN)} + V_{TH\_SR\_\overline{UVLO}\_RISING(MAX)}}{2} = \frac{0.580V + 0.618\,V}{2} = 0.599V \quad (2)$$

- $V_{IN\_UVLO\_DESIRED}$ is the desired external voltage to enable the device during a rising voltage on V_{IN}.

- $R_{TOP\_SR\_\overline{UVLO}}$ is the selected top resistor for the divider.

Once the designer knows the actual (real) resistive divider values, Equation 3 and Equation 4 can be used to calculate the nominal rising and falling external undervoltage lockout as:

$$V_{IN\_UVLO\_RISING\_NOMINAL}\left(V\right) = \left(1 + \frac{R_{TOP\_SR\_\overline{UVLO}}}{R_{BOTTOM\_SR\_\overline{UVLO}}}\right) \times V_{TH\_SR\_\overline{UVLO}\_RISING} \quad (3)$$

$$V_{IN\_UVLO\_FALLING\_NOMINAL}\left(V\right) = \left(1 + \frac{R_{TOP\_SR\_\overline{UVLO}}}{R_{BOTTOM\_SR\_\overline{UVLO}}}\right) \times V_{TH\_SR\_\overline{UVLO}\_FALLING} \quad (4)$$

In Equation 4 the designer can use the centered across temperature, voltage and radiation (TID) as:

$$\frac{V_{TH\_SR\_\overline{UVLO}\_FALLING(MIN)} + V_{TH\_SR\_\overline{UVLO}\_FALLING(MAX)} +}{2} = \frac{0.475V + 0.517\,V}{2} = 0.496V \quad (5)$$

During startup the device needs to have a stable input voltage ($UVLO_{RISE}$ ≤ V_{IN} ≤ 14) for at least 2.8ms ($t_{START\_UP\_DELAY}$). This is to make sure all internal time constants have been passed. This also makes sure that the V_{TH_SENSEx} reference is settled and the accuracy is within specification (1%). When V_{IN} is a fast rising voltage, an external delay capacitance can be add to the resistive divider to enable the device after the $t_{START\_UP\_DELAY}$ have been exceed as shown in Figure 8-4. To select the capacitance (C_{DELAY}) for the SR_$\overline{UVLO}$ pin we can use Equation 6.

$$C_{DELAY}\left(F\right) > \frac{t_{DELAY}(s)}{R_{TH}\left(\Omega\right) \times \ln\left(-\frac{V_{TH}(V)}{V(t) - V_{TH}(V)}\right)} \quad (6)$$

where:

- t_{DELAY} (s) is the desired delay time in seconds (at least 2.8ms after V_{IN} > $UVLO_{RISE}$).
- R_{TH} is the Thévenin equivalent resistance, which is the parallel between $R_{TOP\_SR\_\overline{UVLO}}$ and $R_{BOTTOM\_SR\_\overline{UVLO}}$ in ohms.
  - $R_{TH}\left(\Omega\right) = \frac{R_{TOP\_SR\_\overline{UVLO}}\left(\Omega\right) \times R_{BOTTOM\_SR\_\overline{UVLO}}(\Omega)}{R_{TOP\_SR\_\overline{UVLO}}\left(\Omega\right) + R_{BOTTOM\_SR\_\overline{UVLO}}(\Omega)}$ (7)
- V_{TH} is the Thévenin equivalent voltage, which is the voltage at $V_{SR\_\overline{UVLO}}$ during steady state operation in volts.
  - $V_{TH}\left(V\right) = \left(\frac{R_{BOTTOM\_SR\_\overline{UVLO}}(\Omega)}{R_{TOP\_SR\_\overline{UVLO}}\left(\Omega\right) + R_{BOTTOM\_SR\_\overline{UVLO}}(\Omega)}\right) \times V_{IN}\left(V\right)$ (8)
- V(t) is the voltage at SR_$\overline{UVLO}$ ($V_{SR\_\overline{UVLO}}$) which starts the sequence up. In this case 0.602V.
  - We can use the centered value across temperature and voltage as specified on Equation 2.

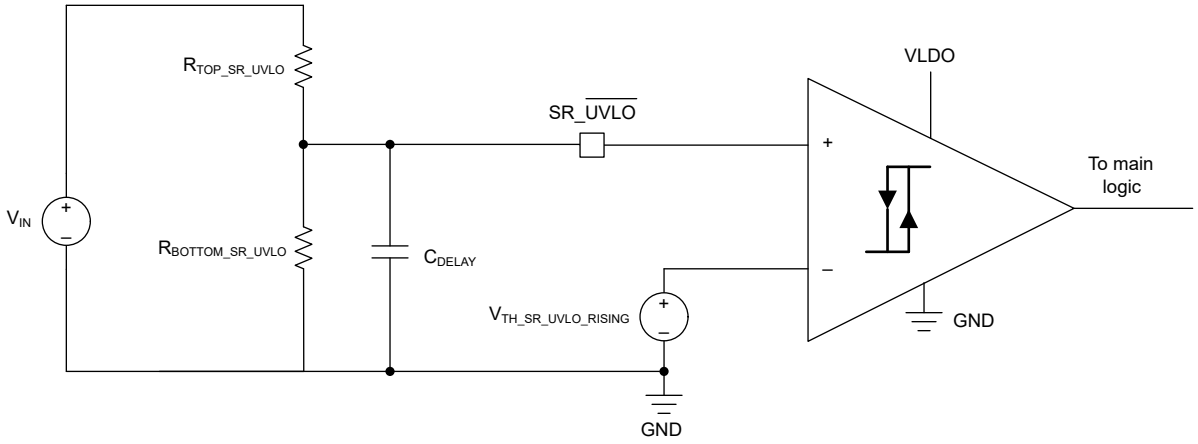
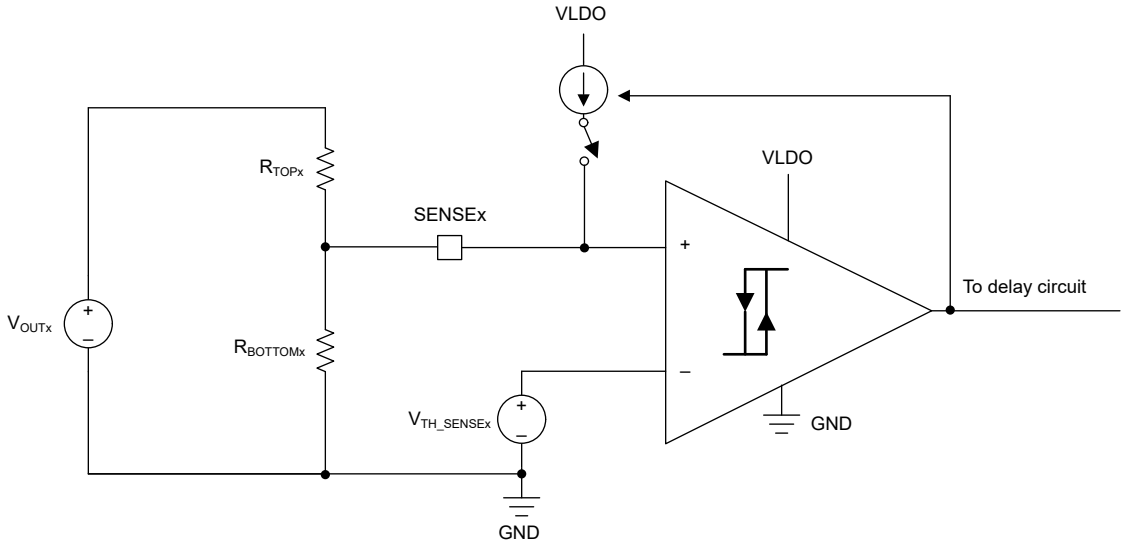


Figure 8-4. Monitor a Main Rail to Automatically Start the Sequence UP and $\overline{\text{DOWN}}$

8.3.3 SENSEx Inputs

8.3.3.1 V_{TH_SENSEx} and V_{OUTx_RISE}

The TPS7H3024 voltage supervisor integrates four input comparators, with an accurate (±1%) threshold voltage of 599.7mV (V_{TH_SENSEx}) typical. V_{TH_SENSEx} is measured at the $\overline{\text{RESET}}$x outputs to account for comparator offsets in the threshold. Maximum flexibility is provided as external resistive dividers can be adjusted to sense a desired voltage rail (V_{OUTx}). Figure 8-5 shows a conceptual diagram of the comparators connected to the SENSEx inputs. As can be observed, the sensed voltage rail (V_{OUTx}) is attenuated (using an external resistive divider, R_{TOPx} and $R_{BOTTOMx}$) and compared against the V_{TH_SENSEx} voltage. Is recommended to maintain the steady-state SENSEx voltage below 1.6V, to maintain good threshold (V_{TH_SENSEx}) accuracy over lifetime.



Note

The comparator by itself does not have a built-in voltage hysteresis. The hysteresis is controlled externally using the hysteresis current (I_{HYS_SENSEx}) and the top resistor (R_{TOPx}). For more details, refer to Section 8.3.3.4. The input comparator does not change for the undervoltage or overvoltage type. The overvoltage is implemented by inverting the signal that drives the output stage.

Figure 8-5. SENSEx Comparators Inputs

When the voltage at the monitored rail (V_{OUTx}) is rising, the hysteresis current (I_{HYS_SENSEx}) is not connected to the SENSEx input. The SENSEx (attenuated V_{OUTx}) voltage is compared to the internal reference (V_{TH_SENSEx}). When $V_{SENSEx} > V_{TH\_SENSEx}$ the voltage is considered as:

1. In regulation: for an undervoltage channel (UV).
2. Not in regulation: for an overvoltage channel (OV)

Calculate the rising voltage threshold voltage on V_{OUTx} by doing a simple voltage divider as:

$$V_{OUTx\_RISE\_NOMINAL}\left(V\right) = \left(1 + \frac{R_{TOPx}}{R_{BOTTOMx}}\right) \times V_{TH\_SENSEx} \quad (9)$$

Where:

- V_{TH_SENSEx} is the typical sense threshold voltage of 599.7mV.
  - If it is desired to minimize the error on the monitored voltage across temperature, the centered value can be used instead of the typical as:

$$V_{TH\_SENSEx} = \frac{V_{TH\_SENSEx(MIN)} + V_{TH\_SENSEx(MAX)}}{2} = 599mV \quad (10)$$

- R_{TOPx} is the top resistor in Ω.
- $R_{BOTTOMx}$ is the bottom resistor in Ω.

As with any system, there is some variation (or errors) of the design variables, in this case the top resistor, bottom resistors and the SENSEx threshold voltage (V_{TH_SENSEx}). Using the derivative method to calculate the total error (with the assumption that all variables are uncorrelated and both resistors have the same tolerance value), the $V_{TH\_RISEx\_NOMINAL}$ error can be calculated as:

$$V_{OUTx\_RISE\_ERROR}\left(V\right) = \pm\sqrt{\frac{V_{TH\_SENSEx}^{2} \times \left[\left(2 \times R_{TOL}^{2} \times R_{TOPx}^{2}\right) + \left(V_{TH\_SENSEx\_ACC}^{2} \times \left(R_{TOPx} + R_{BOTTOMx}\right)^{2}\right)\right]}{R_{BOTTOMx}^{2}}} \quad (11)$$

Where:

- R_{TOL} is the resistors tolerance (same for top and bottom resistors) as numeric value. For example, for 0.1% tolerance resistors, we use 0.001.
- $V_{TH\_SENSEx\_ACC}$ is the SENSEx threshold accuracy as numeric value (in this case 0.01).
- R_{TOPx} and $R_{BOTTOMx}$ are in Ω.
- V_{TH_SENSEx} is 0.599 Volts (center across temperature).

Using Equation 9 and Equation 11, calculate the rising voltage threshold range as:

$$V_{OUTx\_RISE} = V_{OUTx\_RISE\_NOMINAL} \pm V_{OUTx\_RISE\_ERROR} \quad (12)$$

Note

Remember V_{TH_SENSEx} is the reference voltage when accounting for the comparator offsets $V_{TH\_SENSEx} = V_{REF} + V_{IOx}$.

Although it is not required, in noisy applications it is good analog design practice to place a small bypass capacitor at the SENSEx inputs to reduce sensitivity to transient voltages on the monitored signal.

8.3.3.2 I_{HYS_SENSEx} and V_{OUTx_FALL}

The TPS7H3024 has a built-in hysteresis current of 24µA with an accuracy of ±3% (with R_{HYS} = 49.9kΩ). The hysteresis current is approximately equivalent to V_{HYS}/R_{HYS}. A tolerance of 0.1% for the R_{HYS} resistor is recommended as the tolerance ultimately affects the accuracy of the hysteresis current. This current is mirrored internally across all SENSEx inputs. This hysteresis current becomes active when the SENSEx voltage is greater than the threshold voltage (599.7mV ± 1%, refer to Equation 12 and Figure 8-5). This current (I_{HYS_SENSEx}) multiplied by the R_{TOPx} resistance induces a voltage (V_{HYS_SENSEx}) that is added to the SENSEx node. This effectively boost (or increments) the node voltage (in this case V_{SENSEx}).

When the V_{OUTx} voltage is falling and becomes lower than V_{OUT_FALLx}, the voltage is considered as:

1. Not in regulation: for an undervoltage channel (UV).
2. In regulation: for an overvoltage channel (OV).

The hysteresis voltage is defined as:

$$V_{HYS\_SENSEx\_NOMINAL}(V) = I_{HYS\_SENSEx} \times R_{TOPx} \quad (13)$$

Where:

- I_{HYS_SENSEx} = 24 × 10^{-6} Amps (or 24µA)
- R_{TOPx} units are in Ohms (Ω)

The falling voltage threshold can be calculated as:

$$V_{OUTx\_FALL\_NOMINAL}(V) = V_{OUTx\_RISE\_NOMINAL} - V_{HYS\_SENSEx\_NOMINAL} \quad (14)$$

Using Equation 9 and Equation 14

$$V_{OUTx\_FALL\_NOMINAL}\left(V\right) = \left[\left(1 + \frac{R_{TOPx}}{R_{BOTTOMx}}\right) \times V_{TH\_SENSEx}\right] - \left(I_{HYS\_SENSEx} \times R_{TOPx}\right) \quad (15)$$

Where:

- V_{TH_SENSEx} is the nominal sense threshold voltage of 0.599V
- I_{HYS_SENSEx} = 24 × 10^{-6} Amps (or 24µA)
- R_{TOPx} and $R_{BOTTOMx}$ units are in Ohms (Ω)

The V_{OUTx_FALL} error can be calculated as:

$$V_{TH\_FALLx\_ERROR}\left(V\right) = \pm\sqrt{\frac{A + B + C + D}{R_{BOTTOMx}^{2}}} \quad (16)$$

Equation 16 is obtained using the derivative method and under the assumptions that all variables are uncorrelated and both resistors have the same tolerance

Where the equation terms are:

$$A = I_{HYS\_SENSEx}^{2} \times I_{HYS\_SENSEx\_ACC}^{2} \times R_{TOPx}^{2} \times R_{BOTTOMx}^{2} \quad (17)$$

$$B = R_{TOL}^{2} \times R_{TOPx}^{2} \times V_{TH\_SENSEx}^{2} \quad (18)$$

$$C = R_{TOL}^{2} \times R_{TOPx}^{2} \times \left[\left(I_{HYS\_SENSEx} \times R_{BOTTOMx}\right) - V_{TH\_SENSEx}\right]^{2} \quad (19)$$

$$D = V_{TH\_SENSEx}^{2} \times V_{TH\_SENSEx\_ACC}^{2} \times \left(R_{TOPx} + R_{BOTTOMx}\right)^{2} \quad (20)$$

Where:

- R_{TOL} is the resistors tolerance (same for top and bottom resistors) as numeric value. For example, for 0.1% tolerance resistors, we use 0.001.
- $V_{TH\_SENSEx\_ACC}$ is the SENSEx threshold accuracy as numeric value (in this case 0.01).
- $I_{HYS\_SENSEx\_ACC}$ is the hysteresis current accuracy as numeric value (in this case 0.03).
- V_{TH_SENSEx} is the nominal sense threshold voltage of 0.599V.
- I_{HYS_SENSEx} = 24 × 10^{-6} Amps (or 24µA).
- R_{TOPx} and $R_{BOTTOMx}$ units are in Ohms (Ω).

Using Equation 15 and Equation 16 we can calculate the falling voltage range as:

$$V_{OUTx\_FALL} = V_{OUTx\_FALL\_NOMINAL} \pm V_{OUTx\_FALL\_ERROR} \quad (21)$$

Figure 8-6, shows a conceptual diagram of the rising and falling voltage, the diagram also shows the errors on this voltage due to V_{TH} accuracy, I_{HYS} accuracy, and the resistive divider tolerances. At the system level, take into account errors for a robust design.

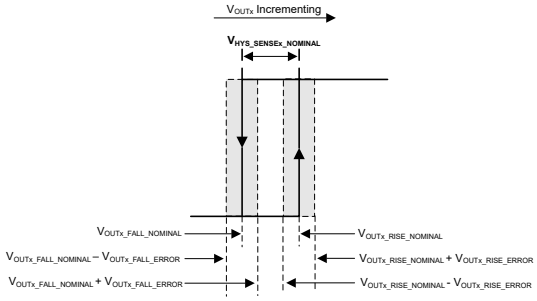
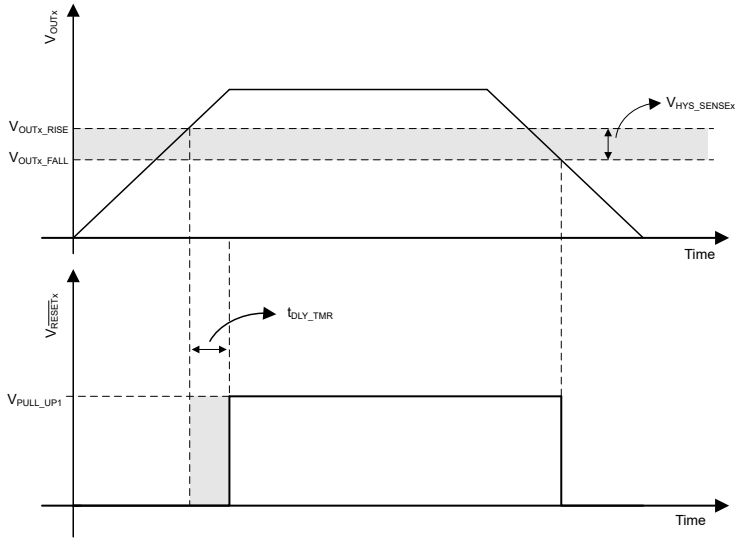


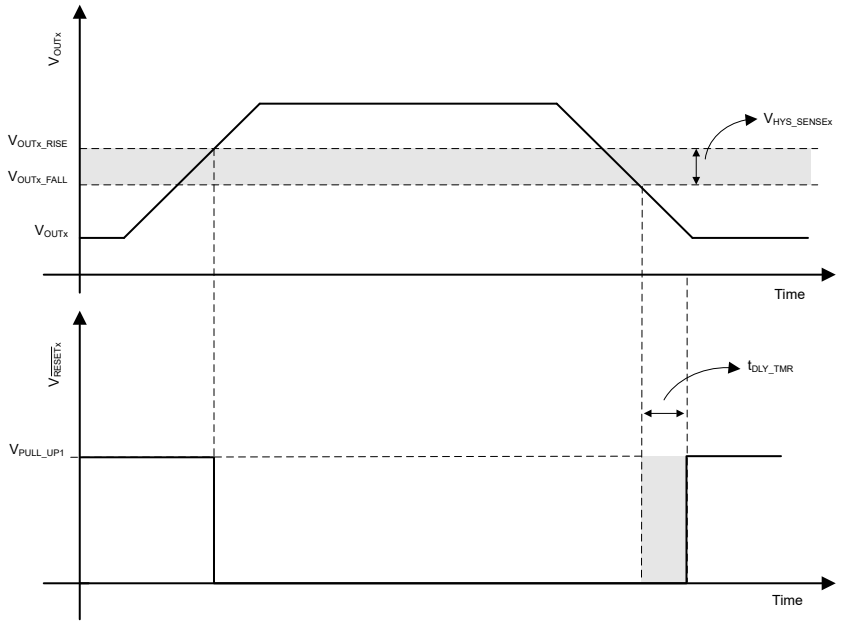
Figure 8-6. Rising and Falling Thresholds Voltages for the $SENSE_x$ Comparators

8.3.3.3 Input to Output Time Diagrams



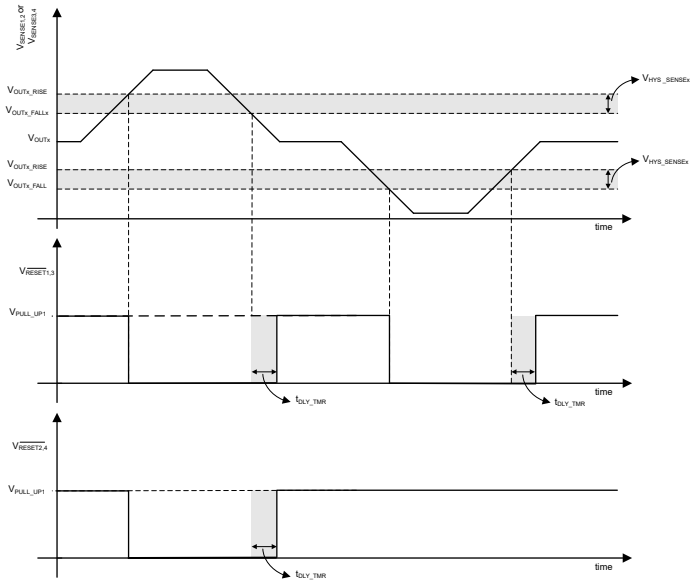
A. In the TPS7H3024 and TPS7H3124 the Channel # 1 (pin # 1) and channel # 3 (pin # 3) are of undervoltage type, when MODE=0.

Figure 8-7. Undervoltage channel (UV) time diagram



A. Channel # 2 (pin # 2) and channel # 4 (pin # 4) are of overvoltage type, when MODE=1.

Figure 8-8. Overvoltage channel (OV) time diagram



A. Channel # 1 (pin # 1) and channel # 2 (pin # 2) are internally or'ed to create a window channel while the channel # 3 (pin # 3) and channel # 4 (pin # 4) are or'ed to create a second window channel, when MODE=1

B. V_{OUTx_RISE},V_{OUTx_FALL} and V_{HYS_SENSEx} for the undervoltage and overvoltage can be different values.

Figure 8-9. Window channel time diagram

8.3.3.4 Top and Bottom Resistive Divider Design Equations

At the system level the designer knows (or selects) the V_{OUTx_RISE} and V_{OUTx_FALL} levels. Usually these voltages are selected as percentages of the nominal rail voltage (V_{OUTx}) being monitored. Knowing this information, we can calculate the nominal resistive divider components values (R_{TOPx} and $R_{BOTTOMx}$) for the desired target levels. Using Equation 13 and Equation 14 we can calculate the top resistor as:

$$R_{TOPx} = \frac{V_{OUTx\_RISE} - V_{OUTx\_FALL}}{I_{HYS\_SENSEx}} \quad (22)$$

From Equation 9 we can calculate the bottom resistor as:

$$R_{BOTTOMx} = \frac{R_{TOPx} \times V_{TH\_SENSEx}}{V_{OUTx\_RISE} - V_{TH\_SENSEx}} \quad (23)$$

It's important to notice that the larger the separation between V_{OUTx_RISE} and V_{OUTx_FALL} (referred to as V_{HYS_SENSEx}), the bigger the error in the falling voltage. Figure 8-10 shows a plot of the error in the V_{OUTx_FALL} for different sense hysteresis voltages (V_{HYS_SENSEx} = V_{OUTx_RISE} – V_{OUTx_FALL}). The plot is created for three different V_{OUTx_RISE} voltages (or percentages of the nominal output voltage as 90, 95, and 97%) and two different output voltages (0.8V and 28V). As can be observed, the output voltage has very little impact on the falling voltage error (differences cannot be easily viewed on the plot). The error (in percent) can go from approximately 1% (at V_{HYS_SENSEx} = 3%) to around 2.6% (at V_{HYS_SENSEx} = 80%).

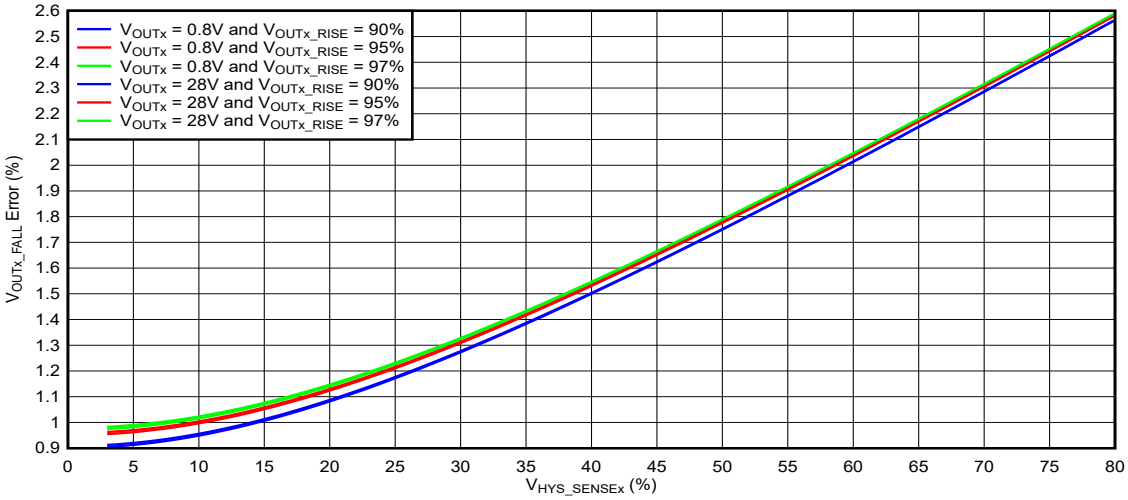


Figure 8-10. V_{OUTx_FALL} Absolute Error vs V_{HYS_SENSEx}

A. This plot does not includes the error on the V_{OUTx_FALL} due to the difference between the calculated top and bottom resistors using Equation 22 and Equation 23 and the actual resistance values that a designer can procure.
B. The resistor tolerance used for the calculation is 0.1%, V_{TH_SENSEx} accuracy is 1%, and the I_{HYS_SENSEx} accuracy is 3%.
C. In this plot the V_{HYS_SENSEx} (%) represents the separation as percentages of the nominal output voltage (V_{OUTx}).
D. In this plot, the V_{OUTx_FALL} error in % is normalized with respect to the full-scale voltage (or V_{OUTx}).

8.3.4 MODE

The mode pin is an input that change the behavior of the output stage to detect for:

1. Undervoltage (UV)
2. Overvoltage (OV)
3. Window

For more details refer to Table 8-1 and Section 8.3.5.

Note

MODE can be connected to the VLDO for a logic high. Use a series resistor for protection.

8.3.5 Output Stages (RESETx, PWRGD, WDO, PULL_UP1, and PULL_UP2)

The output stage's (RESET1 to RESET4), PWRGD and WDO are offered in push-pull and open-drain type. For more details on the output type by the GPN refer to Table 8-1. When the output are of overvoltage type, the RESETx is driven logically inverted from the output of the SENSEx comparators as shown in Figure 8-11 (also refer to Figure 8-16 and Figure 8-18).

In the case of the TPS7H3024 (push-pull outputs) and TPS7H3124 (open-drain outputs) with MODE=1, the SENSE1 (UV) and SENSE2 (OV) are internally AND'ed, the output is used to drive the RESET1 output. In this case RESET1 is the output of a window comparator. RESET2 is left unchanged and is the OV flag of SENSE2. As both the window and the OV flag are available, the system can read the outputs to known which type of fault occurred in the system (UV or OV). The same is true for SENSE3 and SENSE4, which form the second window comparator.

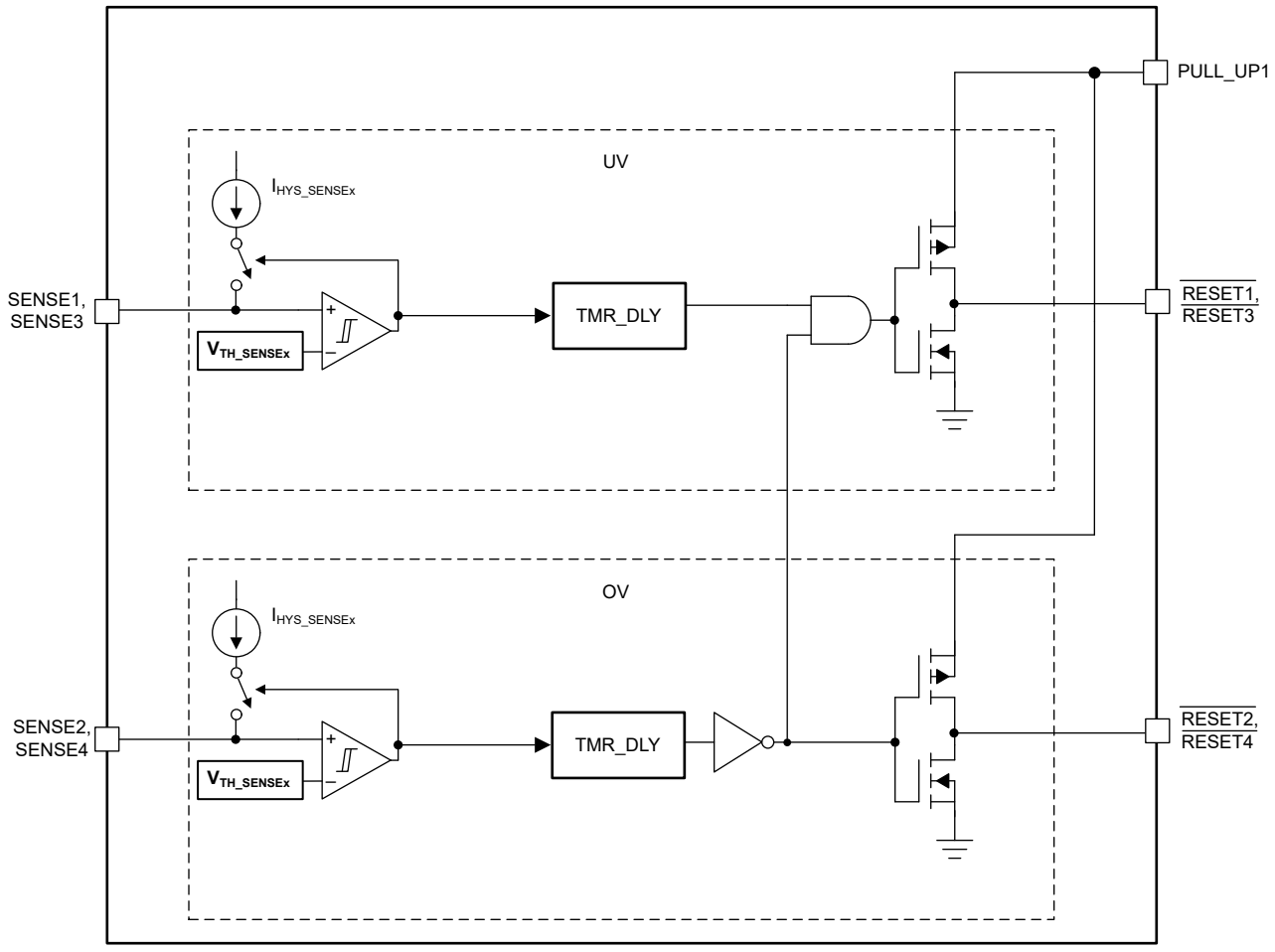


Figure 8-11. Window Comparator for TPS7H3024 when MODE=1

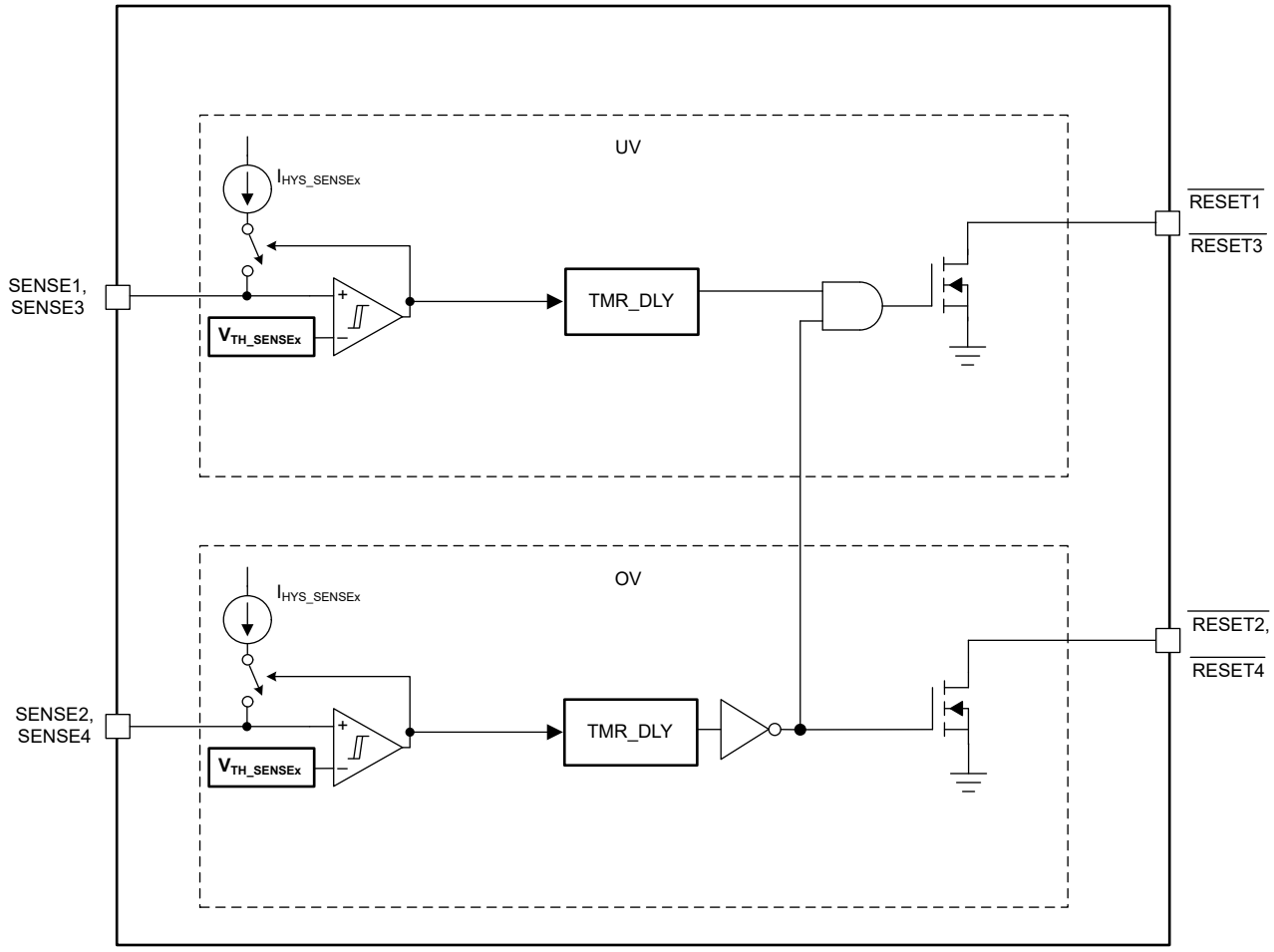


Figure 8-12. Window Comparator for TPS7H3124 when MODE=1

SENSE1 and SENSE2 are one window comparator channel while SENSE3 and SENSE4 create the second window comparator channel.

8.3.5.1 Push-Pull Outputs

The pull-up voltage for the push-pull outputs is externally provided by the user. PULL_UP1 (input) is the pull-up voltage domain for all $\overline{\text{RESETx}}$ outputs ($\overline{\text{RESET1}}$ to $\overline{\text{RESET4}}$), while PULL_UP2 (input) is the pull-up voltage domain for the PWRGD and $\overline{\text{WDO}}$ outputs. Refer to Figure 8-13 to Figure 8-16.

Note

There are no sequencing requirements for IN, PULL_UP1, and PULL_UP2.

Each output stage consists of a high side PMOS and low side NMOS (CMOS) pair. The PMOS resistance is typically 9Ω (max of 20Ω) while the NMOS is 16Ω typically (max of 36Ω), when $V_{PULL\_UPx} \geq 3.3V$. PULL_UP1 and PULL_UP2, have a voltage range of 1.6V to 7V, and can be independently biased or tied to the same voltage rail, however both most be biased. The output resistance of the PMOS leg has a PULL_UPx voltage dependency. The lower the PULL_UPx voltage, the higher the PMOS resistance.

When V_{IN} < V_{POR_IN} (2V maximum) or V_{PULL_UPx} > $V_{POR\_PULL\_UPx}$ (1.1V maximum) the output are in a known pull-down state. At this condition the outputs have reduced sinking capabilities with V_{OL} ≤ 320mV when the device is sinking 100µA of current into the outputs:

- $\overline{\text{RESETx}}$
- PWRGD
- $\overline{\text{WDO}}$

Once the input voltage range is within the recommended input voltage range of 3V to 14V, the outputs have the full strength capabilities of ±10mA, per output.

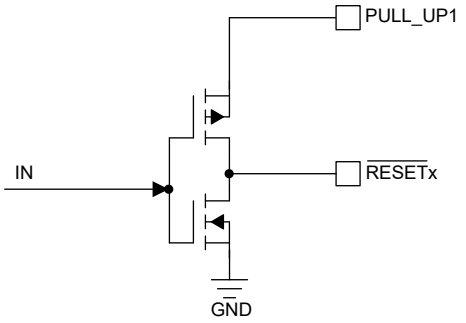


Figure 8-13. $\overline{\text{RESETx}}$ Push-Pull Output Stages for UV Channel Type

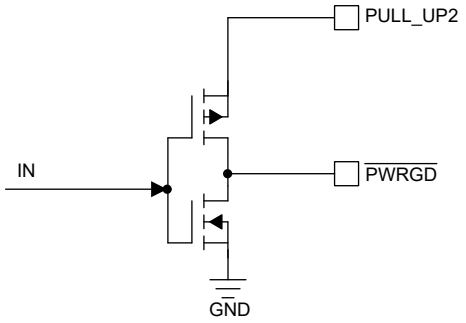


Figure 8-14. PWRGD Push-Pull Output Stage for UV Channel Type

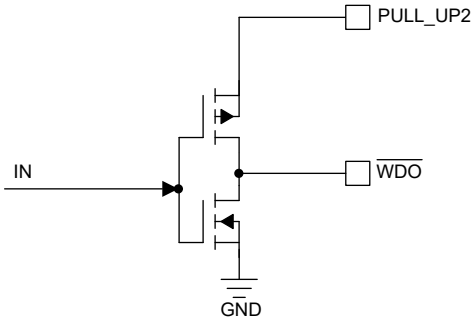
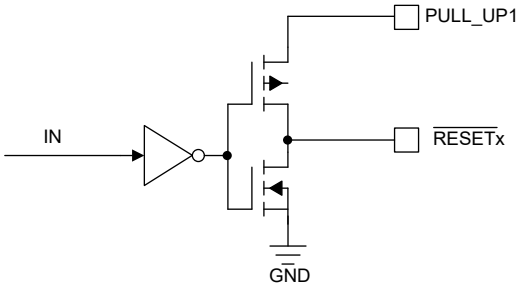


Figure 8-15. $\overline{\text{WDO}}$ Push-Pull Output Stage for UV Channel Type



A. Only the $\overline{\text{RESETx}}$ are dependent on the type of channel as: UV or OV. This is dependent in the logical value of the MODE input pin.

Figure 8-16. $\overline{\text{RESETx}}$ Push-Pull Output Stages for OV Channel Type

8.3.5.2 Open-Drain Outputs (TPS7H3124 and TPS7H3134)

In the open-drain variants (TPS7H31x4) the pins are externally pulled-up through a resistor to a voltage source with the desired logic level. The maximum pull-up voltage for the outputs ($\overline{\text{RESETx}}$, PWRGD and $\overline{\text{WDO}}$) is 7V. Select the pull-up resistor value to keep the maximum current sunk by the outputs below the recommended operating condition maximum of 2mA. Generally a pull up resistor of 10kΩ is sufficient. Using a larger value resistor will minimize power dissipation but can allow noise to couple into the outputs signal due a "weaker" pull-up. Refer to Figure 8-17 and Figure 8-18.

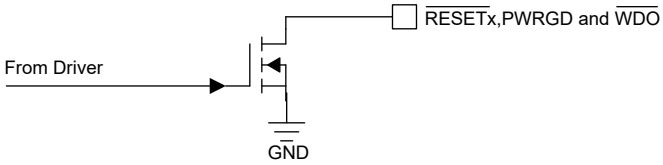
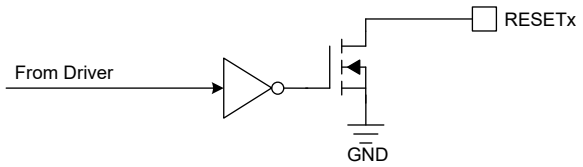


Figure 8-17. $\overline{\text{RESETx}}$, PWRGD and $\overline{\text{WDO}}$ Outputs in Open-Drain



A. Only the $\overline{\text{RESETx}}$ are dependent on the type of channel as: UV or OV. This is dependent in the logical value of the MODE input pin.

Figure 8-18. $\overline{\text{RESETx}}$ overvoltage (OV) Outputs in Open-Drain

8.3.6 WDI

The watchdog input (WDI) pin is the input of the non-inverting input of a comparator with a 602mV voltage reference ($V_{TH\_WDI\_RISING}$). The comparator has a built-in 104mV (fixed) hysteresis voltage to aid in noise immunity. The watchdog state machine clears (or resets the watchdog counter) every time a rising voltage is detected on the WDI pin. To account for the variation of the watchdog time-out, it is recommended to use the minimum value of the WD_TMR when determining how often the processor sends the WDI signal. For example, if the WD_TMR is programmed to 1s, the actual timeout is from 0.8s to 1.2s. Therefore, it is recommended the WDI signal be sent by the processor at least every 0.8s to account for the worst case variation. The WD_TMR (or timeout) is programmed by the user, by using the WD_TMR input. The timer have a programmable range from 520ms to 1.5s. For more details refer to Section 8.3.7.2.

8.3.7 User-Programmable TIMERS

The TPS7H3024 has two adjustable timers:

1. DLY_TMR with a typical range from 260µs to 23.37ms.
2. WD_TMR with a typical range from 520ms to 1.5s.

Both timers are programmed via a single resistor from the DLY_TMR and WD_TMR pins to GND. The resistors are used to program the internal oscillator frequency of the timers. Leaving the DLY_TMR or the WD_TMR pin floating disables the respective timer. Disabling a timer reduces the quiescent (I_{Q_IN}) current of the device. Refer to Figure 6-5 for more details.

Note

The resistor configuration of the timer pins must be valid at power up and must not be dynamically changed.

8.3.7.1 DLY_TMR

The TPS7H3024 includes an adjustable time delay. A single resistor connected between the DLY_TMR pin and GND programs the delay. Possible resistor (R_{DLY}) values are from 10.5kΩ to 1.18MΩ for a delay from 260µs to 23.7ms, respectively. This delay is valid only during the out-of-fault conditions as follow:

1. UV: in the undervoltage channel (UV) the delay is valid when V_{OUTx} voltage is rising and crosses the V_{OUTx_RISE}.
2. OV: in the overvoltage channel (OV) the delay is valid when the V_{OUTx} voltage is falling and crosses the V_{OUTx_FALL}.

For more details refer to Figure 8-7 and Figure 8-8.

If no delay is preferred for the system, the pin (DLY_TMR) can be left floating. Disabling the timer results in a reduced current consumption on the device (I_{Q_IN}). When no delay is preferred, an inherent propagation delay of 4.3µs (maximum) is observed, between V_{OUTx} crossing the V_{OUTx_RISE} and V_{OUTx_FALL}.

The DLY_TMR resistor can be selected using Equation 24. Figure 8-19 shows the linear trend between the DLY_TMR resistor and the delay time.

$$R_{DLY\_TMR}(k\Omega) = \left[49.71 \times t_{DLY\_TMR}(ms)\right] - 2.5 \quad (24)$$

Table 8-2 shows nominal resistors value for different delay times.

Table 8-2. Typical DLY_TMR Resistors

DELAY (ms)	R_{DLY_TMR} (kΩ)
0.260	10.5
12.5	619
23.7	1180

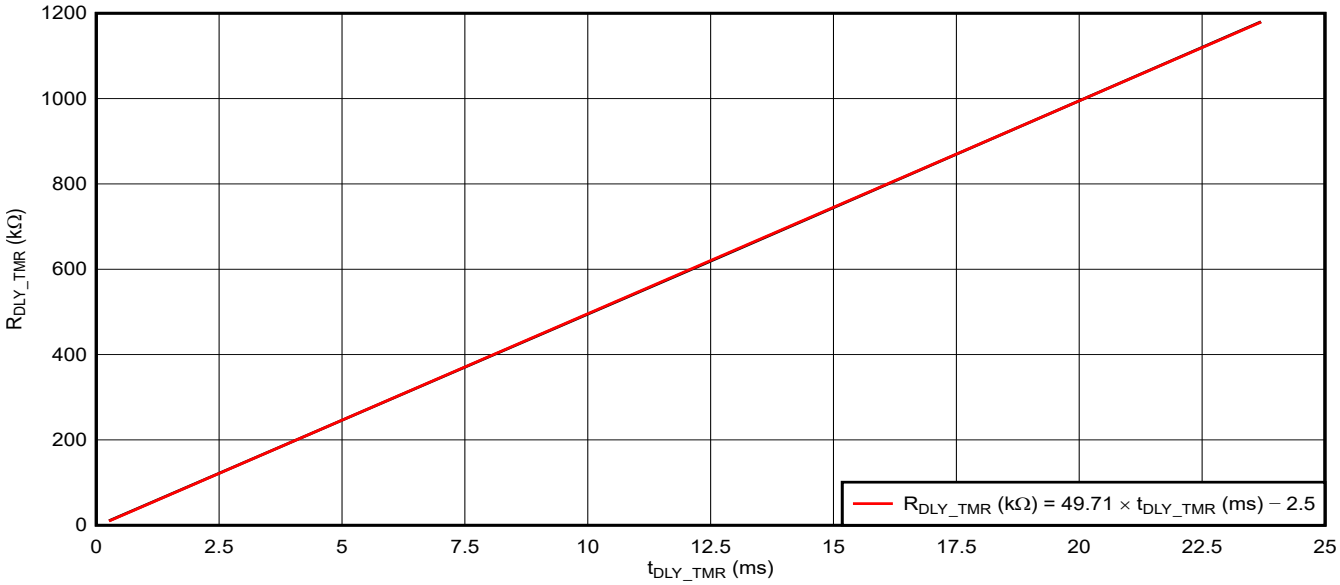


Figure 8-19. R_{DLY_TMR} vs t_{DLY_TMR} Across Full Oscillator Range

8.3.7.2 WD_TMR

The WD_TMR is an adjustable timer that programs the time-out of the internal watchdog timer. The watchdog timer is commonly used to monitor coherent processor execution. If the monitored processor is halted due to a fault, the WDI pin does not detect a rising edge resulting in asserting the $\overline{WDO}$ low, hence resetting the processor to a known state. A typical connection between the monitored processor and the TPS7H3024 is shown in Figure 8-20. Figure 8-21 shows the correct and incorrect (late pulse) handshake between the processor and the watchdog in the TPS7H3024.

The user can program the WD_TMR using a single resistor between the WD_TMR pin and GND. The range of the resistor (R_{WD}) is from 56.2kΩ to 174kΩ, for a time from 520ms to 1.5s, respectively. If the user does not want to use the watchdog timer, the pin can be left floating. Disabling the watchdog timer reduces the quiescent (I_{Q_IN}) current of the device.

Note

When the watchdog timer is disabled (by floating the WD_TMR pin), $\overline{WDO}$ is equal to PWRGD.

The REG_TMR resistor can be selected using Equation 25. Figure 8-22 shows the linear trend between the WD_TMR resistor and the allowed time to clear the watchdog timer (or time-out).

$$R_{WD\_TMR}(k\Omega) = \left[114.5 \times t_{WD\_TMR}(s)\right] - 3.5 \quad (25)$$

Table 8-3 shows typical resistor values for different allowed regulation times. The WDI pin minimum pulse width is specified as twice the watchdog oscillator period. The oscillator period can be calculated using Equation 26.

$$t_{WD\_OSC}(s) = \frac{t_{WD\_TMR}(s)}{57{,}344} \quad (26)$$

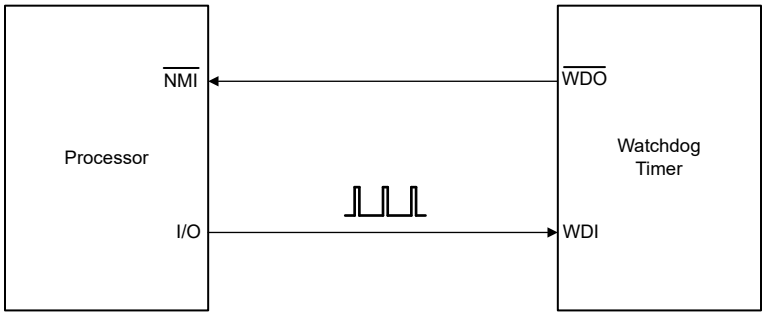


Figure 8-20. Watchdog Timer Typical Handshake Between TPS7H3024 and Monitored Processor

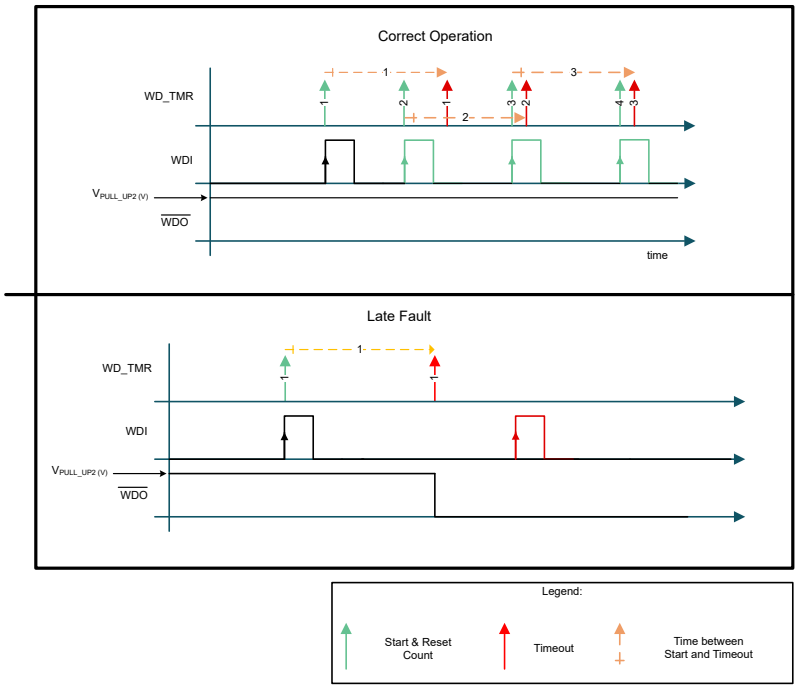


Figure 8-21. Watchdog Timing Diagram

Table 8-3. Typical REG_TMR Resistors

ALLOWED REGULATION TIME (s)	R_{REG_TMR} (kΩ)
0.52	56.2
1	118
1.5	174

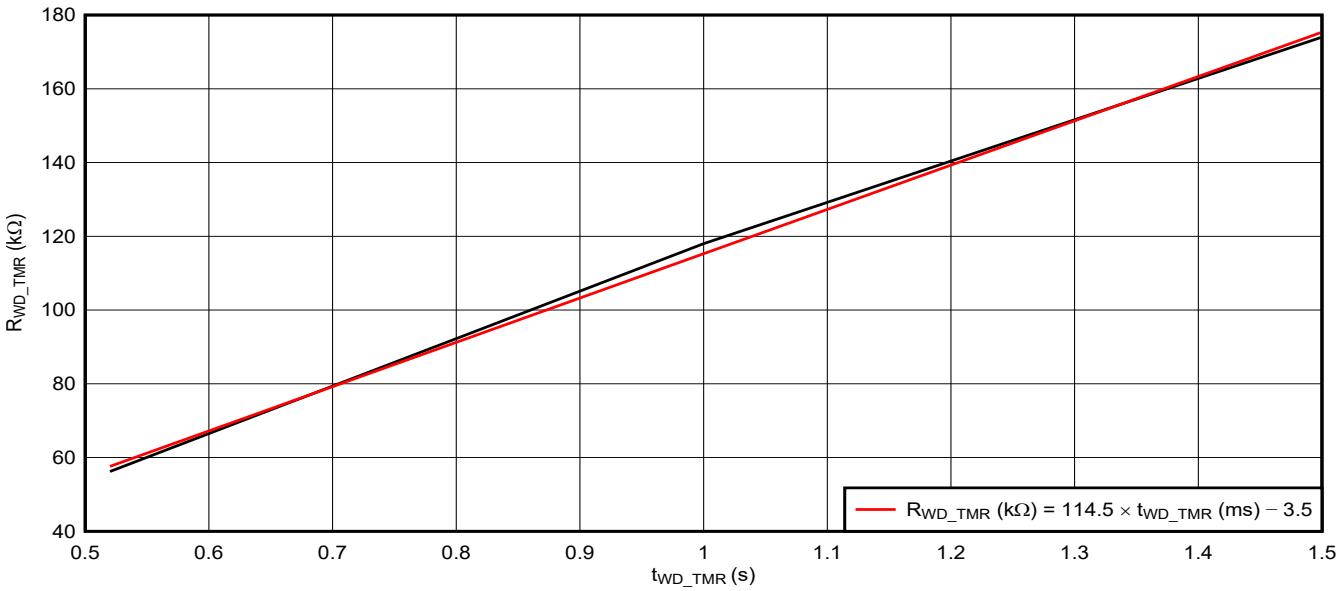


Figure 8-22. R_{WD_TMR} vs t_{WD_TMR} Across Full Oscillator Range

8.4 Device Functional Modes

Table 8-4. $\overline{\text{RESETx}}$, PWRGD and $\overline{\text{WDO}}$ Truth Table when V_{IN} and V_{PULL_UPx} is Lower than the Recommended Minimum Voltage for TPS7H3xx4.

SR_$\overline{\text{UVLO}}$ (1) (2)	SENSEx (3) (4)	$\overline{\text{RESETx}}$	PWRGD	$\overline{\text{WDO}}$	IN	PULL_UPx
0 or 1	0 or 1	Undetermined	Undetermined	Undetermined	$V_{IN} < V_{POR\_IN}$	$V_{PULL\_UPx} < V_{POR\_PULL\_UPx}$
		L	L	L	$V_{IN} < V_{POR\_IN}$	$V_{POR\_PULL\_UPx} < V_{PULL\_UPx} < 1.6V$
		L	L	L	$V_{POR\_IN} < V_{IN} < 3V$	$V_{PULL\_UPx} < V_{POR\_PULL\_UPx}$
		L	L	L	$V_{POR\_IN} < V_{IN} < 3V$	$1.6V < V_{PULL\_UPx} < 7V$

Table 8-5. $\overline{\text{RESETx}}$, PWRGD and WDO Truth Table when V_{IN} and V_{PULL_UPx} is Within Recommended Operating Voltages for the TPS7H3024 and TPS7H3124

SR_$\overline{\text{UVLO}}$ (1) (2)	MODE (5) (6)	SENSE1 (3) (4)	SENSE2 (3) (4)	SENSE3 (3) (4)	SENSE4 (3) (4)	$\overline{\text{RESET1}}$	$\overline{\text{RESET2}}$	$\overline{\text{RESET3}}$	$\overline{\text{RESET4}}$	PWRGD	$\overline{\text{WDO}}$ (7) (8)
0	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	L	L	L	L	L	L
1	0	0	0	0	0	L	H	L	H	L	L
		0	0	0	1	L	H	L	L	L	L
		0	0	1	0	L	H	H	H	L	L
		0	0	1	1	L	H	H	L	L	L
		0	1	0	0	L	L	L	H	L	L
		0	1	0	1	L	L	L	L	L	L
		0	1	1	0	L	L	H	H	L	L
		0	1	1	1	L	L	H	L	L	L
		1	0	0	0	H	H	L	H	L	L
		1	0	0	1	H	H	L	L	L	L
		1	0	1	0	H	H	H	H	H	H
		1	0	1	1	H	H	H	L	L	L
		1	1	0	0	H	L	L	H	L	L
		1	1	0	1	H	L	L	L	L	L
		1	1	1	0	H	L	H	H	L	L
		1	1	1	1	H	L	H	L	L	L
	1	0	0	0	0	L	H	L	H	L	L
		0	0	0	1	L	H	L	L	L	L
		0	0	1	0	L	H	H	H	L	L
		0	0	1	1	L	H	L	L	L	L
		0	1	0	0	L	L	L	H	L	L
		0	1	0	1	L	L	L	L	L	L
		0	1	1	0	L	L	H	H	L	L
		0	1	1	1	L	L	L	L	L	L
		1	0	0	0	H	H	L	H	L	L
		1	0	0	1	H	H	L	L	L	L
		1	0	1	0	H	H	H	H	H	H
		1	0	1	1	H	H	L	L	L	L
		1	1	0	0	L	L	L	H	L	L
		1	1	0	1	L	L	L	L	L	L
		1	1	1	0	L	L	H	H	L	L
		1	1	1	1	L	L	L	L	L	L

Table 8-6. $\overline{\text{RESETx}}$, PWRGD and WDO Truth Table When V_{IN} and V_{PULL_UPx} is Within Recommended Operating Voltages for the TPS7H3034 and TPS7H3134

SR_$\overline{\text{UVLO}}$ (1) (2)	MODE (5) (6)	SENSE1 (3) (4)	SENSE2 (3) (4)	SENSE3 (3) (4)	SENSE4 (3) (4)	$\overline{\text{RESET1}}$	$\overline{\text{RESET2}}$	$\overline{\text{RESET3}}$	$\overline{\text{RESET4}}$	PWRGD	$\overline{\text{WDO}}$ (7) (8)
0	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	L	L	L	L	L	L
1	0	0	0	0	0	L	L	L	L	L	L
		0	0	0	1	L	L	L	H	L	L
		0	0	1	0	L	L	H	L	L	L
		0	0	1	1	L	L	H	H	L	L
		0	1	0	0	L	H	L	L	L	L
		0	1	0	1	L	H	L	H	L	L
		0	1	1	0	L	H	H	L	L	L
		0	1	1	1	L	H	H	H	L	L
		1	0	0	0	H	L	L	L	L	L
		1	0	0	1	H	L	L	H	L	L
		1	0	1	0	H	L	H	L	L	L
		1	0	1	1	H	L	H	H	L	L
		1	1	0	0	H	H	L	L	L	L
		1	1	0	1	H	H	L	H	L	L
		1	1	1	0	H	H	H	L	L	L
		1	1	1	1	H	H	H	H	H	H
	1	0	0	0	0	H	H	H	H	H	H
		0	0	0	1	H	H	H	L	L	L
		0	0	1	0	H	H	L	H	L	L
		0	0	1	1	H	H	L	L	L	L
		0	1	0	0	H	L	H	H	L	L
		0	1	0	1	H	L	H	L	L	L
		0	1	1	0	H	L	L	H	L	L
		0	1	1	1	H	L	L	L	L	L
		1	0	0	0	L	H	H	H	L	L
		1	0	0	1	L	H	H	L	L	L
		1	0	1	0	L	H	L	H	L	L
		1	0	1	1	L	H	L	L	L	L
		1	1	0	0	L	L	H	H	L	L
		1	1	0	1	L	L	H	L	L	L
		1	1	1	0	L	L	L	H	L	L
		1	1	1	1	L	L	L	L	L	L

(1) 0 = $V_{SR\_\overline{UVLO}} < V_{TH\_SR\_\overline{UVLO}\_FALLING}$
(2) 1 = $V_{SR\_\overline{UVLO}} > V_{TH\_SR\_\overline{UVLO}\_RISING}$
(3) 0 = $V_{SENSEx} < V_{TH\_SENSEx}$
(4) 1 = $V_{SENSEx} > V_{TH\_SENSEx}$
(5) 0 = $V_{MODE} < V_{TH\_MODE\_FALLING}$
(6) 1 = $V_{MODE} > V_{TH\_MODE\_RISING}$
(7) Assuming a valid rising edge pulse in WDI before the Watchdog timer is expired.
(8) In the TPS7H3124, the $\overline{\text{WDO}}$ is not masked by PWRDG, $\overline{\text{WDO}}$ remains high as long as a valid pulse in provided in WDI; otherwise, it goes low.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS7H3024 is a radiation hardened 4-channel voltage supervisor with a watchdog timer. It can be used to supervise FPGAs, ASICs, AFEs, and various power system voltage rails and processor coherent execution.

9.2 Typical Application

9.2.1 Window Voltage Monitoring

In many modern systems (or sub-systems), multiple voltage rails are often needed (we refer to this as the power tree). Often these power trees have tight voltage specification for reliable operation. If these specifications are not satisfied, unreliable operation or permanent malfunction can happen. To help enable reliable operation, voltage rails are supervised in real time and corrective action (such as power-down, disabling local regulators, and so forth.) is propagated trough the system.

In this example, two voltage rails are monitored using a window trigger to make sure the rails are operating within specification. Detailed design procedure and component selection is provided below. The design is summarized in Figure 9-1.

Note

All calculated numbers shown in this example are rounded to two decimal places with the exception of the bottom resistor for the sense divider which is rounded to 3 decimal places.

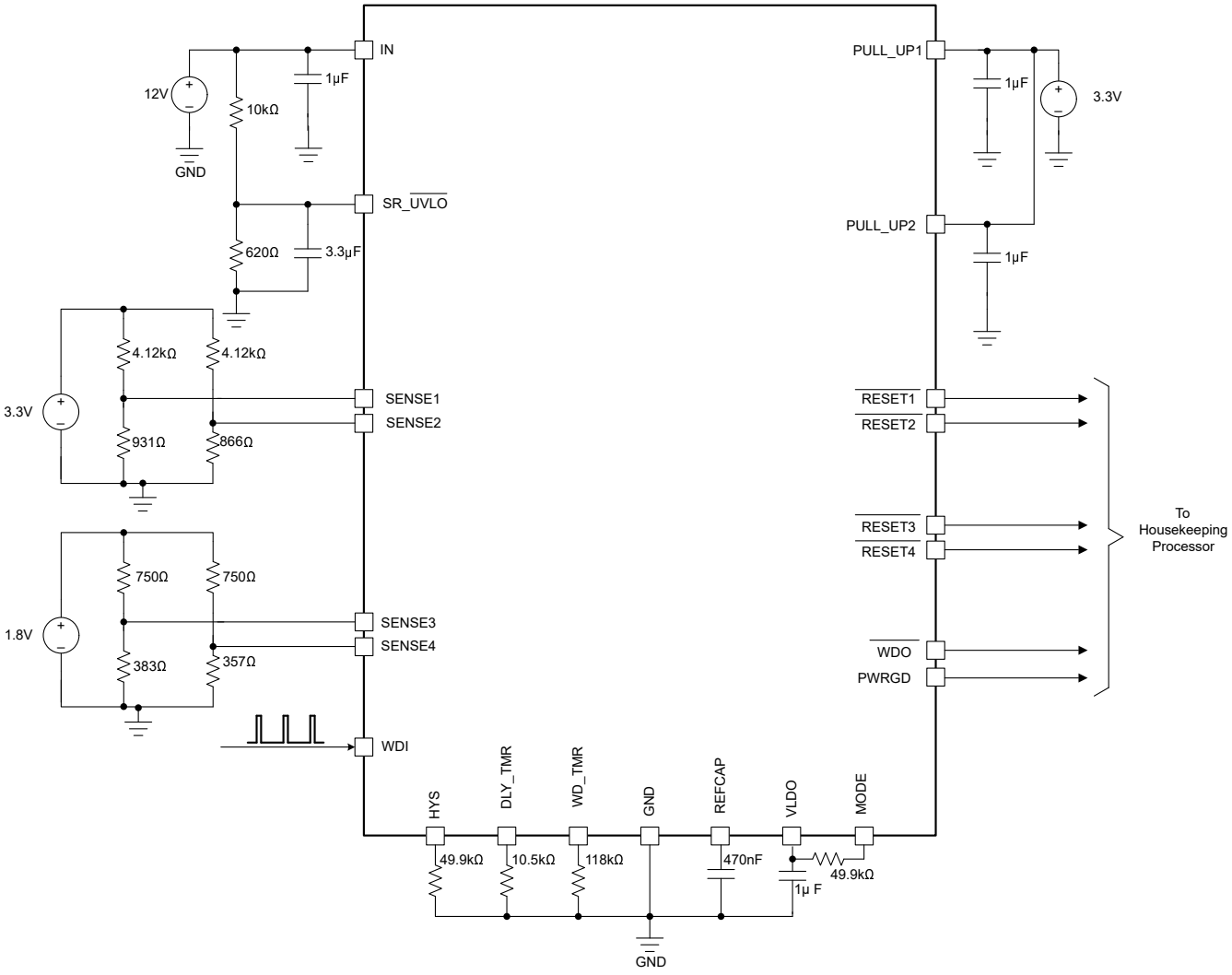


Figure 9-1. Window Voltage Monitoring with Watchdog

9.2.1.1 Design Requirements

This design requires monitoring two voltage rails using window comparators to make sure of reliable operation. As window supervision is used, the upper and lower system specification bounds are monitored. Additionally, coherent processor execution is monitored using the watchdog. The supervisor IC is set to start around 86% (or 10.31V) of the nominal 12V rail, using an external resistive divider driving the SR_$\overline{\text{UVLO}}$ pin.

All flags are assumed to be monitored by a house-keeping processor, and the $\overline{\text{WDO}}$ is used to drive the non-maskable interrupt of the processor. All design conditions are defined in Table 9-1.

Table 9-1. Design Conditions

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
System nominal voltage	Monitor the 12V input voltage to the supervisor and enable the IC when the voltage is greater than 10.3V (86%) for at least 2.8ms. When the voltage decrements below 8.5V (or 71%) the system is disabled.	The TPS7H3024 can be externally enabled accurately by using the SR_$\overline{\text{UVLO}}$. The internal reference is accurate to 3.1% across temperature, voltage and TID. For minimal error, users are recommended to use 0.1% tolerance resistors.

Table 9-1. Design Conditions (continued)

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
V_{OUT1}= 3.3V (nominal)	Undervoltage with: $V_{OUT1\_RISE\_UV}$ = 98% and $V_{OUT1\_FALL\_UV}$ = 95%	$V_{OUT1\_RISE\_UV}$ = 3.25V $V_{OUT1\_FALL\_UV}$ = 3.15V
	Overvoltage with: $V_{OUT1\_RISE\_OV}$ = 105% and $V_{OUT1\_FALL\_OV}$ = 102%	$V_{OUT1\_RISE\_OV}$ = 3.45V $V_{OUT1\_FALL\_OV}$ = 3.35V
V_{OUT2}=1.8V (nominal)	Undervoltage with: $V_{OUT2\_RISE\_UV}$ = 98% and $V_{OUT2\_FALL\_UV}$ = 97%	$V_{OUT2\_RISE\_UV}$ = 1.77V $V_{OUT2\_FALL\_UV}$ = 1.75V
	Overvoltage with: $V_{OUT2\_RISE\_OV}$ = 103% and $V_{OUTx\_FALL\_OV}$ = 102%	$V_{OUT2\_RISE\_OV}$ = 1.86V $V_{OUT2\_FALL\_OV}$ = 1.84V
$\overline{\text{RESET}}$x delay during the out-of-fault state	Delay of 260µs nominal	R_{DLY_TMR} = 10.5kΩ
Watchdog timeout	1 second nominal	R_{WD_TMR} = 118kΩ

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Input Power Supplies and Decoupling Capacitors

The TPS7H3024 has three input power supplies:

1. IN, the input supply to provide power to the TPS7H3024 IC. This power supply must be decoupled with at least 1µF or greater as close to the pin as possible. In this application, V_{IN} = 12V.
2. PULL_UP1, which is the input supply to program the $\overline{\text{RESET}}$x output voltage high (V_{OH}). These outputs are connected to the house-keeping processor. This power supply must be decoupled with at least 1µF or greater as close to the pin as possible. In this application, the V_{PULL_UP1} = 3.3V.
3. PULL_UP2, which is the input supply to program the output voltage high (V_{OH}) of PWRGD and $\overline{\text{WDO}}$ outputs. These outputs are connected to the house-keeping processor, in particular $\overline{\text{WDO}}$ is usually connected to the non maskable ($\overline{\text{NMO}}$) input of the processor that is generating the WDI pulse. This power supply must be decoupled with at least 1µF or greater as close to the pin as possible. In this application, the V_{PULL_UP1} = 3.3V.

The TPS7H3024 also has two regulated voltage outputs that need to be decoupled for good electrical and radiation performance. These are:

1. REFCAP, the 1.2V reference, used internally in the device to generate all radiometric voltage reference such as:
   - V_{TH_SENSEx}
   - I_{HYS_SENSEx}
   - $V_{TH\_SR\_\overline{UVLO}}$
   - V_{TH_WDI}
   - V_{TH_MODE}

   Decouple this reference with a 470nF ceramic capacitor as close to the pin as possible. Do not load this pin externally.
2. VLDO, this is the output of the internal regulator used to provide power to the internal circuits on the TPS7H3024. Decouple this regulator with at least 1µF as close to the pin as possible. This LDO can be loaded up to 5mA. Is important to understand that this LDO is not protected for short circuits.

9.2.1.2.2 SR_$\overline{\text{UVLO}}$ Threshold

In this application the SR_$\overline{\text{UVLO}}$ pin is used to monitored the input voltage supply of 12V and enables the device when the desired voltage is reached.

The IC is enabled when the rail voltage is greater than 10.26V (or 85.5% of the nominal voltage, typically). The falling voltage is not controlled as the hysteresis voltage on the SR_$\overline{\text{UVLO}}$ is internally controlled. However is calculated to be 8.55V (or 71.2% of the nominal voltage, typically). As the TPS7H3024 has an internal time constant ($t_{Start\_up\_delay}$) of 2.8ms (maximum), a delay capacitor of 3.3µF is added to SR_$\overline{\text{UVLO}}$ pin. This capacitor is added to introduce a delay in the SR_$\overline{\text{UVLO}}$ pin when V_{IN} is rising. This capacitor adds a second condition to start the sequence up, if V_{IN} ≥ 10.26V (typical) for at least 2.8ms then the IC is enabled.

Fixing the upper resistor for the resistive divider in SR_$\overline{\text{UVLO}}$, we can calculate the bottom resistor per our design requirements. The upper resistor is fixed to 10kΩ. Using the equation in Equation 1 the bottom resistor is calculated as:

$$V_{BOTTOM\_SR\_\overline{UVLO}} = 10k\Omega \times \frac{0.599V}{10.26V - 0.599V} = 620\Omega \quad (27)$$

Now that the reference resistor is calculated, we can select the actual (or real) resistor. In this case a 0.1% tolerance resistor is used to select the closest value (in this specific case the reference and real resistor is the same)

- $R_{BOTTOM\_SR\_\overline{UVLO}}$ = 620Ω

With the actual resistor values, we can back-calculate the rising and falling voltages that enables and disables the supervisor, respectively. Using Equation 3 and Equation 4 as:

$$V_{IN\_UVLO\_RISING\_NOMINAL}(V) = \left(1 + \frac{10k\Omega}{620\Omega}\right) \times 0.599V \cong 10.26V \quad (28)$$

$$V_{IN\_UVLO\_FALLING\_NOMINAL}(V) = \left(1 + \frac{10k\Omega}{620\Omega}\right) \times 0.496V \cong 8.50V \quad (29)$$

The delay capacitor is calculated using Equation 7, Equation 8, and Equation 6 as:

$$R_{TH}(\Omega) = \frac{10k\Omega \times 620\Omega}{10k\Omega + 620\Omega} = 583.80\Omega \quad (30)$$

$$V_{TH}(\Omega) = \left(\frac{620\Omega}{10k\Omega + 620\Omega}\right) \times 12V = 0.70V \quad (31)$$

$$C_{DELAY}(F) \geq \frac{0.0028s}{582.8\Omega \times \ln\left(-\frac{0.7V}{0.599V - 0.7V}\right)} = 2.48\mu F \quad (32)$$

The delay capacitor is selected as 3.3µF.

9.2.1.2.3 SENSEx Thresholds

The SENSEx inputs are used to monitor the voltage rails against system level bounds (or limits). For this design the output voltages to be monitored are:

1. V_{OUT1} = 3.3V
2. V_{OUT2} = 1.8V

The design V_{OUTx_RISE} and V_{OUTx_FALL} for each rail is specified in Table 9-2

Table 9-2. Rise and Fall Design Requirement by Channel

Channel #	Channel Type	V_{OUTx_NOM} (V)	V_{ONx_RISE} (%)	V_{ONx_RISE} (V)	V_{ONx_FALL} (%)	V_{ONx_FALL} (V)
1	UV	3.3	98	3.23	95	3.14
2	OV		105	3.47	102	3.37
3	UV	1.8	98	1.76	97	1.75
4	OV		103	1.85	102	1.84

Using Equation 22 and Equation 23 we can calculate the top and bottom reference resistors and select the closest resistor values using 0.1% resistor values. Table 9-3 shows the reference (or calculated) top and bottom resistors. Table 9-4 shows the selected resistors for the application.

Table 9-3. SENSEx Reference Nominal Resistors

Channel #	R_{TOP} (kΩ)	R_{BOTTOM} (kΩ)
1	4.13	0.94
2		0.86
3	0.75	0.39
4		0.36

An calculation example for channel 1 (or SENSE1) top and bottom resistor is shown below:

$$\frac{3.23\ \text{V} - 3.14\ \text{V}}{24\ \mu\text{A}} = 4.13\text{k}\Omega \quad (33)$$

$$\frac{4.13\ \text{k}\Omega \times 0.60\ \text{V}}{3.23\ \text{V} - 0.60\ \text{V}} = 0.94\text{k}\Omega \quad (34)$$

Table 9-4. SENSEx Selected Resistors Using 0.1% Tolerance Resistors

Channel #	R_{TOP} (kΩ)	R_{BOTTOM} (kΩ)
1	4.12	0.931
2		0.866
3	0.75	0.383
4		0.357

Now that the actual resistors are known, we can calculate the actual on and off nominal voltages and the error voltages by using Equation 9, Equation 11, Equation 12, Equation 15, Equation 16, and Equation 21. Using the errors, we can calculate the upper and lower voltages and normalize the values with respect to the nominal output voltage.

Table 9-5. V_{OUTx_RISE} Nominal Values With Statistics in Volts and Percentage

Channel #	$V_{OUTx\_RISE\_NOMINAL}$ (V)	$V_{OUTx\_RISE\_NOMINAL}$ (1) (%)
1	3.25	98.48
2	3.45	104.51
3	1.77	98.44
4	1.86	103.19

(1) Values are normalized to the nominal output voltage for that rail.

Table 9-6. V_{OUTx_FALL} Nominal Values with Statistics in Volts and Percentage

Channel #	$V_{OUTx\_FALL\_NOMINAL}$ (V)	$V_{OUTx\_FALL\_NOMINAL}$ (%)(1)
1	3.15	95.48
2	3.35	104.51
3	1.75	98.88
4	1.84	103.19

(1) Values are normalized to the nominal output voltage for that rail.

9.2.1.3 Application Curves

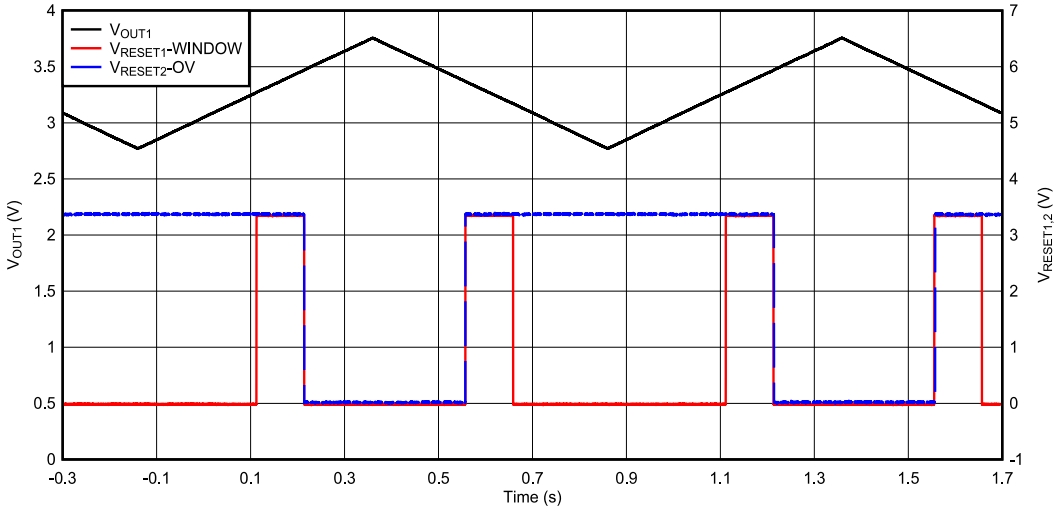


Figure 9-2. V_{OUT1}, $V_{\overline{RESET1}}$, and $V_{\overline{RESET2}}$ vs Time

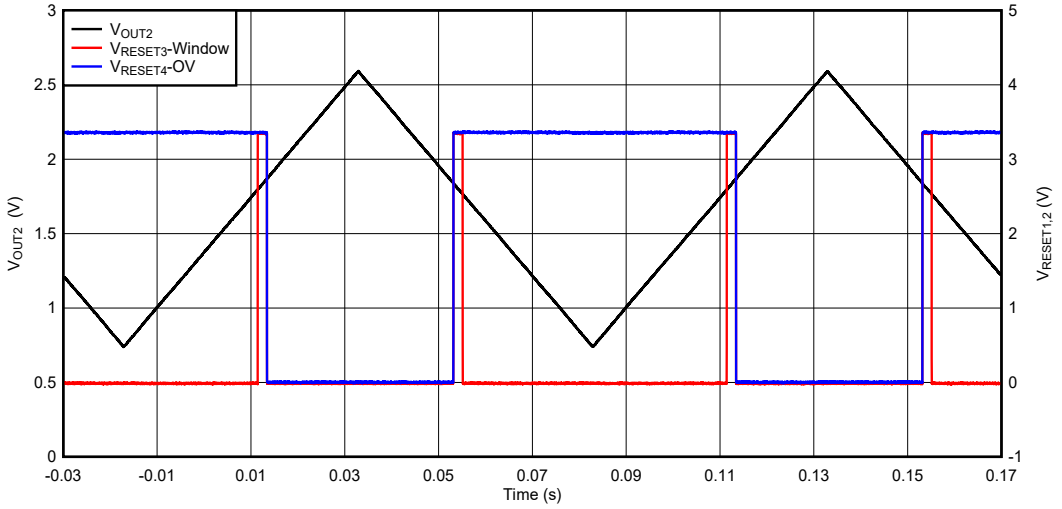


Figure 9-3. V_{OUT2}, $V_{\overline{RESET3}}$, and $V_{\overline{RESET4}}$ vs Time

9.3 Power Supply Recommendations

The TPS7H3024 is designed to operate from an input supply (V_{IN}) with a voltage range from 3V to 14V. V_{IN} needs to be decoupled with at least one 0.1µF ceramic capacitor from V_{IN} to GND, as close to the pin as possible

In the TPS7H3024 the PULL_UP1 and PULL_UP2 are also considered power inputs, in this case for the push-pull outputs. The voltage range on these inputs is from 1.6V to 7V. Connect at least one 1µF ceramic capacitor from PULL_UP1 to GND and from PULL_UP2 to GND. These capacitors must be placed as close to the pins as possible.

9.4 Layout

9.4.1 Layout Guidelines

- Connect a high quality ceramic capacitor (such as X7R) as close to the pins as possible. The signals and capacitor values are:
  - V_{IN} ≥ 0.1µF

  - REFCAP = 470nF
  - VLDO = 1µF
  - PULL_UPx ≥ 1µF
- Avoid passing noisy traces near the VLDO and REFCAP pins as the pins are internal references to the device.
- If needed, place a small capacitor between the SENSEx pins and GND to reduce the sensitivity to transient voltages on the monitored signal.
- As users typically use the supervisor in conjunction with switch mode power supplies, users must keep the SENSEx trace away from noisy sources as much as possible. Avoid routing this trace directly under the noise-source. If not possible, make sure that the trace is routed on another layer with a ground layer separating the trace and noise-source.

9.4.2 Layout Example

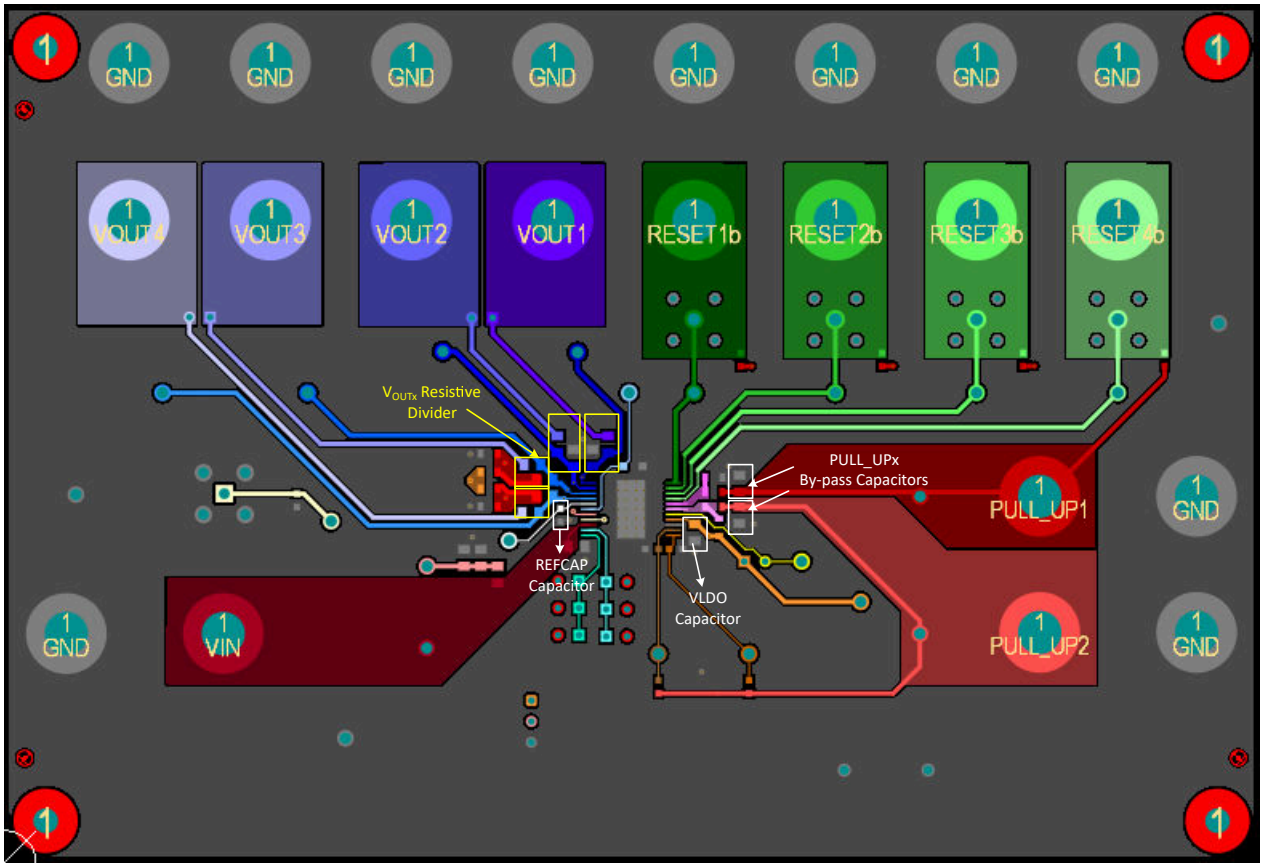


Figure 9-4. Printed Circuit Board Layout Example: Top Layer

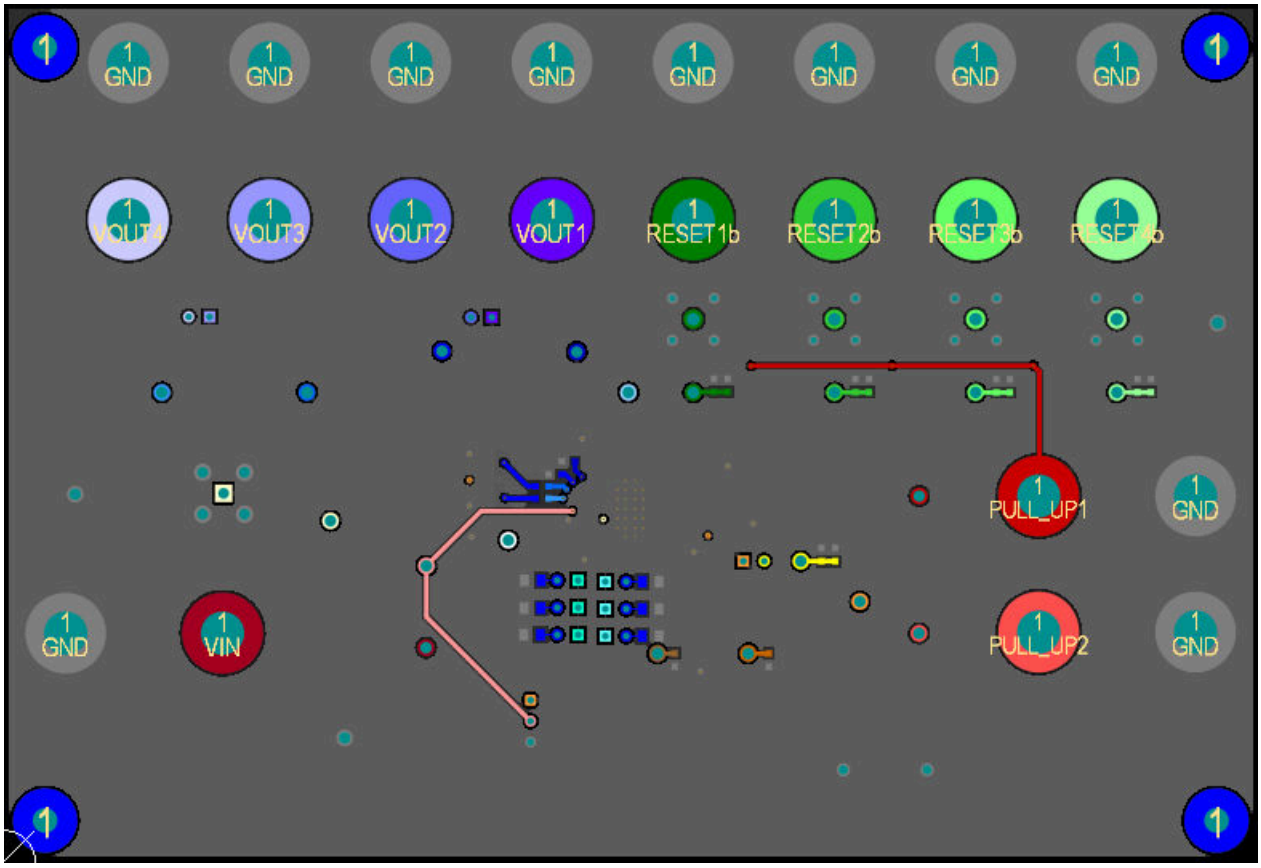


Figure 9-5. Printed Circuit Board Layout Example: Bottom Layer

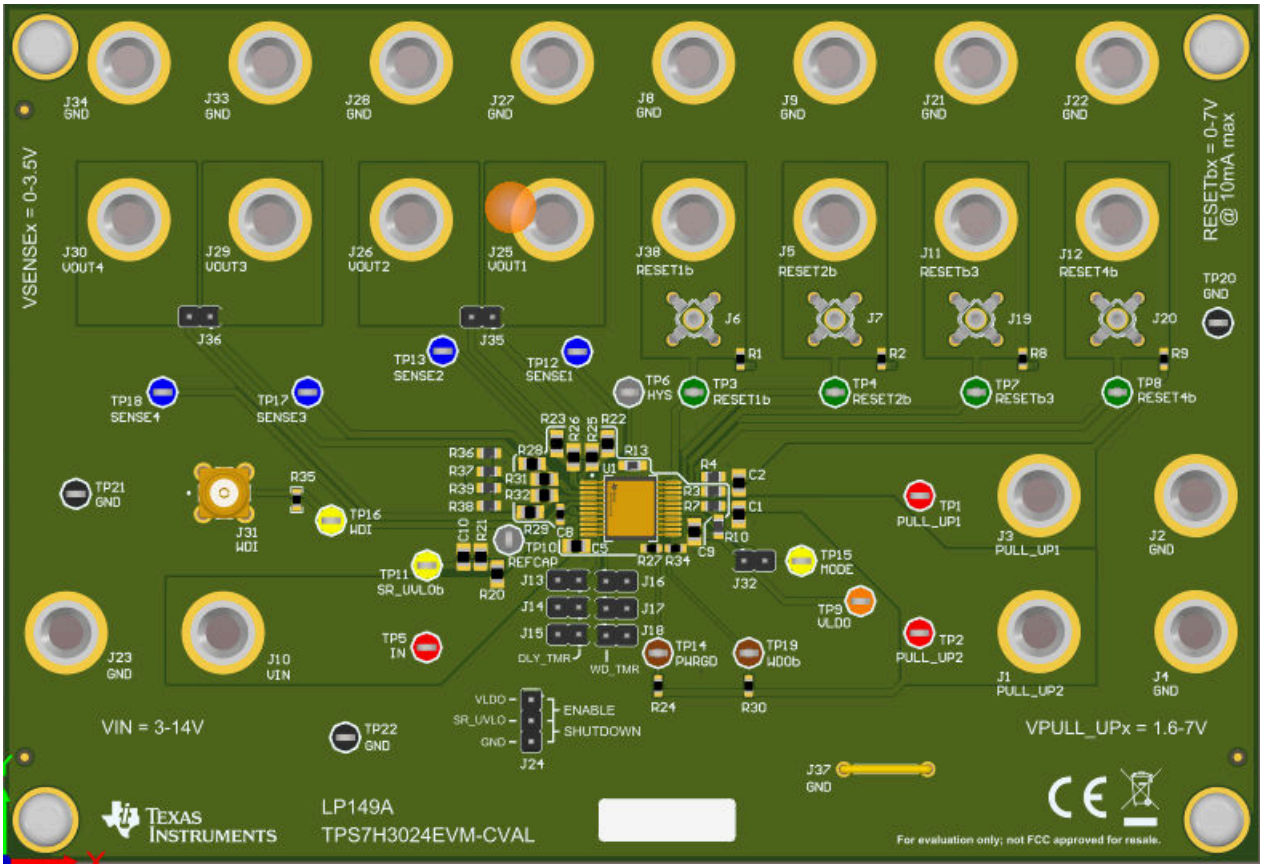


Figure 9-6. Printed Circuit Board Layout Example: Top Layer 3D View

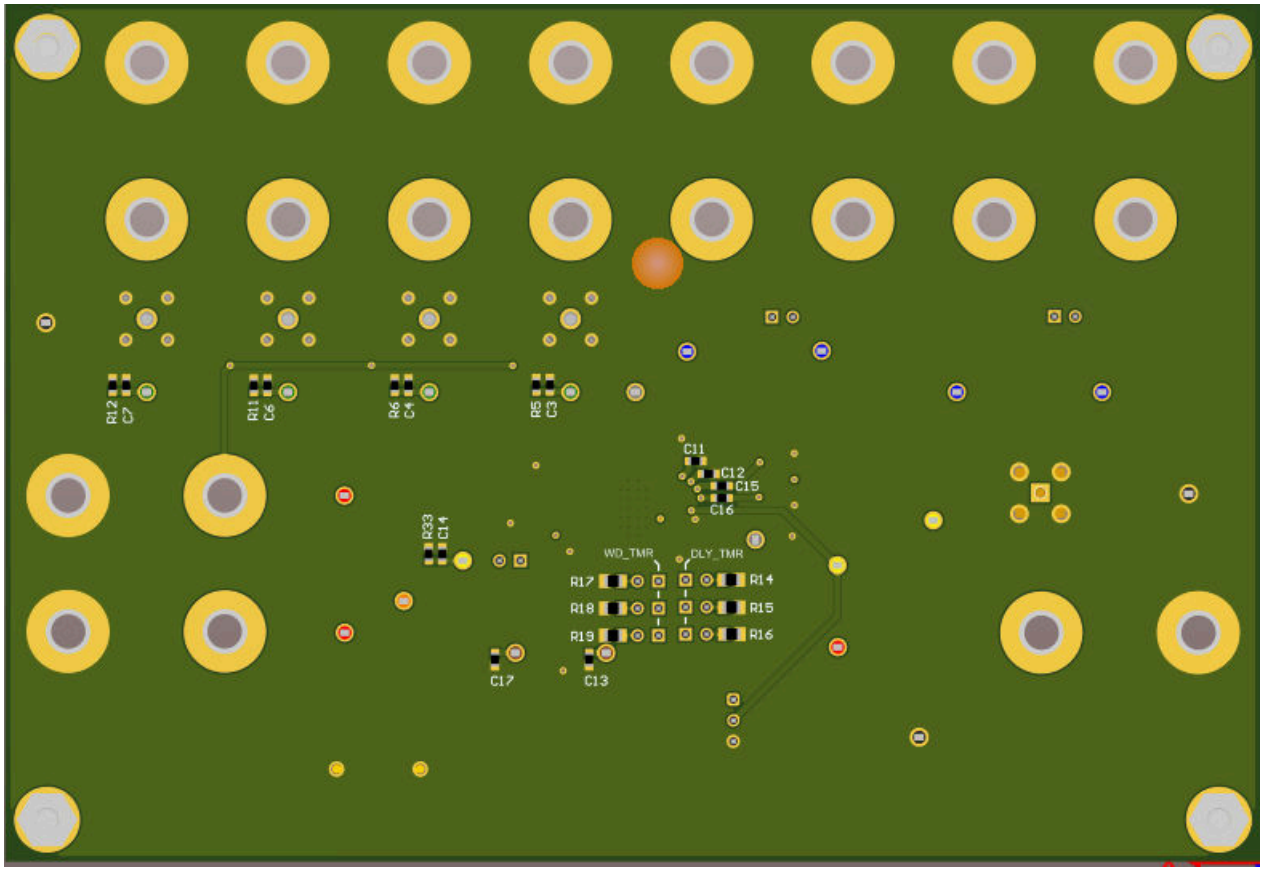


Figure 9-7. Printed Circuit Board Layout Example: Bottom Layer 3D View

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

The following related documents are available for download at www.ti.com:

- Texas Instruments, *Optimizing Resistor Dividers at a Comparator* application note
- Texas Instruments, *TPS7H3024EVM-CVAL Evaluation Module* user's guide
- Texas Instruments, *TPS7H3024-SP Neutron Displacement Damage (NDD) Characterization* radiation report
- Texas Instruments, *TPS7H3024-SP Single-Event Effects (SEE)* radiation report
- Texas Instruments, *TPS7H3024-SP Total Ionizing Dose (TID)* radiation report
- DLA Land and Marine, standard microcircuit drawing

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

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All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (August 2025) to Revision B (May 2026)	Page
• Added TPS7H3034-SP, TPS7H3124-SP, and TPS7H3134-SP QMLV as *Advanced Information* throughout	1
• Updated document to separate TPS7H30x4 and TPS7H31x4 throughout	1
• Added SENSE1, RESET1, and $\overline{\text{RESET1}}$ typical characteristics graphs	13
• Updated TPS7H3xx4 Functional Modes	30

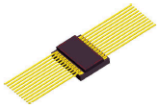
Changes from Revision * (April 2025) to Revision A (August 2025)	Page
• Changed TPS7H3024-SP QMLV from *Advanced Information* to *Production Data*	1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, refer to the left-hand navigation.

12.1 Mechanical Data

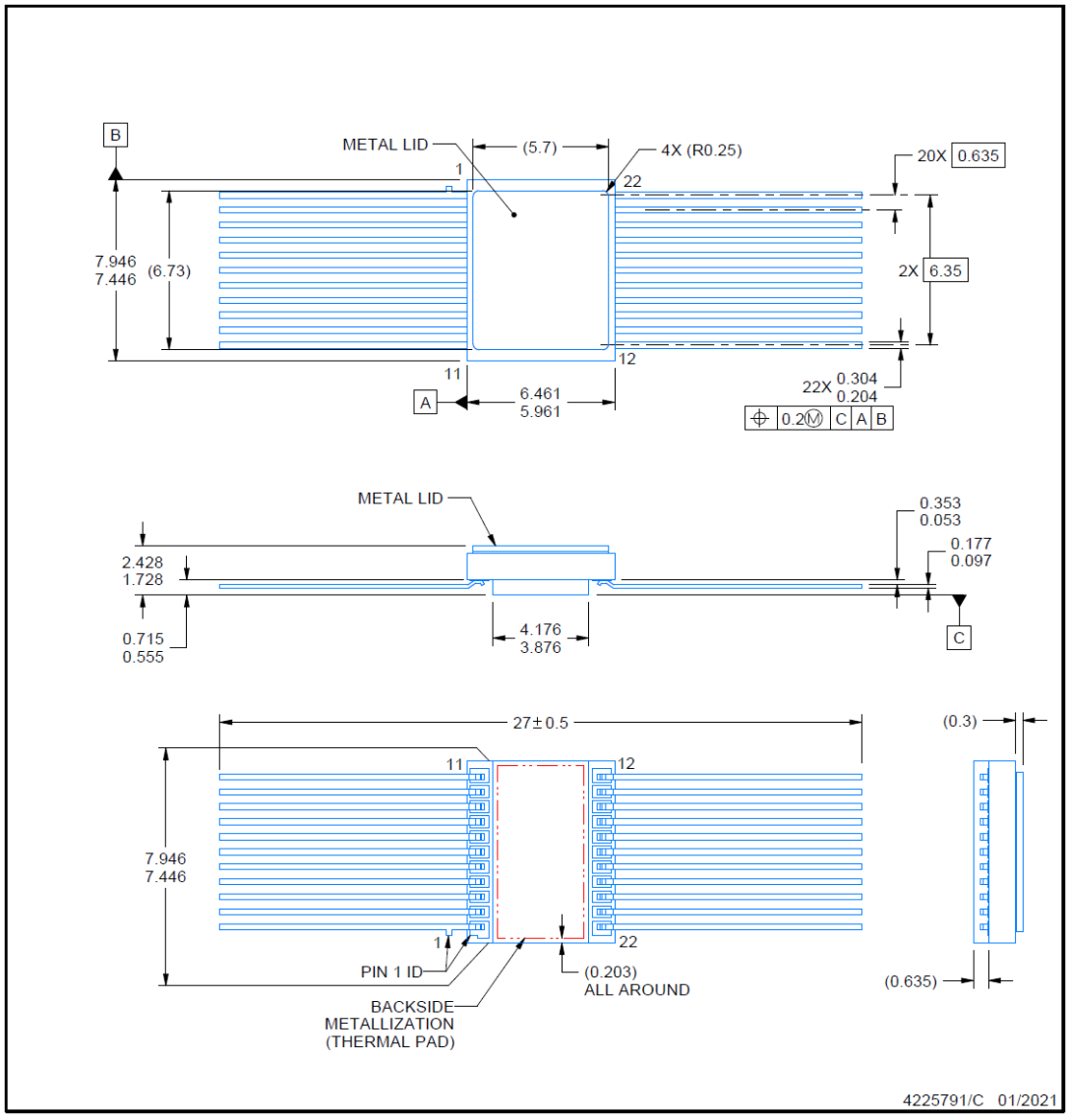
HFT0022A



PACKAGE OUTLINE

CFP - 2.428mm max height

CERAMIC FLATPACK



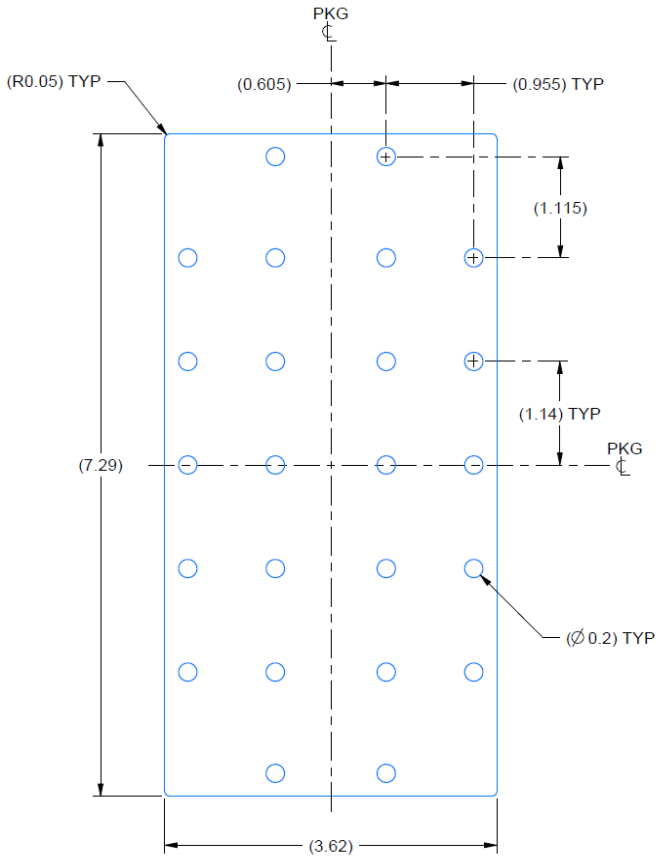
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid. The lid is not connected to any lead.
4. The leads are gold plated.
5. Metal lid is connected to backside metalization

EXAMPLE BOARD LAYOUT

HFT0022A — **CFP - 2.428mm max height**

CERAMIC FLATPACK



HEATSINK LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

4225791/C 01/2021

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962R2420601VXC	Active	Production	CFP (HFT) | 22	15 | TUBE	Yes	NIAU	N/A for Pkg Type	-55 to 125	5962R2420601VXC TPS7H3024MHFTV
TPS7H3024HFT/EM	Active	Production	CFP (HFT) | 22	15 | TUBE	Yes	NIAU	N/A for Pkg Type	25 to 25	TPS7H3024HFTEM EVAL ONLY

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

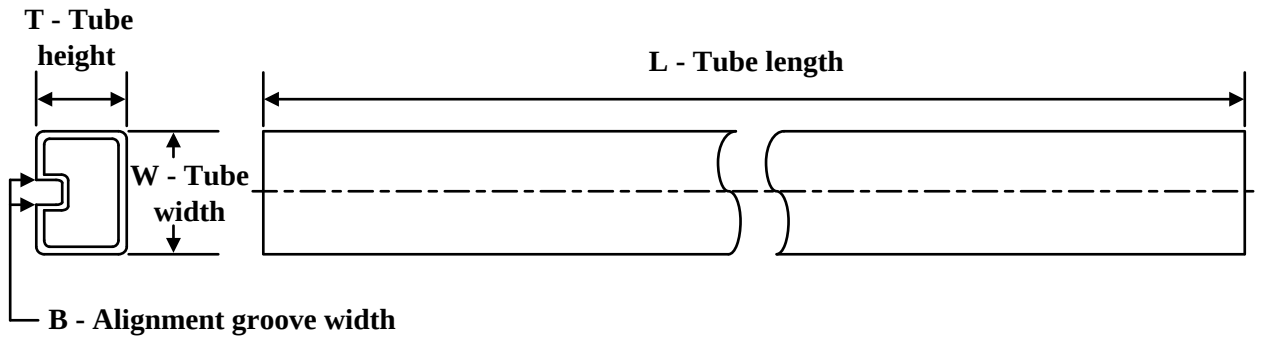
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TUBE



*All dimensions are nominal

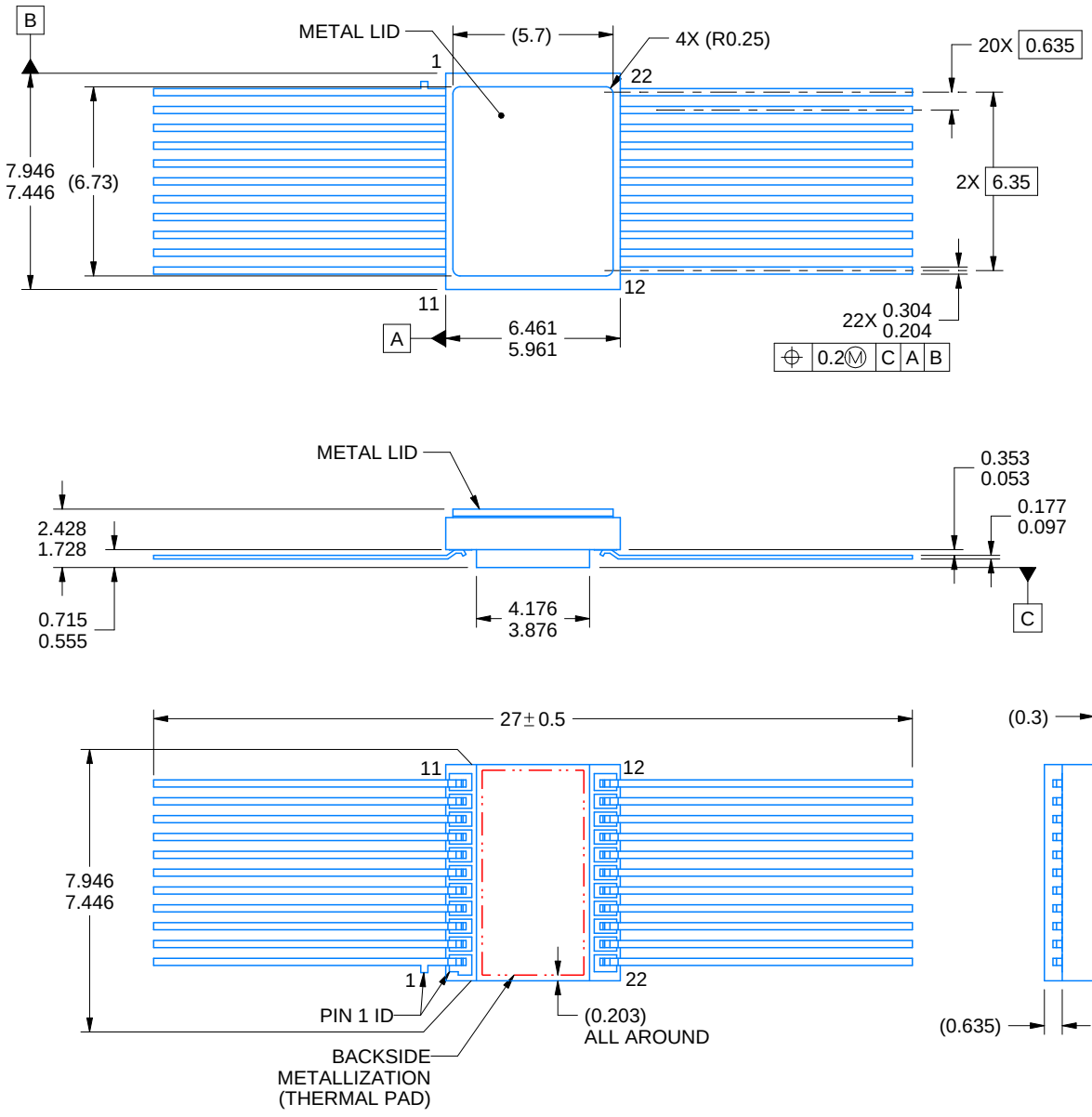
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962R2420601VXC	HFT	CFP	22	15	506.98	32.77	9910	NA
TPS7H3024HFT/EM	HFT	CFP	22	15	506.98	32.77	9910	NA

PACKAGE OUTLINE

HFT0022A

CFP - 2.428mm max height

CERAMIC FLATPACK



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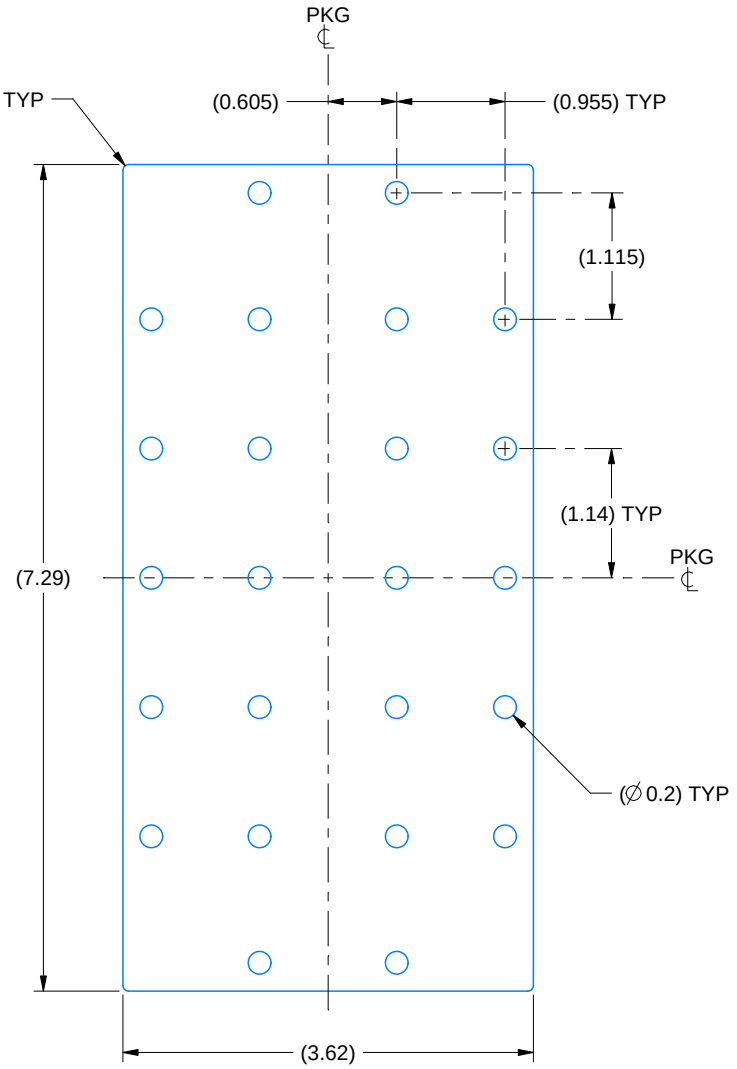

HEATSINK LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

4225791/C 01/2021

REVISIONS

REV	DESCRIPTION	ECR	DATE	ENGINEER / DRAFTER
A	RELEASE NEW DRAWING	2186323	03/13/2020	R. RAZAK / ANIS FAUZI
B	ADD LAND PATTERN VIEW / SHEET	2190485	10/22/2020	R. RAZAK / ANIS FAUZI
C	UPDATE TOTAL LEAD LENGTH TO 27± 0.5	2192775	01/28/2021	R. RAZAK / ANIS FAUZI

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Last updated 10/2025