TPS7N48 1.5A, Low-Dropout Linear Regulator With Programmable Soft-Start

1 Features

- V_{OUT} range: 0.5V to 3.6V
- Ultra-low V_{IN} range: 0.75V to 6.0V
- V_{BIAS} range: 2.7V to 6.0V
- Low dropout: 75mV typical at 1.5A, V_{BIAS} = 5V
- Power-good (PG) output allows supply monitoring or provides a sequencing signal for other supplies
- 2% accuracy
- Programmable soft-start provides linear voltage start-up
- V_{BIAS} permits low V_{IN} operation with good transient response
- Stable with any output capacitor ≥ 10µF
- Available in small, 2mm × 2mm × 0.8mm WSON-10 packages

2 Applications

- Network interface cards, smart NICs
- Routers, switches
- Ultrasound scanners
- MRI scanners

3 Description

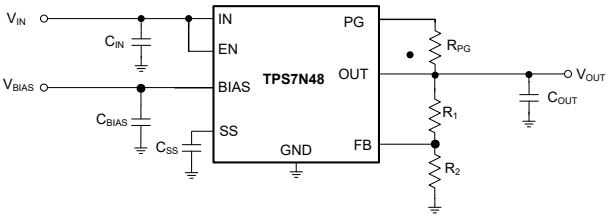
The TPS7N48 low-dropout (LDO) linear regulator provides an easy-to-use robust power-management design for a wide variety of applications. User-programmable soft-start minimizes stress on the input power source by reducing capacitive inrush current on start-up. Soft-start is monotonic and designed for powering many different types of processors and application-specific integrated circuits (ASICs). The enable input and power-good output allow easy sequencing with external regulators. This flexibility enables a design to be configured that meets the sequencing requirements of many applications. Field-programmable gate arrays (FPGAs), digital signal processors (DSPs), and other applications with special start-up requirements are some examples that benefit from this flexibility.

A precision reference and error amplifier deliver 2% accuracy. The device is stable with any type of capacitor greater than or equal to 10µF, and is fully specified for T_J = –40°C to +125°C. The TPS7N48 is offered in a small, 2mm × 2mm, WSON-10 package, yielding a highly compact total design size.

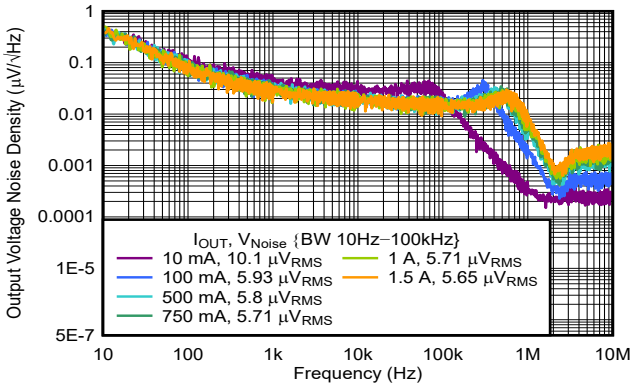
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS7N48	DSQ (WSON, 10)	2mm × 2mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Circuit



Output Voltage Noise Density vs Frequency

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4 Pin Configuration and Functions

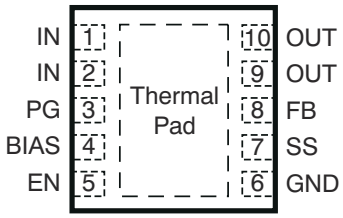


Figure 4-1. DSQ Package, 10-Pin WSON With Thermal Pad (Top View)

Table 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	VSON		
BIAS	4	I	Bias input voltage for error amplifier, reference, and internal control circuits. Use a 1µF or larger input capacitor for optimum performance. If IN is connected to BIAS, use a 4.7µF or larger capacitor.
EN	5	I	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode. Do not leave this pin unconnected.
FB	8	I	Feedback pin. This pin is the feedback connection to the center tap of an external resistor divider network that sets the output voltage. Do not leave this pin floating.
GND	6	—	Ground.
IN	1, 2	I	Input to the device. Use a 1µF or larger input capacitor for optimum performance.
OUT	9, 10	O	Regulated output voltage. A capacitor (≥ 10µF, ceramic) is needed from this pin to ground to provide stability.
PG	3	O	Power-good pin. An open-drain, active-high output that indicates the status of V_{OUT}. When V_{OUT} exceeds the PG trip threshold, the PG pin goes into a high-impedance state. When V_{OUT} is below this threshold the pin is driven to a low-impedance state. Connect a pullup resistor (10kΩ to 100kΩ) from this pin to a supply of up to 6.0V. A higher supply than the input voltage is permissible. Alternatively, leave the PG pin unconnected if output monitoring is not necessary.
SS	7	—	Soft-start pin. A capacitor connected on this pin to ground sets the start-up time. If this pin is left unconnected, the regulator output soft-start ramp time is typically 170µs.
Thermal pad		—	Solder the thermal pad to the ground plane for increased thermal performance. This pad is internally referenced to ground.

5 Specifications

5.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	IN, BIAS, EN, PG, SS	–0.3	6.5	V
	FB	–0.3	V_{BIAS}	
	OUT	–0.3	V_{IN} + 0.3(2)	
Current	PG	0	1.5	mA
	OUT	Internally limited		A
	Output short-circuit duration	Indefinite		
	Continuous total power dissipation, P_{DISS}	See *Thermal Information*		
Temperature	Junction, T_J	–40	150	°C
	Storage, T_{stg}	–55	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The absolute maximum rating is V_{IN} + 0.3V or 6V, whichever is smaller.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	0.75		6.0	V
V_{EN}	Enable supply voltage		V_{IN}	6.0	V
V_{BIAS}	BIAS supply voltage	V_{OUT} + V_{DO} (V_{BIAS})(1)	V_{OUT} + 1.6(1)	6.0	V
V_{OUT}	Output voltage	0.5		3.6	V
I_{OUT}	Output current	0		1.5	A
C_{OUT}	Output capacitor (3)	10			µF
C_{IN}	Input capacitor (2)	1	10		µF
C_{BIAS}	Bias capacitor (2)	0.1	1		µF
R_{PG}	Power-good pull-up resistance	10		100	kΩ
C_{SS}	Soft-start capacitor	1	10	100	nF
T_J	Operating junction temperature	–40		125	°C

(1) V_{BIAS} has a minimum voltage of 2.7 V or V_{OUT} + V_{DO} (V_{BIAS}), whichever is higher.
(2) If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for the supply is 4.7 µF.
(3) A maximum capacitor derating of 50% is considered for minimum capacitance.

5.4 Thermal Information

THERMAL METRIC(1)		TPS7N48 DSQ (WSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	62.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	89.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	28.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	28.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.4	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

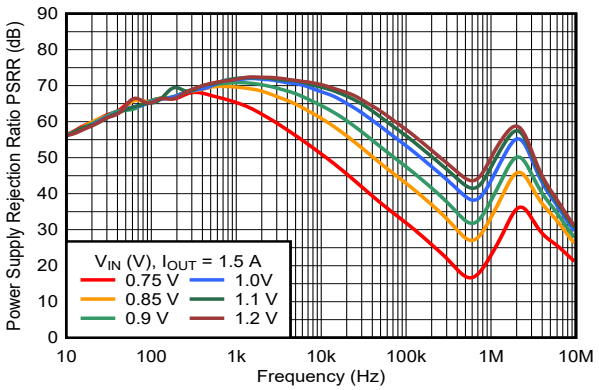
at V_{EN} = 1.1V, V_{IN} = V_{OUT} + 0.25V, C_{BIAS} = 0.1µF, C_{IN} = C_{OUT} = 10µF, C_{SS} = 1nF, I_{OUT} = 50mA, V_{BIAS} = 5.5V (2), and T_J = –40°C to 125°C (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	Internal reference (Adj.)			0.5		V
$V_{BIAS(UVLO)}$	Rising bias supply UVLO		1.0	1.25	1.75	V
$V_{BIAS(UVLO),HYST}$	Bias supply UVLO hysteresis			43		mV
	Accuracy (1) (3)	V_{BIAS} = 5.5V, 50mA ≤ I_{OUT} ≤ 1.5A	–2	±0.8	2	%
ΔV_{OUT} (ΔIOUT)	Line regulation	$V_{OUT(nom)}$ + 0.25V ≤ V_{IN} ≤ 5.5V		0.03		%/V
V_{OUT}	Load regulation	50mA ≤ I_{OUT} ≤ 1.5A		0.09		%/A
$V_{DO(IN)}$	V_{IN} dropout voltage	V_{FB} = 0.97xV_{REF}, 0.75V ≤V_{IN}≤ 3.6V, I_{OUT} = 1.5A		95	150	mV
$V_{DO(BIAS)}$	V_{BIAS} dropout voltage	V_{FB} = 0.97xV_{REF}, I_{OUT} = 1.5A, V_{IN} = V_{BIAS} = 2.7V		1.16	1.35	V
I_{CL}	Output current limit	V_{OUT} = 80% × $V_{OUT(nom)}$, $V_{IN(nom)}$ = $V_{OUT(nom)}$ + 0.5V	2.3		3.1	A
I_{BIAS}	BIAS pin current	I_{OUT} = 0mA		0.04	0.1	mA
		I_{OUT} = 50mA		0.67	1.1	
I_{SHDN}	Shutdown supply current (I_{GND})	V_{EN} ≤ 0.4V, V_{OUT} = 0.5V		0.9	10	µA
I_{FB}	Feedback pin current		–0.3	±0.12	0.3	µA
PSRR	Power-supply rejection ratio (V_{IN} to V_{OUT})	1kHz, I_{OUT} = 1.5A, V_{IN} = 1.1V, V_{OUT} = 0.5V		72		dB
		300kHz, I_{OUT} = 1.5A, V_{IN} = 1.1V, V_{OUT} = 0.5V		46		
	Power-supply rejection ratio (V_{BIAS} to V_{OUT})	1kHz, I_{OUT} = 1.5A, V_{IN} = 1.1V, V_{OUT} = 0.5V		64		
		300kHz, I_{OUT} = 1.5A, V_{IN} = 1.1V, V_{OUT} = 0.5V		33		
V_n	Output noise voltage	BW = 10Hz to 100kHz, I_{OUT} = 1.5A		5.8		µVrms x V_{OUT}
t_{STR}	Minimum start-up time	From when EN is high and 98% of $V_{OUT(NOM)}$, I_{OUT} = 1.0A, C_{SS} = open		170		µs
I_{SS}	Soft-start charging current	V_{SS} = 0.4V		7.5		µA
t_{SS}	Soft-start time	Css = 10nF		0.9		ms
$V_{EN(hi)}$	Enable input high level		1.1		5.5	V
$V_{EN(lo)}$	Enable input low level		0		0.4	V
$V_{EN(hys)}$	Enable pin hysteresis			55		mV
$V_{EN(dg)}$	Enable pin deglitch time			17		µs
I_{EN}	Enable pin current	V_{EN} = 5V		0.1	0.5	µA
V_{IT}	PG trip threshold	V_{OUT} decreasing	85	90	94	%V_{OUT}
V_{HYS}	PG trip hysteresis			2.5		%V_{OUT}
$V_{PG(lo)}$	PG output low voltage	I_{PG} = 1mA (sinking), V_{OUT} < V_{IT}			0.125	V
$I_{PG(lkg)}$	PG leakage current	V_{PG} = 5.25V, V_{OUT} > V_{IT}		0.01	0.1	µA
T_J	Operating junction temperature		–40		125	℃
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		165		℃
		Reset, temperature decreasing		140		

(1) Devices tested at 0.5V; resistor tolerance is not taken into account.
(2) V_{BIAS} = $V_{DO\_MAX(BIAS)}$ + V_{OUT} for V_{OUT} ≥ 3.4V.
(3) The device is not tested under conditions where V_{IN} > V_{OUT} + 1.65V and I_{OUT} = 1.5A, because the power dissipation is higher than the maximum rating of the package. Also, this accuracy specification does not apply on any application condition that exceeds the power dissipation limit of the package under test.

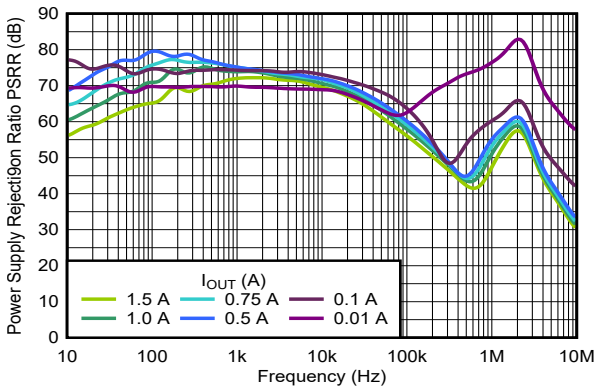
5.6 Typical Characteristics

at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.25V, V_{BIAS} = 5V, I_{OUT} = 50mA, V_{EN} = V_{IN}, C_{IN} = 1µF, C_{SS}= 1nF, C_{BIAS} = 1µF, and C_{OUT} = 10µF (unless otherwise noted)



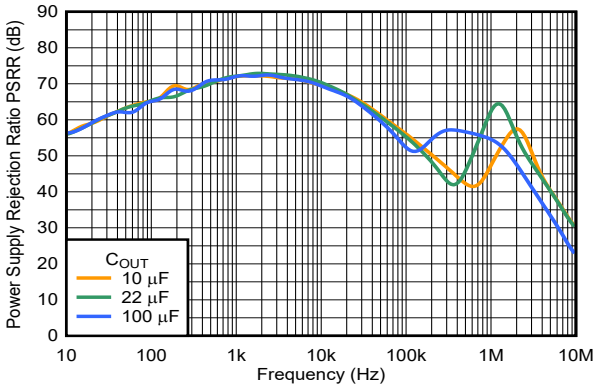
V_{OUT} = 0.5V, I_{OUT} = 1.5A, C_{BIAS} = 0.1µF, C_{OUT} = 10µF, V_{EN} = V_{BIAS} = 6V

Figure 5-1. IN PSRR vs Frequency and V_{IN}



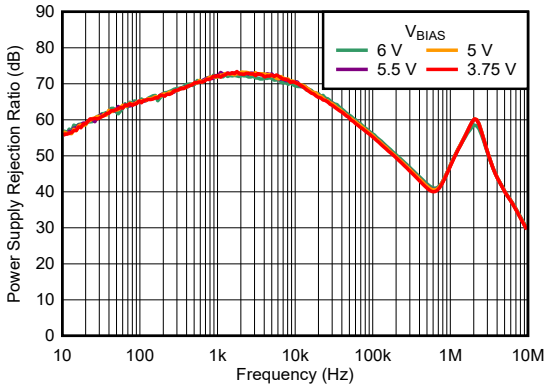
V_{IN} = 1.1V, V_{OUT} = 0.5V, C_{BIAS} = 0.1µF, C_{OUT} = 10µF, V_{EN} = V_{BIAS} = 6V

Figure 5-2. IN PSRR vs Frequency and I_{OUT} for V_{OUT} = 0.5V



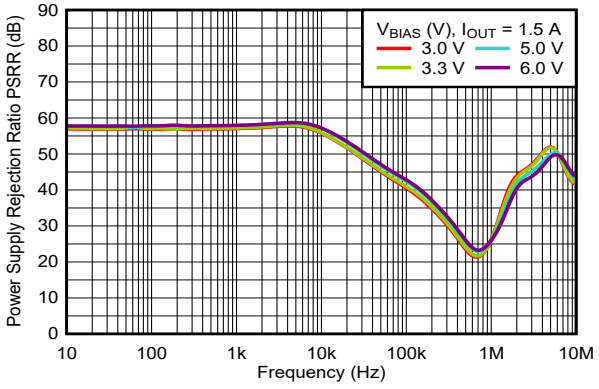
V_{IN} = 1.1V, V_{OUT} = 0.5V, I_{OUT} = 1.5A, C_{BIAS} = 0.1µF, V_{EN} = V_{BIAS} = 6V

Figure 5-3. IN PSRR vs Frequency and C_{OUT}



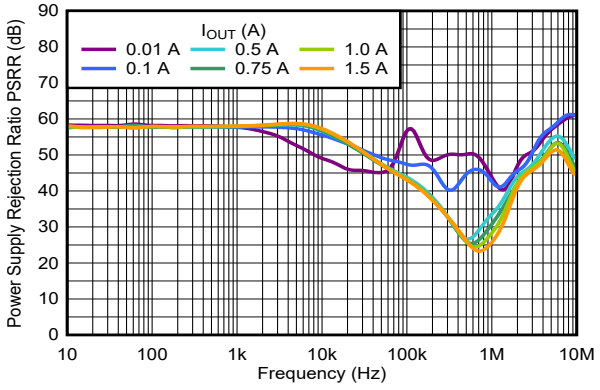
V_{IN} = 1.1V, V_{OUT} = 0.5V, I_{OUT} = 1.5A, C_{OUT} = 10µF, V_{EN} = 6V

Figure 5-4. IN PSRR vs Frequency and V_{BIAS}



V_{IN} = 1.1V, V_{OUT} = 0.5V, I_{OUT} = 1.5A, C_{IN} = 10µF, C_{OUT} = 10µF, V_{EN} = 6V

Figure 5-5. BIAS PSRR vs Frequency and V_{BIAS}

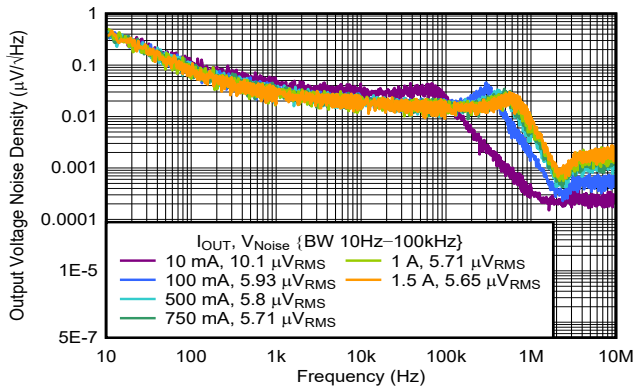


V_{EN} = V_{IN} = 1.1V, V_{OUT} = 0.5V, I_{OUT} = 1.5A, C_{IN} = 10µF, C_{OUT} = 10µF, V_{BIAS} = 6V

Figure 5-6. BIAS PSRR vs Frequency and I_{OUT}

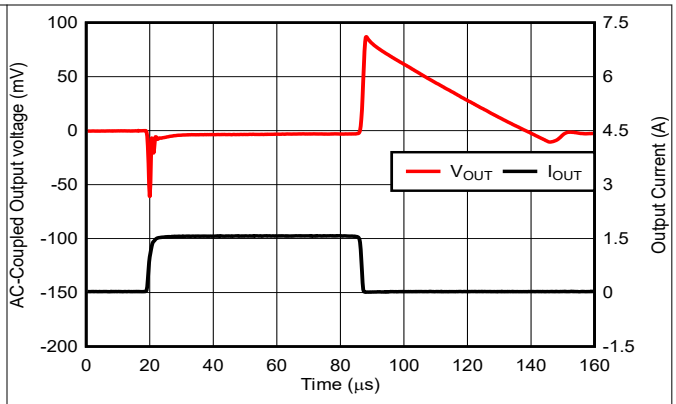
5.6 Typical Characteristics (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.25V, V_{BIAS} = 5V, I_{OUT} = 50mA, V_{EN} = V_{IN}, C_{IN} = 1µF, C_{SS}= 1nF, C_{BIAS} = 1µF, and C_{OUT} = 10µF (unless otherwise noted)



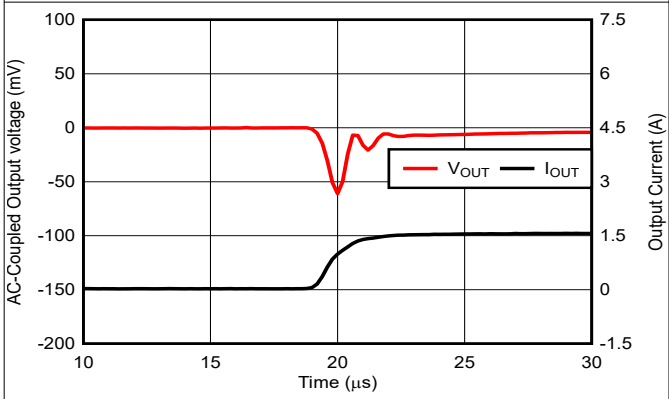
V_{EN} = V_{BIAS}, V_{IN} = 1.1V, V_{OUT} = 0.5V, C_{IN} = 10µF, C_{OUT} = 10µF, C_{BIAS} = 0.1µF

Figure 5-7. Output Voltage Noise Density vs Frequency and I_{OUT}



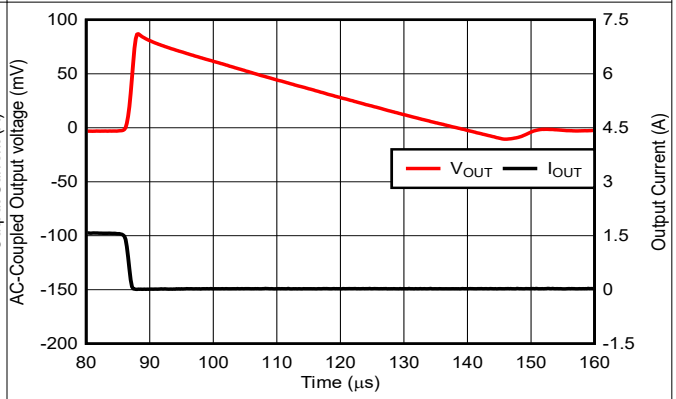
V_{IN} = 0.75V, V_{OUT} = 0.5V, C_{IN} = 10µF, V_{EN} = V_{BIAS}, slew rate = 1A/µs

Figure 5-8. Load Transient 10mA to 1.5A



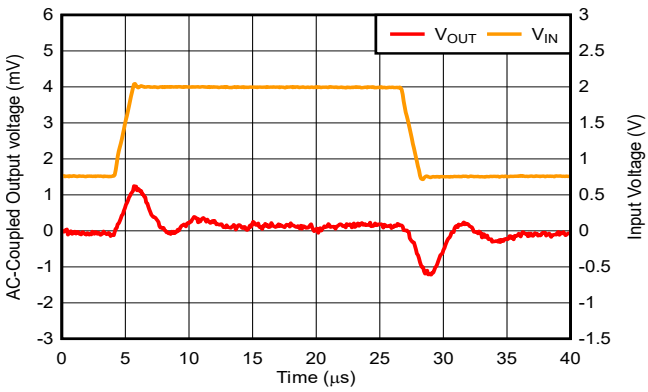
V_{IN} = 0.75V, V_{OUT} = 0.5V, C_{IN} = 10µF, V_{EN} = V_{BIAS}, slew rate = 1A/µs

Figure 5-9. Load Transient 10mA to 1.5A (Rising Edge)



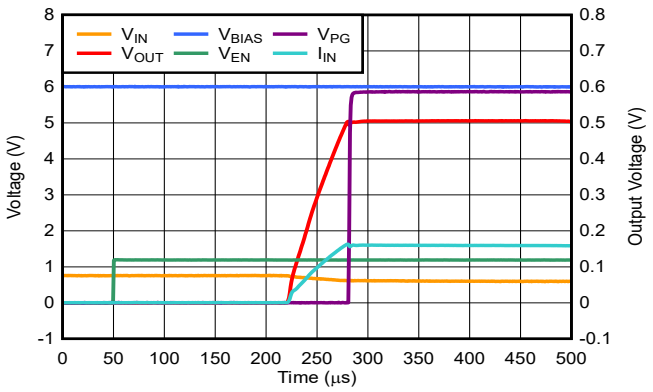
V_{IN} = 0.75V, V_{OUT} = 0.5V, C_{IN} = 10µF, V_{EN} = V_{BIAS}, slew rate = 1A/µs

Figure 5-10. Load Transient 1.5A to 10mA (Falling Edge)



V_{OUT} = 0.5V, V_{EN} = V_{BIAS} slew rate = 1V/µs

Figure 5-11. Line Transient

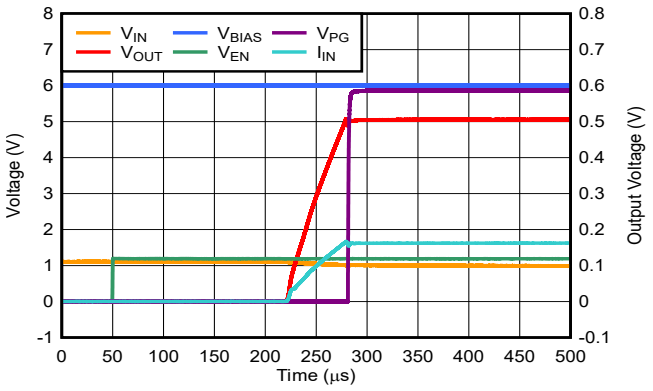


V_{IN} = 0.75V, V_{OUT} = 0.5V, V_{BIAS} = 5.0V, I_{OUT} = 1.5A, C_{OUT} = 10µF, C_{SS} = 1nF, I_{IN} is scaled down by a factor of 10

Figure 5-12. Start-Up With C_{SS} = 1nF

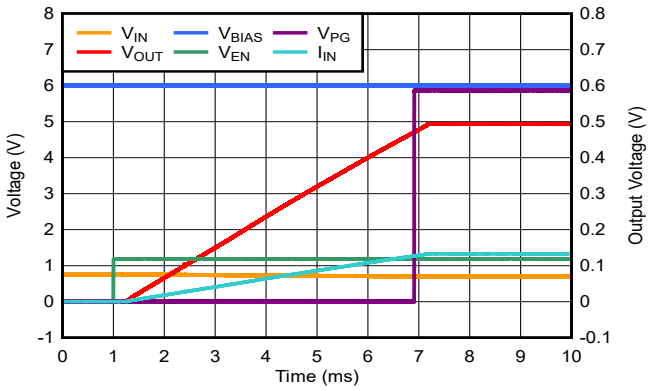
5.6 Typical Characteristics (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.25V, V_{BIAS} = 5V, I_{OUT} = 50mA, V_{EN} = V_{IN}, C_{IN} = 1µF, C_{SS}= 1nF, C_{BIAS} = 1µF, and C_{OUT} = 10µF (unless otherwise noted)



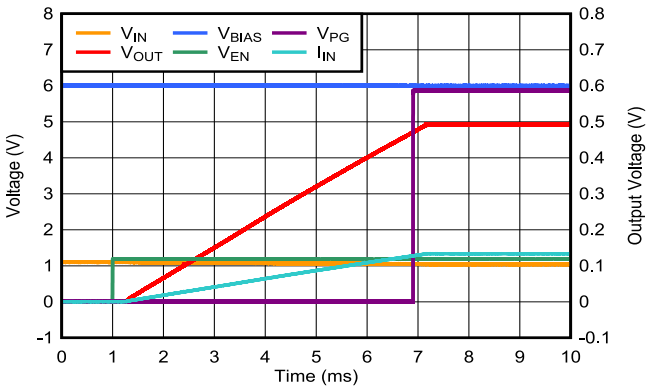
V_{IN} = 1.1V, V_{OUT} = 0.5V, V_{BIAS} = 5.0V, I_{OUT} = 1.5A, C_{OUT} = 10µF, C_{SS} = 1nF, I_{IN} is scaled down by a factor of 10

Figure 5-13. Start-Up With C_{SS} = 1nF



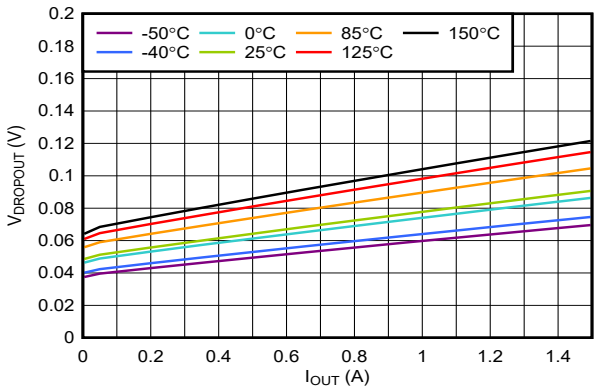
V_{IN} = 0.75V, V_{OUT} = 0.5V, V_{BIAS} = 5.0V, I_{OUT} = 1.5A, C_{OUT} = 10µF, C_{SS} = 100nF, I_{IN} is scaled down by a factor of 10

Figure 5-14. Start-Up With C_{SS} = 100nF



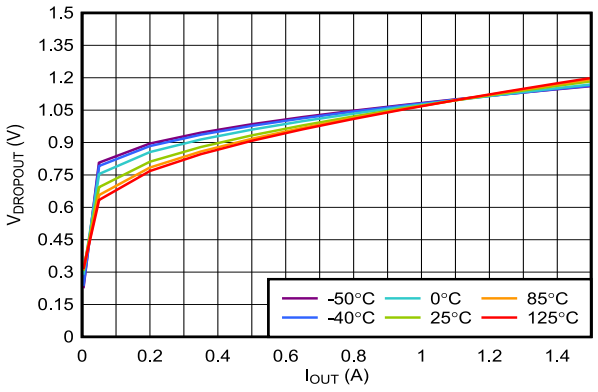
V_{IN} = 1.1V, V_{OUT} = 0.5V, V_{BIAS} = 5.0V, I_{OUT} = 1.5A, C_{OUT} = 10µF, C_{SS} = 100nF, I_{IN} is scaled down by a factor of 10

Figure 5-15. Start-Up With C_{SS} = 100nF



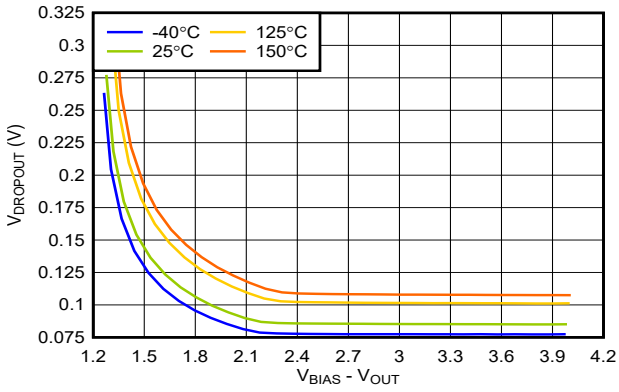
V_{BIAS} = 5V, V_{OUT} = 0.5V

Figure 5-16. IN-to-OUT Dropout Voltage vs I_{OUT} and Temperature (T_J)



V_{IN} = 1.1V, V_{OUT} = 0.5V

Figure 5-17. BIAS-to-OUT Dropout Voltage vs I_{OUT} and Temperature (T_J)

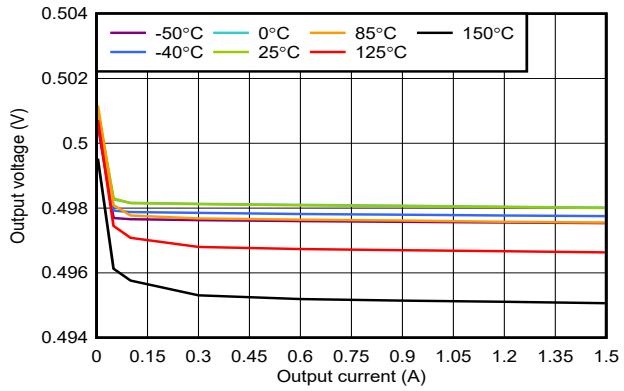


V_{OUT} = 0.5V, I_{OUT} = 1.5A

Figure 5-18. Dropout Voltage vs V_{BIAS}- V_{OUT} and Temperature (T_J)

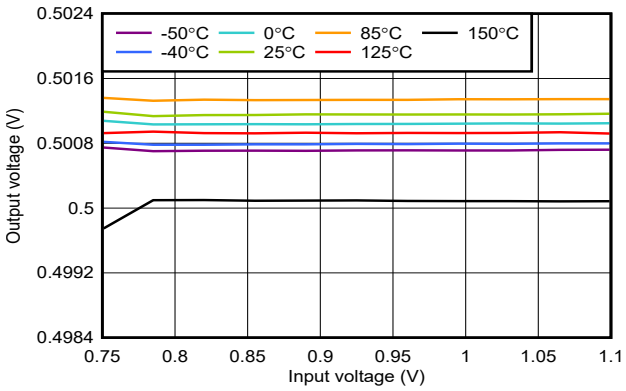
5.6 Typical Characteristics (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.25V, V_{BIAS} = 5V, I_{OUT} = 50mA, V_{EN} = V_{IN}, C_{IN} = 1µF, C_{SS}= 1nF, C_{BIAS} = 1µF, and C_{OUT} = 10µF (unless otherwise noted)



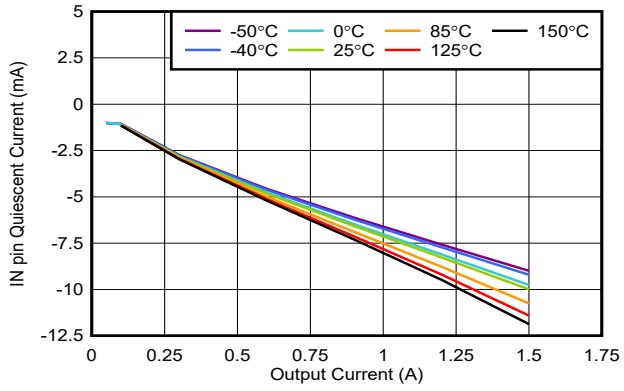
V_{IN} = 1.1V, V_{BIAS} = 5V, V_{OUT} = 0.5V

Figure 5-19. Load Regulation vs Output Current



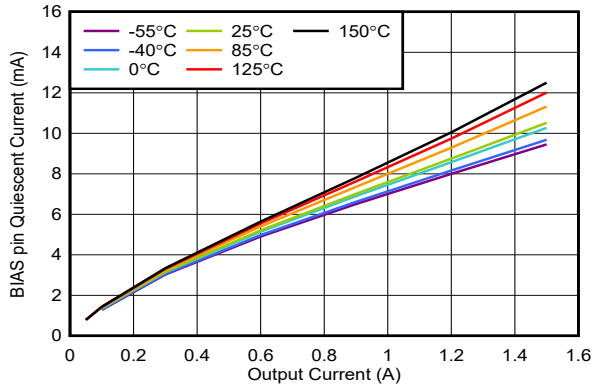
V_{OUT} = 0.5V, V_{BIAS} = 5V, I_{OUT} = 1mA

Figure 5-20. Line Regulation vs Input Voltage



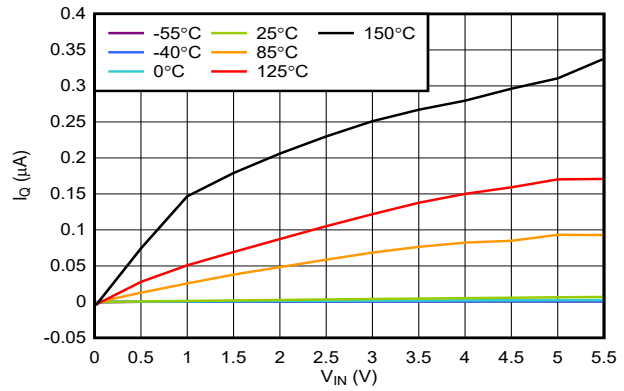
V_{OUT} = 0.5V, V_{BIAS} = 5.0V

Figure 5-21. IN Pin Quiescent Current vs Output Current



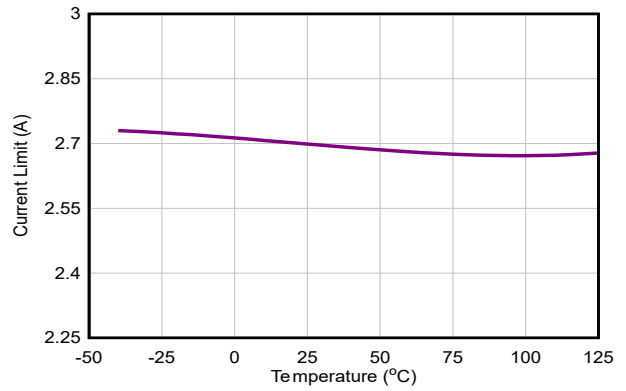
V_{IN} = 1.1V, V_{OUT} = 0.5V, V_{BIAS} = 5.0V

Figure 5-22. BIAS Pin Quiescent Current vs Output Current



V_{BIAS} = 5V, V_{EN} ≤ 0.4V

Figure 5-23. Shutdown Current (GND Pin) vs Input Voltage



V_{IN} = $V_{OUT(NOM)}$ +0.5V

Figure 5-24. Current Limit vs Temperature

6 Detailed Description

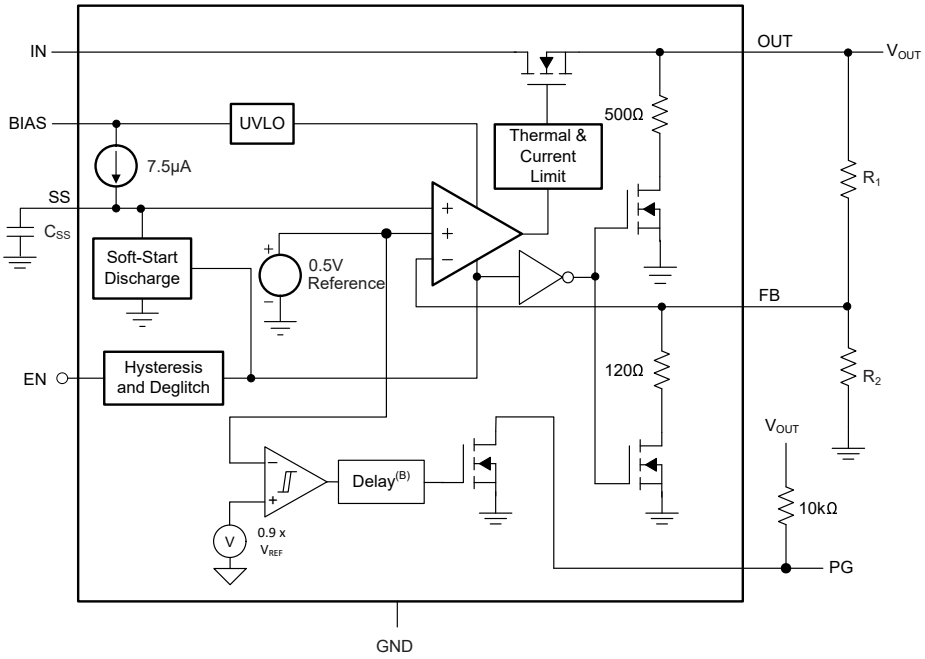
6.1 Overview

The TPS7N48 is a low-input, low-output (LILO), low-quiescent-current linear regulator optimized to support excellent transient performance. This regulator uses a low-current bias rail to power all internal control circuitry. Thus allowing the n-type field effect transistor (NMOS) pass transistor to regulate very-low input and output voltages.

Using an NMOS-pass transistor offers several critical advantages for many applications. Unlike a p-channel metal-oxide-semiconductor field effect transistor (PMOS) topology device, the output capacitor has little effect on loop stability. This architecture allows the TPS7N48 to be stable with ceramic capacitors of 10µF or greater. Transient response is also better than in PMOS topologies, particularly for low V_{IN} applications.

The TPS7N48 features a programmable, voltage-controlled, soft-start circuit that provides a smooth, monotonic start-up and limits start-up inrush currents caused by large capacitive loads. An enable (EN) pin with hysteresis and deglitch allows slow-ramping signals to be used for sequencing the device. The low V_{IN} and V_{OUT} capability allows for inexpensive, easy-to-design, and efficient linear regulation between the multiple supply voltages often required by processor-intensive systems.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Enable and Shutdown

The enable (EN) pin is active high and compatible with standard digital-signaling levels. Setting V_{EN} below 0.4V turns the regulator off, and setting V_{EN} above 1.1V turns the regulator on. Unlike many regulators, the enable circuitry has hysteresis and deglitching for use with relatively slowly ramping analog signals. This configuration allows the device to be enabled by connecting the output of another supply to the EN pin. The enable circuitry typically has 55mV of hysteresis and a deglitch circuit to help avoid on-off cycling resulting from small glitches in the V_{EN} signal.

The enable threshold varies with temperature and process variations. Temperature variation is approximately –1.2mV/°C; process variation accounts for most of the remaining variation to the 0.4V and 1.1V limits. If precise turn-on timing is required, use a fast rise-time signal.

If not used, connect EN to BIAS. Place the connection as close as possible to the bias capacitor.

6.3.2 Active Discharge

The TPS7N48 has an internal active pulldown circuits on the OUT pin.

Each active discharge function uses an internal metal-oxide-semiconductor field-effect transistor (MOSFET). The MOSFET connects a resistor ($R_{PULLDOWN}$) to ground when the low-dropout resistor (LDO) is disabled to actively discharge the output voltage. The active discharge circuit is activated when the device is disabled by driving EN to logic low. The circuit is also activated when the voltage at IN or BIAS is below the UVLO threshold, or when the regulator is in thermal shutdown.

The discharge time after disabling the device depends on the output capacitance (C_{OUT}) and the load resistance (R_L) in parallel with the pulldown resistor.

The first active pulldown circuit connects the output to GND through a 500Ω resistor when the device is disabled.

The second circuit connects FB to GND through a 120Ω resistor when the device is disabled. This resistor discharges the FB pin. Equation 1 calculates the output capacitor discharge time constant when OUT is shorted to FB, or when the output voltage is set to 0.5V.

$$\tau_{OUT} = (500 \,||\, 120 \times R_L / (500 \,||\, 120 + R_L) \times C_{OUT} \quad (1)$$

If the LDO is set to an output voltage greater than 0.5V, a resistor divider network is in place and minimizes the FB pin pulldown. Equation 2 and Equation 3 calculate the time constants set by these discharge resistors.

$$R_{DISCHARGE} = (120 \,||\, R_2) + R_1 \quad (2)$$

$$\tau_{OUT} = R_{DISCHARGE} \times R_L / (R_{DISCHARGE} + R_L) \times C_{OUT} \quad (3)$$

Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply collapses. Reverse current potentially flows from the output to the input and causes damage to the device. Limit reverse current to no more than 5% of the device-rated current.

6.3.3 Power-Good Output (PG)

The PG signal provides an easy way to meet demanding sequencing requirements because PG signals when the output nears the nominal value. PG signals other devices in a system when the output voltage is near, at, or above the set output voltage ($V_{OUT(nom)}$). Figure 6-1 shows a simplified schematic.

The PG signal is an open-drain digital output that requires a pullup resistor to a voltage source and is active high. The PG circuit sets the PG pin into a high-impedance state to indicate that the power is good.

Using a large feed-forward capacitor (C_{FF}) delays the output voltage. Because the PG circuit monitors the FB pin, the PG signal indicates a false positive.

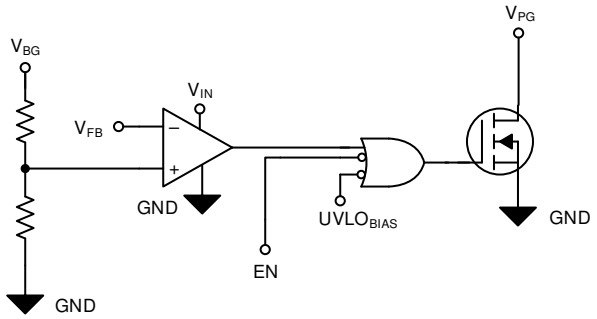


Figure 6-1. Simplified PG Circuit

6.3.4 Internal Current Limit

The fixed internal current limit of the TPS7N48 helps protect the regulator during fault conditions. The current limit is a brick-wall scheme. The maximum amount of current the device sources is the current limit (3.1A, max), and is largely independent of output voltage. For reliable operation, do not operate the device in current limit for extended periods of time.

The output voltage is not regulated when the device is in current limit. When a current-limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in a brick-wall current limit, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{CL}]. If thermal shutdown is triggered, the device turns off. When the device sufficiently cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note.

6.3.5 Thermal Shutdown Protection (T_{SD})

The internal thermal shutdown protection circuit disables the output when the pass transistor T_J reaches $T_{SD(shutdown)\ (typical)}$. T_J is the thermal junction temperature and $T_{SD(shutdown)\ (typical)}$ is the thermal shutdown temperature threshold. The thermal shutdown circuit hysteresis verifies the LDO resets (turns on) when the temperature falls to $T_{SD(reset)\ (typical)}$.

The thermal time constant of the semiconductor die is fairly short. Thus, the device cycles on and off when thermal shutdown is reached until the power dissipation is reduced. Power dissipation during start-up is high from large V_{IN} – V_{OUT} voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start-up completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the internal protection circuitry is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the regulator into thermal shutdown, or above the maximum recommended junction temperature, reduces long-term reliability.

6.4 Device Functional Modes

Table 6-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

Table 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER				
	V_{IN}	V_{BIAS}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} \geq V_{OUT\ (nom)} + V_{DO(IN)}$ and $V_{IN} \geq V_{IN(min)}$	$V_{BIAS} \geq V_{OUT} + V_{DO(BIAS)}$	$V_{EN} \geq V_{HI(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$ for shutdown
Dropout mode	$V_{IN(min)} < V_{IN} < V_{OUT\ (nom)} + V_{DO(IN)}$	$V_{BIAS} < V_{OUT} + V_{DO(BIAS)}$	$V_{EN} > V_{HI(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$ for shutdown
Disabled mode (any true condition disables the device)	$V_{IN} < V_{UVLO(IN)}$	$V_{BIAS} < V_{BIAS(UVLO)}$	$V_{EN} < V_{LO(EN)}$	—	$T_J \geq T_{SD}$ for shutdown

6.4.1 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO(IN)}$)
- The bias voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO(BIAS)}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD(shutdown)}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, the device operates in dropout mode. However, verify all other conditions are met for normal operation. Similarly, if the bias voltage is lower than the nominal output voltage plus the specified dropout voltage, the device operates in dropout mode as well. Again, verify all other conditions are met for normal operation. In this mode, the output voltage tracks the input voltage. During this mode, the device transient performance becomes significantly degraded because the pass transistor is in the ohmic or triode region. Therefore, during this mode, the device transient functions as a switch. Line or load transients in dropout result in large output voltage deviations.

When the device is in a steady dropout state, the pass transistor is driven into the ohmic or triode region. This state is defined as when the device is in dropout, directly after being in normal regulation state, but not during start-up. During dropout, $V_{IN} < V_{OUT} + V_{DO(IN)}$ or $V_{BIAS} < V_{OUT} + V_{DO(BIAS)}$. When the input voltage returns to a value $\geq V_{OUT(NOM)} + V_{DO(IN)}$, the output voltage overshoots for a short time. During this period, the device pulls the pass transistor back into the linear region.

6.4.3 Disabled

The output of the device is shutdown when the voltage of the enable pin to less than $V_{IL(EN)}$ (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground. The output voltage is discharged by an internal discharge circuit from the output to ground.

The device is disabled under the following conditions:

- The input or bias voltages are below the respective minimum specifications
- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold
- The device junction temperature is greater than the thermal shutdown temperature

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TPS7N48 is a low-input, low-output (LILO), low-dropout regulator (LDO) that features soft-start capability. This regulator uses a low-current bias input to power all internal control circuitry. Thus allowing the NMOS pass transistor to regulate very low input and output voltages.

Using an NMOS pass transistor offers several critical advantages for many applications. Unlike a PMOS topology device, the output capacitor has little effect on loop stability. This architecture allows stability with ceramic capacitors of 10µF or greater on the output. Transient response is also better than PMOS topologies, particularly for low V_{IN} applications.

A programmable voltage-controlled, soft-start circuit provides a smooth, monotonic start-up and limits start-up inrush currents caused by large capacitive loads. An enable (EN) pin with hysteresis and deglitch allows slow-ramping signals to be used for sequencing the device. The low V_{IN} and V_{OUT} capability allows for inexpensive, easy-to-design, and efficient linear regulation between the multiple supply voltages often required by processor-intensive systems.

7.1.1 Input, Output, and Bias Capacitor Requirements

The device is designed to be stable for ceramic capacitors greater than or equal to 10µF on the output. The device is also stable with multiple capacitors in parallel and any type (tantalum, electrolytic, and so on.)

The capacitance required on the IN and BIAS pins strongly depends on the input supply source impedance. To counteract any inductance in the input, the minimum recommended capacitor for V_{IN} is 1µF and the minimum recommended capacitor for V_{BIAS} is 0.1µF. If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for V_{BIAS} is 4.7µF. Use good quality, low equivalent series resistance (ESR) and equivalent series inductance (ESL) capacitors on the input; ceramic X5R and X7R capacitors are preferred. Place these capacitors as close the pins as possible for optimum performance.

Low ESR and ESL capacitors improve high-frequency PSRR.

7.1.2 Dropout Voltage

The TPS7N48 offers very low dropout performance, making the device designed for high-current, low V_{IN} and low V_{OUT} applications. The low dropout allows the device to be used in place of a dc/dc converter and still achieve good efficiency. Equation 4 provides a quick estimate of the efficiency.

$$\text{Efficiency} \approx \frac{V_{OUT} \times I_{OUT}}{\left[V_{IN} \times (I_{IN} + I_Q)\right]} \approx \frac{V_{OUT}}{V_{IN}} \text{ at } I_{OUT} >> I_Q \tag{4}$$

This efficiency provides designers with the power architecture for applications to achieve the smallest, simplest, and lowest cost designs.

For this architecture, there are two different specifications for dropout voltage. The first specification (see Figure 5-16) is referred to as *V_{IN} dropout* and is used when an external bias voltage is applied to achieve low dropout. This specification assumes that V_{BIAS} has enough headroom. If V_{BIAS} is higher than the specified V_{BIAS} dropout (1.35V), then, V_{IN} dropout can be less than specified.

The second specification (illustrated in Figure 5-17) is referred to as *V_{BIAS} dropout* and applies to applications where IN and BIAS are tied together. This option allows the device to be used in applications where an auxiliary

bias voltage is not available or low dropout is not required. Dropout is limited by BIAS in these applications because V_{BIAS} provides the gate drive to the pass transistor; therefore, verify V_{BIAS} is 1.35V above V_{OUT}. Because of this usage, having IN and BIAS tied together become a highly inefficient design that consumes large amounts of power.

7.1.3 Output Noise

Most of the output noise is generated by the internal reference. The TPS7N48 has a low noise bandgap, thus leading to a low output noise. The noise performance does not depend on the C_{SS}, therefore, increasing the C_{SS} has no effect on noise. Because most of the output noise is generated by the internal reference, the noise is a function of the set output voltage. Equation 5 provides an estimate of the RMS noise:

$$V_N(\mu V_{RMS}) = 11.6 \left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}\,(V) \tag{5}$$

The low output noise makes this LDO a good choice for powering transceivers, phase-locked loops (PLLs), or other noise-sensitive circuitry.

7.1.4 Estimating Junction Temperature

By using the thermal metrics Ψ_{JT} and Ψ_{JB}, estimate the junction temperature with the following formulas. Ψ_{JT} and Ψ_{JB} are given in the *Thermal Information* table. For backwards compatibility, an older $\theta_{JC(top)}$ parameter is listed as well.

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D$$
$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D \tag{6}$$

where:

- P_D is the power dissipation
- T_T is the temperature at the center-top of the package
- T_B is the PCB temperature measured 1mm away from the package *on the PCB surface*

Note

Both T_T and T_B are measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the *Using New Thermal Metrics* application note, available for download at www.ti.com.

For a more detailed discussion of why TI does not recommend using $\theta_{JC(top)}$ to determine thermal characteristics, see the *Using New Thermal Metrics* application note. For further information, see the *Semiconductor and IC Package Thermal Metrics* application note. These application notes are also available on the TI website.

7.1.5 Soft Start, Sequencing, and Inrush Current

Soft-start refers to the ramp-up characteristic of the output voltage during LDO turn-on after EN and UVLO achieve threshold voltage.

To achieve a linear and monotonic soft-start, the TPS7N48 error amplifier tracks the voltage ramp of the external soft-start capacitor. This tracking continues until the voltage exceeds the internal reference. The soft-start ramp time depends on the soft-start charging current (I_{SS}), soft-start capacitance (C_{SS}), and the internal reference voltage (V_{REF}). Equation 7 calculates this voltage.

$$t_{SS} = \frac{(V_{REF} \times C_{SS})}{I_{SS}} \tag{7}$$

If large output capacitors are used, the device current limit (I_{CL}) and the output capacitor potentially sets the start-up time. In this case, Equation 8 gives the start-up time.

$$t_{SSCL} = \frac{(V_{OUT(NOM)} \times C_{OUT})}{I_{CL(MIN)}} \tag{8}$$

The maximum recommended soft-start capacitor is 100nF. Larger soft-start capacitors do not damage the device; however, the soft-start capacitor discharge circuit is potentially unable to fully discharge the soft-start capacitor when enabled. Soft-start capacitors larger than 100nF are potentially a problem in applications where rapidly pulsing the enable pin is required but the device soft-starts from ground. Confirm C_{SS} is low-leakage; X7R, X5R, or C0G dielectric materials are preferred. See Table 7-1 for suggested soft-start capacitor values.

Table 7-1. Standard Capacitor Values for Programming the Soft-Start Time

C_{SS} (nF)	RAMP-UP TIME (ms)
1	0.067
4.7	0.31
10	0.67
22	1.5
47	3.1
100	6.7

$V_{OUT(NOM)}$ is the nominal set output voltage, C_{OUT} is the output capacitance, and $I_{CL(MIN)}$ is the minimum current limit for the device. In applications where monotonic start-up is required, the soft-start time given by Equation 7 cannot be greater than Equation 8.

Although the device does not have sequencing requirements, following the sequencing order of BIAS, IN, and EN verifies the soft-start starts from zero.

The following figure shows an example of the device behavior when the EN pin is enabled after V_{IN} and V_{BIAS}.

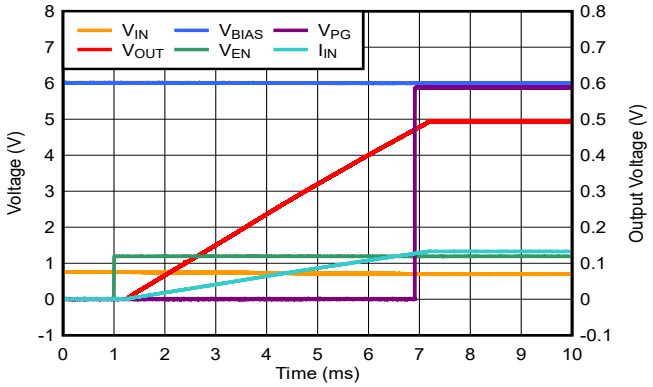


Figure 7-1. Soft-Start Behavior

Note

For further information on calculating start-up, please refer to:

Inrush current is defined as the current into the LDO at the IN pin during start-up. Inrush current then consists primarily of the sum of load current and the current used to charge the output capacitor. This current is difficult to measure because the input capacitor is removed, which is not recommended. However, Equation 9 estimates this soft-start current:

$$I_{OUT(t)} = \left[\frac{C_{OUT} \times dV_{OUT}(t)}{dt}\right] + \left[\frac{V_{OUT}(t)}{R_{LOAD}}\right] \quad (9)$$

where:

- $V_{OUT}(t)$ is the instantaneous output voltage of the turn-on ramp
- $dV_{OUT}(t) / dt$ is the slope of the V_{OUT} ramp
- R_{LOAD} is the resistive load impedance

7.1.6 Power-Good Operation

For proper operation of the power-good circuit, verify the pullup resistor value is between 10kΩ and 100kΩ. The lower limit of 10kΩ results from the maximum pulldown strength of the power-good transistor. The upper limit of 100kΩ results from the maximum leakage current at the power-good node. If the pullup resistor is outside of this range, then the power-good signal possibly does not read a valid digital logic level.

The state of PG is only valid when the device operates above the minimum supply voltage. During short UVLO events and at light loads, power-good does not assert because the output voltage is sustained by the output capacitance.

7.2 Typical Application

This section discusses the implementation of the TPS7N48 to regulate a 1A load requiring good PSRR at high frequency with low noise. Figure 7-2 provides a schematic for this typical application circuit. Table 7-2 lists standard resistor values for the output voltage used in this design example.

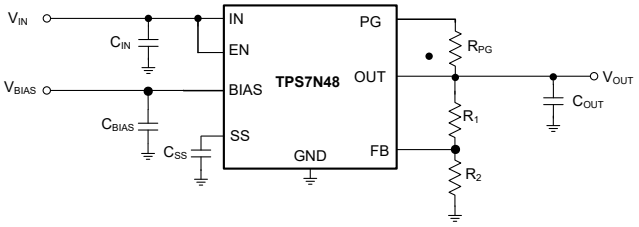


Figure 7-2. Typical ADJ Voltage Application

Table 7-2. Standard 1% Resistor Values for Programming the Output Voltage

R_1 (kΩ)	R_2 (kΩ)	V_{OUT} (V)
Short	Open	0.5
2.1	2.61	0.9
2.1	1.5	1.0
2.1	1.05	1.5
2.1	0.806	1.8
2.1	0.523	2.5
2.1	0.374	3.3

Set the output voltage with the following equation:

$$V_{OUT} = 0.5V \times (1 + [R_1 / R_2]) \quad (10)$$

7.2.1 Design Requirements

For this design example, use the parameters listed in Table 7-3 as the input parameters.

Table 7-3. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	1.0V, provided by the dc/dc converter switching at 500kHz
Bias voltage	5.0V
Output voltage	0.5V
Output current	1.0A (maximum), 10mA (minimum)
RMS noise, 10Hz to 100kHz	< 10μV_{RMS}
PSRR at 500kHz	> 40dB
Start-up time	< 25ms

7.2.2 Detailed Design Procedure

At 1.5A and 0.5V_{OUT}, the dropout of the TPS7N48 has a 150mV maximum dropout over temperature. Thus, a 250mV headroom is sufficient for operation over both input and output voltage accuracy. The TPS7N48 enters dropout if both the input and output supply are beyond the edges of the respective accuracy specification. This dropout occurs at full load and high temperature on some devices.

To satisfy the required start-up time and still maintain low noise performance, a 100nF C_{SS} is selected. Equation 11 estimates this value.

$$t_{SS} = (V_{SS} \times C_{SS}) / I_{SS} \quad (11)$$

At the 1A maximum load, the internal power dissipation is 0.5W. This value corresponds to a 31.4°C junction temperature rise for the DSQ package on a standard JEDEC board. With an 55°C maximum ambient temperature, the junction temperature is at 86.4°C.

7.2.3 Application Curve

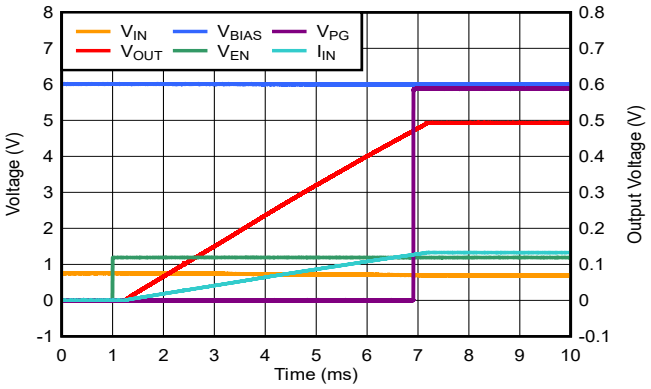


Figure 7-3. Start-Up

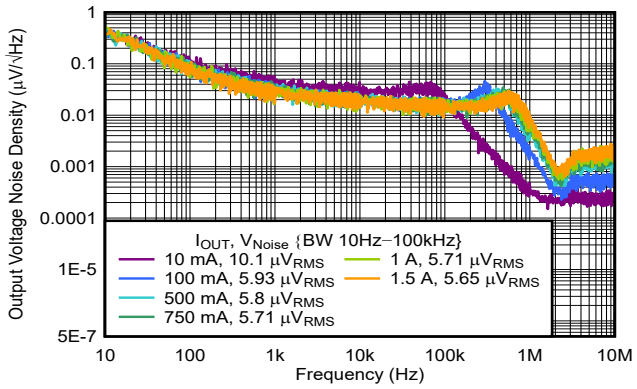


Figure 7-4. Output Voltage Noise Density vs Frequency

7.3 Power Supply Recommendations

The TPS7N48 is designed to operate from an input voltage of 0.75V up to 6.0V. Confirm the bias rail and the input supply both provide adequate headroom and current for the device to operate normally. Connect a low impedance power supply directly to the IN pin. This supply requires at least a 1µF of capacitor near the IN pin, or a 10µF for optimum performance. A supply with similar requirements is also connected directly to the BIAS rail with a separate 0.1µF or larger capacitor. If the IN pin is tied to the BIAS pin, a minimum 4.7µF capacitor is required for performance. To increase the overall PSRR of the design at higher frequencies, use a pi-filter or ferrite bead before the input capacitor.

7.4 Layout

7.4.1 Layout Guidelines

Proper layout greatly improves transient performance, PSRR, and noise. To minimize voltage drop on the device input during load transients, connect the capacitance on IN and BIAS as close as possible to the device. This capacitance also minimizes the effects of parasitic inductance and resistance of the input source and, therefore, improves stability. To achieve optimum transient performance and accuracy, connect the top side of R_1 in Figure 7-2 as close as possible to the load. If BIAS is connected to IN, connect BIAS as close to the sense point of the input supply as possible. This connection minimizes the voltage drop on BIAS during transient conditions and improves turn-on response.

Knowing the device power dissipation and proper sizing of the thermal plane connected to the thermal pad is critical. These parameters avoid thermal shutdown and provide reliable operation. Device power dissipation is calculated using Equation 12 and depends on input voltage and load conditions.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (12)$$

Power dissipation is minimized and greater efficiency achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On the WSON (DSQ) package, the primary conduction path for heat is through the exposed pad to the printed circuit board (PCB). Connect the pad to ground or leave floating. However, confirm the thermal pad is attached to an appropriate amount of copper PCB area to verify the device does not overheat. The maximum junction-to-ambient thermal resistance is calculated using Equation 13 and depends on the maximum ambient temperature, maximum device junction temperature, and device power dissipation.

$$R_{\theta JA} = \frac{(+125°C - T_A)}{P_D} \quad (13)$$

Note

When the device is mounted on an application PCB, use Ψ_{JT} and Ψ_{JB}, as explained in the *Estimating Junction Temperature* section.

7.4.1.1 Board Layout

For best overall performance, place all circuit components on the same side of the circuit board. Furthermore, place these components as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to each other as possible. Use wide, component-side, copper surface for these connections. To avoid negative system performance, do not use vias and long traces to the input and output capacitors. The grounding and layout scheme illustrated in Figure 7-5 minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability.

To improve performance, use a ground reference plane, either embedded in the PCB or placed on the bottom side of the PCB opposite the components. This reference plane provides accuracy of the output voltage, shield noise. Additionally, this reference plane behaves similar to a thermal plane to spread (or sink) heat from the LDO device when connected to the thermal pad. In most applications, this ground plane is necessary to meet thermal requirements.

7.4.2 Layout Example

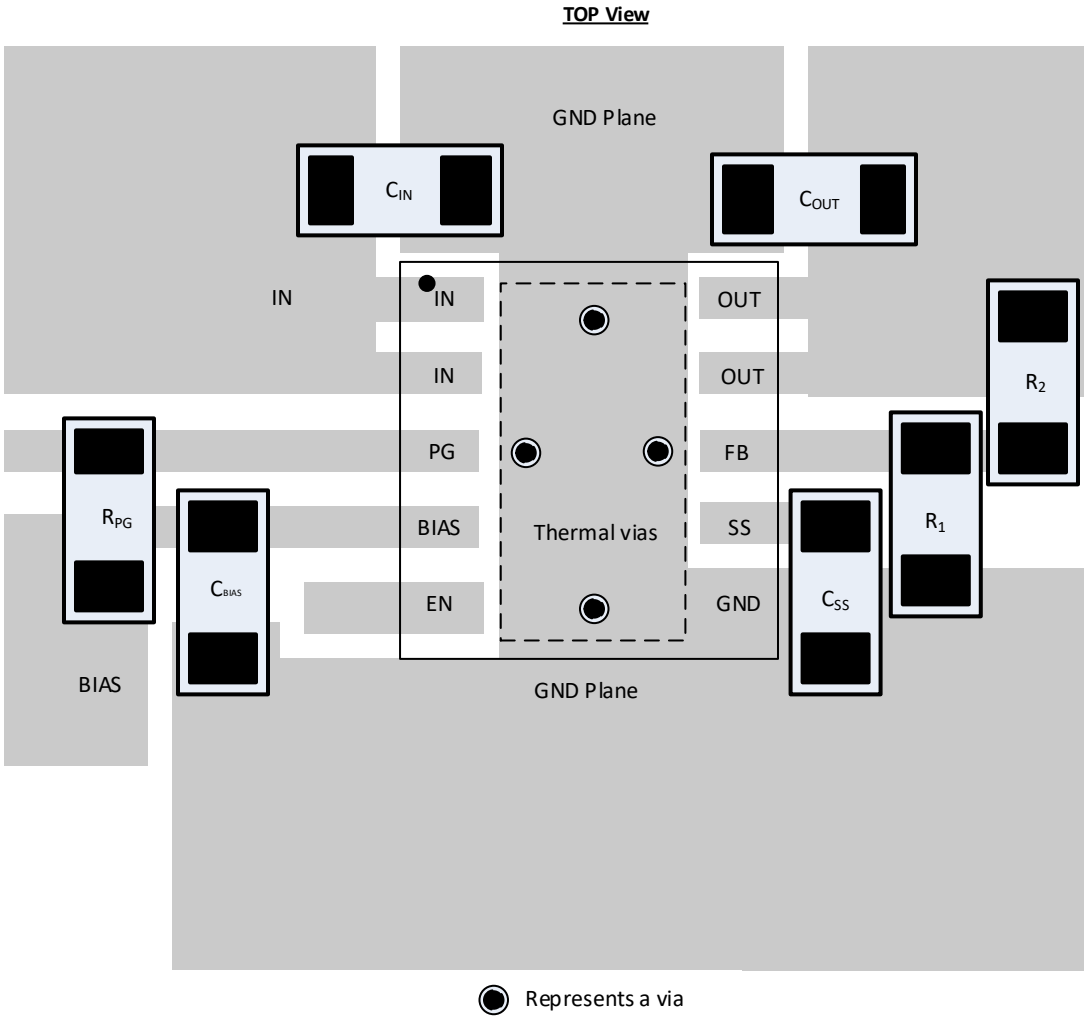


Figure 7-5. Example Layout

8 Device and Documentation Support

8.1 Device Support

8.1.1 Device Nomenclature

Table 8-1. Available Options

PRODUCT(1)	DESCRIPTION
TPS7N4801yyyz	**yyy** is the package designator. **Z** is the package quantity. R is for reel (3000 pieces).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Using New Thermal Metrics* application note
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note
- Texas Instruments, *Pros and Cons of Using a Feed-Forward Capacitor with a Low Dropout Regulator* application note

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.5 Trademarks

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8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2025	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7N4801PDSQR	Active	Production	WSON (DSQ) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3OHH

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

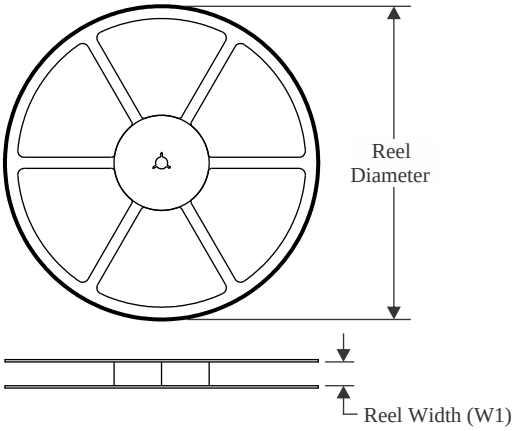
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

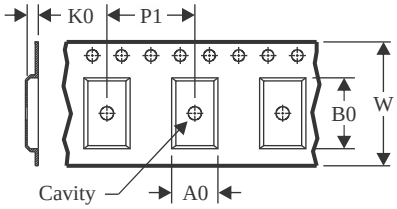
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

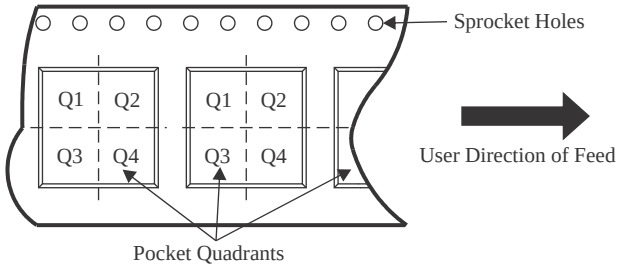


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

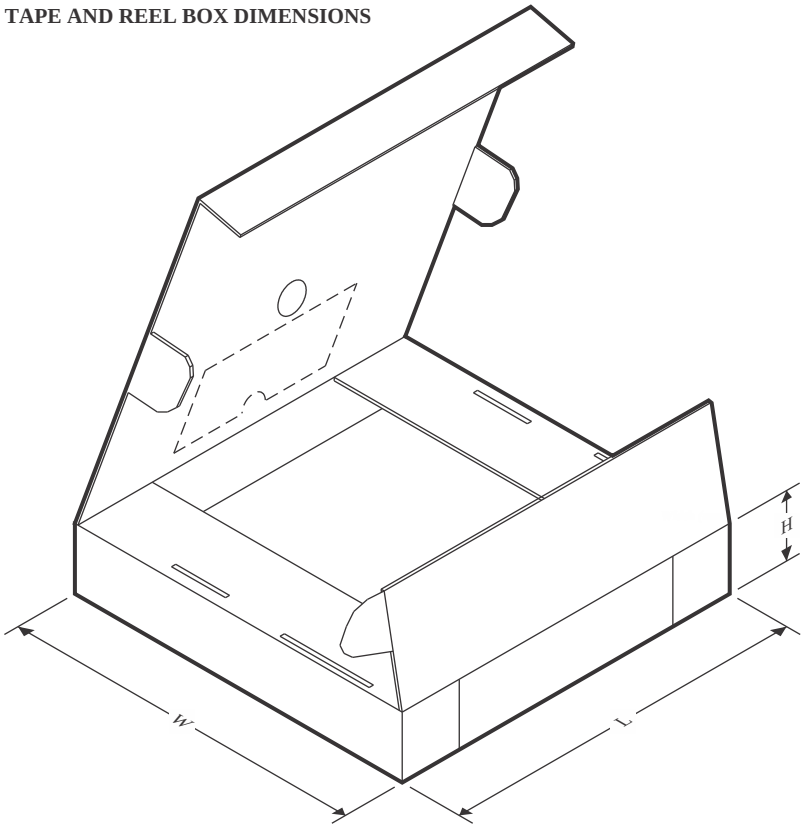
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7N4801PDSQR	WSON	DSQ	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

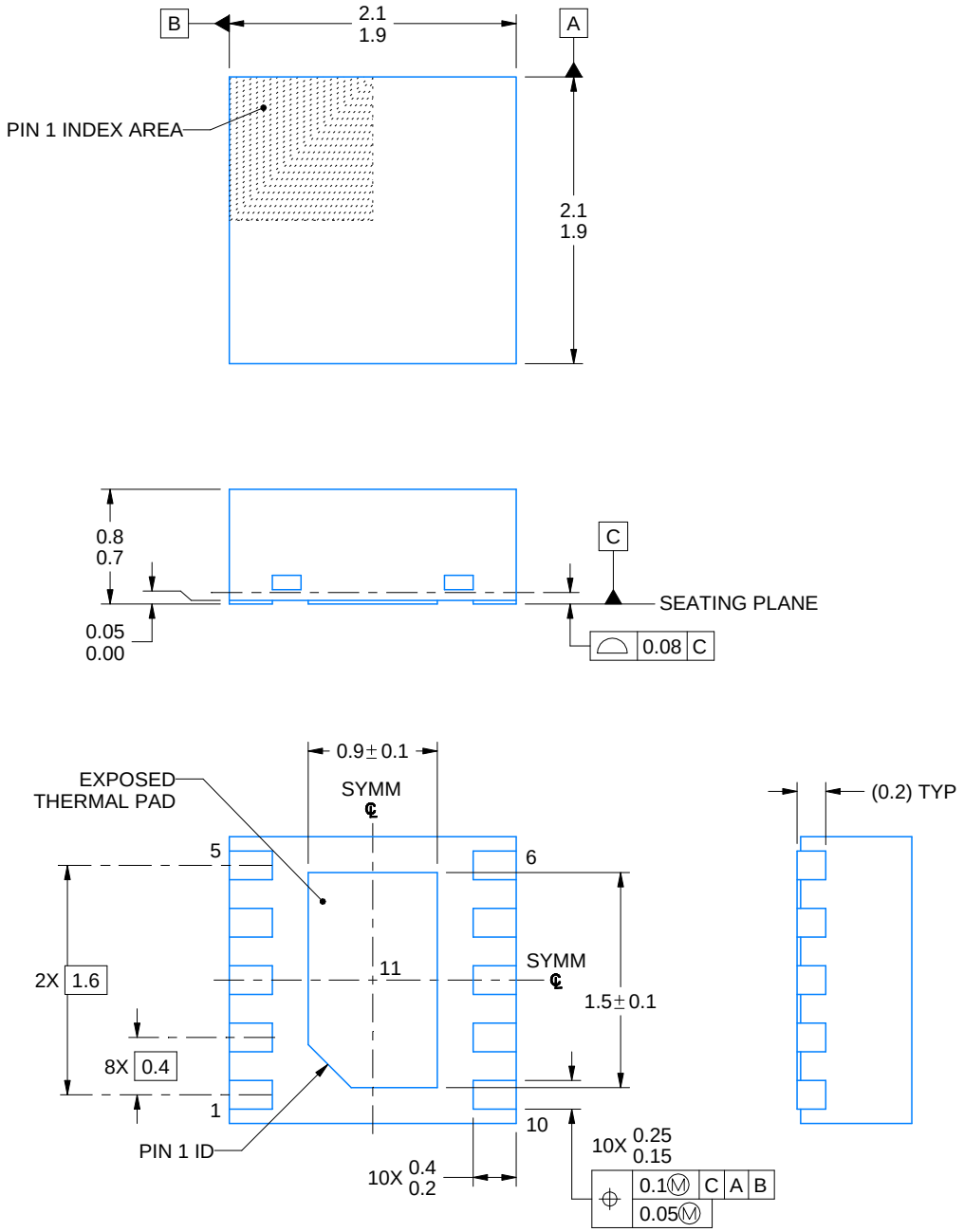
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7N4801PDSQR	WSON	DSQ	10	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DSQ0010A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4218906/A 04/2019

NOTES:

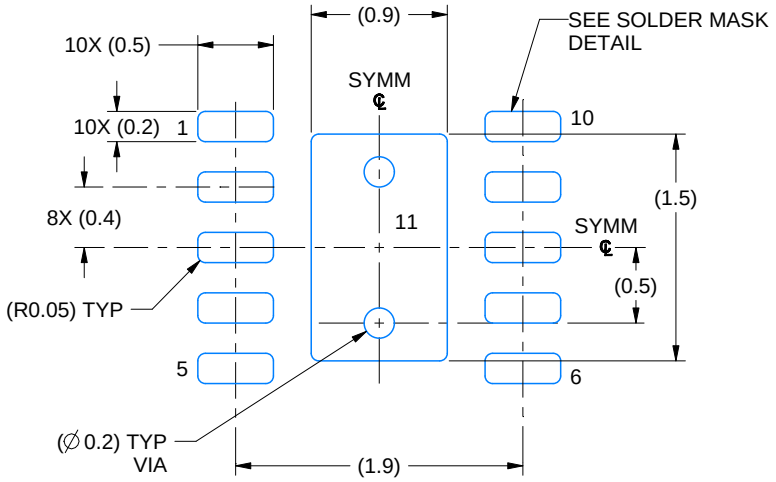
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

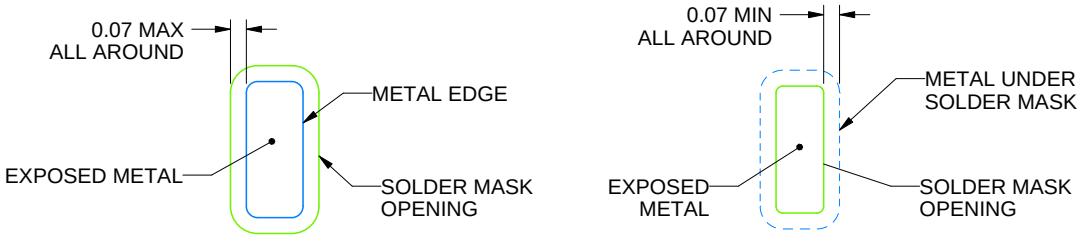
DSQ0010A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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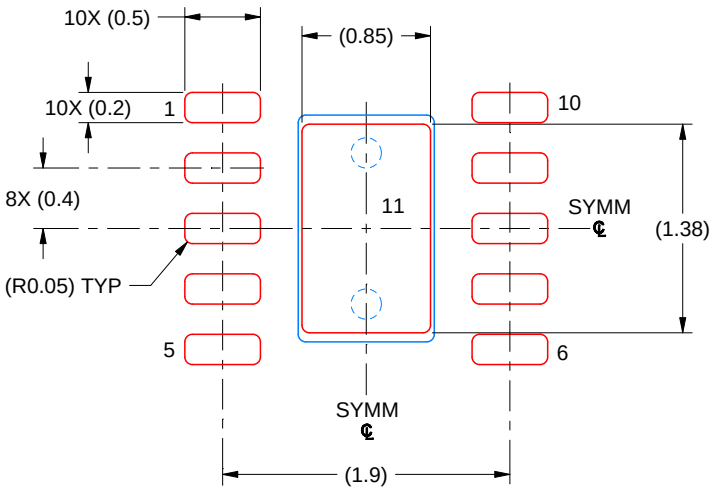
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 11
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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