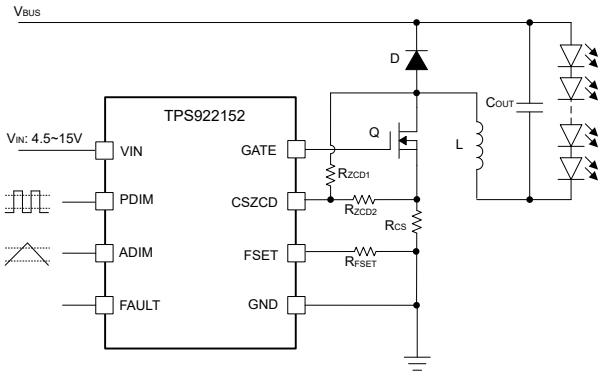
TPS922152 Average-Current Buck LED Driver with Wide Range Dimming

1 Features

- 4.5V to 15V input voltage range
- Wide application voltage up to 500V
- LED common anode connection
- Adjustable switching frequency: 50kHz ~ 1MHz
- Adative Off-Time mode
- Advanced dimming options:
  - Analog dimming (1000:1)
  - PWM dimming (50ns pulse width, 1000:1 @ 20kHz)
  - Flexible dimming (100,000:1)
- Low standby current
- Full protection features:
  - LED open and short protection
  - Cycle-by-cycle current limit
  - Sense resistor open and short protection
- Package: SOIC-8 and SOT583

2 Applications

- Constant Illumination:
  - Indoor and Outdoor Lighting
  - Stage and Photography Lighting
  - Projector, Laser TV, Printer, IP Camera
  - High Voltage LED Driver
- Instant Illumination:
  - Machine Vision and Camera Flash
  - Fire Alarm and Strobe
- LED Backlight:
  - Flat Panel Display
  - LCD TV and Monitor



Simplified Schematic

3 Description

The TPS922152 is non-synchronous Average-Current control Buck LED drivers with 4.5V to 500V wide application voltage range. The TPS922152 is capable of driving external switching FETs at adjustable switching frequency up to 1MHz with Adative Off-Time (AOT) mode. The AOT mode allows low LED current ripple and fast transient response with small output capacitor. The device also supports single layer PCB design and common anode connection.

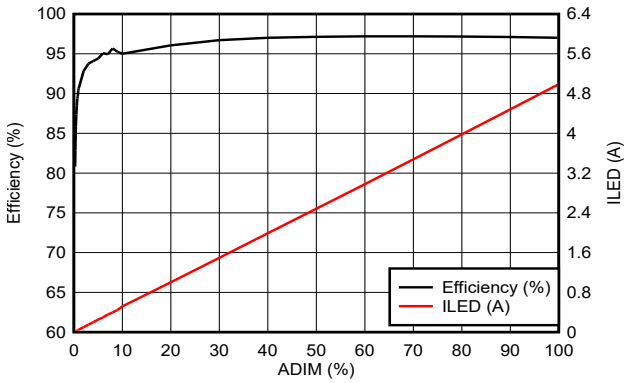
The TPS922152 supports high-accuracy and high-ratio analog dimming by configuring analog signals through the ADIM input pins. The full-scale output current is configured by an external resistor and high analog dimming ratio is achievable by the unique corrective sensing. The device also supports high-frequency and high-ratio PWM dimming by configuring simple high and low signals through the PDIM input pins. High-accuracy and high-ratio of PWM dimming is achievable by the unique inductive fast dimming (IFD).

The TPS922152 also provides multiple systematic protections, including LED open and short, sense resistor open and short.

Device Information

PART NUMBER(1)	PACKAGE	PACKAGE SIZE(2)
TPS922152	SOIC (8)	4.9mm × 3.9mm
	SOT23 (8)	2.9mm × 1.6mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Efficiency and Dimming Linearity of V_{BUS}=60V, V_{LED}=48V, L=33µH, F_{SW}=400kHz

ADVANCE INFORMATION

ADVANCE INFORMATION

Table of Contents

4 Pin Configuration and Functions

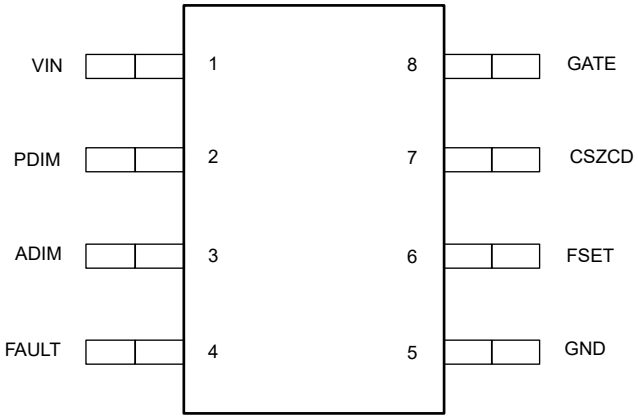


Figure 4-1. 8-Pin SOIC Top View

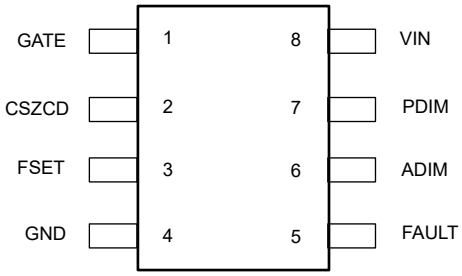


Figure 4-2. 8-Pin SOT23 Top View

ADVANCE INFORMATION

Table 4-1. Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	SOIC Package	SOT Package		
VIN	1	8	P	Input power pin with an internal zener clamping circuit.
PDIM	2	7	I	PWM dimming pin. Input a PWM signal for PWM dimming. Input a >1.2V pull up voltage for pure analog dimming or shunt dimming. Pull down to ground to stop switching. Do not leave the pin floating.
ADIM	3	6	I	Analog dimming pin. Input a 0.2V~2.4V analog signal for analog dimming. Input a >2.4V pull up voltage for pure PWM dimming. Pull down to ground to disable the device for low-power standby mode. Do not leave the pin floating.
FAULT	4	5	O	Open drain fault output with >2.4V pull up voltage. It can be configured by 1.2V~2.4V input to enable shunt dimming mode. Do not leave the pin floating, connect it to GND when not use
GND	5	4	G	Ground pin.
FSET	6	3	I	Switching frequency set pin for TPS922152. Connect a resistor to ground to config the switching frequency. Current ripple set pin for TPS922153. Connect a resistor to ground to config the inductor current ripple.
CSZCD	7	2	I	Output current sense and zero current detection pin. 200mV at full current.
GATE	8	1	O	Gate drive pin for external switching FET.

(1) I = Input, O = Output, P = Supply, G = Ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage on pins	VIN	–0.3	18	V
Voltage on pins	GATE	–0.3	VIN+0.3	V
Voltage on pins	PDIM, ADIM, FSET, CSZCD	–0.3	5.5	V
Operation junction temperature	T_J	–40	125	°C
Storage temperature	T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage range	VIN	4.5	15	V
Output voltage range	FAULT	0	20	V
Output voltage range	GATE	0	VIN+0.3	V
Input voltage range	PDIM, ADIM, CSZCD, FSET	0	5	V
Operation ambient temperature	T_A	–40	85	°C

5.4 Thermal Information

THERMAL METRIC(1)		TPS922152 SOIC 8 PINS	TPS922152 SOT583 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	96.0	113.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.5	41.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.1	24.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	1.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	32.9	23.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics*application note, SPRA953.

ADVANCE INFORMATION

5.5 Electrical Characteristics

The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product containingit. T_J = –40°C to +125°C, V_{IN} = 15 V, V_{BUS} = 60 V (unlessotherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{VIN_UVLO}	V_{IN} undervoltage lockout	Rising V_{IN}	3.7	3.95	4.1	V
		Falling V_{IN}	3.5	3.65	3.8	V
	Hysteresis			0.3		V
I_{OFF}	ADIM off quiesent current from V_{IN}	V_{IN} = 12 V, V_{GATE} = 0 V, ADIM = 0 V	70	93	116	µA
I_{OP}	Normal operating current	28-kHz switching frequency, C_{LOAD} = 1 nF		2.05		mA
FEEDBACK AND ERROR AMPLIFIER						
$g_{m(ea)}$	OTA transconductance gain	ADIM = 2.4 V, PDIM = 100%	29	47	71	µA/V
Z_{COMP}	Zero compensation	ADIM = 2.4 V, PDIM = 100%		5		kHz
V_{CS}	Current sense threshold	ADIM = 2.4 V	194	200	206	mV
V_{CS}	Current sense threshold	ADIM = 0.42 V		20		mV
I_{LEAK_CS}	CSZCD pin leakage current	V_{CS} = 200 mV			5	µA
I_{LEAK_CS}	CSZCD pin leakage current	V_{CS} = 20 mV			1	µA
DIMMING						
V_{PWM_L}	Low-level input voltage		0.58	0.68	0.74	V
V_{PWM_H}	High-level input voltage		0.98	1.12	1.19	V
V_{ADIM}	Input voltage		0.2		2.4	V
$V_{ADIM\_LOW\_CLAMP}$	Input voltage low clamp			0.16		V
$V_{ADIM\_HIGH\_CLAMP}$	Input voltage high clamp			2.8		V
$t_{PWM\_OUT\_ON}$	PWM output minimum on time				50	ns
$t_{PWM\_IN\_ON}$	PWM input minimum on time				50	ns
CURRENT LIMIT						
V_{CS_LIM}	CS cycle-by-cycle current limit		335	351	365	mV
V_{CS_OCP}	CS overcurrent protection		322	435	505	mV
V_{CS_OVP}	CS overvoltage protection		549	550	554	mV
GATE DRIVER						
V_{GATE-H}	GATE high saturation	V_{IN} = 15V, I_{GATE} = 100mA source	14.47	14.77		V
V_{GATE-L}	GATE low saturation	V_{IN} = 15V, I_{GATE} = 100mA sink		140	280	mV
t_{GATE_RISE}	Rise time	C_{LOAD} = 1nF		10		ns
t_{GATE_FALL}	Fall time	C_{LOAD} = 1nF		10		ns
t_{ON_MIN}	Minimum on time			130		ns
t_{ON_MAX}	Maximum on time			50		µs
t_{OFF_MIN}	Minimum off time			150		ns
t_{OFF_MAX}	Maximum off time			40		µs
FAULT						
V_{OL}	Output level low	I = 1 mA			0.1	V
$I_{LEAKAGE}$	Output leakage current	V = 20 V			1	µA
THERMAL PROTECTION						
T_{TSD}	Thermal shutdown temperature			165		°C
T_{TSD}	Hysteresis			15		°C

5.6 Typical Characteristics

V_{IN} = 15V, V_{BUS} = 60V, LED = 16, unless otherwise specified

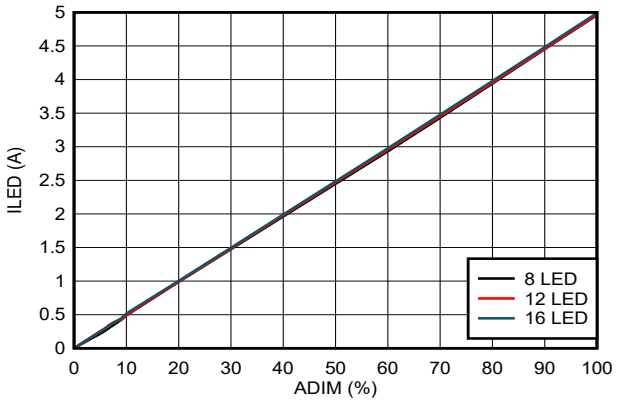


Figure 5-1. ADIM: Output Current vs. LED Count

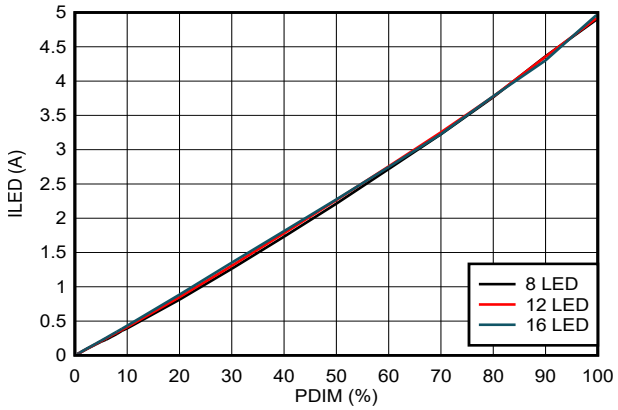


Figure 5-2. PDIM: Output Current vs. LED Count

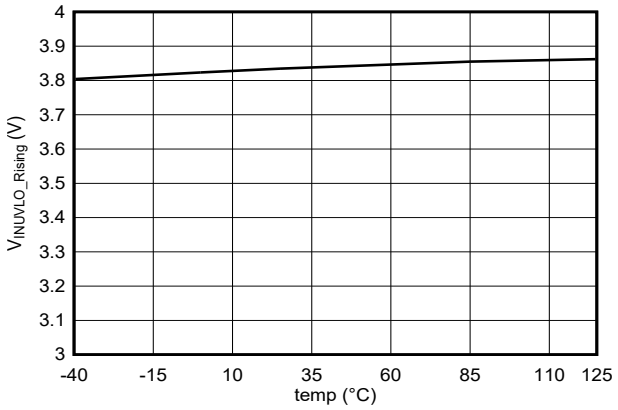


Figure 5-3. VIN UVLO rising vs. Junction Temperature

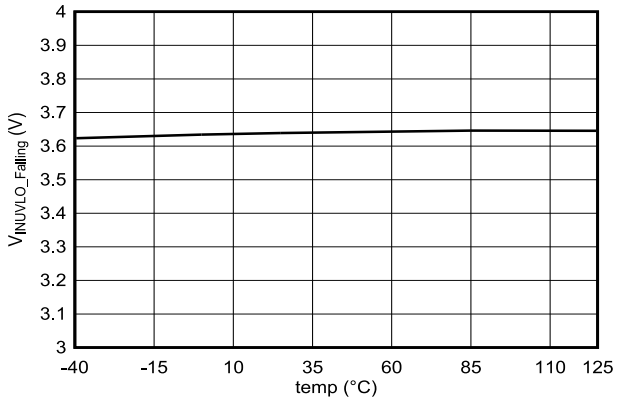


Figure 5-4. VIN UVLO falling vs. Junction Temperature

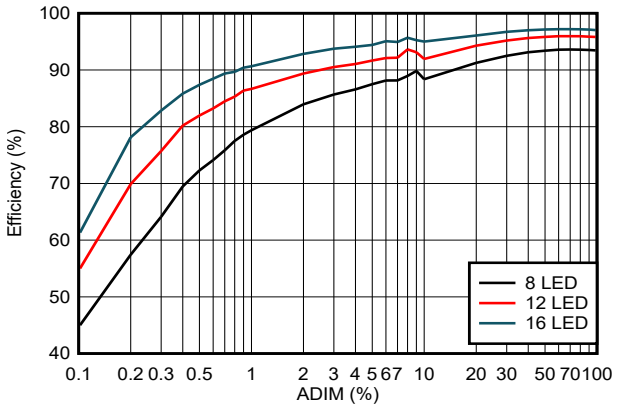


Figure 5-5. Efficiency at 5A Full Loading Output Current, 33µH Inductor, 60V Input Voltage

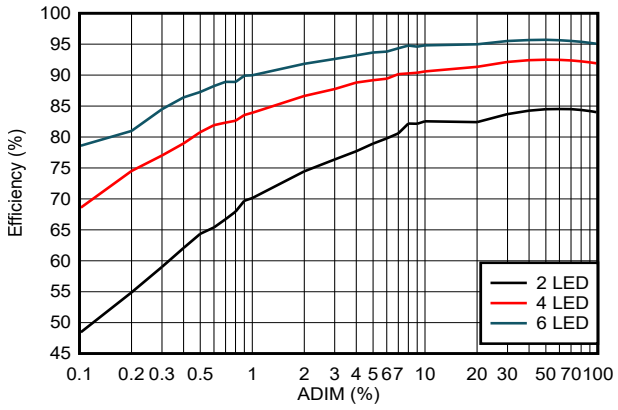


Figure 5-6. Efficiency at 5A Output Current, 33µH Inductor, 24V Input Voltage

ADVANCE INFORMATION

ADVANCE INFORMATION

6 Detailed Description

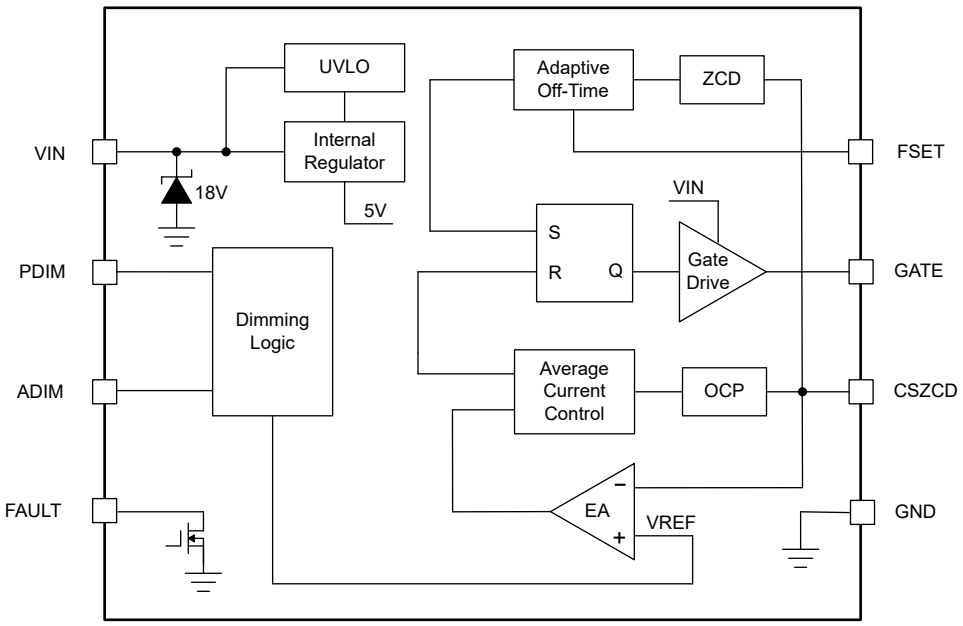
6.1 Overview

The TPS922152 is non-synchronous Average-Current control Buck LED drivers with 4.5V to 500V wide application voltage range. The TPS922152 is capable of driving external switching FETs at adjustable switching frequency up to 1MHz with Adative Off-Time (AOT) mode. In AOT mode, the switching off time is set through an external resistor and the switching frequency is adjustable in the range of 50kHz~1MHz, suitable for constant frequency operation over a wide load range. It allows low LED current ripple and fast transient response with small output capacitors. Furthermore, the switching frequency is folded back at light load for higher efficiency and higher dimming ratio. The device also supports single layer PCB design and common anode connection, hence saving cost of connector, harness and PCB.

The TPS922152 supports high-accuracy and high-ratio analog dimming by configuring analog signals through the ADIM input pins. The full-scale output current is configured by an external sense resistor and is regulated corresponding to the analog input voltage at ADIM pin. High analog dimming ratio is achievable by the unique corrective sensing function. The devices also support high-frequency and high-ratio PWM dimming by configuring simple high and low signals through the PDIM input pin. The output current is regulated in PWM shape corresponding to on and off input signal at PDIM pin. Due to the unique inductive fast dimming (IFD), the device is capable of responding to an ultra-narrow pulse width input signal down to 50ns for a high PWM dimming ratio. The compensation bandwidth is determined by the internal capacitor and resistor. The devices are also capable of supplying continuously constant current to support shunt dimming where the LED output is periodically shorted.

For safety and protection, the devices support full systematic protections with hiccup mode including LED open and short, sense resistor open and short, switching FET open protection. The open-drain FAULT pin can send out the fault signal by connecting to a pull-up resistor. The input voltage is clamped at 15V to protect the gating voltage from exceeding the limit. The devices can be supplied through an individual source or an RC circuit from the application input bus voltage.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Adaptive Off-Time Mode

The TPS922152 device operates in AOT mode average-current control with constant frequency to support accurate current regulation and fast transient response over a wide load range.

For average output current regulation, the sensed voltage across the sensing resistor between the CSZCD pin and ground is averaged and compared with the internal voltage reference, V_{REF} , through the error amplifier. V_{REF} is controllable through the analog input voltage at ADIM pin. During each switching cycle, when the switching FET is turned on, the current rising edge is sensed through the CSZCD pin. The output of the error amplifier, V_{COMP}, passes through an internal compensation network and is then compared with the current rising edge. When the sensed current reaches V_{COMP} at the input of PWM comparator, the switching FET is turned off to generate the peak current.

An off-time counter starts counting after the switching FET is turned off. The counting off time corresponding to a switching frequency is determined by the external resistor connected to the FSET pin. Once the off-time counter stops counting, the counter is reset until when the switching FET stays off. Thus, the device is able to maintain a nearly constant switching frequency at steady state CCM and DCM. By connecting an external resistor between FSET pin and ground, the switching frequency is set in the range of 50kHz to 1MHz. The resistor value and the corresponding switching frequency can be calculated using Equation 1

$$F_{SW} = \frac{1}{R_{FSET} \times C_{FSET}} \quad (1)$$

where

- C_{FSET} = 100pF

At light load, the off time continuously increases by pulse frequency modulation for accurate light load control. The minimum switching frequency is clamped at 20kHz.

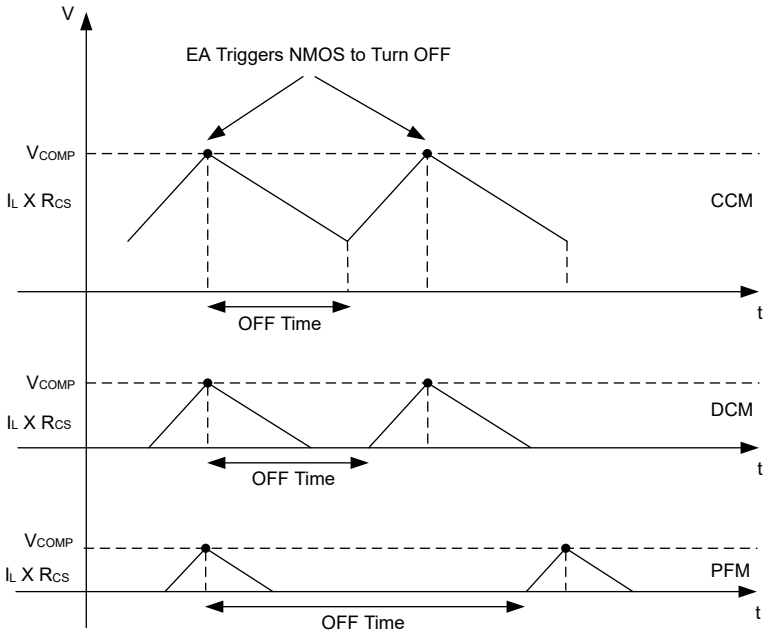


Figure 6-1. AOT mode average-current control

ADVANCE INFORMATION

6.3.2 Setting LED Current

The LED current is set by the external sensing resistor R_{CS} between the switching FET source and ground. The internal voltage reference, V_{REF}, is 200mV for full-scale LED current where ADIM=2.4V, I_{LED_FS}, and the sensing resistor can be calculated using Equation 2.

$$R_{CS} = \frac{V_{REF}}{I_{LED\_FS}} \quad (2)$$

where

- V_{REF} = 200mV

The switching FET source is connected to the CSZCD pin through a switch-node voltage divider for current sense feedback and zero current detection. The ZCD voltage is set as

- V_{ZCD} = 0.9V

The ratio of voltage divider should guarantee

$$V_{BUS} \times \frac{R_{ZCD2}}{R_{ZCD1} + R_{ZCD2}} > 0.9V \quad (3)$$

$$V_{LED-} \times \frac{R_{ZCD2}}{R_{ZCD1} + R_{ZCD2}} < 0.9V \quad (4)$$

where V_{LED-} is the LED Anode voltage. R_{ZCD1} and $R_{ZCD2}$is recommend to be between 1kΩ and 1MΩ to reduce the noise as well as keep LED leakage current.

Considering the current sensing mismatch due to the voltage divider, the corrected sensing resistor can be calculated using

$$R_{CS} = \frac{V_{REF}}{I_{LED\_FS}} - \frac{R_{DS\_ON} \times R_{ZCD2}}{R_{ZCD1} + R_{ZCD2}} \quad (5)$$

6.3.3 VIN UVLO & Clamping

The TPS922152 implement an internal undervoltage-lockout (UVLO) circuit connecting to the VIN pin. The UVLO is triggered and then the device is disabled when the VIN pin voltage falls below the internal UVLO threshold voltage, V_{VIN_UVLO} typically 3.8V, with a typical 0.3V hysteresis. The VIN pin is the input of an internal regulator. Therefore, if VIN pin voltage falls close to above the V_{VIN_UVLO} (around 500mV above), the UVLO will be triggered.

In addition, an internal zener clamping circuit is connected to the VIN pin to limit the voltage of both VIN pin and GATE pin. The VIN pin is the input of internal gate driver. The zener starts to drain current once VIN pin voltage rises above the V_{VIN_CLAMP} (around 15V). The maximum zener drain current is around 20mA. An external source VCC less than 15V such as an external LDO or auxiliary transformer winding can power supply the device. Alternatively, an $R_{IN1}C_{IN}$ circuit can be used to power supply the device through the application input bus voltage VBUS directly. VIN pin is clamped to V_{VIN_CLAMP} with the $R_{IN1}C_{IN}$ circuit and can be lower voltage if an optional voltage divider R_{IN2} is used. An optional gate resistor R_{GATE} can be used to limit the gating current and reduce the switching slew rate.

TI recommends to get VBus ready before powering on VIN, and power off VIN before powering off VBus.

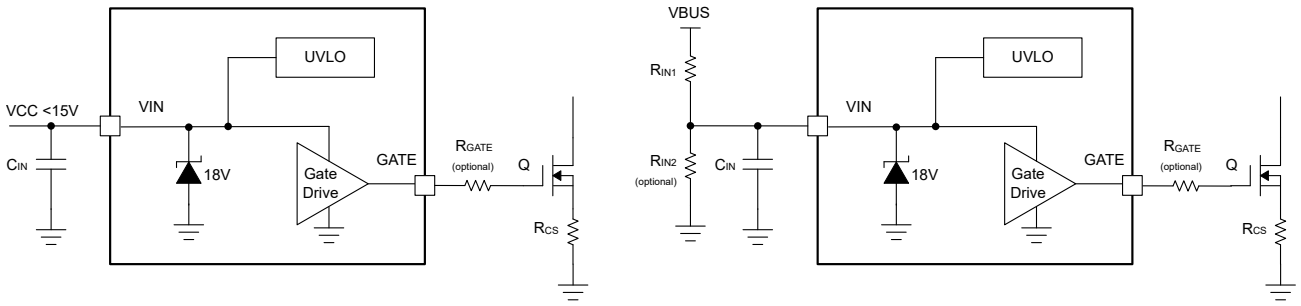


Figure 6-2. VIN Power Supply and Clamping

6.3.4 Dimming Mode

The TPS922152 enables both analog dimming, PWM dimming, shunt dimming, and flexible dimming. Flexible dimming can be achieved by configuring both ADIM and PDIM pins at the same time.

The configuration to dimming modes are shown as below

Table 6-1. Dimming Mode Configuration

Dimming Mode	DIM Pin	Input Signal
PWM Dimming	PDIM	PWM Voltage
Analog Dimming	ADIM	Analog Voltage
Flexible Dimming	PDIM + ADIM	PWM Voltage + Analog Voltage
Shunt Dimming	FAULT	Voltage Divider

ADVANCE INFORMATION

6.3.4.1 PWM Dimming

The PWM dimming mode is enabled when the PDIM input pin is configured by a PWM input signal. The TPS922152 supports PWM input signals with ultra-narrow pulse width down to 50ns for high PWM dimming ratio.

In PWM dimming mode, when the PWM input signal at the PDIM pin turns from low to high, the switching FET starts switching and the inductor current rises to the determined value. The LED current is then regulated at the determined value as long as the PWM input signal stays high. When the PWM input signal turns from high to low, the switching FET is turned off causing the inductor current falling to zero. The switching FET maintains off and the LED current stays zero as long as the PWM input signal stays low.

6.3.4.2 Analog Dimming

The TPS922152 supports analog dimming which regulates the LED current through the analog voltage signal at the ADIM pin.

The internal voltage reference, V_{REF}, starts to rise after an analog voltage higher than 0.2V appears at the ADIM pin. V_{REF} continues to increase until changing to the desired value in proportion to the analog voltage. V_{REF} is 200mV when the analog input signal at the ADIM pin is 2.4V. The ADIM pin analog voltage and corresponding V_{REF} can be calculated using Equation 6

$$V_{REF} = \frac{V_{ADIM} - 0.2\text{V}}{11} \tag{6}$$

The analog input signal to the ADIM pin is recommend to be 0.2V-2.4V to regulate the LED current. The high clamp voltage of ADIM pin is 2.8V. V_{REF} is 0V when the analog input signal is lower than 0.2V. The device works in low-power standby mode with low quiescent current when analog input signal is lower than 0.16V. The circuit is able to respond to the voltage change of the analog input signal with tens of micro-seconds delay.

ADVANCE INFORMATION

6.3.4.3 External Shunt Dimming

The TPS922152 supports external shunt dimming where an external shunt FET is placed in parallel with LEDs. The shunt dimming mode is enabled when LEDs are shorted and the FAULT pin is configured with a voltage in the range of 1.2V to 2.4V. Thus, the device keeps normal switching when LEDs are shorted by the shunt FET.

In external shunt dimming, the external shunt FET bypasses the LEDs periodically at a dimming frequency. During bypassing, the LED voltage is close to zero and LED short protection can be triggered if shunt dimming mode is disabled. If the FAULT pin is connected to the LED cathode through a voltage divider, the FAULT pin voltage is set in the range of 1.2V to 2.4V when LEDs are shorted by the shunt FET, and less than 1.2V when the shunt FET is turned off. Thus, the LED short protection is disabled and the shunt dimming mode is enabled. The device is able to continuously regulate output current when LEDs are shorted. Other fault protections are still active and the FAULT pin is pulled down if any other fault occurs. The ratio of voltage divider for shunt dimming mode can be calculated using

$$\frac{R_{SHNT1}}{R_{SHNT2}} > \frac{MAX\left(0.5 \times V_{BUS\_MAX}, V_{BUS\_MAX} - V_{LED\_MIN}\right)}{V_{SHNT}} - 1 \quad (7)$$

where

- V_{SHNT} = 1.2V

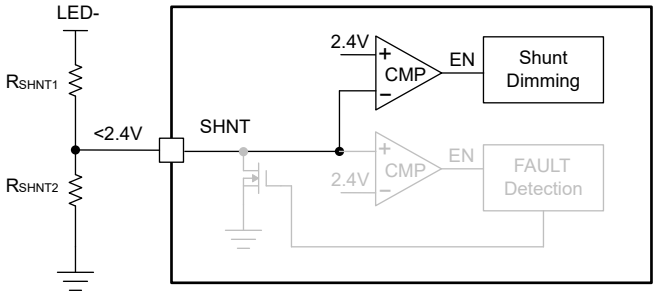


Figure 6-3. Shunt Dimming Mode Enable Setting

ADVANCE INFORMATION

6.3.5 Fault Protection

The TPS922152 and TPS922153 are able to provide fault protections and send fault report signals by pulling down the open-drain FAULT pin in many fault conditions, including LED open, LED ± short, LED short to PGND, sense resistor open and short, switching FET open. The device stops switching after the fault protection occurs. It hiccups every 1.6 second and recovers once fault is removed. The device is disabled without hiccups when $V_{CS} > V_{CS\_OVP}$ and then recovers after UVLO and restart with fault removed.

Table 6-2. Protections

TYPE	CRITERION	BEHAVIOR
LED open load	$t_{ON} > t_{ON\_MAX}$	The device stops switching. It hiccups every 1.6s and recovers when fault is removed.
LED+ and LED- short circuit during switching operation (shunt dimming mode is disabled)	$V_{CS} > V_{CS\_OVP}$	The device stops switching. It recovers after UVLO and restart with fault removed.
LED- short to PGND	$t_{ON} > t_{ON\_MAX}$	The device stops switching. It hiccups every 1.6s and recovers when fault is removed.
Sense-resistor open circuit	$V_{CS} > V_{CS\_OVP}$	The device stops switching. It recovers after UVLO and restart with fault removed.
Sense-resistor short circuit	$t_{ON} > t_{ON\_MAX}$	The device stops switching. It hiccups every 1.6s and recovers when fault is removed.
Switching FET open circuit	$t_{ON} > t_{ON\_MAX}$	The device stops switching. It hiccups every 1.6s and recovers when fault is removed.

The FAULT pin open drain is active by connecting the pin to a VCC higher than 2.4V through a pull-up resistor R_{FAULT}. Thus, the FAULT pin is pulled down to ground once fault occurs. When FAULT pin is not used, please connect it to GND, do not let FAULT pin floating.

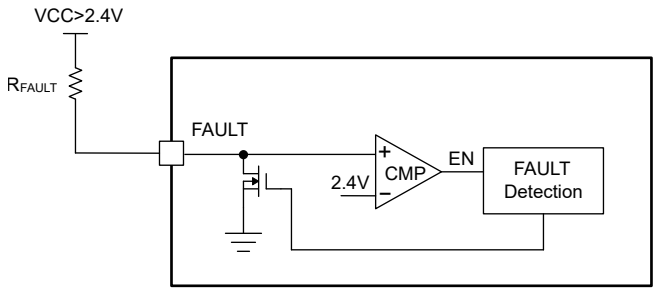


Figure 6-4. FAULT Open Drain

7 Application and Implementation

7.1 Application Information

The TPS922152 is used as Average-Current control Buck controller to drive one or more LEDs from an input from 4.5V to 500V range.

7.2 Typical Application

7.2.1 TPS922152 60V Input Bus, 5A Output, 16-piece WLED With Analog and PWM Dimming

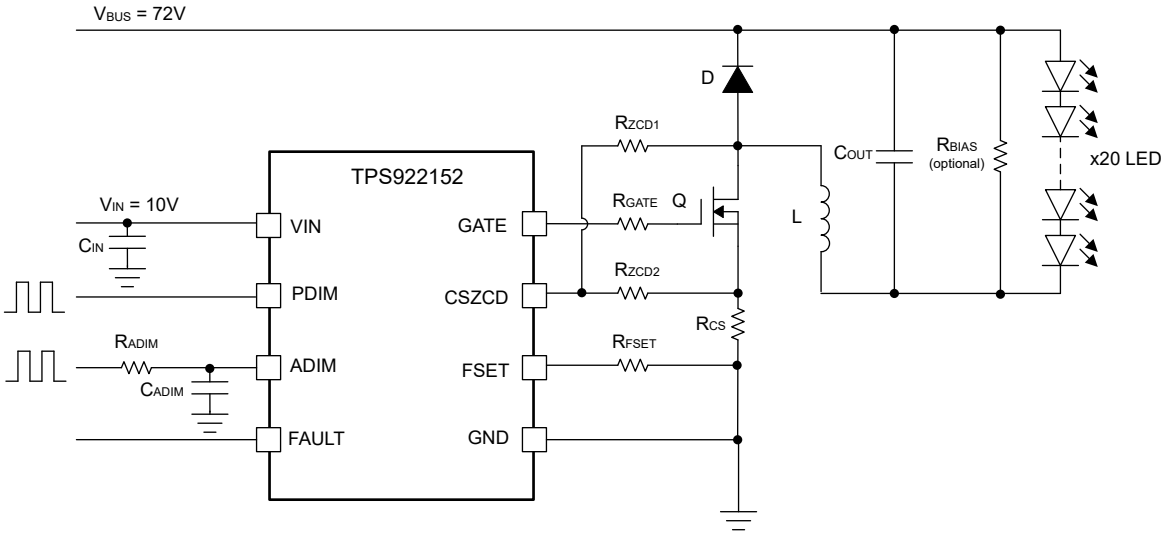


Figure 7-1. 60V Input Bus, 5A Output, 16-piece WLED, Buck AOT Mode Reference Design

7.2.1.1 Design Requirements

For this design example, use the parameters in the following table.

Table 7-1. Design Parameters

PARAMETER	VALUE
Input bus voltage range	60V ±10%
LED forward voltage	3.0 V
Output voltage	48V (3.0 × 16)
Maximum LED current	5A
Inductor current ripple	60% of maximum inductor current
LED current ripple	100mA or less
Dimming type	Analog dimming: 0.2V to 2.4V analog input at the ADIM pin; PWM dimming: 0% to 100% PWM input at the PDIM pin

Component Specs

- L = 33µH
- C_{IN} = 1µF
- C_{OUT} = 3.3µF
- R_{FSET} = 25kΩ
- R_{ZCD1} = 200kΩ
- R_{ZCD2} = 3.6kΩ
- R_{CS} = 40mΩ
- R_{GATE} = 5Ω

ADVANCE INFORMATION

7.2.1.2 Detailed Design Procedure

7.2.1.2.1 Inductor Selection

For this design, the input bus voltage is a 60V rail with 10% variation. The output is 16 white LEDs in series and the inductor current ripple by requirement is less than 60% of maximum inductor current. To select a proper peak-to-peak inductor current ripple, the low-side FET current limit must not be violated when the converter works in full-load condition. This requires half of the peak-to-peak inductor current ripple to be lower than that limit. Another consideration is to ensure reasonable inductor core loss and copper loss caused by the peak-to-peak current ripple. Once this peak-to-peak inductor current ripple is chosen, use Equation 8 to calculate the recommended value of the switching inductor L_{SW}.

$$L_{SW} = \frac{V_{LED} \times (V_{BUS\_MAX} - V_{LED})}{K_{IND} \times I_{LED\_MAX} \times F_{SW} \times V_{BUS\_MAX}} \quad (8)$$

where

- K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum inductor current.
- I_{LED_MAX} is the maximum LED current.
- F_{SW} is the switching frequency.
- V_{BUS_MAX} is the maximum input bus voltage.
- V_{LED} is the sum of the voltage across LED load.

With the chosen inductor value, the user can calculate the actual inductor current ripple using Equation 9.

$$I_{L\_RIP} = \frac{V_{LED} \times (V_{BUS\_MAX} - V_{LED})}{L_{SW} \times F_{SW} \times V_{BUS\_MAX}} \quad (9)$$

The ratings of inductor RMS current and saturation current must be greater than those seen in the system requirement. This is to maintain no inductor overheat or saturation occurring. During power up, transient conditions or fault conditions, the inductor current can exceed the normal operating current and reach the current limit. Therefore, selecting a saturation current rating equal to or greater than the converter current limit is preferred. The peak-inductor-current and RMS current equations are shown in Equation 10 and Equation 11.

$$I_{L\_PEAK} = I_{L\_MAX} + \frac{I_{L\_RIP}}{2} \quad (10)$$

$$I_{L\_RMS} = \sqrt{{I_{L\_MAX}}^2 + \frac{{I_{L\_RIP}}^2}{12}} \quad (11)$$

In this design, V_{BUS_MAX} = 66V, V_{LED} = 48V, I_{LED} = 5A, F_{SW} = 400kHz, select K_{IND} = 0.6, the calculated switching inductance is 38µH. A 33µH inductor is chosen. With this inductor, the ripple, peak, and rms currents of the inductor are 0.7A, 1.35A, and 1.02A, respectively.

7.2.1.2.2 Input Capacitor Selection

An input capacitor is required to reduce the surge current drawn from the gate driver. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of the low ESR and small temperature coefficients. For most applications, ti recommend to place a 10µF ceramic capacitor along with a 0.1µF capacitor from VIN to GND to provide high-frequency filtering. The input capacitor voltage rating must be greater than the maximum input voltage. Use Equation 12 to calculate the input capacitance, where Q_{GATE} is the total charge of switching FET, and K_{DR} is the derating coefficient of ceramic capacitance at the applied DC voltage.

$$C_{IN} > \frac{2 \times Q_{GATE}}{K_{DR} \times (V_{IN\_MIN} - V_{GATE\_MIN})} \quad (12)$$

In this design, a 1µF, 25V X7R ceramic capacitor and a 0.1µF, 50V X7R ceramic capacitor are chosen, yielding around 1V input ripple voltage at 10V input.

7.2.1.2.3 Output Capacitor Selection

The output capacitor reduces the high-frequency current ripple through the LED string. Excessive current ripple increases the RMS current in the LED string, therefore increasing the LED temperature.

1. Calculate the total dynamic resistance of the LED string (R_{LED}) using the LED manufacturer's data sheet.

2. Calculate the required impedance of the output capacitor (Z_{COUT}) given the acceptable peak-to-peak ripple current through the LED string, I_{LED_RIP} . I_{L_RIP} is the peak-to-peak inductor ripple current I_{L_MAX} is the inductor maximum current as calculated with the selected inductor.

3. Calculate the minimum effective output capacitance required.

4. Increase the output capacitance appropriately due to the derating effect of applied DC voltage.

See Equation 13, Equation 14, and Equation 15.

$$R_{LED} = \frac{\Delta V_F}{\Delta I_F} \times \#\ of\ LEDs \tag{13}$$

$$Z_{COUT} = \frac{R_{LED} \times I_{LED\_RIP}}{I_{L\_RIP} - I_{LED\_RIP}} \tag{14}$$

$$C_{OUT} = \frac{1}{2\pi \times F_{SW} \times K_{DR} \times Z_{COUT}} \tag{15}$$

Once the output capacitor is chosen, Equation 16 can be used to estimate the peak-to-peak ripple current through the LED string.

$$I_{LED\_RIP} = \frac{Z_{COUT} \times I_{L\_RIP}}{Z_{COUT} + R_{LED}} \tag{16}$$

CREE WLED is used here. The dynamic resistance of the LED is 0.67Ω at 3A forward current. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of the low ESR and small temperature coefficients. In this design, a 3.3µF, 100V X7R ceramic capacitor and a 0.1µF, 100V X7R ceramic capacitor are chosen. The calculated ripple current of the LED is about 100mA.

7.2.1.2.4 Sense Resistor Selection

The maximum LED current is 5A at 2.4V analog input and the corresponding V_{REF} is 200mV. By using Equation 2, select the resistors of the voltage divider R_{ZCD1} and R_{ZCD2} as 200kΩ and 3.6kΩ. By using Equation 2, the sense resistance is calculated as 100mΩ.

Note that the power consumption of the sense resistor is 400mW, requiring enough margin of the resistor's power rating in selection.

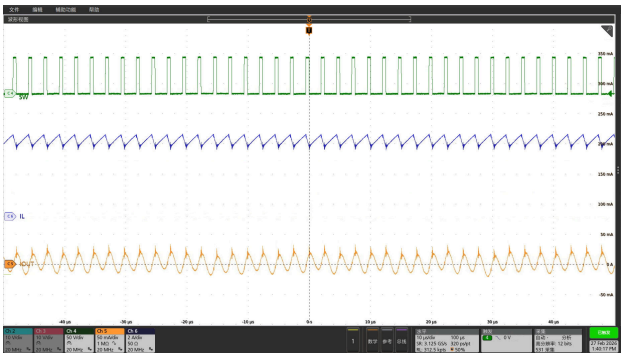
7.2.1.2.5 Other External Components Selection

In this design, a 5Ω resistor R_{GATE} is chosen between GATE pin and the switching FET gate to limit the gating current and switching slew rate. A 25kΩ resistor is used to set 400kHz switching frequency.

ADVANCE INFORMATION

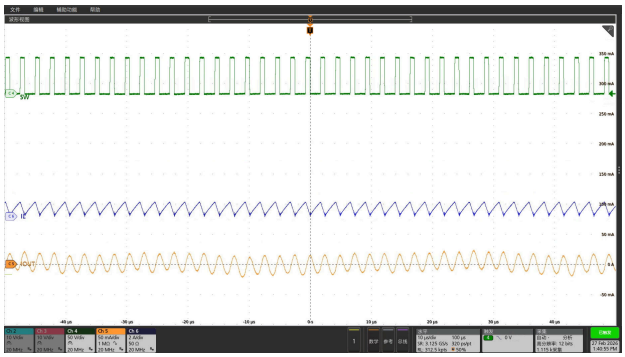
ADVANCE INFORMATION

7.2.1.3 Application Curves



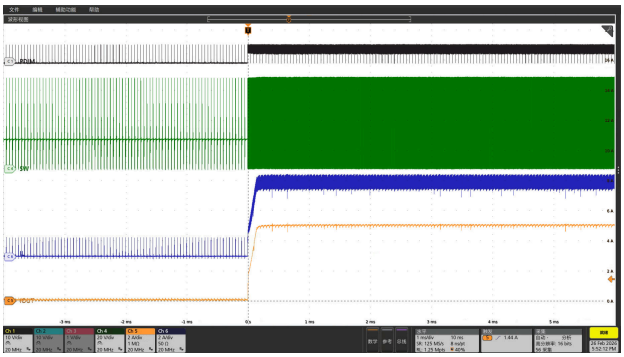
Green: SW, Blue: Inductor Current, Orange: LED Current Ripple (AC)

Figure 7-2. LED Current Ripple at ADIM = 2.4V and F_{SW} = 400kHz



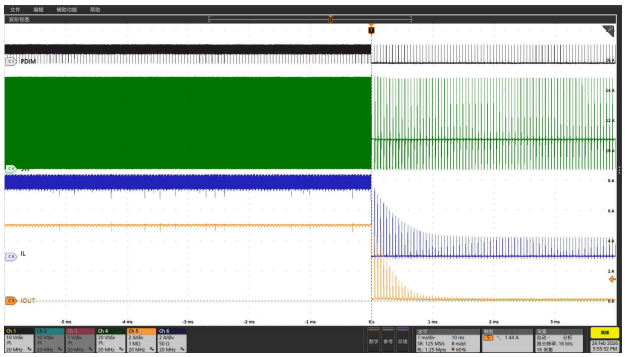
Green: SW, Blue: Inductor Current, Orange: LED Current Ripple (AC)

Figure 7-3. LED Current Ripple at ADIM = 0.42V and F_{SW} = 400kHz



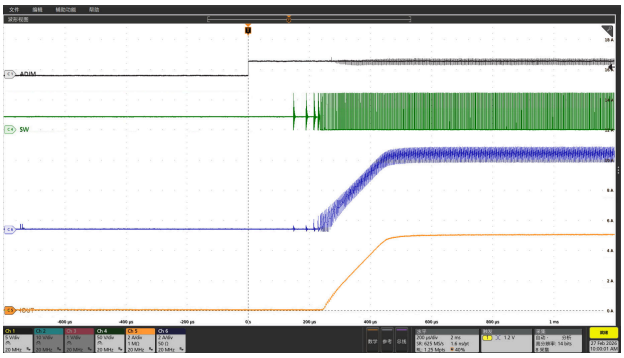
Black: PDIM, Green: SW, Blue: Inductor Current, Orange: LED Current

Figure 7-4. LED Current Transient for PDIM Transition from 1% to 99% @20kHz



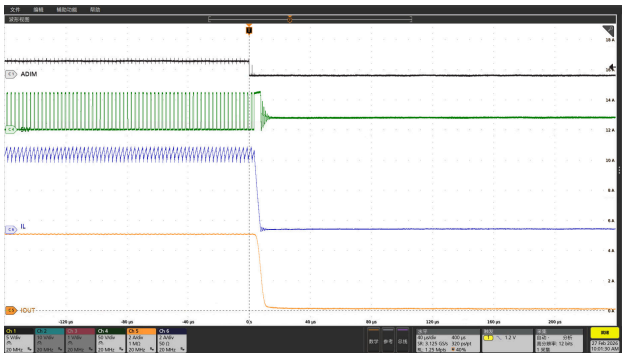
Black: PDIM, Green: SW, Blue: Inductor Current, Orange: LED Current

Figure 7-5. LED Current Transient for PDIM Transition from 99% to 1% @20kHz



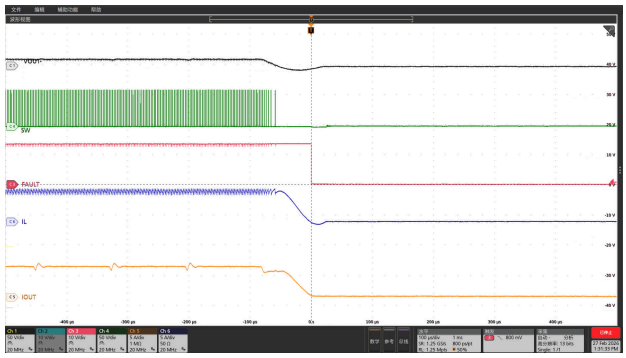
Black: ADIM, Green: SW, Blue: Inductor Current, Orange: LED Current

Figure 7-6. Start-Up at ADIM = 2.4V



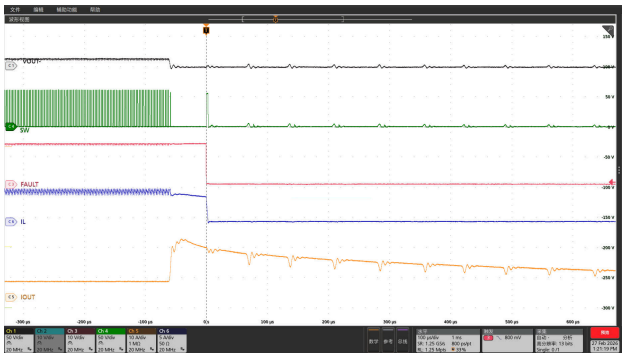
Black: ADIM, Green: SW, Blue: Inductor Current, Orange: LED Current

Figure 7-7. Shutdown at ADIM = 2.4V



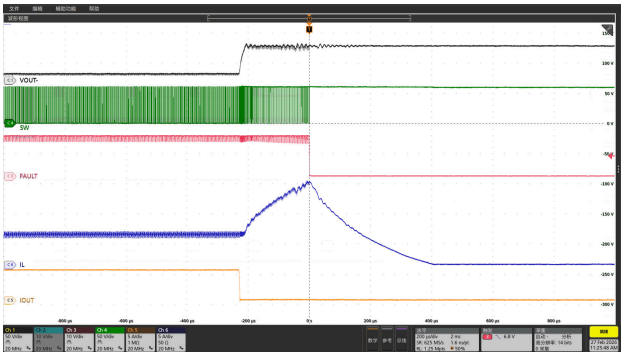
Black: VLED-, Green: SW, Red: FAULT, Blue: Inductor Current, Orange: LED Current

Figure 7-8. LED Open-Load Protection



Black: VLED-, Green: SW, Red: FAULT, Blue: Inductor Current, Orange: LED Current

Figure 7-9. LED– Short-to-PGND Protection



Black: VLED-, Green: SW, Red: FAULT, Blue: Inductor Current, Orange: LED Current

Figure 7-10. LED+ and LED– Short-Circuit Protection

ADVANCE INFORMATION

ADVANCE INFORMATION

7.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply ranging between 4.5V and 15V. This input supply must be well regulated. The device requires an input capacitor to reduce the surge current drawn from the input supply and the switching noise from the device. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 10µF capacitor is enough.

7.4 Layout

The TPS922152 and TPS922153 requires a proper layout for optimal performance. The following section gives some guidelines to ensure a proper layout.

7.4.1 Layout Guidelines

An example of a proper layout for the TPS922152 and TPS922153 device is shown in Figure 7-11.

- Creating a large GND plane for good electrical and thermal performance is important.
- The VIN and GND traces should be as wide as possible to reduce trace impedance. Wide traces have the additional advantage of providing excellent heat dissipation.
- Thermal vias can be used to connect the top-side GND plane to additional printed-circuit board (PCB) layers for heat dissipation and grounding.
- The input capacitors must be located as close as possible to the VIN pin and the GND pin.
- The GATE trace must be kept as short as possible to reduce parasitic inductance and thereby reduce noise injection. Short GATE trace also reduces radiated noise and EMI.
- Do not allow switching current to flow under the device.
- The routing of CSZCD trace is recommended to be kept as short as possible and placed away from the high-voltage switching trace and the ground shield.

7.4.2 Layout Example

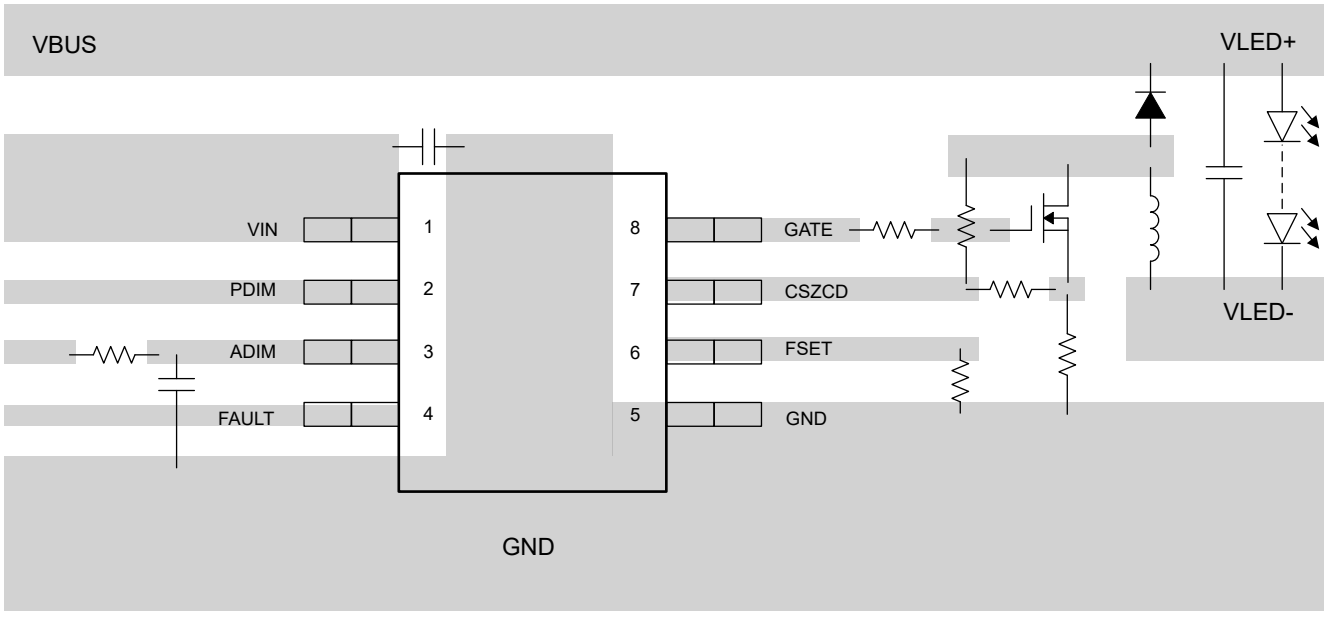


Figure 7-11. 8-Pin SOIC Top View Layout Example

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

DATE	REVISION	NOTES
July 2024	*	Advance Information release.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

ADVANCE INFORMATION

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025