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TS5A23166 0.9-Ω Dual-SPST Analog Switch
5-V and 3.3-V 2-Channel Analog Switch

1 Features

- Isolation in Powered-Down Mode, $V_+ = 0$
- Low ON-state resistance (0.9 Ω)
- Control inputs are 5.5-V Tolerant
- Low charge injection
- Excellent ON-state resistance matching
- Low total harmonic distortion (THD)
- 1.65-V to 5.5-V Single-supply operation
- Latch-up performance exceeds 100 mA per JESD 78, class II
- ESD Performance tested per JESD 22
  - 2000-V Human-body model (A114-B, Class II)
  - 1000-V Charged-device model (C101)

2 Applications

- Cell phones
- Portable instrumentation
- Audio and video signal routing
- Low-voltage data-acquisition systems
- Communication circuits
- Modems
- Hard Drives
- Computer Peripherals
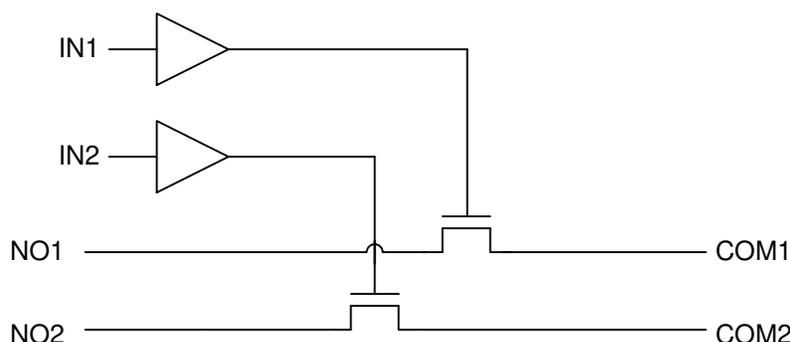- Wireless Terminals and Peripherals

3 Description

The TS5A23166 device is a dual single-pole single-throw (SPST) analog switch that is designed to operate from 1.65 V to 5.5 V. The TS5A23166 device offers a low ON-state resistance and an excellent channel-to-channel ON-state resistance matching. The TS5A23166 device has excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS5A23166	VSSOP (8)	2.30 mm × 2.00 mm
	DSBGA (8)	1.91 mm × 0.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (March 2018) to Revision J   **Page**

- Changed the *Thermal Information* table 4

Changes from Revision H (May 2015) to Revision I   **Page**

- Added Note: "Not tested in production" to leakage current at 25°C in the *Electrical Characteristics* tables......................... 4

Changes from Revision G (February 2013) to Revision H   **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- Updated document to new TI data sheet format - no specification changes. 1
- Removed *Ordering Information* table. 1
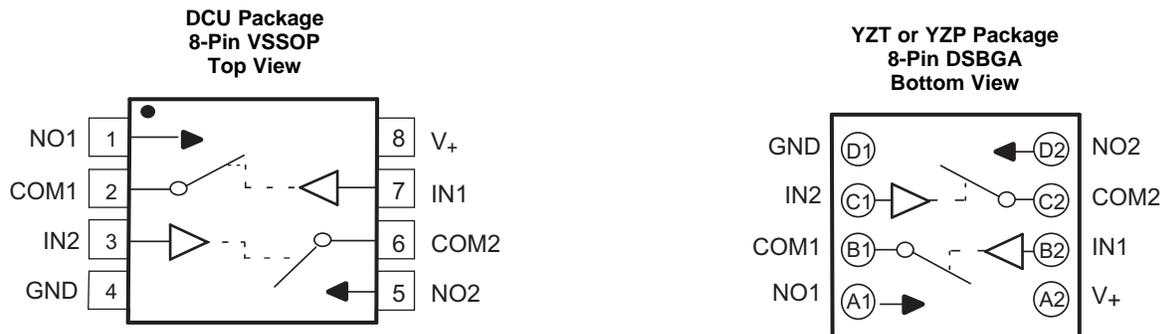
Changes from Revision F (September 2012) to Revision G   **Page**

- Changed pin numbers for YZT or YZP package pinout. 3

5 Pin Configuration and Functions

**DCU Package
8-Pin VSSOP
Top View**

**YZT or YZP Package
8-Pin DSBGA
Bottom View**

Pin Functions

PIN			TYPE	DESCRIPTION
NAME	TSSOP NO.	DSBGA NO.		
COM1	2	B1	I/O	Common port for switch 1
COM2	6	C2	I/O	Common port for switch 2
GND	4	D1	GND	Ground
IN1	7	B2	I	Active-high control pin connecting NO1 to COM1.
IN2	3	C1	I	Active-high control pin connecting NO2 to COM2.
NO1	1	A1	I/O	Normally open switch path 1
NO2	5	D2	I/O	Normally open switch path 2
V+	8	A2	PWR	Power supply pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1][2]

			MIN	MAX	UNIT
V_+	Supply voltage[3]		−0.5	6.5	V
V_{NO} V_{COM}	Analog voltage[3][4][5]		−0.5	$V_+ + 0.5$	V
I_K	Analog port diode current	$V_{NO}, V_{COM} < 0$	−50		mA
I_{NO} I_{COM}	ON-state switch current	$V_{NO}, V_{COM} = 0$ to V_+	−200	200	mA
	ON-state peak switch current[6]	$V_{NO}, V_{COM} = 0$ to V_+	−400	400	mA
V_I	Digital input voltage[3][4]		−0.5	6.5	V
I_{IK}	Digital input clamp current	$V_I < 0$	−50		mA
I_+	Continuous current through V_+			100	mA
I_{GND}	Continuous current through GND		−100	100	mA

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 5.5 V maximum.
(6) Pulse at 1-ms duration < 10% duty cycle.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	+2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	+1000	

(1)   JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2)   JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{I/O}$	Input/output voltage	0	V_+	V
V_+	Supply voltage	1.65	5.5	V
V_I	Control Input Voltage	0	5.5	V
T_A	Operating free-air temperature	−40	85	°C

6.4 Thermal Information

	THERMAL METRIC[1]	TS5A23166			UNIT
		DCU (VSSOP)	YZP (DSBGA)	YZT (DSBGA)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	212.2	99.9	99.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	77.6	1.0	1.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	91.7	27.8	27.8	°C/W
φ_{JT}	Junction-to-top characterization parameter	7.1	0.4	0.5	°C/W
φ_{JB}	Junction-to-board characterization parameter	91.1	27.8	27.7	°C/W

(1)   For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: 5-V Supply

V_+ = 4.5 V to 5.5 V, T_A = −40°C to 85°C (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
V_{COM}, V_{NO}	Analog signal					0		V_+	V
r_{peak}	Peak ON resistance	$0 \le V_{NO} \le V_+$, I_{COM} = −100 mA,	Switch ON, see Figure 11	25°C	4.5 V		0.9	1.1	Ω
				Full				1.2	
r_{on}	ON-state resistance	V_{NO} = 2.5 V, I_{COM} = −100 mA,	Switch ON, see Figure 11	25°C	4.5 V		0.75	0.9	Ω
				Full				1	
Δr_{on}	ON-state resistance match between channels	V_{NO} = 2.5 V, I_{COM} = −100 mA,	Switch ON, see Figure 11	25°C	4.5 V		0.04	0.1	Ω
				Full				0.1	
$r_{on(flat)}$	ON-state resistance flatness	$0 \le V_{NO} \le V_+$, I_{COM} = −100 mA,	Switch ON, see Figure 11	25°C	4.5 V		0.2		Ω
		V_{NO} = 1 V, 1.5 V, 2.5 V, I_{COM} = −100 mA,	Switch ON, see Figure 11	25°C			0.15	0.25	
				Full				0.25	
$I_{NO(OFF)}$	NO OFF leakage current	V_{NO} = 1 V, V_{COM} = 4.5 V, or V_{NO} = 4.5 V, V_{COM} = 1 V,	Switch OFF, see Figure 12	25°C	5.5 V	0 V	4	20[2]	nA
				Full		−150		150	
$I_{NO(PWROFF)}$		V_{NO} = 0 to 5.5 V, V_{COM} = 5.5 V to 0,	Switch OFF, see Figure 12	25°C	0 V	−10	0.2	10[2]	μA
				Full		−50		50	

(1)   The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(2)   Not tested in production.

Electrical Characteristics: 5-V Supply (continued)

V_+ = 4.5 V to 5.5 V, T_A = −40°C to 85°C (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
$I_{COM(OFF)}$	COM OFF leakage current	V_{COM} = 1 V, V_{NO} = 4.5 V, or V_{COM} = 4.5 V, V_{NO} = 1 V,	Switch OFF, see Figure 12	25°C	5.5 V	0 V	4	20[2]	nA
				Full		−150		150	
$I_{COM(PWROFF)}$		V_{COM} = 0 to 5.5 V, V_{NO} = 5.5 V to 0,	Switch OFF, see Figure 12	25°C	0 V	−10	0.2	10[2]	µA
				Full		−50		50	
$I_{NO(ON)}$	NO ON leakage current	V_{NO} = 1 V, V_{COM} = Open, or V_{NO} = 4.5 V, V_{COM} = Open,	Switch ON, see Figure 13	25°C	5.5 V	−5	0.4	5[2]	nA
				Full		−50		50	
$I_{COM(ON)}$	COM ON leakage current	V_{COM} = 1 V, V_{NO} = Open, or V_{COM} = 4.5 V, V_{NO} = Open,	Switch ON, see Figure 13	25°C	5.5 V	−5	0.4	5[2]	nA
				Full		−50		50	
Digital Control Inputs (IN1, IN2)[3]									
V_{IH}	Input logic high			Full		2.4		5.5	V
V_{IL}	Input logic low			Full		0		0.8	V
I_{IH}, I_{IL}	Input leakage current	V_I = 5.5 V or 0		25°C	5.5 V	−2	0.3	2	nA
				Full		−20		20	
Dynamic									
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, see Figure 19	25°C	5 V		6		pC
$C_{NO(OFF)}$	NO OFF capacitance	V_{NO} = V_+ or GND, Switch OFF,	See Figure 14	25°C	5 V		19		pF
$C_{COM(OFF)}$	COM OFF capacitance	V_{COM} = V_+ or GND, Switch OFF,	See Figure 14	25°C	5 V		18		pF
$C_{NO(ON)}$	NO ON capacitance	V_{NO} = V_+ or GND, Switch ON,	See Figure 14	25°C	5 V		35.5		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_+ or GND, Switch ON,	See Figure 14	25°C	5 V		35.5		pF
C_I	Digital input capacitance	V_I = V_+ or GND,	See Figure 14	25°C	5 V		2		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON,	See Figure 16	25°C	5 V		150		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz,	Switch OFF, see Figure 17	25°C	5 V		−62		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz,	Switch ON, see Figure 18	25°C	5 V		−85		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, see Figure 20	25°C	5 V		0.005%		
Supply									
I_+	Positive supply current	V_I = V_+ or GND,	Switch ON or OFF	25°C	5.5 V		0.01	0.1	µA
				Full				1	

(3) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.6 Electrical Characteristics: 3.3-V Supply

V_+ = 3 V to 3.6 V, T_A = −40°C to 85°C (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
V_{COM}, V_{NO}	Analog signal range					0		V_+	V
r_{peak}	Peak ON resistance	$0 \le V_{NO} \le V_+$, I_{COM} = −100 mA,	Switch ON, see Figure 11	25°C	3 V		1.3	1.6	Ω
				Full				1.8	
r_{on}	ON-state resistance	V_{NO} = 2 V, I_{COM} = −100 mA,	Switch ON, see Figure 11	25°C	3 V		1.1	1.5	Ω
				Full				1.7	
Δr_{on}	ON-state resistance match between channels	V_{NO} = 2 V, 0.8 V, I_{COM} = −100 mA,	Switch ON, see Figure 11	25°C	3 V		0.04	0.1	Ω
				Full				0.1	
$r_{on(flat)}$	ON-state resistance flatness	$0 \le V_{NO} \le V_+$, I_{COM} = −100 mA	Switch ON, see Figure 11	25°C	3 V		0.3		Ω
		V_{NO} = 2 V, 0.8 V, I_{COM} = −100 mA,	Switch ON, see Figure 11	25°C			0.15	0.25	
				Full				0.25	
$I_{NO(OFF)}$	NO OFF leakage current	V_{NO} = 1 V, V_{COM} = 3 V, or V_{NO} = 3 V, V_{COM} = 1 V,	Switch OFF, see Figure 12	25°C	3.6 V	−5	0.5	5[2]	nA
				Full		−50		50	
$I_{NO(PWROFF)}$		V_{NO} = 0 to 3.6 V, V_{COM} = 3.6 V to 0,	Switch OFF, see Figure 12	25°C	0 V	−5	0.1	5[2]	μA
				Full		−25		25	
$I_{COM(OFF)}$	COM OFF leakage current	V_{COM} = 1 V, V_{NO} = 3 V, or V_{COM} = 3 V, V_{NO} = 1 V,	Switch OFF, see Figure 12	25°C	3.6 V	−5	0.5	5[2]	nA
				Full		−50		50	
$I_{COM(PWROFF)}$		V_{COM} = 0 to 3.6 V, V_{NO} = 3.6 V to 0,	Switch OFF, see Figure 12	25°C	0 V	−5	0.1	5[2]	μA
				Full		−25		25	
$I_{NO(ON)}$	NO ON leakage current	V_{NO} = 1 V, V_{COM} = Open, or V_{NO} = 3 V, V_{COM} = Open,	Switch ON, see Figure 13	25°C	3.6 V	−2	0.3	2[2]	nA
				Full		−20		20	
$I_{COM(ON)}$	COM ON leakage current	V_{COM} = 1 V, V_{NO} = Open, or V_{COM} = 3 V, V_{NO} = Open,	Switch ON, see Figure 13	25°C	3.6 V	−2	0.3	2[2]	nA
				Full		−20		20	
Digital Control Inputs (IN1, IN2)[3]									
V_{IH}	Input logic high			Full		2		5.5	V
V_{IL}	Input logic low			Full		0		0.8	V
I_{IH}, I_{IL}	Input leakage current	V_I = 5.5 V or 0		25°C	3.6 V	−2	0.3	2	nA
				Full		−20		20	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(2) Not tested in production.
(3) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics: 3.3-V Supply (continued)

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, see Figure 19	25°C	5 V		6		pC
$C_{NO(OFF)}$	NO OFF capacitance	V_{NO} = V_+ or GND, Switch OFF,	See Figure 14	25°C	3.3 V		19.5		pF
$C_{COM(OFF)}$	COM OFF capacitance	V_{COM} = V_+ or GND, Switch OFF,	See Figure 14	25°C	3.3 V		18.5		pF
$C_{NO(ON)}$	NO ON capacitance	V_{NO} = V_+ or GND, Switch ON,	See Figure 14	25°C	3.3 V		36		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_+ or GND, Switch ON,	See Figure 14	25°C	3.3 V		36		pF
C_I	Digital input capacitance	V_I = V_+ or GND,	See Figure 14	25°C	3.3 V		2		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON,	See Figure 16	25°C	3.3 V		150		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz,	Switch OFF, see Figure 17	25°C	3.3 V		–62		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz,	Switch ON, see Figure 18	25°C	3.3 V		–85		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, see Figure 20	25°C	3.3 V		0.01%		
Supply									
I_+	Positive supply current	V_I = V_+ or GND,	Switch ON or OFF	25°C	3.6 V		0.001	0.05	µA
				Full				0.3	

6.7 Electrical Characteristics: 2.5-V Supply

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
V_{COM}, V_{NO}	Analog signal range					0		V_+	V
r_{peak}	Peak ON resistance	$0 \le V_{NO} \le V_+$, I_{COM} = –8 mA,	Switch ON, see Figure 11	25°C	2.3 V		1.8	2.4	Ω
				Full				2.6	
r_{on}	ON-state resistance	V_{NO} = 1.8 V, I_{COM} = –8 mA,	Switch ON, see Figure 11	25°C	2.3 V		1.2	2.1	Ω
				Full				2.4	
Δr_{on}	ON-state resistance match between channels	V_{NO} = 1.8 V, 0.8 V, I_{COM} = –8 mA,	Switch ON, see Figure 11	25°C	2.3 V		0.04	0.15	Ω
				Full				0.15	
$r_{on(flat)}$	ON-state resistance flatness	$0 \le V_{NO} \le V_+$, I_{COM} = –8 mA,	Switch ON, see Figure 11	25°C	2.3 V		0.7		Ω
		V_{NO} = 1.8 V, 0.8 V, I_{COM} = –8 mA,	Switch ON, see Figure 11	25°C			0.4	0.6	
				Full				0.6	
$I_{NO(OFF)}$	NO OFF leakage current	V_{NO} = 0.5 V, V_{COM} = 2.3 V, or V_{NO} = 2.3 V, V_{COM} = 0.5 V,	Switch OFF, see Figure 12	25°C	2.7 V	–5	0.3	5[2]	nA
				Full		–50		50	
$I_{NO(PWROFF)}$		V_{NO} = 0 to 2.7 V, V_{COM} = 2.7 V to 0,	Switch OFF, see Figure 12	25°C	0 V	–2	0.05	2[2]	µA
				Full		–15		15	

(1) The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.
(2) Not tested in production.

Electrical Characteristics: 2.5-V Supply (continued)

V_+ = 2.3 V to 2.7 V, T_A = −40°C to 85°C (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
$I_{COM(OFF)}$	COM OFF leakage current	V_{NO} = 2.3 V, V_{COM} = 0.5 V, or V_{NO} = 0.5 V, V_{COM} = 2.3 V,	Switch OFF, see Figure 12	25°C	2.7 V	−5	0.3	5[2]	nA
				Full		−50		50	
$I_{COM(PWROFF)}$		V_{COM} = 0 to 2.7 V, V_{NO} = 2.7 V to 0,	Switch OFF, see Figure 12	25°C	0 V	−2	0.05	2[2]	µA
				Full		−15		15	
$I_{NO(ON)}$	NO ON leakage current	V_{NO} = 0.5 V, V_{COM} = Open, or V_{NO} = 2.3 V, V_{COM} = Open,	Switch ON, see Figure 13	25°C	2.7 V	−2	0.3	2[2]	nA
				Full		−20		20	
$I_{COM(ON)}$	COM ON leakage current	V_{COM} = 0.5 V, V_{NO} = Open, or V_{COM} = 2.3 V, V_{NO} = Open,	Switch ON, see Figure 13	25°C	2.7 V	−2	0.3	2[2]	nA
				Full		−20		20	
Digital Control Inputs (IN1, IN2)									
V_{IH}	Input logic high			Full		1.8		5.5	V
V_{IL}	Input logic low			Full		0		0.6	V
I_{IH}, I_{IL}	Input leakage current	V_I = 5.5 V or 0		25°C	2.7 V	−2	0.3	2	nA
				Full		−20		20	
Dynamic									
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, see Figure 19	25°C	2.5 V		4		pC
$C_{NO(OFF)}$	NO OFF capacitance	V_{NO} = V_+ or GND, Switch OFF,	See Figure 14	25°C	2.5 V		19.5		pF
$C_{COM(OFF)}$	COM OFF capacitance	V_{COM} = V_+ or GND, Switch OFF,	See Figure 14	25°C	2.5 V		18.5		pF
$C_{NO(ON)}$	NO ON capacitance	V_{NO} = V_+ or GND, Switch ON,	See Figure 14	25°C	2.5 V		36.5		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_+ or GND, Switch ON,	See Figure 14	25°C	2.5 V		36.5		pF
C_I	Digital input capacitance	V_I = V_+ or GND,	See Figure 14	25°C	2.5 V		2		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON,	See Figure 16	25°C	2.5 V		150		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz,	Switch OFF, see Figure 17	25°C	2.5 V		−62		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz,	Switch ON, see Figure 18	25°C	2.5 V		−85		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, see Figure 20	25°C	2.5 V		0.02%		
Supply									
I_+	Positive supply current	V_I = V_+ or GND,	Switch ON or OFF	25°C	2.7 V		0.001	0.02	µA
				Full				0.25	

6.8 Electrical Characteristics: 1.8-V Supply

V_+ = 1.65 V to 1.95 V, T_A = −40°C to 85°C (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
V_{COM}, V_{NO}	Analog signal range					0		V_+	V
r_{peak}	Peak ON resistance	$0 \le V_{NO} \le V_+$, I_{COM} = −2 mA,	Switch ON, see Figure 11	25°C	1.65 V		4.2	25	Ω
				Full				30	
r_{on}	ON-state resistance	V_{NO} = 0.6 V, 1.5 V, I_{COM} = −2 mA,	Switch ON, see Figure 11	25°C	1.65 V		1.6	3.9	Ω
				Full				4	
Δr_{on}	ON-state resistance match between channels	V_{NO} = 1.5 V, I_{COM} = −2 mA,	Switch ON, see Figure 11	25°C	1.65 V		0.04	0.2	Ω
				Full				0.2	
$r_{on(flat)}$	ON-state resistance flatness	$0 \le V_{NO} \le V_+$, I_{COM} = −2 mA,	Switch ON, see Figure 11	25°C	1.65 V		2.8		Ω
		V_{NO} = 0.6 V, 1.5 V, I_{COM} = −2 mA,	Switch ON, see Figure 11	25°C			4.1	22	
				Full				27	
$I_{NO(OFF)}$	NO OFF leakage current	V_{NO} = 0.3 V, V_{COM} = 1.65 V, or V_{NO} = 1.65 V, V_{COM} = 0.3 V,	Switch OFF, see Figure 12	25°C	1.95 V	−5	0.3	5[2]	nA
				Full		−50		50	
$I_{NO(PWROFF)}$		V_{NO} = 0 to 1.95 V, V_{COM} = 1.95 V to 0,	Switch OFF, see Figure 12	25°C	0 V	−2	0.05	2[2]	μA
				Full		−10		10	
$I_{COM(OFF)}$	COM OFF leakage current	V_{NO} = 1.65 V, V_{COM} = 0.3 V, or V_{NO} = 0.3 V, V_{COM} = 1.65 V,	Switch OFF, see Figure 12	25°C	1.95 V	−5	0.3	5[2]	nA
				Full		−50		50	
$I_{COM(PWROFF)}$		V_{COM} = 0 to 1.95 V, V_{NO} = 1.95 V to 0,	Switch OFF, see Figure 12	25°C	0 V	−2	0.05	[2]2	μA
				Full		−10		10	
$I_{NO(ON)}$	NO ON leakage current	V_{NO} = 0.3 V, V_{COM} = Open, or V_{NO} = 1.65 V, V_{COM} = Open,	Switch ON, see Figure 13	25°C	1.95 V	−2	0.3	2[2]	nA
				Full		−20		20	
$I_{COM(ON)}$	COM ON leakage current	V_{NO} = Open, V_{COM} = 0.3 V, or V_{NO} = Open, V_{COM} = 1.65 V,	Switch ON, see Figure 13	25°C	1.95 V	−2	0.3	2	nA
				Full		−20		20	
Digital Control Inputs (IN1, IN2)									
V_{IH}	Input logic high			Full		1.5		5.5	V
V_{IL}	Input logic low			Full		0		0.6	V
I_{IH}, I_{IL}	Input leakage current	V_I = 5.5 V or 0		25°C	1.95 V	−2	0.3	2	μA
				Full		−20		20	
Dynamic									
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, see Figure 19	25°C	1.8 V		2		pC
$C_{NO(OFF)}$	NO OFF capacitance	V_{NO} = V_+ or GND, Switch OFF,	See Figure 14	25°C	1.8 V		19.5		pF
$C_{COM(OFF)}$	COM OFF capacitance	V_{COM} = V_+ or GND, Switch OFF,	See Figure 14	25°C	1.8 V		18.5		pF
$C_{NO(ON)}$	NO ON capacitance	V_{NO} = V_+ or GND, Switch ON,	See Figure 14	25°C	1.8 V		36.5		pF

(1)   The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.
(2)   Not tested in production.

Electrical Characteristics: 1.8-V Supply (continued)

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_+ or GND, Switch ON,	See Figure 14	25°C	1.8 V		36.5		pF
C_I	Digital input capacitance	V_I = V_+ or GND,	See Figure 14	25°C	1.8 V		2		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON,	See Figure 16	25°C	1.8 V		150		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz,	Switch OFF, see Figure 17	25°C	1.8 V		–62		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, see Figure 20	25°C	1.8 V		0.055%		
Supply									
I_+	Positive supply current	V_I = V_+ or GND,	Switch ON or OFF	25°C	1.95 V		0.001	0.01	μA
				Full				0.15	

6.9 Switching Characteristics: 5-V Supply

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
t_{ON}	Turnon time	V_{COM} = V_+, R_L = 50 Ω,	C_L= 35 pF, see Figure 15	25°C	5 V	1	4.5	7.5	ns
				Full	4.5 V to 5.5 V	1		9	
t_{OFF}	Turnoff time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 15	25°C	5 V	4.5	8	11	ns
				Full	4.5 V to 5.5 V	3.5		13	

(1) The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

6.10 Switching Characteristics: 3.3-V Supply

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
t_{ON}	Turnon time	V_{COM} = V_+, R_L = 50 Ω,	C_L= 35 pF, see Figure 15	25°C	3.3 V	1.5	5	9.5	ns
				Full	3 V to 3.6 V	1		10	
t_{OFF}	Turnoff time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 15	25°C	3.3 V	4.5	8.5	11	ns
				Full	3 V to 3.6 V	3		12.5	

(1) The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

6.11 Switching Characteristics: 2.5-V Supply

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
t_{ON}	Turnon time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 15	25°C	2.5 V	2	6	10	ns
				Full	2.3 V to 2.7 V	1		12	
t_{OFF}	Turnoff time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 15	25°C	2.5 V	4.5	8	12.5	ns
				Full	2.3 V to 2.7 V	3		15	

(1) The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

6.12 Switching Characteristics: 1.8-V Supply

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted) [1]

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
t_{ON}	Turnon time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 15	25°C	1.8 V	3	9	18	ns
				Full	1.65 V to 1.95 V	1		20	
t_{OFF}	Turnoff time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 15	25°C	1.8 V	5	10	15.5	ns
				Full	1.65 V to 1.95 V	4		18.5	

(1)   The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

6.13 Typical Characteristics
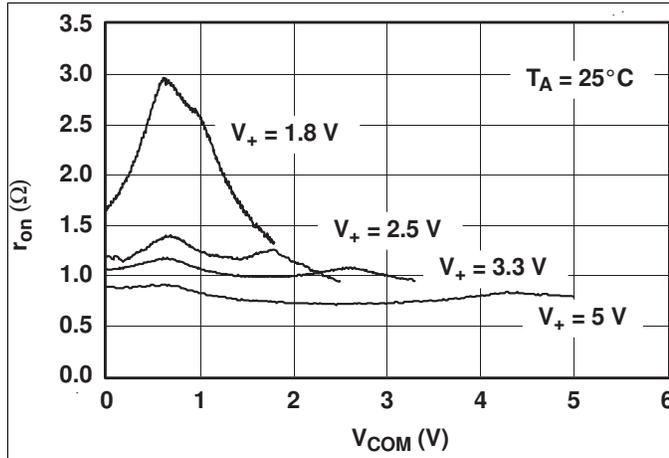
Figure 1. r_{on} vs V_{COM}
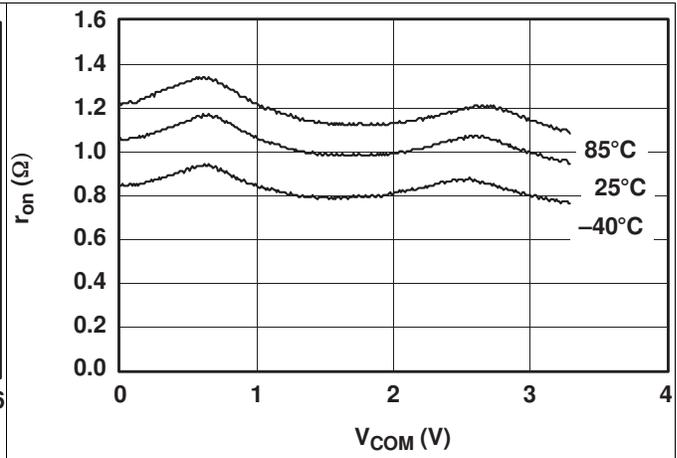
Figure 2. r_{on} vs V_{COM} (V_+ = 3.3 V)
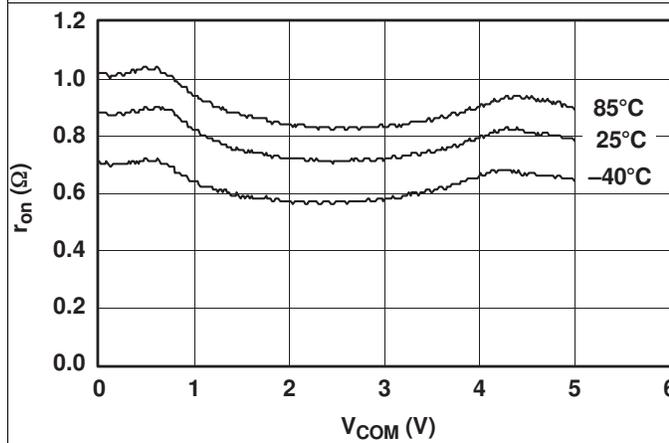
Figure 3. r_{on} vs V_{COM} (V_+ = 5 V)
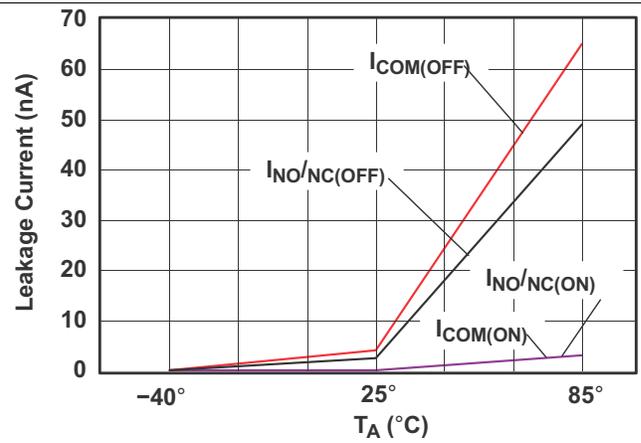
Figure 4. Leakage Current vs Temperature (V_+ = 5.5 V)
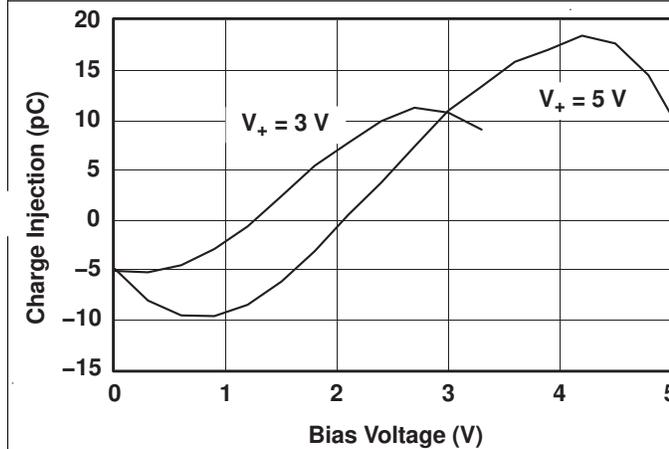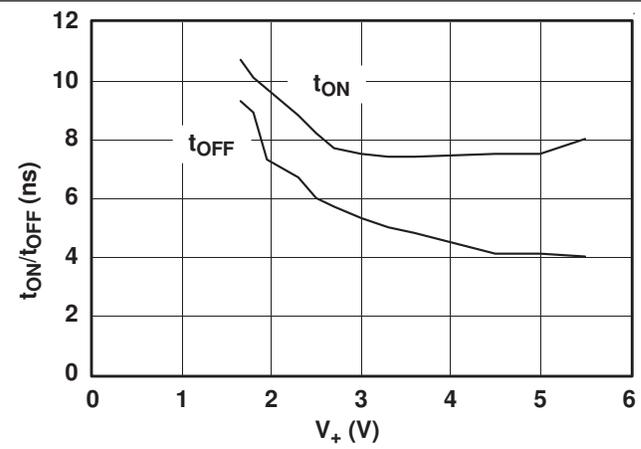
Figure 5. Charge Injection (Q_C) vs V_{COM}

Figure 6. t_{ON} and t_{OFF} vs Supply Voltage
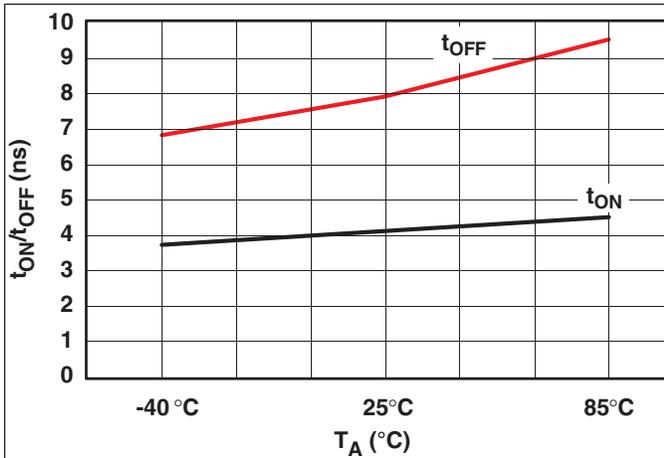
Typical Characteristics (continued)

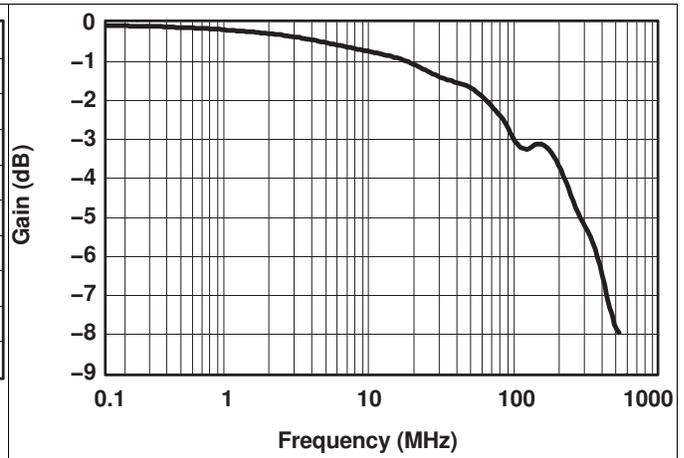Figure 7. t$_{ON}$ and t$_{OFF}$ vs Temperature (V$_+$ = 5 V)
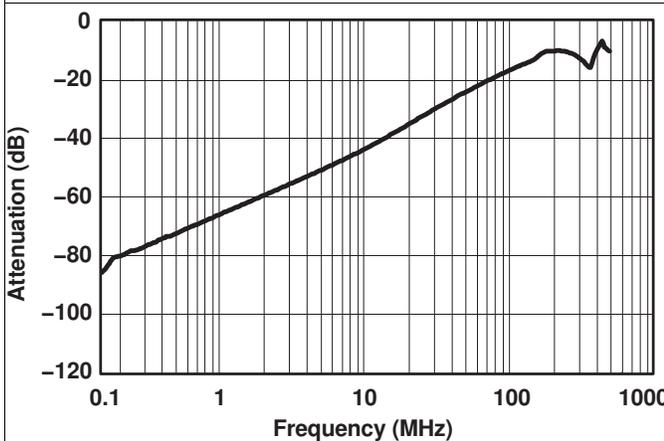

Figure 8. Bandwidth (V$_+$ = 5 V)

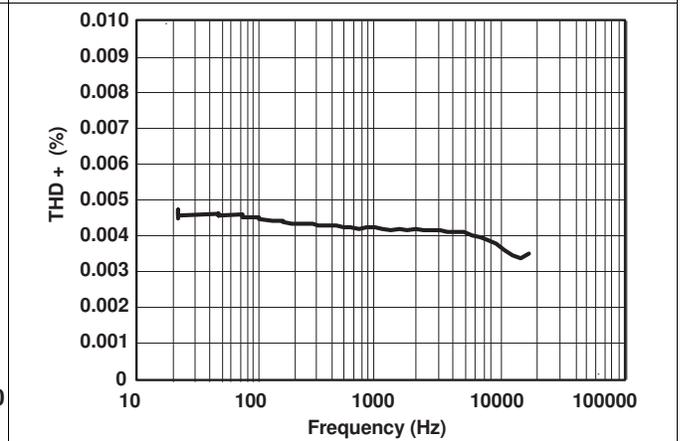Figure 9. OFF Isolation and Crosstalk (V$_+$ = 5 V)

Figure 10. Total Harmonic Distortion vs Frequency

Product Folder Links: *TS5A23166*

7 Parameter Measurement Information

Channel ON

$$r_{on} = \frac{V_{COM} - V_{NO}}{I_{COM}} \, \Omega$$

$V_I = V_{IH}$ or V_{IL}
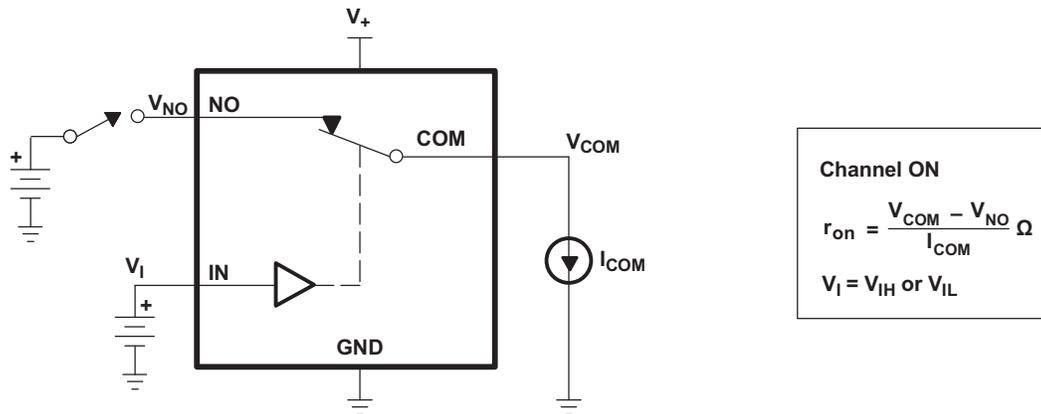
Figure 11. ON-State Resistance (r_{on})

**OFF-State Leakage Current
Channel OFF**
$V_I = V_{IH}$ or V_{IL}

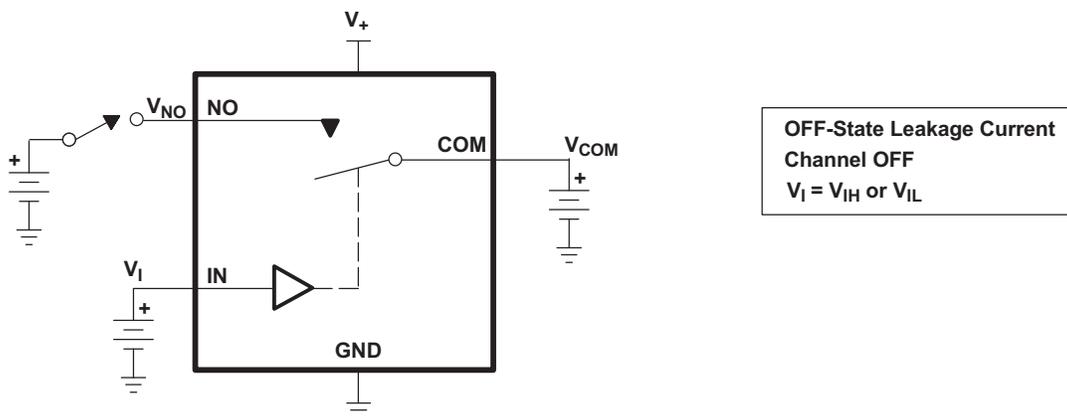**Figure 12. OFF-State Leakage Current ($I_{COM(OFF)}$, $I_{NC(OFF)}$, $I_{COM(PWROFF)}$, $I_{NC(PWR(FF)}$)**

**ON-State Leakage Current
Channel ON**
$V_I = V_{IH}$ or V_{IL}
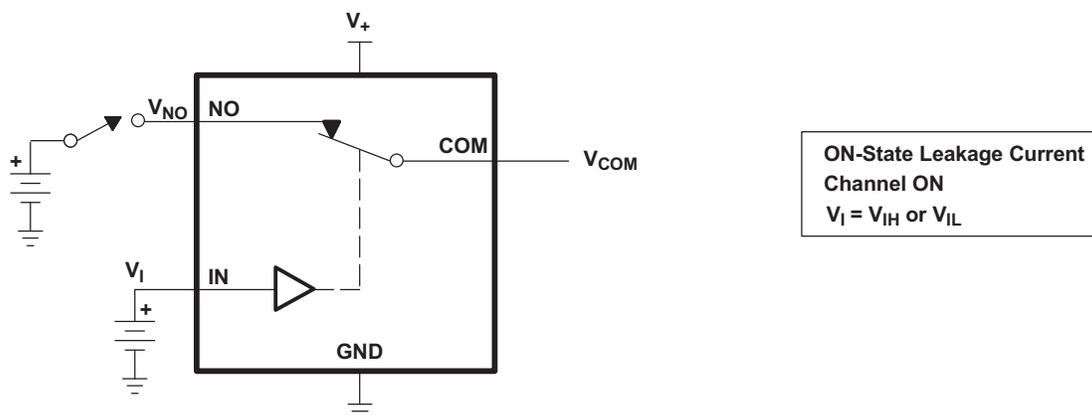
Figure 13. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$)

Product Folder Links: *TS5A23166*
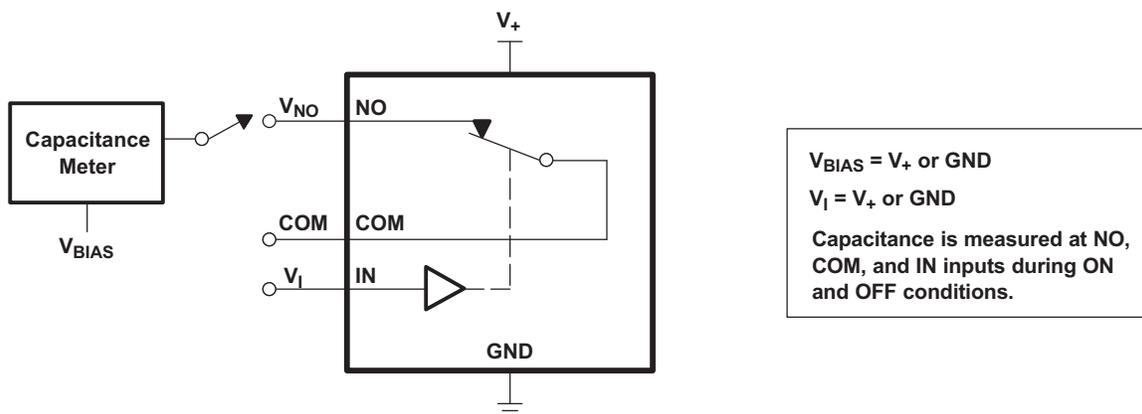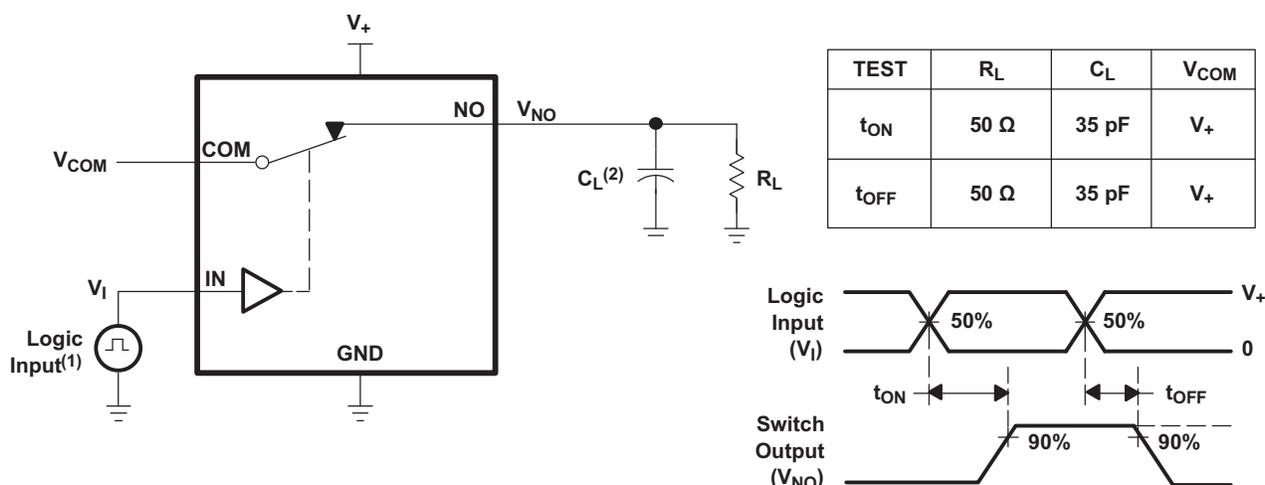
Parameter Measurement Information (continued)

Figure 14. Capacitance (C_I, $C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NC(ON)}$)

(1) All input pulses are supplied by generators having the following characteristics:
PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

(2) C_L includes probe and jig capacitance.

Figure 15. Turnon (t_{ON}) and Turnoff Time (t_{OFF})

Figure 16. Bandwidth (BW)

Product Folder Links: *TS5A23166*
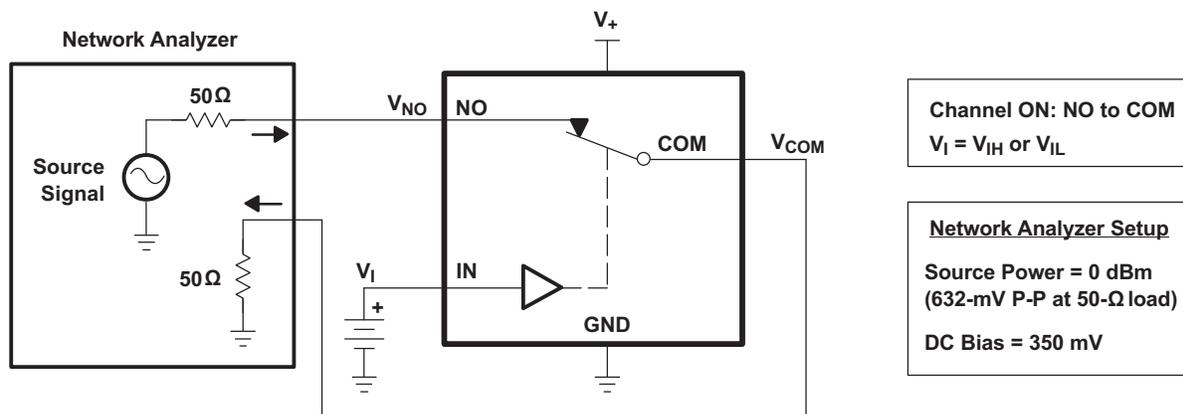
Parameter Measurement Information (continued)

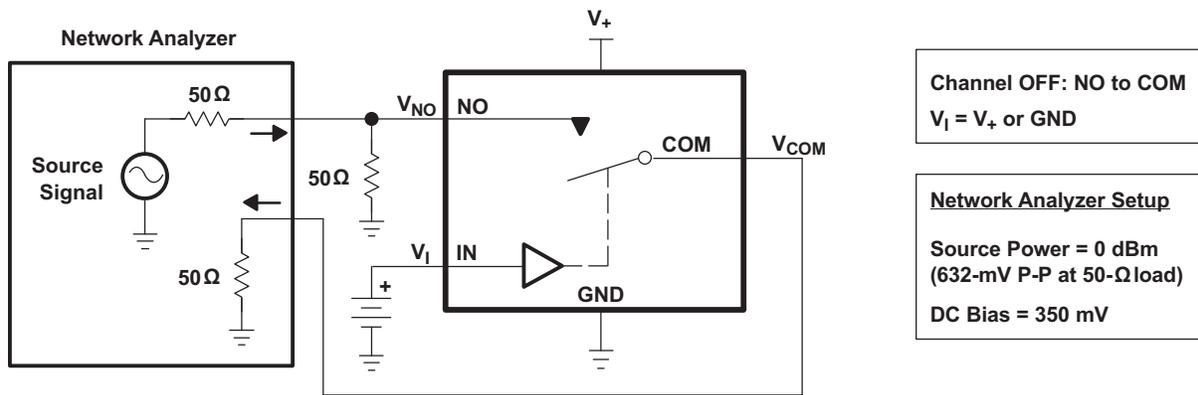**Figure 17. OFF Isolation (O_{ISO})**

Network Analyzer

$50\,\Omega$

Source
Signal

$50\,\Omega$

$50\,\Omega$

V_{NO} NO

V_+

COM V_{COM}

V_I IN

GND

Channel OFF: NO to COM

$V_I = V_+$ or GND

Network Analyzer Setup

Source Power = 0 dBm
(632-mV P-P at 50-Ω load)

DC Bias = 350 mV

Figure 18. Crosstalk (X_{TALK})

Network Analyzer

$50\,\Omega$

Source
Signal

$50\,\Omega$

V_{NO1} NO1

V_{NO2} NO2

V_I IN

V_+

COM1

COM2 $50\,\Omega$

GND

Channel ON: NO to COM

Network Analyzer Setup

Source Power = 0 dBm
(632-mV P-P at 50-Ω load)

DC Bias = 350 mV

Figure 19. Charge Injection (Q_C)

R_{GEN} NO

V_{GEN}

V_I IN

Logic
Input[2]

V_+

COM V_{COM}

C_L[1]

GND

Logic
Input
(V_I)   OFF   ON   OFF

V_{IH}

V_{IL}

V_{COM}

ΔV_{COM}

$V_{GEN} = 0$ to V_+
$R_{GEN} = 0$
$C_L = 1$ nF
$Q_C = C_L \times \Delta V_{COM}$
$V_I = V_{IH}$ or V_{IL}
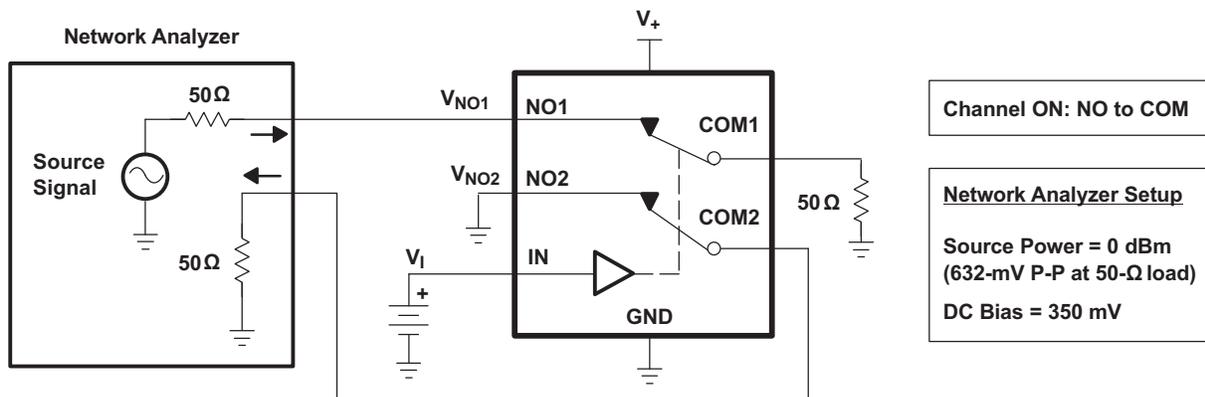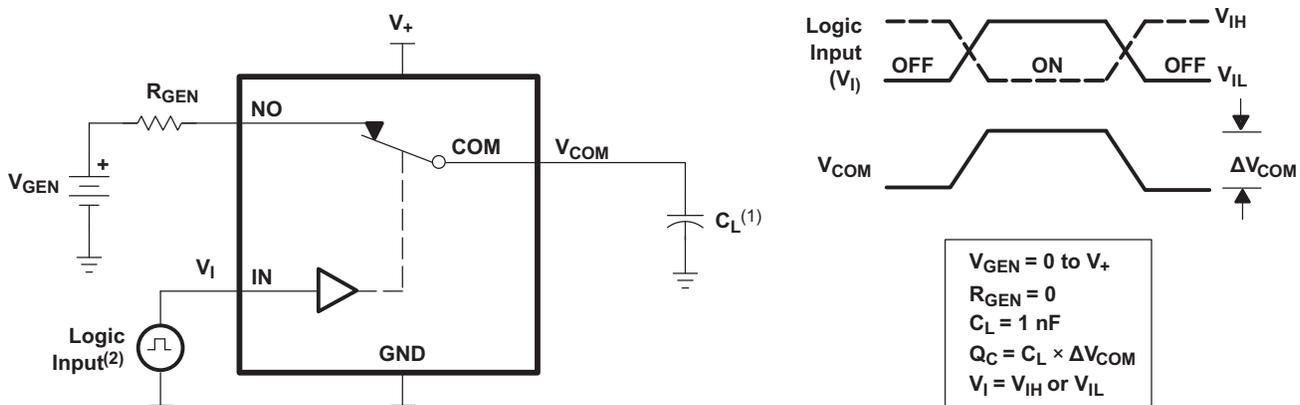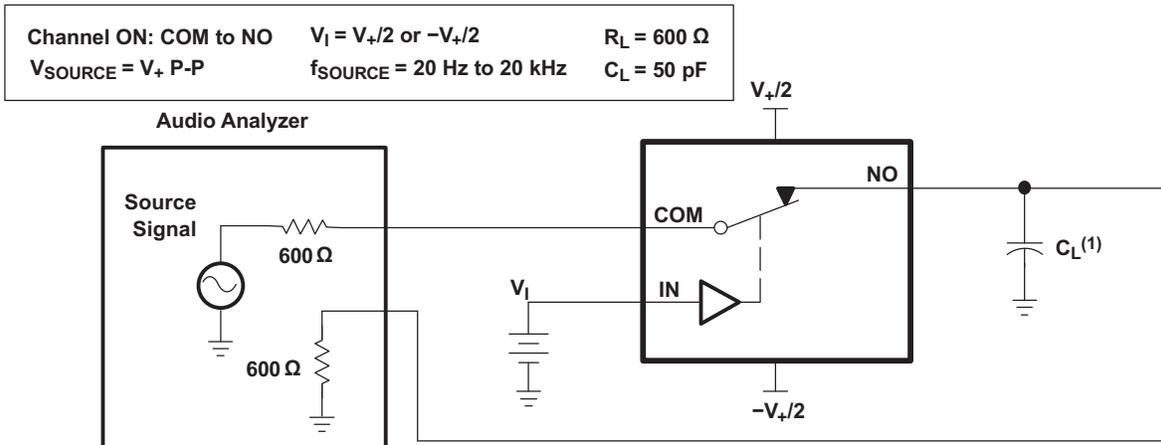
(1) C_L includes probe and jig capacitance.

(2)   All input pulses are supplied by generators having the following characteristics:
      PRR ≤ 10 MHz, $Z_O = 50\ \Omega$, $t_r < 5$ ns, $t_f < 5$ ns.

Parameter Measurement Information (continued)



(1) C_L includes probe and jig capacitance.

Figure 20. Total Harmonic Distortion (THD)

8 Detailed Description

8.1 Overview

The TS5A23166 is a dual single-pole single-throw (SPST) analog switch that is designed to operate from 1.65 V to 5.5 V. The device offers a low ON-state resistance. The device has excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications. Table 2 shows the descriptions of each parameter specified in the datasheet.

8.2 Functional Block Diagram
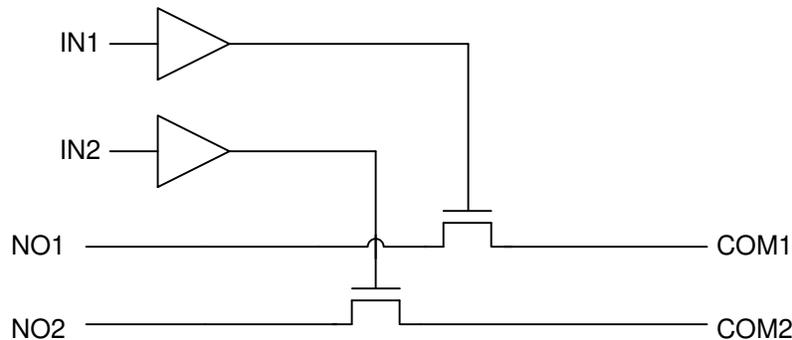
8.3 Feature Description

Tolerant control inputs allow 5-V logic levels to be present on the IN pin at any value of V_{CC}. Low ON-resistance allows minimal signal distortion through device.

8.4 Device Functional Modes

Table 1 shows the functional modes for TS5A23166.

Table 1. Function Table

IN	NO TO COM, COM TO NO
L	OFF
H	ON

9 Application and Implementation

> **NOTE**
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TS5A23166 dual SPST analog switch is a basic component that could be used in any electrical system design. One example application is a gain selector, which is described in the *Typical Application* section.
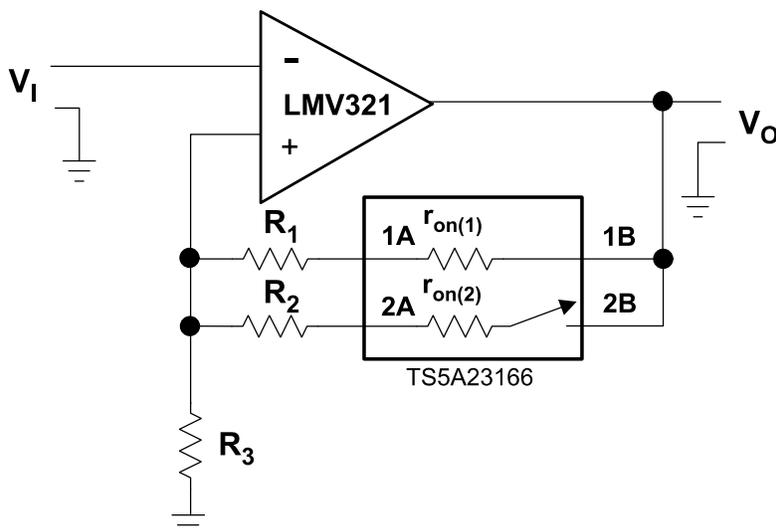
9.2 Typical Application

Figure 21. Gain-Control Circuit for OP Amplifier

9.2.1 Design Requirements

By selecting values of R1 and R2, such that Rx >> $r_{on(x)}$, r_{on} of TS5A23166 can be ignored. The gain of op amp can be calculated as follow:

Vo / VI = 1+ R|| / R3   (1)

R|| = (R1+$r_{on(1)}$) || (R2+$r_{on(2)}$)   (2)

9.2.2 Detailed Design Procedure

Place a switch in series with the input of the op amp. Because the op amp input impedance is very large, a switch on $r_{on(1)}$ is irrelevant.

Typical Application (continued)
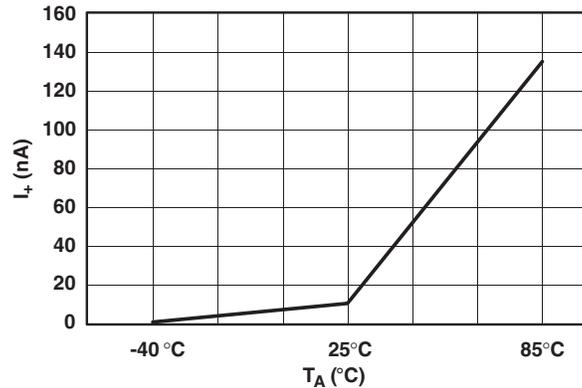
9.2.3 Application Curve

Figure 22. Power-Supply Current vs Temperature (V₊ = 5 V)

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF bypass capacitor is recommended. If there are multiple pins labeled V_{CC}, then a 0.01-µF or 0.022-µF capacitor is recommended for each V_{CC} because the VCC pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1-µF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self−inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. Figure 23 shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.
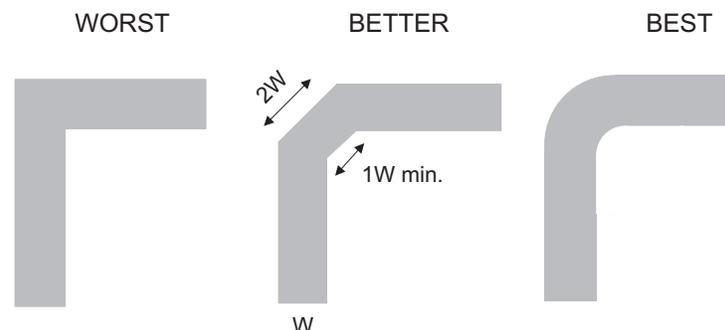
11.2 Layout Example

Figure 23. Trace Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

Table 2. Parameter Description

SYMBOL	DESCRIPTION
V_{COM}	Voltage at COM
V_{NO}	Voltage at NO
r_{on}	Resistance between COM and NO ports when the channel is ON
r_{peak}	Peak on-state resistance over a specified voltage range
$r_{on(flat)}$	Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF-state under worst-case input and output conditions
$I_{NO(PWROFF)}$	Leakage current measured at the NO port during the power-down condition, $V_+ = 0$
$I_{COM(OFF)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO) in the OFF-state under worst-case input and output conditions
$I_{COM(PWROFF)}$	Leakage current measured at the COM port during the power-down condition, $V_+ = 0$
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON-state and the output (COM) open
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO) in the ON-state and the output (NO) open
V_{IH}	Minimum input voltage for logic high for the control input (IN)
V_{IL}	Maximum input voltage for logic low for the control input (IN)
V_I	Voltage at the control input (IN)
I_{IH}, I_{IL}	Leakage current measured at the control input (IN)
t_{ON}	Turnon time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning ON.
t_{OFF}	Turnoff time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning OFF.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NO or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$, C_L is the load capacitance, and ΔV_{COM} is the change in analog output voltage.
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
$C_{COM(OFF)}$	Capacitance at the COM port when the corresponding channel (COM to NO) is OFF
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NO) is ON
C_I	Capacitance of control input (IN)
O_{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NO to COM) in the OFF state.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic.
I_+	Static power-supply current with the control (IN) pin at V_+ or GND

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: *TS5A23166*

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS5A23166DCUR	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(AM, JAMQ, JAMR) JZ
TS5A23166DCUR.B	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(AM, JAMQ, JAMR) JZ
TS5A23166DCURG4	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JAMR
TS5A23166DCURG4.B	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JAMR
TS5A23166YZPR	Active	Production	DSBGA (YZP) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	JMN
TS5A23166YZPR.B	Active	Production	DSBGA (YZP) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	JMN
TS5A23166YZTR	Active	Production	DSBGA (YZT) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	JMN
TS5A23166YZTR.B	Active	Production	DSBGA (YZT) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	JMN

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
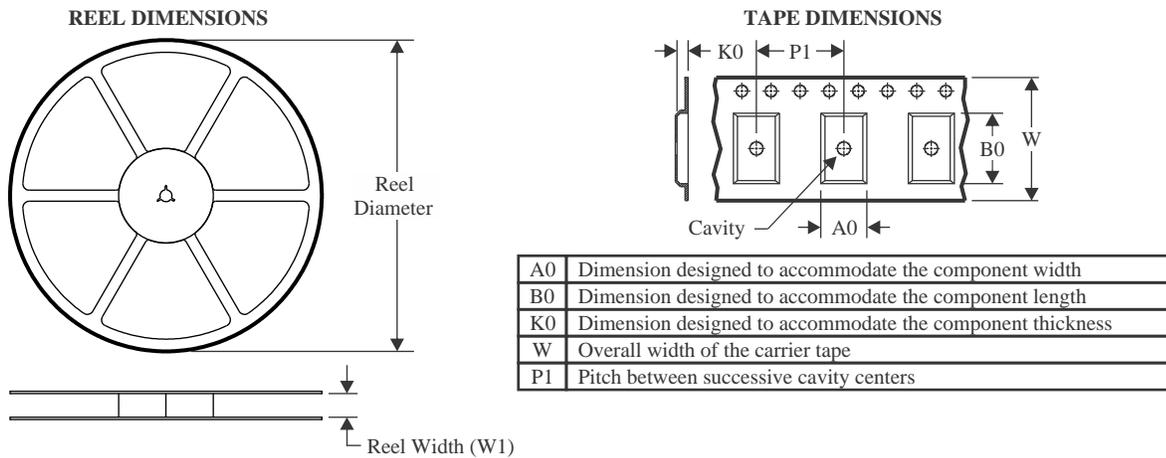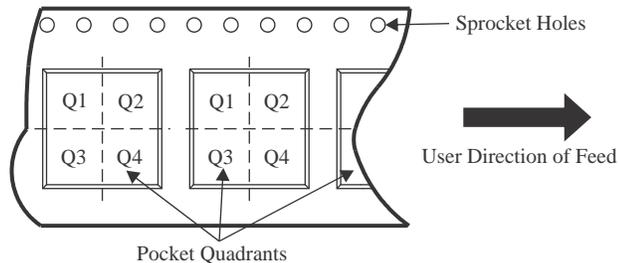
(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A23166DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TS5A23166DCUR	VSSOP	DCU	8	3000	178.0	9.5	2.25	3.35	1.05	4.0	8.0	Q3
TS5A23166DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TS5A23166YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1
TS5A23166YZTR	DSBGA	YZT	8	3000	178.0	9.2	1.02	2.02	0.75	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A23166DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
TS5A23166DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
TS5A23166DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
TS5A23166YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0
TS5A23166YZTR	DSBGA	YZT	8	3000	220.0	220.0	35.0

3.2 / 3.0 TYP

A

PIN 1 INDEX AREA

6X 0.5

8

1

2X 1.5

2.1 / 1.9 NOTE 3

4

5

8X 0.25 / 0.17

⊕ 0.08 Ⓜ C A B

B

2.4 / 2.2 NOTE 3

C

⌒ 0.1 C

SEATING PLANE

SEE DETAIL A

(0.13) TYP

0.12 GAGE PLANE

0° -6°

0.35 / 0.20

0.9 / 0.6

0.1 / 0.0

DETAIL A
TYPICAL
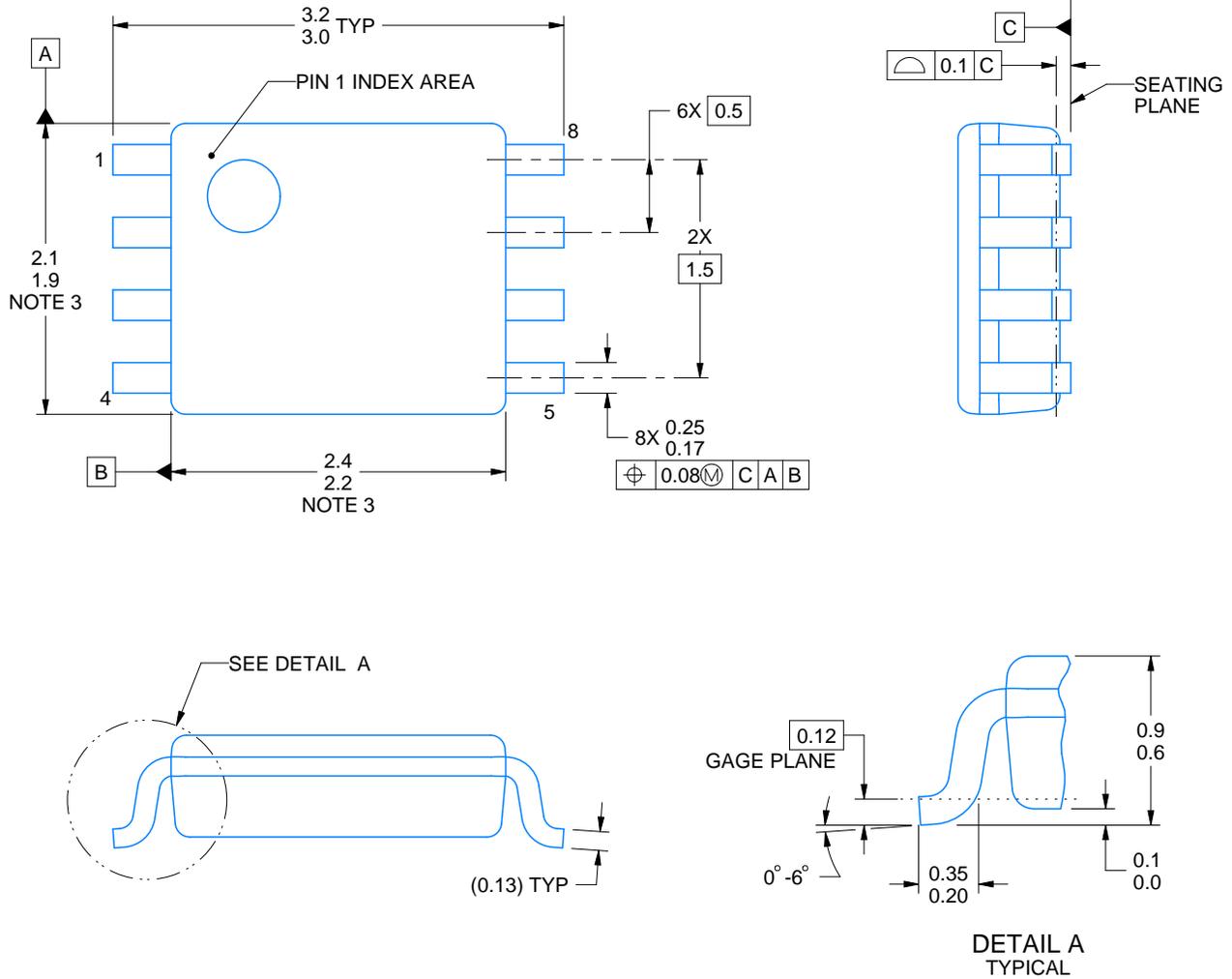
4225266/A 09/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.

TEXAS INSTRUMENTS
www.ti.com

8X (0.85)

SYMM

SEE SOLDER MASK
DETAILS

(R0.05) TYP

8X (0.3) 1

8

6X (0.5)

SYMM

4

5

(3.1)
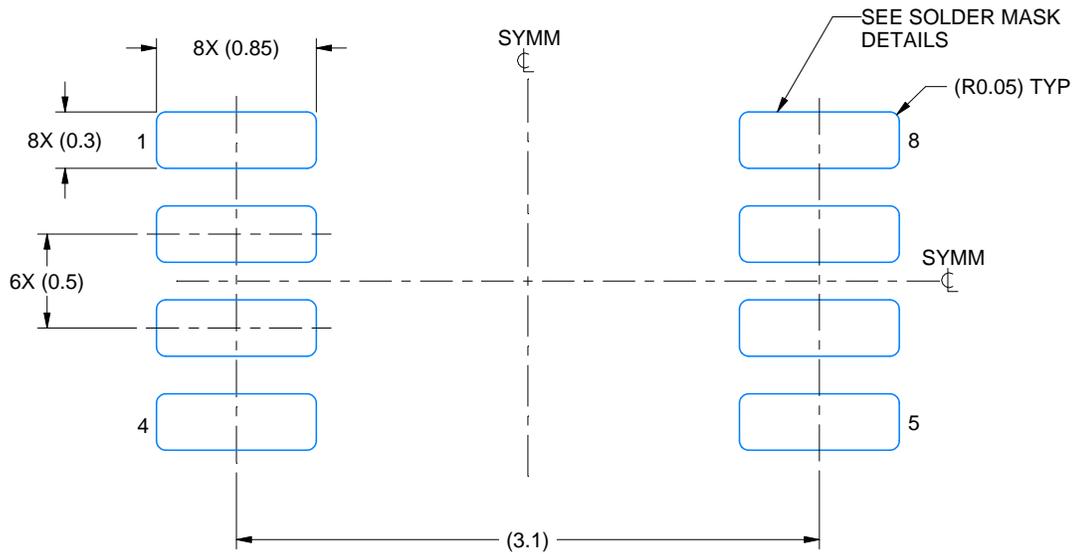
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
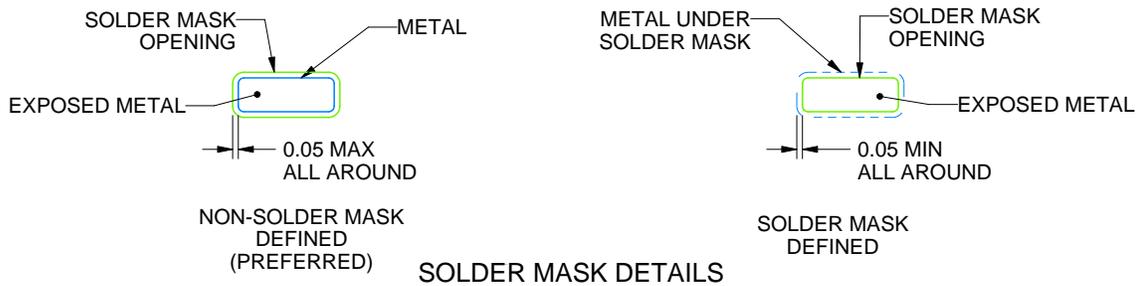
4225266/A   09/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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8X (0.85)

SYMM
℄

(R0.05) TYP

8X (0.3)   1

8

6X (0.5)

SYMM
℄

4

5

(3.1)
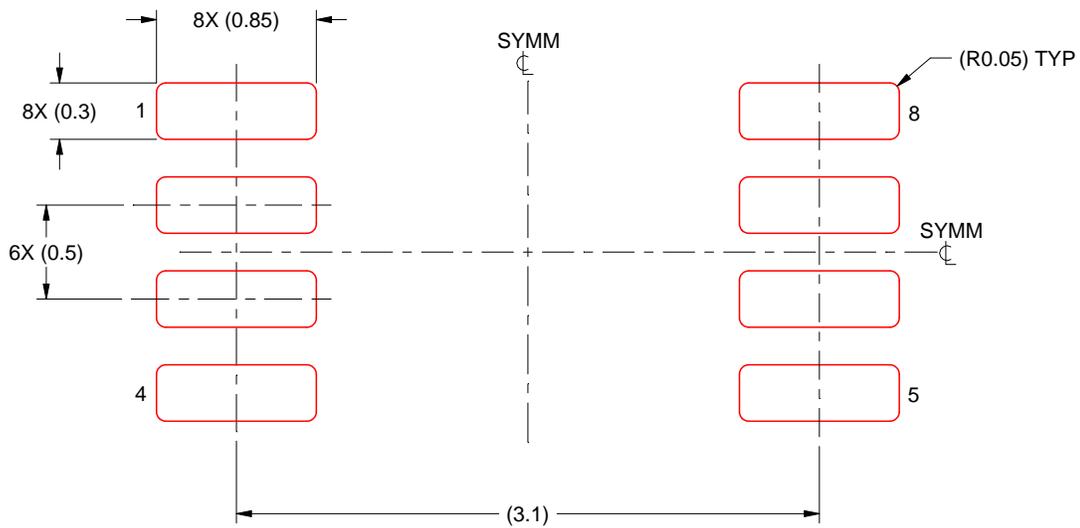
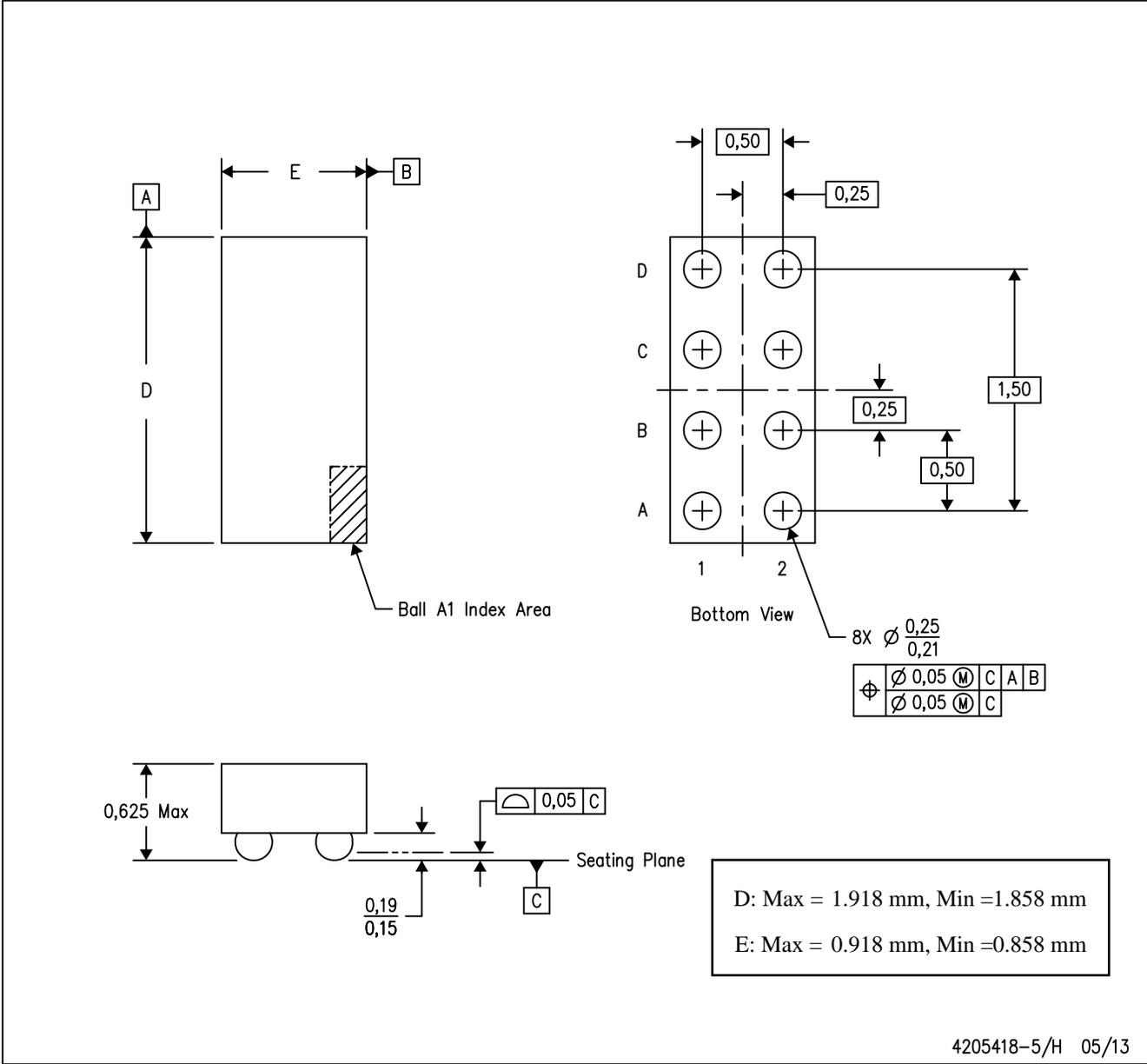SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A   09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
8. Board assembly site may have different recommendations for stencil design.

B ◄— E —► A

BALL A1
CORNER

D

0.5 MAX

C

SEATING PLANE

0.19
0.15

BALL TYP

⌒ 0.05 C

0.5 TYP

D

C

SYMM
℄

1.5
TYP

B

D: Max = 1.918 mm, Min =1.858 mm

E: Max = 0.918 mm, Min =0.858 mm

0.5
TYP

A

1   2

8X ∅ 0.25
0.21

SYMM
℄

⊕ 0.015 Ⓜ C A B

4223082/A   07/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.

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8X (∅ 0.23)

(0.5) TYP

(0.5) TYP

1   2

A

B

SYMM ₵

C

D

SYMM ₵
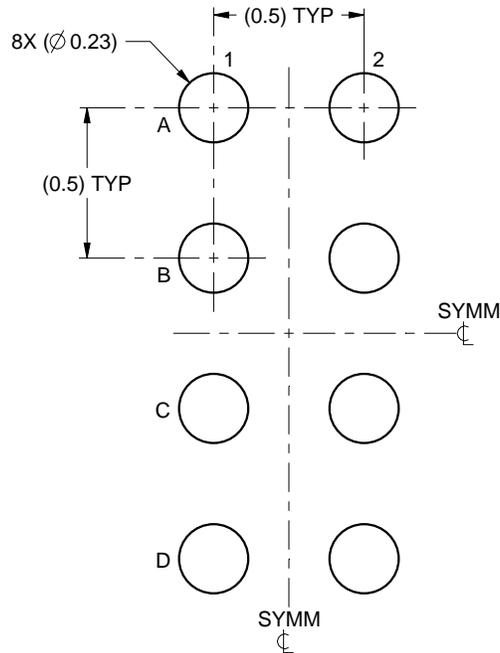
LAND PATTERN EXAMPLE
SCALE:40X

SOLDER MASK OPENING

0.05 MAX

(∅ 0.23) METAL

NON-SOLDER MASK DEFINED (PREFERRED)

0.05 MIN

(∅ 0.23) SOLDER MASK OPENING

METAL UNDER SOLDER MASK

SOLDER MASK DEFINED
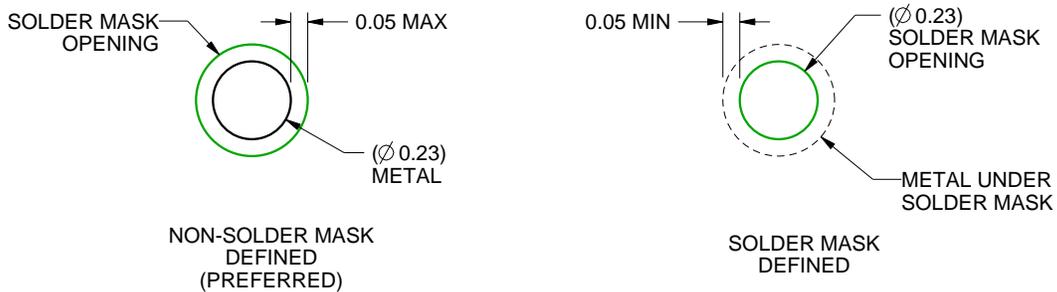
SOLDER MASK DETAILS
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

(0.5) TYP

8X (□ 0.25)

(R0.05) TYP

1   2

A

(0.5)
TYP

B

SYMM
℄

C

METAL
TYP

D

SYMM
℄
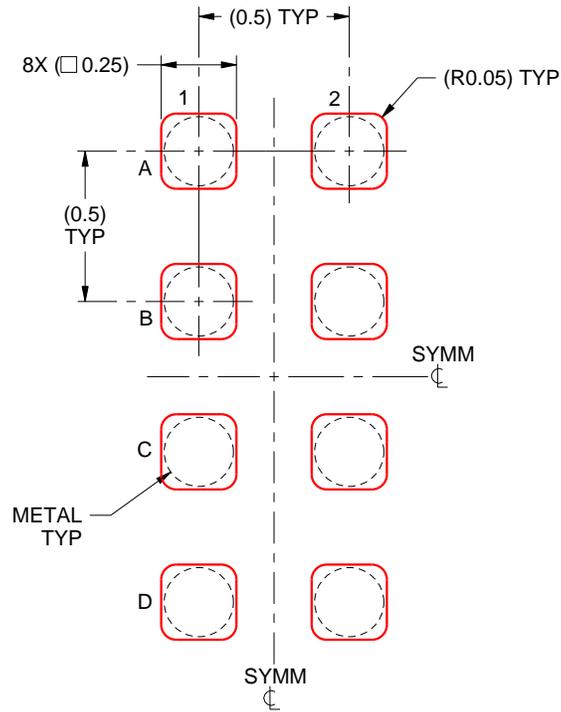
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4223082/A   07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

YZT (R−XBGA−N8)   DIE−SIZE BALL GRID ARRAY

Ball A1 Index Area

Bottom View

8X Ø $\frac{0,25}{0,21}$

| ⊕ | Ø 0,05 Ⓜ | C | A | B |
| | Ø 0,05 Ⓜ | C | | |

Seating Plane

0,625 Max

$\frac{0,19}{0,15}$

D: Max = 1.918 mm, Min =1.858 mm

E: Max = 0.918 mm, Min =0.858 mm

4205418−5/H   05/13

NOTES: A.   All linear dimensions are in millimeters.   Dimensioning and tolerancing per ASME Y14.5M−1994.
             B.   This drawing is subject to change without notice.
             C.   NanoFree™ package configuration.

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