Meter-Bus Transceiver

FEATURES

- Meter-Bus Transceiver (for Slave) Meets Standard EN1434-3
- Receiver Logic With Dynamic Level Recognition
- Constant-Current Sink Adjustable By Resistor
- Polarity Independent
- Power-Fail Function
- Module Supply Voltage Switch
- 3.3-V Constant Voltage Source
- Up to 9600 Baud in Half Duplex for UART Protocol
- Slave Power Support
  - Supply From Meter-Bus by Output VDD
  - Supply From Meter-Bus by Output VDD or From Backup Battery
  - Supply From Battery – Meter-Bus Active for Data Transmission Only

APPLICATIONS

- E-metering
- Advanced Metering Infrastructure (AMI)
- Water Meters
- Gas Meters
- Heat Meters

DESCRIPTION

The TSS521 device is a single-chip transceiver developed for Meter-Bus standard (EN1434-3) applications.

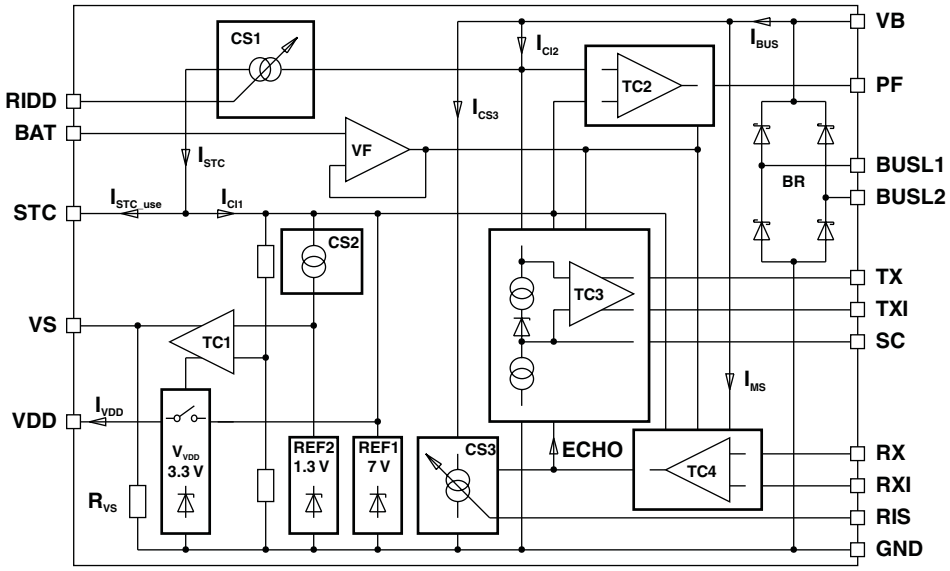
The TSS521 interface circuit adjusts the different potentials between a slave system and the Meter-Bus master. The connection to the bus is polarity independent and supports full galvanic slave isolation with optocouplers.

The circuit is supplied by the master through the bus. Therefore, this circuit offers no additional load for the slave battery. A power-fail function is integrated.

The receiver has dynamic level recognition, and the transmitter has a programmable current sink.

A 3.3-V voltage regulator with power reserve for a delayed switch off at bus fault is integrated.

Functional Schematic



D PACKAGE
(TOP VIEW)

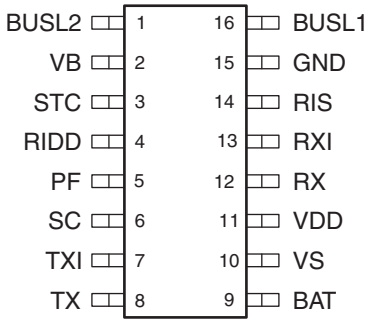


Table 1. Terminal Functions

TERMINAL		DESCRIPTION
NAME	NO.	
BUSL2	1	Meter-Bus
VB	2	Differential bus voltage after rectifier
STC	3	Support capacitor
RIDD	4	Current adjustment input
PF	5	Power fail output
SC	6	Sampling capacitor
TXI	7	Data output inverted
TX	8	Data output
BAT	9	Logic level adjust
VS	10	Switch for bus or battery supply output
VDD	11	Voltage regulator output
RX	12	Data input
RXI	13	Data input inverted
RIS	14	Adjust input for modulation current
GND	15	Ground
BUSL1	16	Meter-Bus

Functional Description

Data Transmission, Master to Slave

The mark level on the bus lines V_{BUS} = MARK is defined by the difference of BUSL1 and BUSL2 at the slave. It depends on the distance from Master to Slave, which affects the voltage drop on the wire. To make the receiver independent, a dynamic reference level on the SC pin is used for the voltage comparator TC3 (see Figure 1).

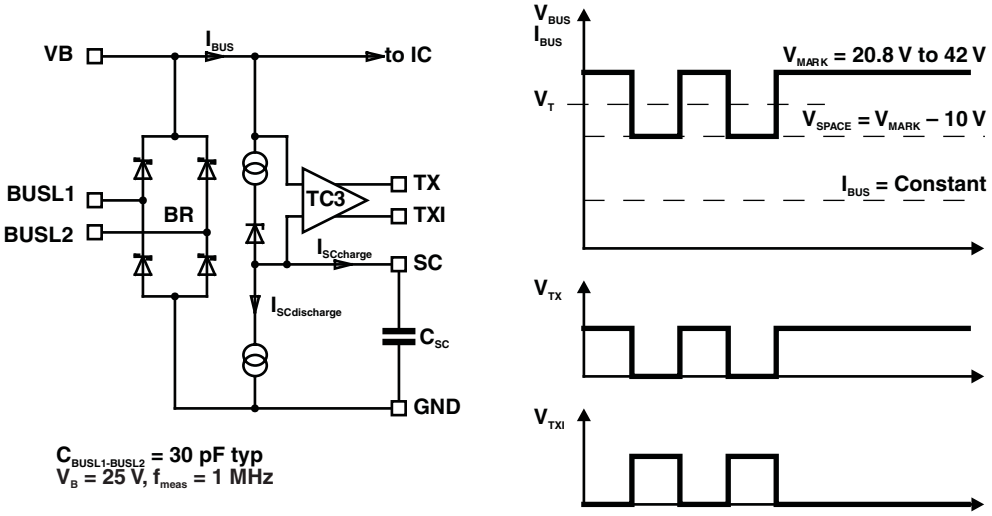


Figure 1. Data Transmission, Master to Slave

A capacitor (C_{SC}) at the SC pin is charged by a current ($I_{SCcharge}$) and is discharged with a current ($I_{SCdischarge}$) where:

$$I_{SCdisharge} = \frac{I_{SCcharge}}{40\ (typ)} \quad (1)$$

This ratio is necessary to run any kind of UART protocol independent of the data contents (for example, if an 11-bit UART protocol is transmitted with all data bits at 0 and only the stop bit at 1). There must be sufficient time to recharge the capacitor C_{SC}. The input level detector TC3 detects voltage modulations from the master (V_{BUS} = SPACE or MARK conditions) and switches the inverted output TXI and the noninverted output TX.

Data Transmission, Slave to Master

The device uses current modulation to transmit information from the slave to the master while the bus voltage remains constant. The current source CS3 modulates the bus current and the master detects the modulation. The constant current source CS3 is controlled by the inverted input RXI or the noninverted input RX. The current source CS3 can be programmed by an external resistor R_{RIS}. The modulation supply current I_{MS} flows in addition to the current source CS3 during the modulation time.

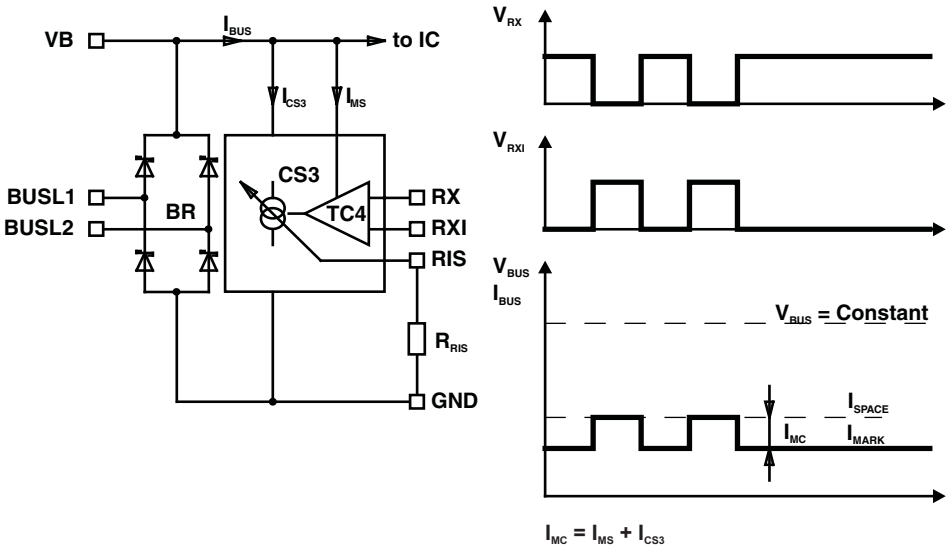
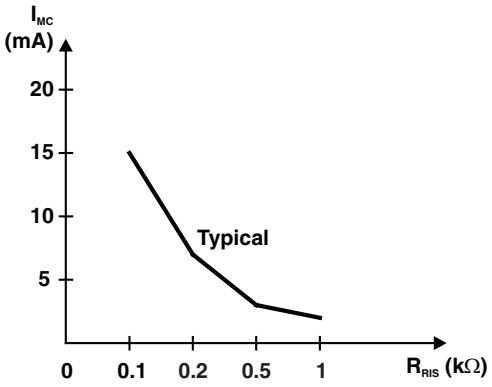


Figure 2. Data Transmission, Slave to Master

Because the TSS521 is configured for half-duplex only, the current modulation from RX or RXI is repeated concurrently as ECHO on the outputs TX and TXI. If the slave, as well as the master, is trying to send information on the lines, the added signals appear on the outputs TX and TXI, which indicates the data collision to the slave (see).

The bus topology requires a constant current consumption by each connected slave.

To calculate the value of the programming resistor R_{RIS}, use the formula shown in Figure 3.



$$R_{RIS} = \frac{V_{RIS}}{I_{CS3}} = \frac{V_{RIS}}{I_{MC} - I_{MS}}$$

V_{RIS} = Voltage on pin RIS
R_{RIS} = Programming resistor
I_{CS3} = Programmable current
I_{MC} = Modulation current
I_{MS} = Modulation supply current (220 µA typ)

Figure 3. Calculate Programming Resistor R_{RIS}

Slave Supply, 3.3 V

The TSS521 has an internal 3.3-V voltage regulator. The output power of this voltage regulator is supplied by the storage capacitor C_{STC} at the STC pin. The storage capacitor C_{STC} at the STC pin is charged with constant current I_{STC_use} from the current source CS1. The maximum capacitor voltage is limited to REF1. The charge current I_{STC} has to be defined by an external resistor at pin RIDD.

The adjustment resistor R_{RIDD} can be calculated using Equation 2.

$$R_{RID} = 25 \frac{V_{RIDD}}{I_{STC}} = 25 \frac{V_{RIDD}}{I_{STC\_use} + I_{IC1}} \quad (2)$$

Where,

I_{STC} = current from current source CS1
I_{STC_use} = charge current for support capacitor
I_{CI} = internal current
V_{RIDD} = voltage on pin RIDD
R_{RIDD} = value of adjustment resistor

The voltage level of the storage capacitor C_{STC} is monitored with comparator TC1. Once the voltage V_{STC} reaches V_{VDD_on}, the switch S_{VDD} connects the stabilized voltage V_{VDD} to pin VDD. VDD is turned off if the voltage V_{STC} drops below the V_{VDD_off} level.

Voltage variations on the capacitor C_{STC} create bus current changes (see Figure 4).

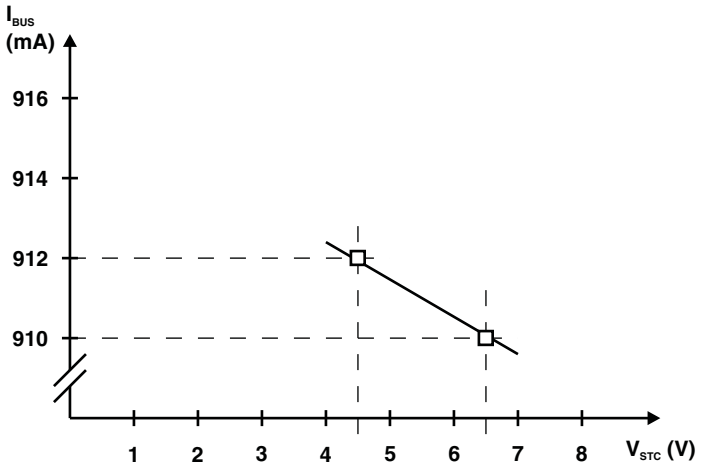


Figure 4. Single Mode Bus Load

At a bus fault the shut down time of VDD (t_{off}) in which data storage can be performed depends on the system current I_{VDD} and the value of capacitor C_{STC}. See Figure 5, which shows a correlation between the shutdown of the bus voltage V_{BUS} and V_{DD_off} and t_{off} for dimensioning the capacitor.

The output VS is meant for slave systems that are driven by the bus energy, as well as from a battery should the bus line voltage fail. The switching of VS is synchronized with VDD and is controlled by the comparator TC1. An external transistor at the output VS allows switching from the Meter-Bus remote supply to battery.

Power On and Off

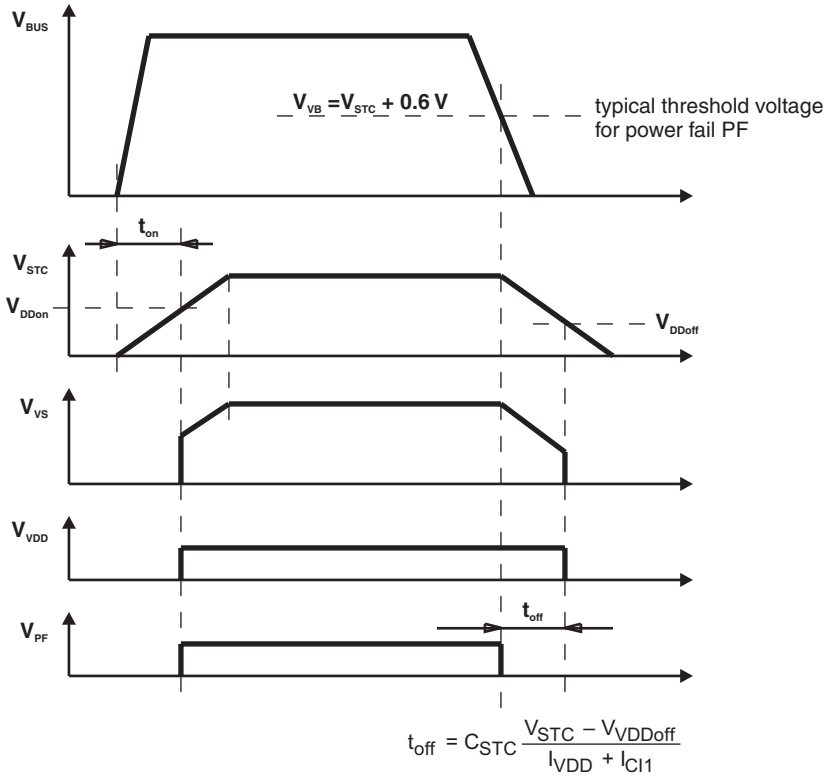


Figure 5. Power On/Off Timing

Power Fail Function

Because of the rectifier bridge BR at the input, BUSL1, and BUSL2, the TSS521 is polarity independent. The pin VB to ground (GND) delivers the bus voltage V_{VB} less the voltage drop over the rectifier BR. The voltage comparator TC2 monitors the bus voltage. If the voltage $V_{VB} > V_{STC} + 0.6$ V, then the output PF = 1. The output level PF = 0 (power fail) provides a warning of a critical voltage drop to the microcontroller to save the data immediately.

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

V_{MB}	Voltage, BUSL1 to BUSL2		±50 V
V_I	Input voltage range	RX and RXI	–0.3 V to 5.5 V
		BAT	–0.3 V to 5.5 V
T_J	Operating junction temperature range		–25°C to 150°C
T_A	Operating free-air temperature range		–25°C to 85°C
T_{STG}	Storage temperature range		–65°C to 150°C
	Power derating factor, junction to ambient		8 mW/°C

Recommended Operating Conditions

See note (1). Typical values are specified at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

			MIN	MAX	UNIT
V_{MB}	Bus voltage, |BUSL2 – BUSL1|	Receiver	10.8	42	V
		Transmitter	12	42	
V_I	Input voltage	VB (receive mode)	9.3		V
		BAT(2)	2.5	3.8	
R_{RIDD}	RIDD resistor		13	80	kΩ
R_{RIS}	RIS resistor		100		Ω
T_A	Operating free-air temperature		–25	85	°C

(1) All voltage values are measured with respect to the GND terminal unless otherwise noted.
(2) $V_{BAT}(max) \le V_{STC} - 1$ V

Electrical Characteristics

See note (1). Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ΔV_{BR}	Voltage drop at rectifier BR	I_{BUS} = 3 mA				1.5	V
ΔV_{CS1}	Voltage drop at current source CS1	R_{RIDD} = 13 kΩ				1.8	V
I_{BUS}	BUS current	V_{STC} = 6.5 V, I_{MC} = 0 mA	R_{RIDD} = 13 kΩ			3	mA
			R_{RIDD} = 30 kΩ			1.5	
ΔI_{BUS}	BUS current accuracy	ΔV_{BUS} = 10 V, I_{MC} = 0 mA, R_{RIDD} = 13 kΩ to 30 kΩ				2	%
I_{CC}	Supply current	V_{STC} = 6.5 V, I_{MC} = 0 mA, V_{BAT} = 3.8 V, R_{RIDD} = 13 kΩ (2)				650	µA
I_{CI1}	CI1 current	V_{STC} = 6.5 V, I_{MC} = 0 mA, V_{BAT} = 3.8 V, R_{RIDD} = 13 kΩ, V_{BUS} = 6.5 V, RX/RXI = off (2)				350	µA
V_{VDD}	VDD voltage	$-I_{VDD}$ = 1 mA, V_{STC} = 6.5 V		3.1		3.4	V
R_{VDD}	VDD resistance	$-I_{VDD}$ = 2 to 8 mA, V_{STC} = 4.5 V				5	Ω
V_{STC}	STC voltage	V_{DD} = on, VS = on		5.6		6.4	V
		V_{DD} = off, VS = off		3.8		4.3	
		$I_{VDD} < I_{STC\_use}$		6.5		7.5	
I_{STC_use}	STC current	V_{STC} = 5 V	R_{RIDD} = 30 kΩ	0.65		1.1	mA
			R_{RIDD} = 13 kΩ	1.85		2.4	
V_{RIDD}	RIDD voltage	R_{RIDD} = 30 kΩ		1.23		1.33	V
V_{VS}	VS voltage	V_{DD} = on, I_{VS} = –5 µA		V_{STC} – 0.4		V_{STC}	V
R_{VS}	VS resistance	V_{DD} = off		0.3		1	MΩ
V_{PF}	PF voltage	V_{STC} = 6.5 V	$V_{VB} = V_{STC} + 0.8$ V, I_{PF} = –100 µA	V_{BAT} – 0.6		V_{BAT}	V
			$V_{VB} = V_{STC} + 0.3$ V, I_{PF} = 1 µA	0		0.6	
			$V_{VB} = V_{STC} + 0.3$ V, I_{PF} = 5 µA	0		0.9	

(1) All voltage values are measured with respect to the GND terminal unless otherwise noted.
(2) Inputs RX/RXI and outputs TX/TXI are open, $I_{CC} = I_{CI1} + I_{CI2}$

Electrical Characteristics (continued)

See note (1). Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{on}	Turn-on time	C_{STC} = 50 µF, Bus voltage slew rate: 1 V/µs			3	s

Receiver Section Electrical Characteristics

See note (1). Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_T		See Figure 1	MARK – 8.2		MARK – 5.7	V
V_{SC}	SC voltage				V_{VB}	V
$I_{SCcharge}$	SC charge current	V_{SC} = 24 V, V_{VB} = 36 V	–15		–40	µA
$I_{SCdischarge}$	SC discharge current	V_{SC} = V_{VB} = 24 V	0.3		–0.033 × $I_{SCcharge}$	µA
V_{OH}	High-level output voltage (TX, TXI)	I_{TX}, I_{TXI} = –100 µA (see Figure 1)	V_{BAT} – 0.6		V_{BAT}	V
V_{OL}	Low-level output voltage (TX, TXI)	I_{TX}, I_{TXI} = 100 µA	0		0.5	V
		I_{TX} = 1.1 mA	0		1.5	
I_{TX} I_{TXI}	TX, TXI current	V_{TX} = 7.5, V_{VB} = 12 V, V_{STC} = 6 V, V_{BAT} = 3.8 V			16	µA

(1) All voltage values are measured with respect to the GND terminal unless otherwise noted.

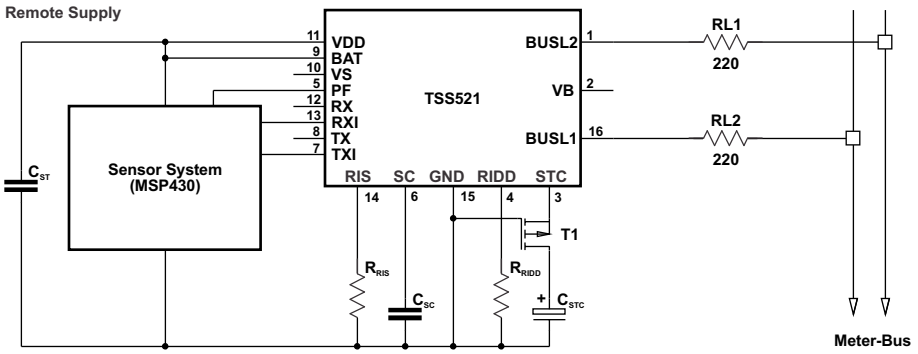
Transmitter Section Electrical Characteristics

See note (1). Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{MC}	MC voltage	R_{RIS} = 100 Ω	11.5		19.5	mA
V_{RIS}	RIS voltage	R_{RIS} = 100 Ω	1.4		1.7	V
		R_{RIS} = 1000 Ω	1.5		1.8	
V_{IH}	High-level input voltage (RX, RXI)	See Figure 2, see (2)	V_{BAT} – 0.8		5.5	V
V_{IL}	Low-level input voltage (RX, RXI)	See Figure 2	0		0.8	V
I_{RX}	RX current	V_{RX} = 0 V, V_{BAT} = 3 V, V_{STC} = 6.5 V	-10		-40	µA
I_{RXI}	RXI current	V_{RXI} = V_{BAT} = 3 V, V_{STC} = 6.5 V	10		40	µA

(1) All voltage values are measured with respect to the GND terminal unless otherwise noted.
(2) V_{IH}(max) = 5.5 V is valid only when V_{STC} ≥ 6.5 V.

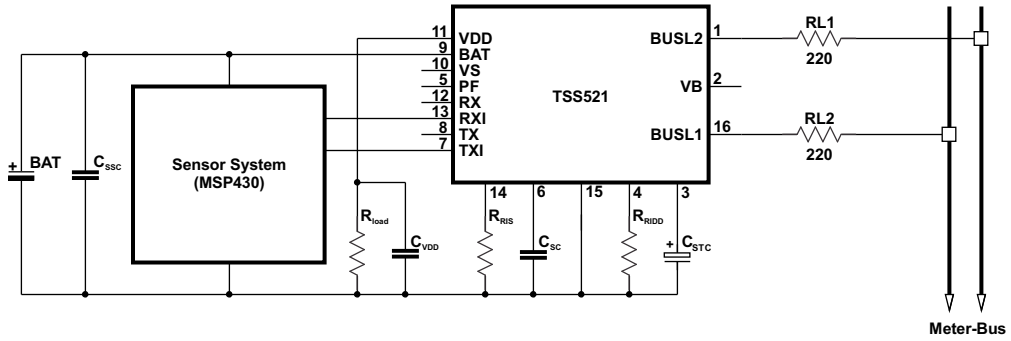
APPLICATION INFORMATION



R_{RIDD} = 30 kΩ	C_{STC} =< 220 µF	single load 1UL
R_{RIDD} = 13 kΩ	C_{STC} =< 470 µF	double load 2UL

NOTE: Transistor T1 should be a BSS84.

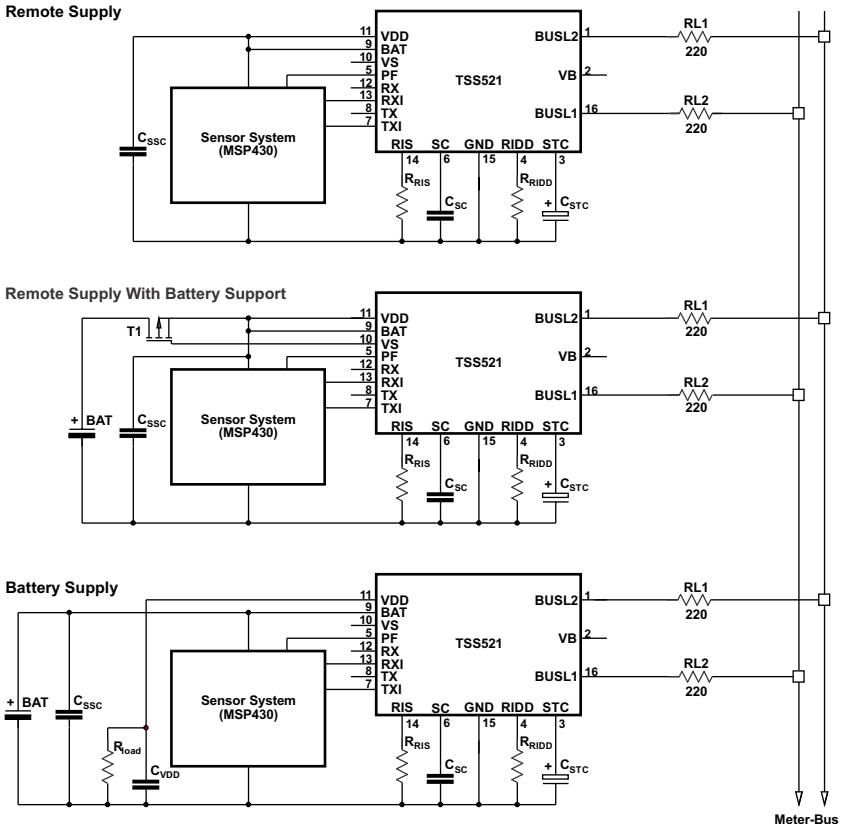
Figure 6. Basic Application Circuit With Support Capacitor C_{STC} > 50 µF



C_{SSC} = system stabilizing capacitor
C_{STC} = support capacitor
C_{SC} = sampling capacitor
C_{VDD} = stabilizing capacitor (100 nF)
C_{STC}:C_{VDD} ≥ 4:1

R_{RIDD} = slave=current adjustment resistor
R_{RIS} = modulation-current resistor
RL1,RL2 = protection resistors
R_{load} = discharge resistor (100 kΩ recommended)

Figure 7. Basic Application Circuit for Supply From Battery



NOTE: R_{DSon} of the transistor T1 (BSS84) at low battery voltage must be considered during application design.

Figure 8. Basic Applications for Different Supply Modes

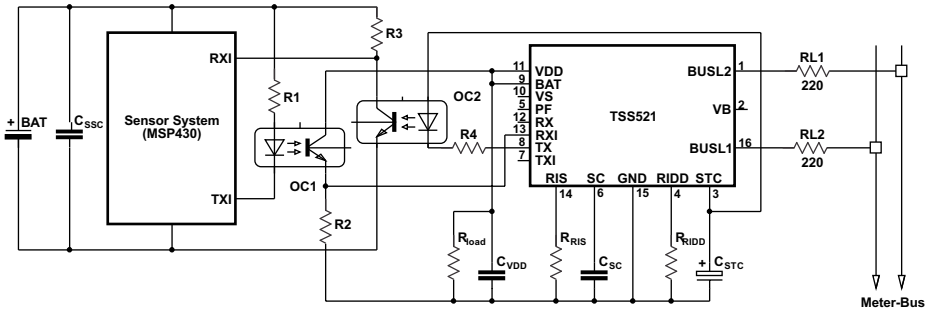


Figure 9. Basic Optocoupler Application

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TSS521D	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-25 to 85	TSS521
TSS521DR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	TSS521
TSS521DR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	TSS521

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

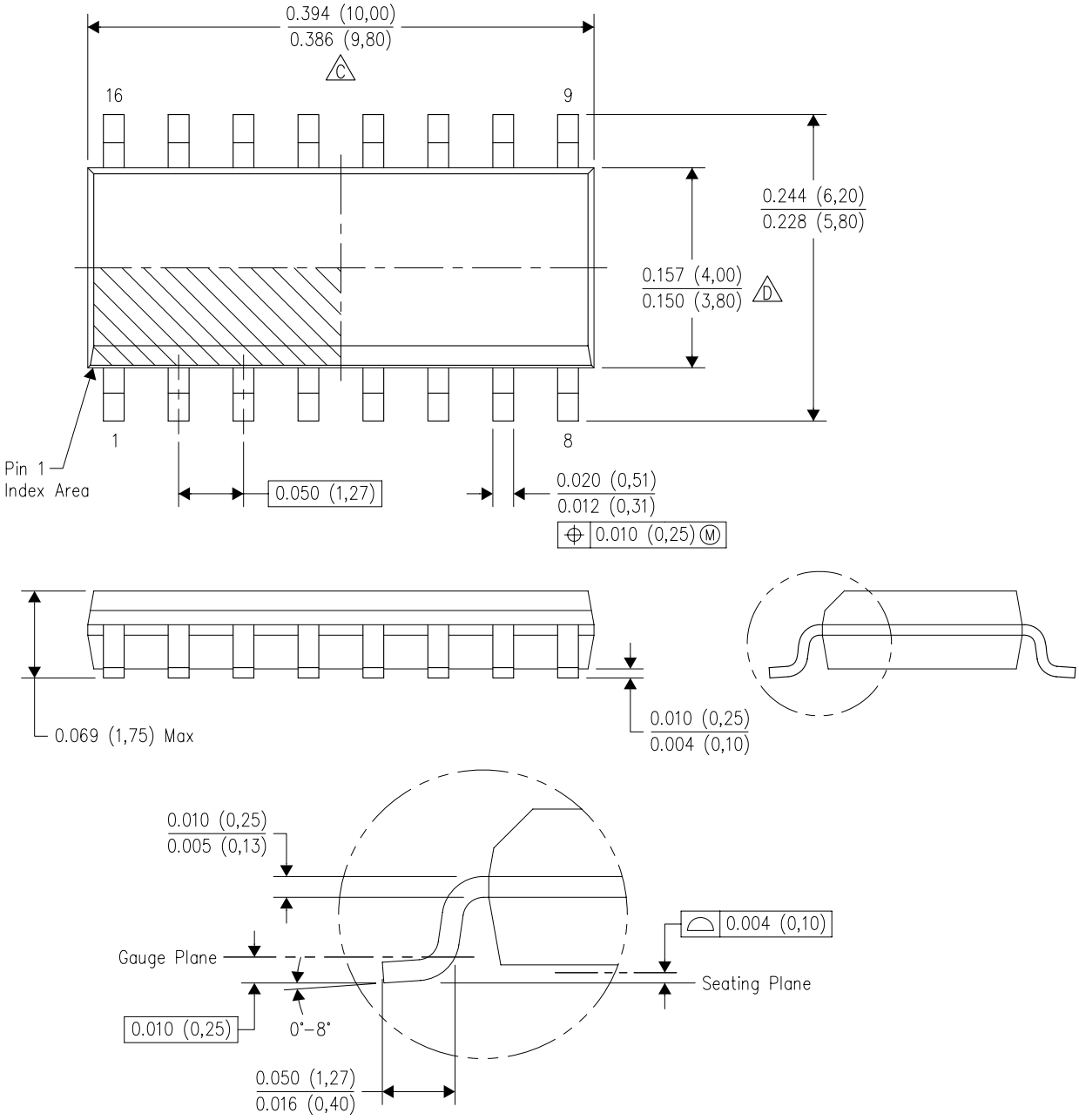
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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