TUSB4041I-Q1 Four-Port USB 2.0 Hub

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results
  - Device temperature grade 3: –40°C to 85°C ambient operating temperature
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C5
- Four port USB 2.0 hub
- USB 2.0 hub features:
  - Multi transaction translator (MTT) hub: four transaction translators
  - Four asynchronous endpoint buffers per transaction translator
- Supports USB battery charging
  - CDP mode (upstream port connected)
  - DCP mode (upstream port unconnected)
  - DCP mode complies with Chinese telecommunications industry standard YD/T 1591-2009
  - Supports D+ and D– divider mode
- Per port or ganged power switching and overcurrent notification inputs
- OTP ROM, serial EEPROM or I^2C and SMBus target interface for custom configurations:
  - V_{ID} and P_{ID}
  - Customizable ports
  - Manufacturer and product strings (not by OTP ROM)
  - Serial number (not by OTP ROM)
- Application feature selection using pin selection or EEPROM, I^2C, or SMBus target interface
- Provides 128-bit Universally Unique Identifier (UUID)
- Supports on-board and in-system OTP and EEPROM programming through the USB 2.0 upstream port
- Single clock input, 24MHz crystal or oscillator
- DM/DP polarity swap
- Type C compatible
- No special driver requirements; works seamlessly on any operating system with USB stack support
- 64-pin HTQFP package (PAP)

2 Applications

- Automotive
- Computer Systems
- Docking Stations
- Monitors
- Set-Top Boxes

3 Description

The TUSB4041I-Q1 device is a four-port USB 2.0 hub. The device provides USB high-speed or full-speed connections on the upstream port. The device also provides USB high-speed, full-speed, or low-speed connections on the downstream ports. When the upstream port is connected to an electrical environment that only supports high-speed, full-speed, and low-speed connections, the USB high-speed, full-speed and low-speed connectivity is enabled on the downstream ports. When the upstream port is connected to an electrical environment that only supports full-speed or low-speed connections, the USB high-speed connectivity are disabled on the downstream ports.

The TUSB4041I-Q1 device supports per-port or ganged power switching and overcurrent protection. The device also supports battery charging applications.

An individually port-power-controlled hub switches power on or off to each downstream port as requested by the USB host. Also when an individually port-power-controlled hub senses an overcurrent event, only power to the affected downstream port is switched off.

A ganged hub switches on power to all of the downstream ports when power is required to be on for any port. The power to the downstream ports is not switched off unless all ports are in a state that allows power to be removed. Also, when a ganged hub senses an overcurrent event, power to all downstream ports are switched off.

The TUSB4041I-Q1 device downstream ports provide support for battery charging applications by providing USB battery charging downstream-port (CDP) handshaking support. The device also supports a dedicated charging-port (DCP) mode when the upstream port is not connected. The DCP mode is compliant with the USB battery charging specification and Chinese Telecommunications Industry Standard YD/T 1591-2009. Also, an automatic mode provides transparent support for BC devices and devices supporting divider-mode charging solutions when the upstream port unconnected.

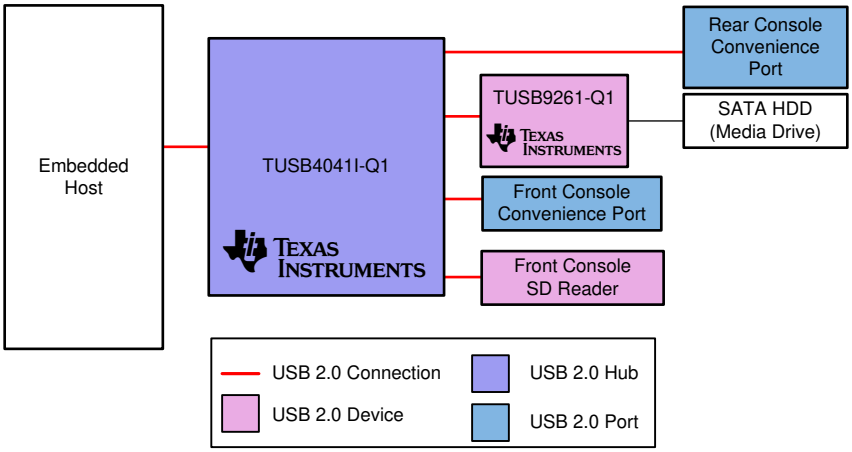
The TUSB4041I-Q1 device provides pin-strap configuration for some features including battery charging support, and also provides customization though OTP ROM, I^2C EEPROM, or through an I^2C and SMBus target interface for P_{ID}, V_{ID}, and custom port and phy configurations. Custom string support is also available when using an I^2C EEPROM or the I^2C and SMBus target interface.

The device is available in a 64-pin PAP package and is offered in a industrial version for operation over the temperature range of –40°C to 85°C.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TUSB4041I-Q1	HTQFP (64)	12mm × 12mm

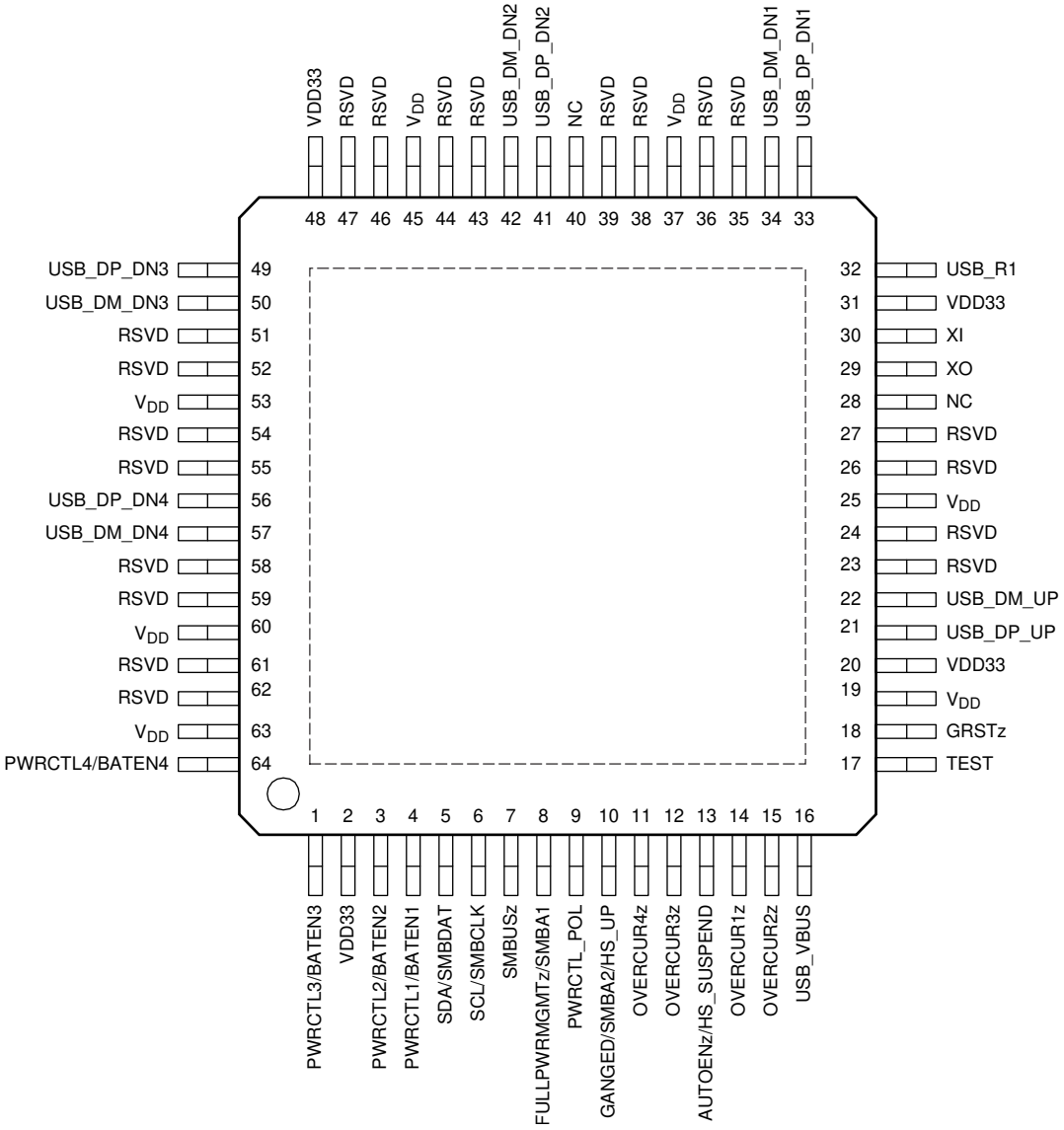
(1) For all available packages, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application

Table of Contents

4 Pin Configuration and Functions



NC = No internal connection

Figure 4-1. PAP Package 64-Pin HTQFP With PowerPAD™ Top View

Table 4-1. Pin Functions

PIN		I/O[1]	TYPE[1]	DESCRIPTION
NAME	NO.			
CLOCK AND RESET SIGNALS				
GRSTz	18	I	PU	Global power reset. This reset brings all of the TUSB4041I-Q1 device internal registers to the default state. When the GRSTz pin is asserted, the device is completely nonfunctional.
XI	30	I	—	Crystal input. This pin is the crystal input for the internal oscillator. The input can alternately be driven by the output of an external oscillator. When using a crystal, a 1MΩ feedback resistor is required between the XI and XO pins.
XO	29	O	—	Crystal output. This pin is the crystal output for the internal oscillator. If the XI pin is driven by an external oscillator, this pin can be left unconnected. When using a crystal, a 1MΩ feedback resistor is required between the XI and XO pins.
USB UPSTREAM SIGNALS				
USB_DM_UP	22	I/O	—	USB high-speed differential transceiver (negative)
USB_DP_UP	21	I/O	—	USB high-speed differential transceiver (positive)
USB_R1	32	I	—	Precision resistor reference. Connect a 9.53-kΩ ±1% resistor between the USB_R1 pin and ground.
USB_VBUS	16	I	—	USB upstream port power monitor. The VBUS detection requires a voltage divider. The signal USB_VBUS must be connected to VBUS through a 90.9kΩ ±1% resistor and to ground through a 10kΩ ±1% resistor from the signal to ground.
USB DOWNSTREAM SIGNALS				
OVERCUR1z	14	I	PU	USB port 1 overcurrent detection. This pin is used to connect the overcurrent output of the downstream port power switch for port 1. 0 = An overcurrent event occurred. 1 = An overcurrent event has not occurred. This pin can be left unconnected if power management is not implemented. If power management is enabled, review the power switch to determine the necessary external circuitry.
OVERCUR2z	15	I	PU	USB port 2 overcurrent detection. This pin is used to connect the overcurrent output of the downstream port power switch for port 2. 0 = An overcurrent event occurred. 1 = An overcurrent event has not occurred. If power management is not implemented, leave this pin unconnected. If power management is enabled, review the power switch to determine the necessary external circuitry.
OVERCUR3z	12	I	PU	USB port 3 overcurrent detection. This pin is used to connect the overcurrent output of the downstream port power switch for port 3. 0 = An overcurrent event occurred. 1 = An overcurrent event has not occurred. This pin can be left unconnected if power management is not implemented. If power management is enabled, review the power switch to determine the necessary external circuitry.
OVERCUR4z	11	I	PU	USB port 4 overcurrent detection. This pin is used to connect the overcurrent output of the downstream port power switch for port 4. 0 = An overcurrent event occurred. 1 = An overcurrent event has not occurred. This pin can be left unconnected if power management is not implemented. If power management is enabled, review the power switch to determine the necessary external circuitry.

Table 4-1. Pin Functions (continued)

PIN		I/O[1]	TYPE[1]	DESCRIPTION
NAME	NO.			
PWRCTL1/BATEN1	4	I/O	PD	USB port 1 power-on control for downstream power and battery charging enable. The pin is used for control of the downstream power switch for port 1. The value of the pin is sampled at the deassertion of reset to determine the value of the battery charging support for port 1 as indicated in the *Battery Charging Support Register*: 0 = Battery charging not supported 1 = Battery charging supported
PWRCTL2/BATEN2	3	I/O	PD	USB port 2 power-on control for downstream power and battery charging enable. The pin is used for control of the downstream power switch for port 2. The value of the pin is sampled at the deassertion of reset to determine the value of the battery charging support for Port 2 as indicated in the *Battery Charging Support Register*: 0 = Battery charging not supported 1 = Battery charging supported
PWRCTL3/BATEN3	1	I/O	PD	USB port 3 power-on control for downstream power and battery charging enable. The pin is used for control of the downstream power switch for port 3. The value of the pin is sampled at the deassertion of reset to determine the value of the battery charging support for Port 3 as indicated in the *Battery Charging Support Register*: 0 = Battery charging not supported 1 = Battery charging supported
PWRCTL4/BATEN4	64	I/O	PD	USB port 4 power-on control for downstream power and battery charging enable. The pin is used for control of the downstream power switch for port 4. The value of the pin is sampled at the deassertion of reset to determine the value of the battery charging support for Port 4 as indicated in the *Battery Charging Support Register*: 0 = Battery charging not supported 1 = Battery charging supported
USB_DM_DN1	34	I/O	—	USB high-speed differential transceiver (negative)
USB_DM_DN2	42			
USB_DM_DN3	50			
USB_DM_DN4	57			
USB_DP_DN1	33	I/O	—	USB high-speed differential transceiver (positive)
USB_DP_DN2	41			
USB_DP_DN3	49			
USB_DP_DN4	56			
I²C AND SMBus SIGNALS				
SCL/SMBCLK	6	I/O	PD	I²C clock/SMBus clock. The function of this pin depends on the setting of the SMBUSz input. When SMBUSz = 1, this pin functions as the serial clock interface for an I²C EEPROM. When SMBUSz = 0, this pin functions as the serial clock interface for an SMBus host. This pin can be left unconnected if external interface not implemented.

Table 4-1. Pin Functions (continued)

PIN		I/O[1]	TYPE[1]	DESCRIPTION
NAME	NO.			
SDA/SMBDAT	5	I/O	PD	I^2C data/SMBus data. The function of this pin depends on the setting of the SMBUSz input. When SMBUSz = 1, this pin functions as the serial data interface for an I^2C EEPROM. When SMBUSz = 0, this pin functions as the serial data interface for an SMBus host. This pin can be left unconnected if the external interface is not implemented.
SMBUSz	7	I/O	PU	I^2C/SMBus mode select. The value of the pin is sampled at the deassertion of reset set I^2C or SMBus mode as follows: 1 = I^2C mode selected 0 = SMBus mode selected This pin can be left unconnected if the external interface is not implemented. After reset, this signal is driven low by the TUSB4041I-Q1. Because of this behavior, TI recommends not to tie directly to supply, but instead pull up or pull down using external resistor.
TEST AND MISCELLANEOUS SIGNALS				
AUTOENz/ HS_SUSPEND	13	I/O	PU	Automatic charge mode enable/HS suspend status The value of the pin is sampled at the deassertion of reset to determine if automatic mode is enabled as follows: 0 = Automatic mode is enabled on ports that are enabled for battery charging when the hub is unconnected. Note that CDP is not supported on port 1 when operating in automatic mode. 1 = Automatic mode is disabled. This value is also used to set the autoEnz bit in the *Battery Charging Support Register*. After reset, this signal indicates the high-speed USB Suspend status of the upstream port if enabled through the *Additional Feature Configuration Register*. When enabled, a value of 1 indicates the connection is suspended.
FULLPWRMGMTz/ SMBA1	8	I/O	PD	Full power management enable/SMBus address bit 1 The value of the pin is sampled at the deassertion of reset to set the power switch control follows: 0 = Power switching and overcurrent inputs supported 1 = Power switching and overcurrent inputs not supported Full power management is the ability to control power to the downstream ports of the TUSB4041I-Q1 device using PWRCTL[4:1]/BATEN[4:1]. When SMBus mode is enabled using SMBUSz, this pin sets the value of the SMBus target address bit 1. This pin can be left unconnected if full power management and SMBus are not implemented. After reset, this signal is driven low by the TUSB4041I-Q1. Because of this behavior, TI recommends not to tie directly to supply, but instead pull up or pull down using an external resistor. Note: Power switching must be supported for battery charging applications.

Table 4-1. Pin Functions (continued)

PIN		I/O[1]	TYPE[1]	DESCRIPTION
NAME	NO.			
GANGED/SMBA2/ HS_UP	10	I/O	PD	Ganged operation enable/SMBus address bit 2/HS connection status upstream port The value of the pin is sampled at the deassertion of reset to set the power switch and overcurrent detection mode as follows: 0 = Individual power control supported when power switching is enabled 1 = Power control gangs supported when power switching is enabled When SMBus mode is enabled using SMBUSz, this pin sets the value of the SMBus target address bit 2. After reset, this signal indicates the high-speed USB connection status of the upstream port if enabled through the *Additional Feature Configuration Register*. When enabled, a value of 1 indicates the upstream port is connected to a high-speed USB capable port. Note: Individual power control must be enabled for battery charging applications.
PWRCTL_POL	9	I/O	PU	Power control polarity. The value of the pin is sampled at the deassertion of reset to set the polarity of PWRCTL[4:1]. 0 = PWRCTL polarity is active low 1 = PWRCTL polarity is active high
RSVD	23, 24, 26, 27, 35, 36, 38, 39, 43, 44, 46, 47, 51, 52, 54, 55, 58, 59, 61, 62	I/O		Reserved. For internal use only and leave unconnected on the PCB.
TEST	17	I	PD	This pin is reserved for factory test.
POWER AND GROUND SIGNALS				
NC	28	—	—	No connection, leave floating
	40			
V_{DD}	19	—	PWR	1.1V power rail
	25			
	37			
	45			
	53			
	60			
	63			
V_{DD33}	2	—	PWR	3.3V power rail
	20			
	31			
	48			
Thermal Pad		—	—	Ground. The thermal pad must be connected to ground.

(1) I = Input, O = Output, I/O = Input/output, PU = Internal pullup resistor, PD = Internal pulldown resistor, and PWR = Power signal

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	V_{DD} steady-state supply voltage	–0.3	1.4	V
	V_{DD33} steady-state supply voltage	–0.3	3.8	V
Voltage	USB_VBUS pin	–0.3	1.4	V
	XI pins	–0.3	2.45	V
	All other pins	–0.3	3.8	V
Junction temperature, $T_{J(max)}$		–40	125	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed as *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated as *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD} (1)	1.1V supply voltage	0.99	1.1	1.26	V
V_{DD33}	3.3V supply voltage	3	3.3	3.6	V
$V_{(USB\_VBUS)}$	Voltage at USB_VBUS pin	0		1.155	V
T_A	Operating free-air temperature	–40		85	°C
T_J	Operating junction temperature	–40		105	°C

(1) A 1.05V, 1.1V, or 1.2V supply can be used as long as minimum and maximum supply conditions are met.

5.4 Thermal Information

THERMAL METRIC(1)		TUSB4041I-Q1 PAP (HTQFP) 64 PINS	UNIT
$R_{\theta\ JA}$	Junction-to-ambient thermal resistance	26.2	°C/W
$R_{\theta\ JC(top)}$	Junction-to-case (top) thermal resistance	11.5	°C/W
$R_{\theta\ JB}$	Junction-to-board thermal resistance	10.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	10.3	°C/W
$R_{\theta\ JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 3.3V I/O Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		OPERATION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage(1)	V_{DD33}		2		V_{DD33}	V
V_{IL}	Low-level input voltage(1)	V_{DD33}	JTAG pins only	0		0.55	V
			Other pins	0		0.8	
V_I	Input voltage			0		V_{DD33}	V
V_O	Output voltage(2)			0		V_{DD33}	V
t_t	Input transition time (t_r and t_f)			0		25	ns
V_{hys}	Input hysteresis(3)					0.13 x V_{DD33}	V
V_{OH}	High-level output voltage	V_{DD33}	I_{OH} = –4mA	2.4			V
V_{OL}	Low-level output voltage	V_{DD33}	I_{OL} = 4mA			0.4	V
I_{OZ}	High-impedance, output current(2)	V_{DD33}	V_I = 0 to V_{DD33}			±20	µA
$I_{OZ(P)}$	High-impedance, output current with internal pullup or pulldown resistor(4)	V_{DD33}	V_I = 0 to V_{DD33}			±250	µA
I_I	Input current(5)	V_{DD33}	V_I = 0 to V_{DD33}			±15	µA

(1) Applies to external inputs and bidirectional buffers.
(2) Applies to external outputs and bidirectional buffers.
(3) Applies to GRSTz.
(4) Applies to pins with internal pull-ups and pull-downs.
(5) Applies to external input buffers.

5.6 Power-Up Timing Requirements

		MIN	NOM	MAX	UNIT
t_{d1}	VDD33 stable before VDD stable(1)	See (2)			ms
t_{d2}	VDD and VDD33 stable before deassertion of GRSTz	3			ms
t_{su_io}	Setup for MISC inputs(3) sampled at the deassertion of GRSTz	0.1			µs
t_{hd_io}	Hold for MISC inputs(3) sampled at the deassertion of GRSTz	0.1			µs
t_{VDD33_RAMP}	VDD33 supply ramp requirements	0.2		100	ms
t_{VDD_RAMP}	VDD supply ramp requirements	0.2		100	ms

(1) An active reset is required if the VDD33 supply is stable before the VDD11 supply. This active Reset shall meet the 3ms power-up delay counting from both power supplies being stable to the de-assertion of GRSTz.
(2) The VDD33 and VDD have no power-on relationship unless GRSTz is only connected to a capacitor to GND. Then VDD must be stable minimum of 10 µs before the VDD33.
(3) MISC pins sampled at de-assertion of GRSTz: FULLPWRMGMTz, GANGED, PWRCTL_POL, SMBUSz, BATEN[4:1], and AUTOENz.

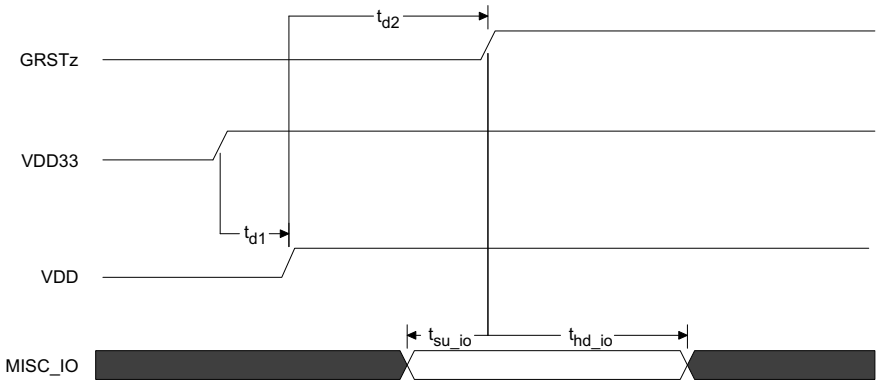


Figure 5-1. Power-Up Timing Requirements

5.7 Hub Input Supply Current

Typical values measured at T_A = 25°C

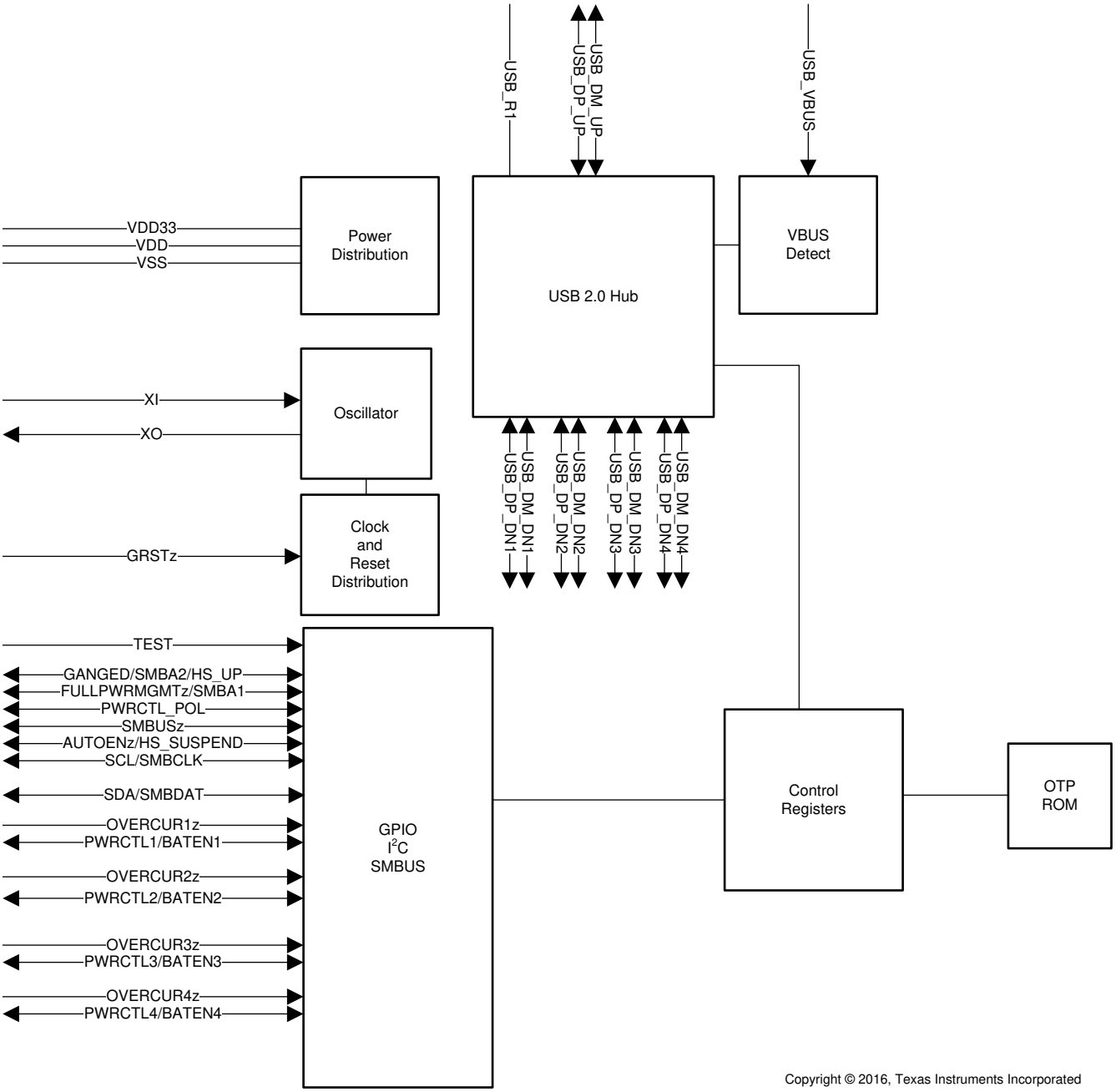
PARAMETER	3.3V		1.1V		UNIT
	V_{DD33} Typ	V_{DD33} Max	V_{DD} Typ	V_{DD} Max	
LOW POWER MODES					
Power on (after reset)	2.3	2.6	28	32	mA
Upstream disconnect	2.3	2.6	28	32	mA
Suspend	2.5	2.8	33	38	mA
ACTIVE MODES (US STATE AND DS STATE)					
2.0 host / 1 HS device	45	51	63	72	mA
2.0 host / 4 HS devices	76	87	86	98	mA
SMBUS Programming current	79	90	329	378	mA
Global Reset Mode current	77	88	332	370	mA

6 Detailed Description

6.1 Overview

The TUSB4041I-Q1 device is a four-port USB 2.0 hub. The device provides USB high-speed and full-speed connections on the upstream port and provides USB high-speed, full-speed, or low-speed connections on the downstream ports. When the upstream port is connected to an electrical environment that only supports high-speed connections. USB high-speed connectivity is enabled on the downstream ports. When the upstream port is connected to an electrical environment that only supports full-speed and low-speed connections. USB high-speed connectivity is disabled on the downstream ports.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Battery Charging Features

The TUSB4041I-Q1 device provides support for USB battery charging. Battery charging support can be enabled on a per port basis through the REG_6h(batEn[3:0]).

Battery charging support includes both CDP and DCP modes. The DCP mode is compliant with the Chinese Telecommunications Industry Standard YD/T 1591-2009.

In addition to standard DCP mode, the TUSB4041I-Q1 device provides a mode (AUTOMODE), which automatically provides support for DCP devices and devices that support custom charging indication. When in AUTOMODE, the port automatically switches between a divider mode and the DCP mode depending on the portable device connected. The divided mode places a fixed DC voltage on the ports DP and DM signals, which allows some devices to identify the capabilities of the charger. The default divider mode indicates support for up to 10W. The divider mode can be configured to report a legacy current setting (up to 5W) through REG_Ah(HiCurAcpModeEn).

The battery charging mode for each port is dependent on the state of Reg_6h(batEn[n]), the status of the VBUS input, and the state of REG_Ah(autoModeEnz) upstream port as identified in Table 6-1.

Table 6-1. TUSB4041I-Q1 Battery Charging Modes

batEn[n]	VBUS	autoModeEnz	BC MODE PORT *x* (*x* = *n* + 1)
0	Don't care	Don't care	Don't Care
1	<4V	0	Automode(1) (2)
		1	DCP(3) (4)
	>4V	Don't care	CDP(3)

(1) Auto-mode automatically selects divider-mode or DCP mode.
(2) Divider mode can be configured for legacy current mode through register settings.
(3) Attached USB device is USB battery-charging specification revision 1.2 compliant
(4) Chinese Telecommunications Industry Standard YD/T 1591-2009

6.3.2 USB Power Management

The TUSB4041I-Q1 device can be configured for power-switched applications using either per-port or ganged power-enable controls and overcurrent status inputs.

Power switch support is enabled by REG_5h(fullPwrMgmtz), and the per-port or ganged mode is configured by REG_5h(ganged).

The TUSB4041I-Q1 device supports both active-high and active-low power-enable controls. The PWRCTL[4:1] polarity is configured by REG_Ah(pwrctlPol).

6.3.3 One-Time Programmable Configuration

The TUSB4041I-Q1 device allows device configuration through one-time programmable (OTP) non-volatile memory. The programming of the OTP is supported using vendor-defined USB device requests. Contact TI for details using the OTP features

Table 6-2 lists features that can be configured using the OTP.

Table 6-2. OTP Configurable Features

CONFIGURATION REGISTER OFFSET	BIT FIELD	DESCRIPTION
REG_01h	[7:0]	Vendor ID LSB
REG_02h	[7:0]	Vendor ID MSB
REG_03h	[7:0]	Product ID LSB
REG_04h	[7:0]	Product ID MSB
REG_07h	[0]	Port-removable configuration for downstream ports 1. OTP configuration is inverse of rmbl[3:0], that is 1 = not removable, 0 = removable.
REG_07h	[1]	Port-removable configuration for downstream ports 2. OTP configuration is inverse of rmbl[3:0], that is 1 = not removable, 0 = removable.
REG_07h	[2]	Port-removable configuration for downstream ports 3. OTP configuration is inverse of rmbl[3:0], that is 1 = not removable, 0 = removable.
REG_07h	[3]	Port-removable configuration for downstream ports 4. OTP configuration is inverse of rmbl[3:0], that is 1 = not removable, 0 = removable.
REG_0Ah	[3]	Enable device attach detection
REG_0Ah	[4]	High-current divider mode enable
REG_0Bh	[0]	USB 2.0 port polarity configuration for downstream ports 1
REG_0Bh	[1]	USB 2.0 port polarity configuration for downstream ports 2
REG_0Bh	[2]	USB 2.0 port polarity configuration for downstream ports 3
REG_0Bh	[3]	USB 2.0 port polarity configuration for downstream ports 4
REG_F0h	[3:1]	USB power switch power-on delay

6.3.4 Clock Generation

The TUSB4041I-Q1 device accepts a crystal input to drive an internal oscillator or an external clock source. If a clock is provided to the XI pin instead of a crystal, the XO pin is left open. Otherwise, if a crystal is used, the connection must follow these guidelines. Because the XI and XO pins are coupled to other leads and supplies on the PCB, keep traces as short as possible and away from any switching leads. Minimize the capacitance between the XI and XO pins by shielding C1 and C2 with the clean ground lines.

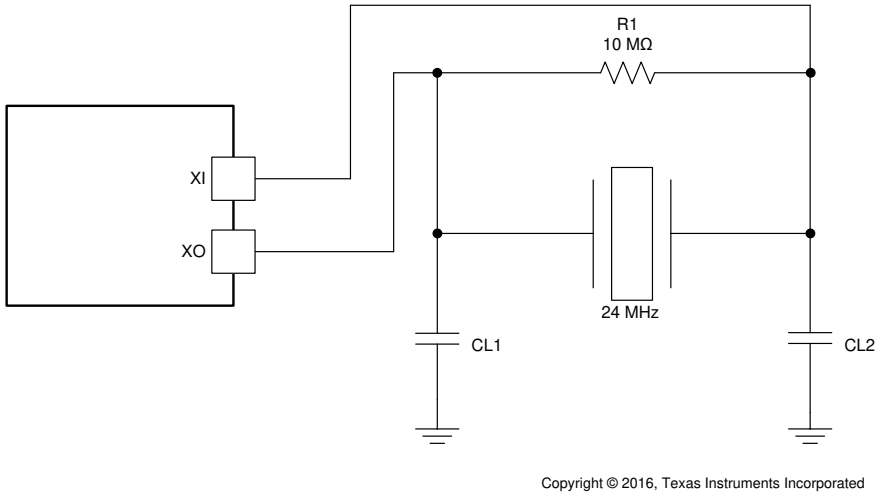


Figure 6-1. TUSB4041I-Q1 Clock

6.3.5 Crystal Requirements

The crystal must be fundamental mode with load capacitance of 12pF to 24pF and frequency stability rating of ±100PPM or better. To ensure proper start-up oscillation condition, TI recommends a maximum crystal equivalent series resistance (ESR) of 50Ω. If a crystal source is used, use a parallel load capacitor. The exact load capacitance value used depends on the crystal vendor. Refer to the *Selection and Specification for Crystals for Texas Instruments USB 2.0 Devices* for details on how to determine the load capacitance value.

6.3.6 Input Clock Requirements

When using an external clock source such as an oscillator, make sure the reference clock has a frequency stability of ±100PPM or better and has less than 50ps absolute peak-to-peak jitter. Tie XI to the 1.8V clock source, and leave XO floating.

6.3.7 Power-Up and Reset

The TUSB4041I-Q1 device does not have specific power-sequencing requirements with respect to the core power (V_{DD}) or I/O and analog power (V_{DD33}). The core power (V_{DD}) or I/O power (V_{DD33}) can be powered up for an indefinite period of time while the other is not powered up if all of the following constraints are met:

- Observe all maximum ratings and recommended operating conditions.
- Observe all warnings about exposure to maximum rated and recommended conditions, particularly junction temperature. These apply to power transitions and normal operation.
- Limit bus contention to 100 hours over the projected lifetime of the device while V_{DD33} is powered-up.
- Do not exceed the ratings listed in the *Absolute Maximum Ratings* table for bus contention while V_{DD33} is powered-down.

A supply bus is powered-up when the voltage is within the recommended operating range. A supply bus is powered-down when it is below that range, and either stable or in transition.

The device requires a minimum reset duration of 3ms. This reset duration is defined as the time when the power supplies are in the recommended operating range to the deassertion of the GRSTz pin. Generate the reset pulse using a programmable-delay supervisory device or using an RC circuit.

6.4 Device Functional Modes

6.4.1 External Configuration Interface

The TUSB4041I-Q1 device supports a serial interface for configuration register access. The device can be configured by an attached I^2C EEPROM or accessed as a target by an SMBus-capable host controller. The external interface is enabled when both the SCL/SMBCLK and SDA/SMBDAT pins are pulled up to 3.3V at the deassertion of reset. The mode, I^2C controller or SMBus target, is determined by the state of SMBUSz pin at reset.

6.4.2 I^2C EEPROM Operation

The TUSB4041I-Q1 device supports a single-controller, standard mode (100 kb/s) connection to a dedicated I^2C EEPROM when the I^2C interface mode is enabled. In I^2C mode, the TUSB4041I-Q1 device reads the contents of the EEPROM at bus address 1010000b using 7-bit addressing starting at address 0.

If the value of the EEPROM contents at byte 00h equals 55h, the TUSB4041I-Q1 device loads the configuration registers according to the EEPROM map. If the first byte is not 55h, the TUSB4041I-Q1 device exits the I^2C mode and continues execution with the default values in the configuration registers. The hub does not connect on the upstream port until the configuration is completed. If the hub detected an unprogrammed EEPROM (value other than 55h), the hub enters programming mode and a programming endpoint within the hub is enabled.

Note

The bytes located above offset Ah are optional. The requirement for data in those addresses is dependent on the options configured in the *Device Configuration Register* and *Device Configuration Register 2*.

For details on I^2C operation, refer to the UM10204 I^2C-bus Specification and User Manual.

6.4.3 SMBus Target Operation

When the SMBus interface mode is enabled, the TUSB4041I-Q1 device supports read block and write block protocols as a target-only SMBus device.

The TUSB4041I-Q1 device target address is 1000 1xyz, where:

- x is the state of GANGED/SMBA2/HS_UP pin at reset
- y is the state of FULLPWRMGMTz/SMBA1 pin at reset
- z is the read-write (R/W) bit; 1 = read access, 0 = write access

If the TUSB4041I-Q1 device is addressed by a host using an unsupported protocol, the device does not respond. The TUSB4041I-Q1 device waits indefinitely for configuration by the SMBus host and does not connect on the upstream port until the SMBus host indicates configuration is complete by clearing the CFG_ACTIVE bit.

For details on SMBus requirements, refer to the *System Management Bus (SMBus) Specification*.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TUSB4041I-Q1 device is a four-port USB 2.0 hub. The provides USB high-speed and full-speed connections on the upstream port and provides USB high-speed, full-speed, or low-speed connections on the downstream port. The TUSB4041I-Q1 device can be used in any application that requires additional USB-compliant ports. For example, a specific notebook can only have two downstream USB ports. By using the TUSB4041I-Q1 device, the notebook can increase the downstream port count to five.

7.2 Typical Application

A common application for the TUSB4041I-Q1 device is as a self-powered standalone USB-hub product. The product is powered by an external 5V DC power adapter. In this application, using a USB cable, the upstream port of the TUSB4041I-Q1 device is plugged into a USB host controller. The downstream ports of the TUSB4041I-Q1 device are exposed to users for connecting USB hard drives, cameras, flash drives, and so forth.

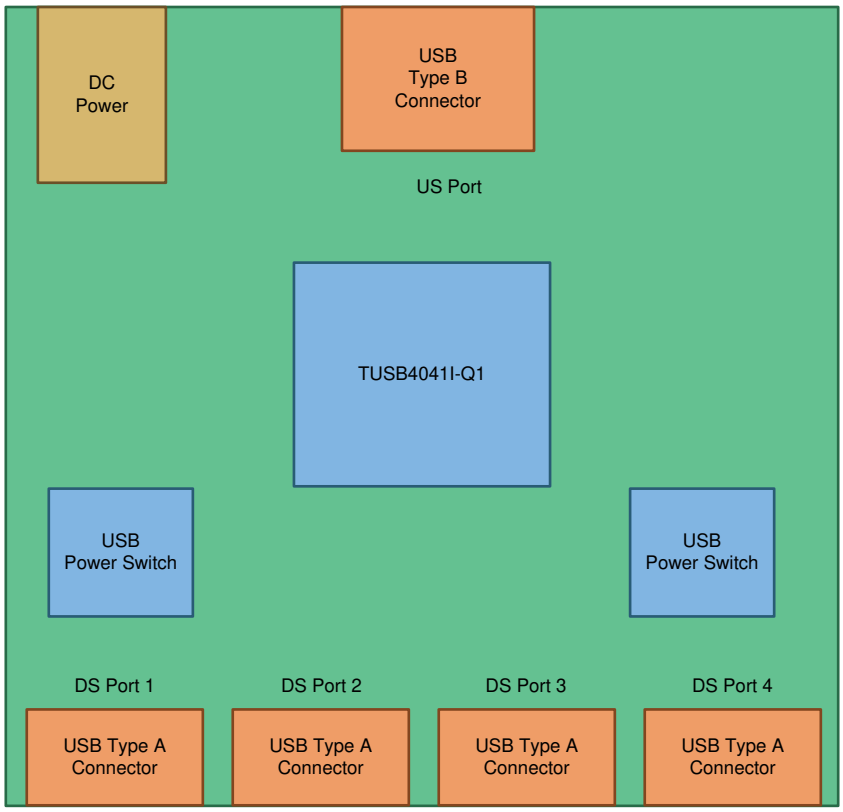


Figure 7-1. Discrete USB Hub Product

7.2.1 Design Requirements

For this design example, use the parameters listed in Table 7-1.

Table 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{DD} supply	1.1V
VDD33 supply	3.3V
Upstream port USB support (HS, FS)	HS, FS
Downstream port 1 USB support (HS, FS, LS)	HS, FS, LS
Downstream port 2 USB support (HS, FS, LS)	HS, FS, LS
Downstream port 3 USB support (HS, FS, LS)	HS, FS, LS
Downstream port 4 USB support (HS, FS, LS)	HS, FS, LS
Number of removable downstream ports	4
Number of non-removable downstream ports	0
Full power management of downstream ports	Yes (FULLPWRMGMTZ = 0)
Individual control of downstream port power switch	Yes (GANGED = 0)
Power switch enable polarity	Active high (PWRCTL_POL = 1)
Battery charge support for downstream port 1	Yes
Battery charge support for downstream port 2	Yes
Battery charge support for downstream port 3	Yes
Battery charge support for downstream port 4	Yes
I^2C EEPROM support	No
24MHz clock source	Crystal

7.2.2 Detailed Design Procedure

7.2.2.1 Upstream Port Implementation

The upstream of the TUSB4041I-Q1 device is connected to a USB2 Type B connector. This particular example has GANGED pin and FULLPWRMGMTZ pin pulled low, which results in individual power support each downstream port. The VBUS signal from the USB2 Type B connector is fed through a voltage divider. The purpose of the voltage divider is to make sure the level meets USB_VBUS input requirements.

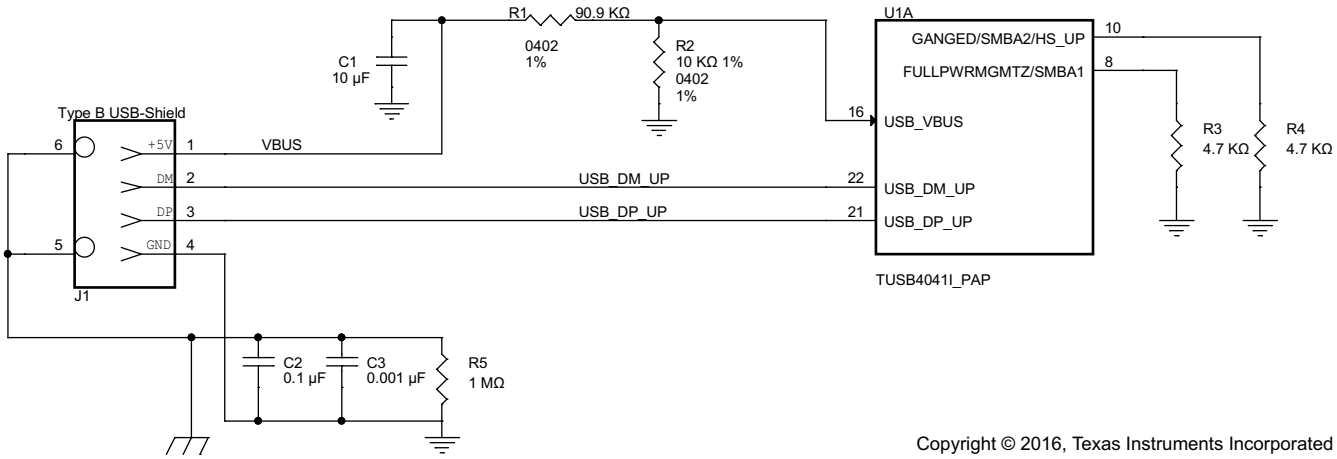


Figure 7-2. Upstream Port Implementation

7.2.2.2 Downstream Port 1 Implementation

The downstream port 1 of the TUSB4041I-Q1 device is connected to a USB2 type A connector. With BATEN1 pin pulled up, battery charge support is enabled for Port 1. If battery charge support is not needed, then uninstall the pullup resistor on BATEN1.

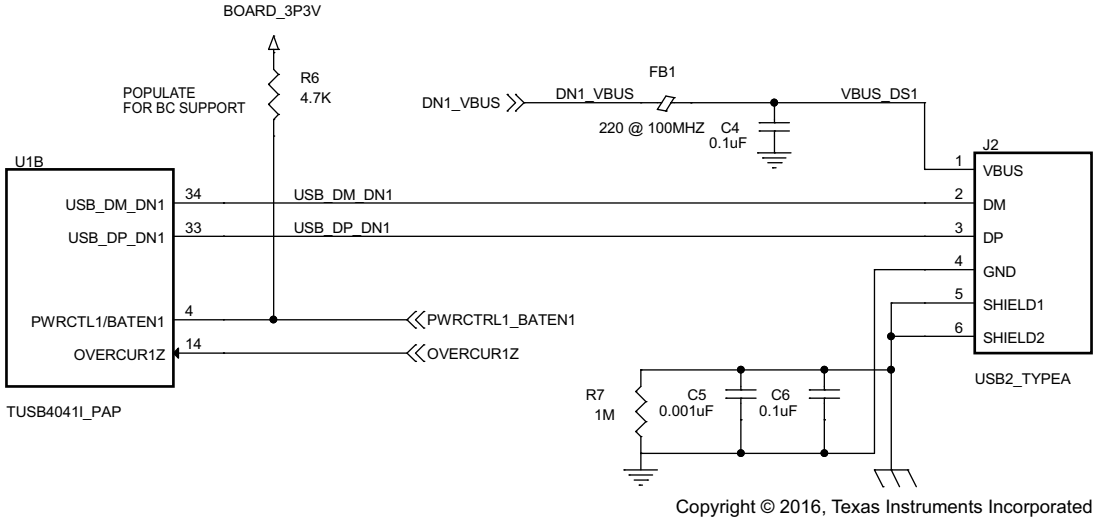


Figure 7-3. Downstream Port 1 Implementation

7.2.2.3 Downstream Port 2 Implementation

The downstream port 2 of the TUSB4041I-Q1 device is connected to a USB2 type A connector. With BATEN2 pin pulled up, battery charge support is enabled for port 2. If battery charge support is not needed, then uninstall the pullup resistor on BATEN2.

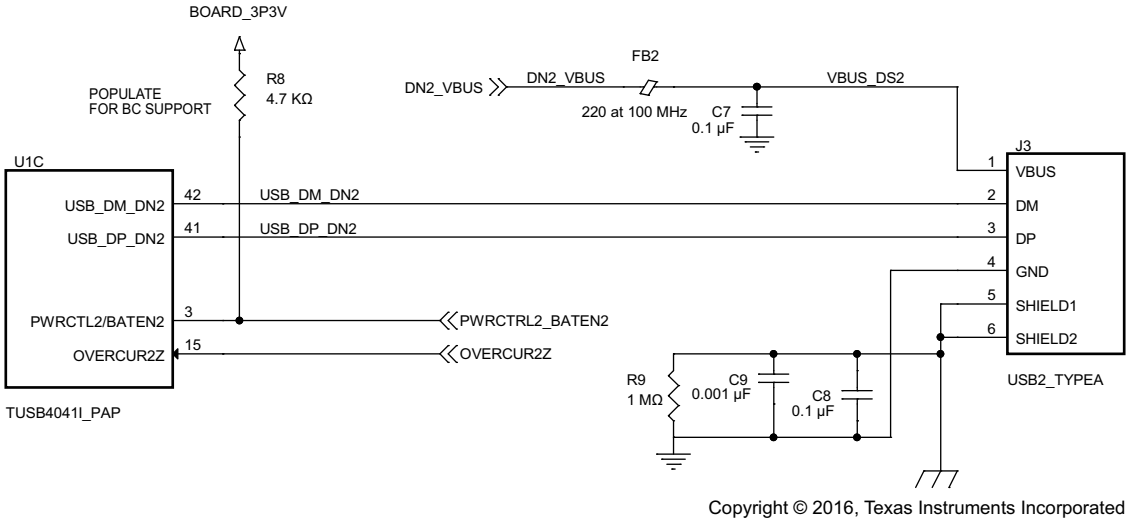


Figure 7-4. Downstream Port 2 Implementation

7.2.2.4 Downstream Port 3 Implementation

The downstream port3 of the TUSB4041I-Q1 device is connected to a USB2 type A connector. With BATEN3 pin pulled up, battery charge support is enabled for port 3. If battery charge support is not needed, then uninstall the pullup resistor on BATEN3.

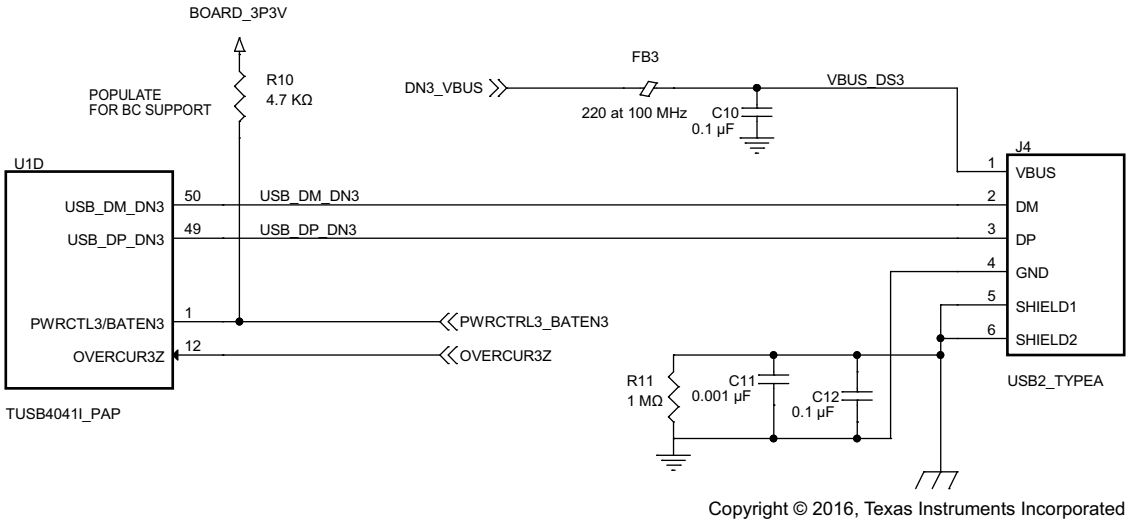


Figure 7-5. Downstream Port 3 Implementation

7.2.2.5 Downstream Port 4 Implementation

The downstream port 4 of the TUSB4041I-Q1 device is connected to a USB2 Type A connector. With BATEN4 pin pulled up, Battery Charge support is enabled for Port 4. If Battery Charge support is not needed, then uninstall the pullup resistor on BATEN4.

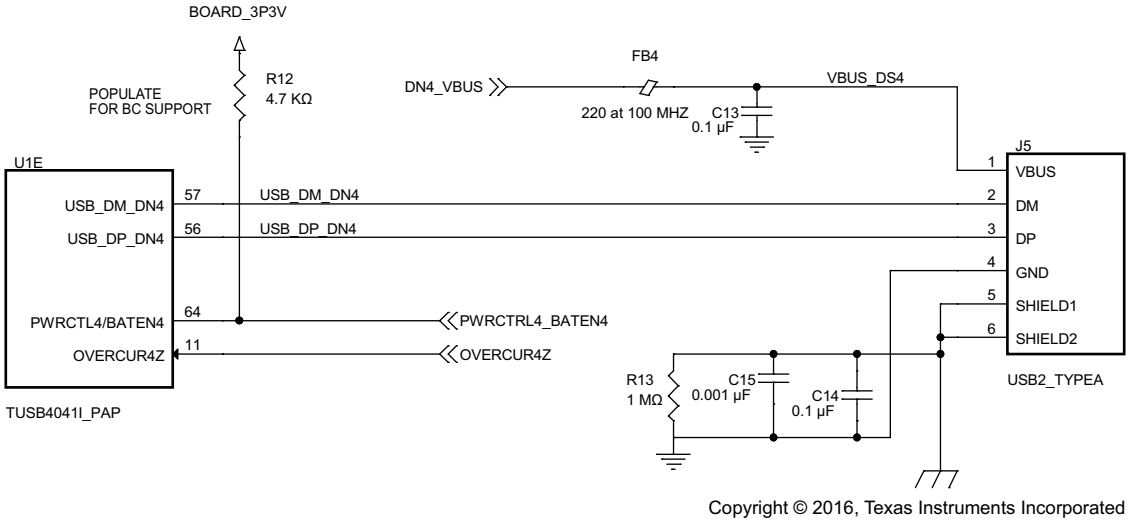


Figure 7-6. Downstream Port 4 Implementation

7.2.2.6 VBUS Power Switch Implementation

This particular example uses TI's TPS2561 dual-channel precision adjustable current-limited power switch. For details on this power switch or other power switches available from TI, refer to www.ti.com.

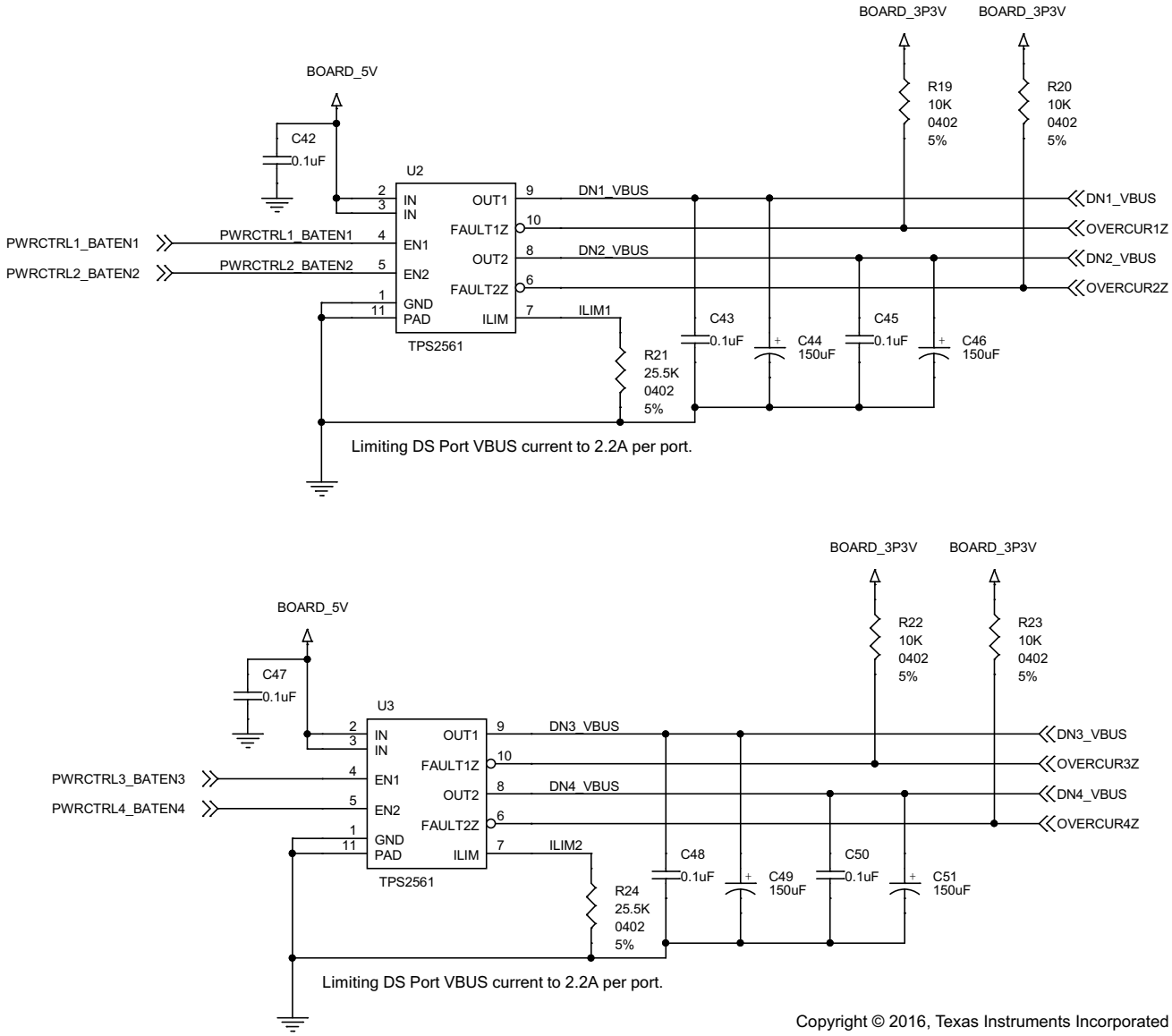


Figure 7-7. VBUS Power Switch Implementation

7.2.2.7 Clock, Reset, and Miscellaneous

The PWRCTL_POL is left unconnected which results in active-high power enable (PWRCTL1, PWRCTL2, PWRCTL3, and PWRCTL4) for a USB VBUS power switch. The 1-µF capacitor on the GRSTN pin can only be used if the VDD11 supply is stable before the VDD33 supply. Depending on the supply ramp of the two supplies, the user may need to adjust the capacitor.

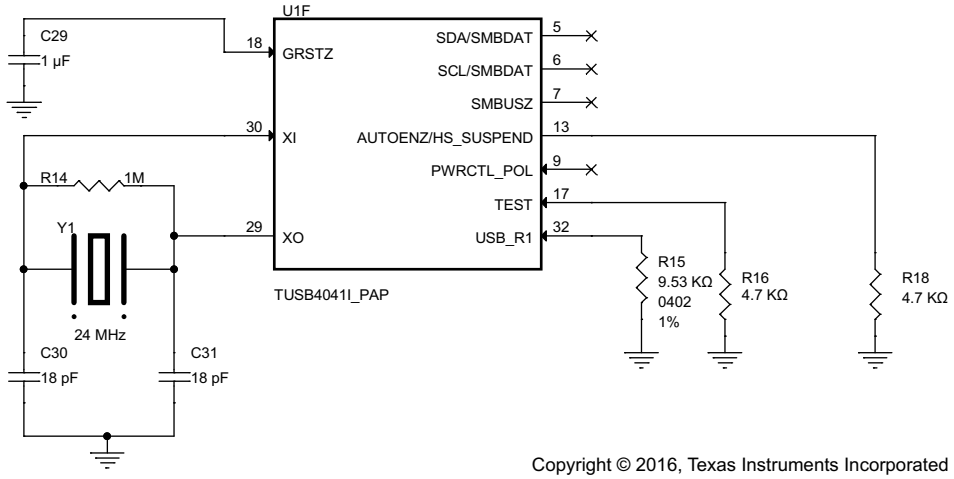


Figure 7-8. Clock, Reset, and Miscellaneous

7.2.2.8 TUSB4041I-Q1 Power Implementation

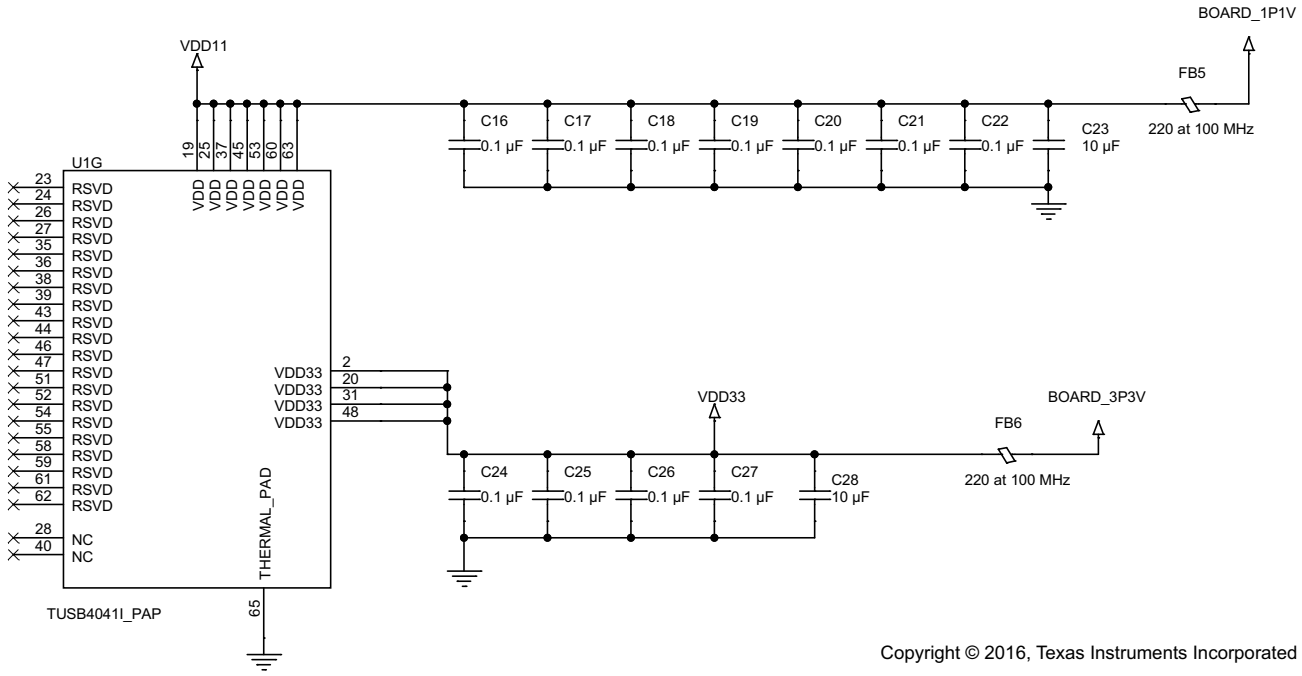


Figure 7-9. TUSB4041I-Q1 Power Implementation

7.2.3 Application Curves

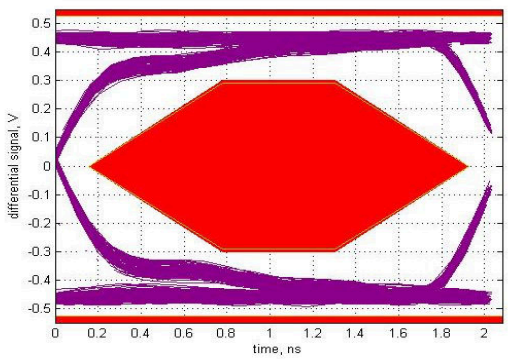


Figure 7-10. High-Speed Upstream Port

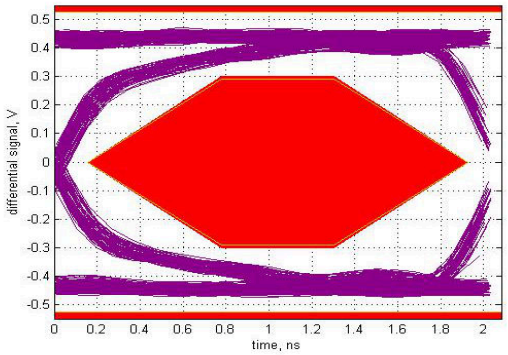


Figure 7-11. High-Speed Downstream Port 1

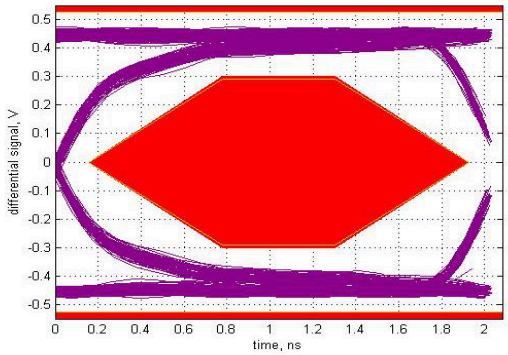


Figure 7-12. High-Speed Downstream Port 2

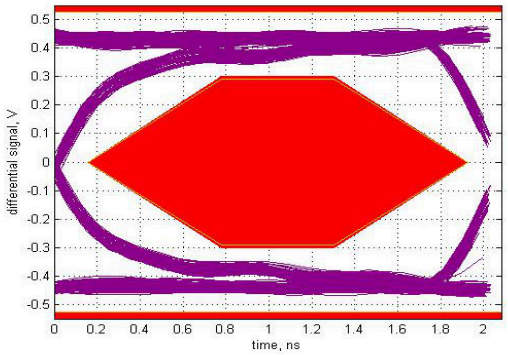


Figure 7-13. High-Speed Downstream Port 3

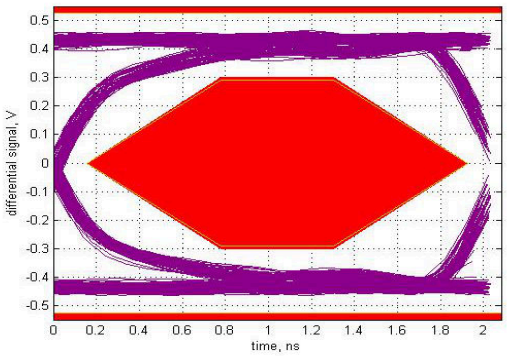


Figure 7-14. High-Speed Downstream Port 4

7.3 Power Supply Recommendations

7.3.1 TUSB4041I-Q1 Power Supply

Implement V_{DD} as a single power plane, as well as V_{DD33}.

- The V_{DD} pins of the TUSB4041I-Q1 supply 1.1V (nominal) power to the core of the TUSB4041I-Q1 device. This power rail can be isolated from all other power rails by a ferrite bead to reduce noise.
- The DC resistance of the ferrite bead on the core power rail can affect the voltage provided to the device because of the high current draw on the power rail. The user may need to adjust the output of the core voltage regulator to account for this, or select a ferrite bead with low DC resistance (less than 0.05Ω).

- The V_{DD33} pins of the TUSB4041I-Q1 device supply 3.3V power rail to the I/O of the TUSB4041I-Q1 device. This power rail can be isolated from all other power rails by a ferrite bead to reduce noise.
- All power rails require a 10µF capacitor or 1µF capacitors for stability and noise immunity. These bulk capacitors can be placed anywhere on the power rail. Place the smaller decoupling capacitors as close to the TUSB4041I-Q1 power pins as possible with an optimal grouping of two capacitors of differing values per pin.

7.3.2 Downstream Port Power

- A source capable of supplying 5V and up to 500mA per port must supply the downstream port power, VBUS. The TUSB4041I-Q1 signals can control the downstream port power switches. Leaving the downstream port power as always enabled is also possible.
- The VBUS of each downstream port requires a large-bulk low-ESR capacitor of 22µF or larger to limit in-rush current.
- TI recommends the ferrite beads on the VBUS pins of the downstream USB port connections for both ESD and EMI reasons. A 0.1µF capacitor on the USB connector side of the ferrite provides a low-impedance path to ground for fast rise time ESD current that might have coupled onto the VBUS trace from the cable.

7.3.3 Ground

TI recommends to use only one board ground plane in the design which provides the best image plane for signal traces running above the plane. Connect the thermal pad of the TUSB4041I-Q1 and any of the voltage regulators to this plane with vias. An earth or chassis ground is implemented only near the USB port connectors on a different plane for EMI and ESD purposes.

7.4 Layout

7.4.1 Layout Guidelines

Use the layout guidelines listed in this section for proper PCB layout design.

7.4.1.1 Placement

- Place a 9.53-kΩ ±1% resistor connected to pin USB_R1 as close as possible to the TUSB4041I-Q1 device.
- Place a 0.1-µF capacitor as close as possible on each V_{DD} and VDD33 power pin.
- Place the ESD and EMI protection devices (if used) as close as possible to the USB connector.
- If a crystal is used, place the crystal as close as possible to the XI and XO pins of the TUSB4041I-Q1 device.
- Place voltage regulators as far away as possible from the TUSB4041I-Q1 device, the crystal, and the differential pairs.
- In general, place the large bulk capacitors associated with each power rail as close as possible to the voltage regulators.

7.4.1.2 Package Specific

- The TUSB4041I-Q1 device package has a 0.5mm pin pitch.
- The TUSB4041I-Q1 device package has a 4.64mm × 4.64mm thermal pad. This thermal pad must be connected to ground through a system of vias.
- Solder mask all vias under device, except for those connected to the thermal pad, to avoid any potential issues with thermal pad layouts.

7.4.1.3 Differential Pairs

This section describes the layout recommendations for all the TUSB4041I-Q1 device differential pairs: USB_DP_XX, USB_DM_XX.

- The differential pairs must be designed with a differential impedance of 90 Ω ± 10%.
- To minimize crosstalk, TI recommends to keep high-speed signals away from each other. Separate each pair by at least 5 times the signal trace width. Separating with ground as depicted in the layout example also helps minimize crosstalk.
- Route all differential pairs on the same layer adjacent to a solid ground plane.
- Do not route differential pairs over any plane split.

- Adding test points causes impedance discontinuity and therefore negatively impacts signal performance. If test points are used, place them in series and symmetrically. Do not place them in a manner that causes stub on the differential pair.
- Avoid 90° turns in trace. Keep the use of bends in differential traces to a minimum. When bends are used, make sure the number of left and right bends are as equal as possible and that the angle of the bend is ≥135°. This guideline minimizes any length mismatch caused by the bends and therefore minimize the impact bends have on EMI.
- Minimize the trace lengths of the differential pair traces. Eight inches is the maximum recommended trace length for USB 2.0 differential pair signals. Longer trace lengths require very careful routing to ensure proper signal integrity.
- Match the etch lengths of the differential pair traces (that is DP and DM). Make sure the USB 2.0 differential pairs do not exceed 50 mils relative trace length difference.
- Minimize the use of vias in the differential pair paths as much as possible. If this is not practical, make sure that the same via type and placement are used for both signals in a pair. Place any vias used as close as possible to the TUSB4041I-Q1 device.
- To ease routing of the USB 2.0 DP and DM pair, the polarity of these pins can be swapped. If this is done, set the appropriate Px_usb2pol register, where x = 0, 1, 2, 3, or 4.
- Do not place power fuses across the differential pair traces.

7.4.2 Layout Example

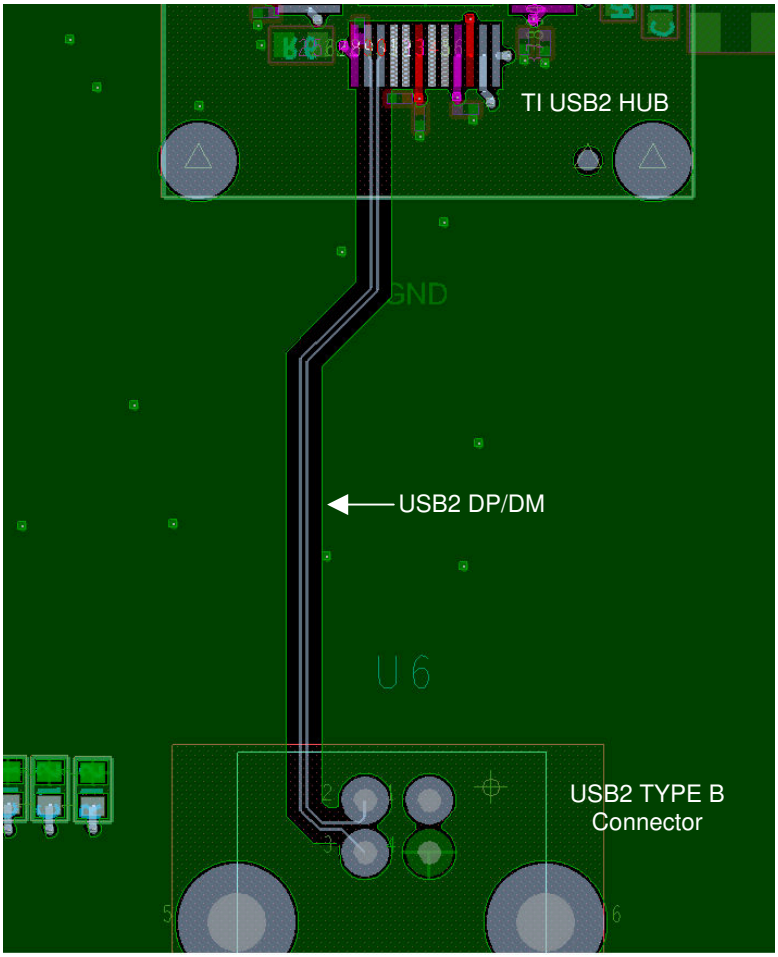


Figure 7-15. Example Routing of Upstream Port

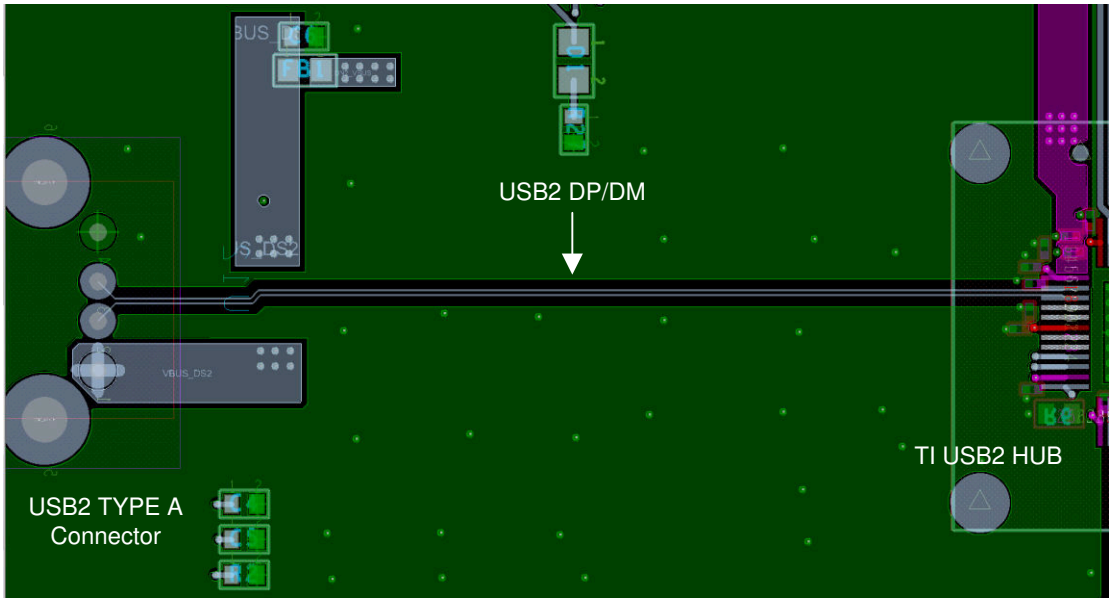


Figure 7-16. Example Routing of Downstream Port

8 Register Maps

8.1 Configuration Registers

The internal configuration registers are accessed on byte boundaries. The configuration register values are loaded with defaults, but can be overwritten when the TUSB4041I-Q1 device is in I^2C or SMBus mode.

Table 8-1. Memory Map

BYTE ADDRESS	CONTENTS	EEPROM CONFIGURABLE
00h	ROM Signature Register	No
01h	Vendor ID LSB	Yes
02h	Vendor ID MSB	Yes
03h	Product ID LSB	Yes
04h	Product ID MSB	Yes
05h	Device Configuration Register	Yes
06h	Battery Charging Support Register	Yes
07h	Device Removable Configuration Register	Yes
08h	Port Used Configuration Register	Yes
09h	Reserved	Yes, program to 00h
0Ah	Device Configuration Register 2	Yes
0Bh	USB 2.0 Port Polarity Control Register	Yes
0Ch to 0Fh	Reserved	No
10h to 1Fh	UUID Byte [15:0]	No
20h to 21h	LangID Byte [1:0]	Yes, if customStrings is set
22h	Serial Number String Length	Yes, if customSerNum is set
23h	Manufacturer String Length	Yes, if customStrings is set
24h	Product String Length	Yes, if customStrings is set
25h to 2Fh	Reserved	No
30h to 4Fh	Serial Number String Byte [31:0]	Yes, if customSerNum is set
50h to 8Fh	Manufacturer String Byte [63:0]	Yes, if customStrings is set
90h to CFh	Product String Byte [63:0]	Yes, if customStrings is set
D0 to DFh	Reserved	No
F0h	Additional Feature Configuration Register	Yes
F1 to F7h	Reserved	No
F8h	Device Status and Command Register	No
F9 to FFh	Reserved	No

8.2 ROM Signature Register

Offset = 0h

Figure 8-1. ROM Signature Register

7	6	5	4	3	2	1	0
romSignature							
RW-0							

Table 8-2. ROM Signature Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	romSignature	RW	0	ROM signature register The TUSB4041I-Q1 device uses this register in I^2C mode to validate whether the attached EEPROM has been programmed. The first byte of the EEPROM is compared to the mask 55h and if not a match, the TUSB4041I-Q1 device aborts the EEPROM load and executes with the register defaults.

8.3 Vendor ID LSB Register

Offset = 1h, reset = 51h

Figure 8-2. Vendor ID LSB Register

7	6	5	4	3	2	1	0
vendorIdLsb[7]	vendorIdLsb[6]	vendorIdLsb[5]	vendorIdLsb[4]	vendorIdLsb[3:1]			vendorIdLsb[0]
R/RW-0	R/RW-1	R/RW-0	R/RW-1	R/RW-0			R/RW-1

Table 8-3. Vendor ID LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7	vendorIdLsb[7]	R/RW	0	Vendor ID LSB Least significant byte of the unique vendor ID assigned by the USB-IF; the default value of this register is 51h representing the LSB of the TI Vendor ID 0451h. The value can be overwritten to indicate a customer vendor ID. This field is R/W unless the OTP ROM VID and OTP ROM PID values are non-zero. If both values are non-zero, the value when reading this register reflects the OTP ROM value.
6	vendorIdLsb[6]	R/RW	1	
5	vendorIdLsb[5]	R/RW	0	
4	vendorIdLsb[4]	R/RW	1	
3:1	vendorIdLsb[3:1]	R/RW	0	
0	vendorIdLsb[0]	R/RW	1	

8.4 Vendor ID MSB Register

Offset = 2h, reset = 04h

Figure 8-3. Vendor ID MSB Register

7	6	5	4	3	2	1	0
vendorIdMsb[7:3]					vendorIdMsb[2]	vendorIdMsb[1:0]	
R/RW-0					R/RW-1	R/RW-0	

Table 8-4. Vendor ID MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	vendorIdMsb[7:3]	R/RW	0	Vendor ID MSB Most significant byte of the unique vendor ID assigned by the USB-IF; the default value of this register is 04h representing the MSB of the TI Vendor ID 0451h. The value can be overwritten to indicate a customer vendor ID. This field is R/W unless the OTP ROM VID and OTP ROM PID values are non-zero. If both values are non-zero, the value when reading this register shall reflect the OTP ROM value.
2	vendorIdMsb[2]	R/RW	1	
1:0	vendorIdMsb[1:0]	R/RW	0	

8.5 Product ID LSB Register

Offset = 3h, reset = 40h

Figure 8-4. Product ID LSB Register

7	6	5	4	3	2	1	0
productIdLsb[7]	productIdLsb[6]	productIdLsb[5:0]					
R/RW-0	R/RW-1	R/RW-0					

Table 8-5. Product ID LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7	productIdLsb[7]	R/RW	0	Product ID LSB. The default value of this register is 40h representing the LSB of the product ID assigned by TI. The value reported in the USB 2.0 device descriptor is the value of this register bit wise XORed with 00000010b. The value can be overwritten to indicate a customer product ID. This field is R/W unless the OTP ROM VID and OTP ROM PID values are non-zero. If both values are non-zero, the value when reading this register reflects the OTP ROM value.
6	productIdLsb[6]	R/RW	1	
5:0	productIdLsb[5:0]	R/RW	0	

8.6 Product ID MSB Register

Offset = 4h, reset = 81h

Figure 8-5. Product ID MSB Register

7	6	5	4	3	2	1	0
productIdMsb[7]	productIdMsb[6:1]						productIdMsb[0]
R/RW-1	R/RW-0						R/RW-1

Table 8-6. Product ID MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7	productIdMsb[7]	R/RW	1	Product ID MSB Most significant byte of the product ID assigned by TI; the default value of this register is 81h representing the MSB of the product ID assigned by TI. The value can be overwritten to indicate a customer product ID. This field is R/W unless the OTP ROM VID and OTP ROM PID values are non-zero. If both values are non-zero, the value when reading this register reflects the OTP ROM value.
6:1	productIdMsb[6:1]	R/RW	0	
0	productIdMsb[0]	R/RW	1	

8.7 Device Configuration Register

Offset = 5h

Figure 8-6. Device Configuration Register

7	6	5	4	3	2	1	0
customStrings	customSernum	RSVD	RSVD	ganged	fullPwrMgmtz	RSVD	RSVD
RW-0	RW-0	RW-0	R-1	RW-X	RW-X	RW-0	R-0

Table 8-7. Device Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
7	customStrings	RW	0	Custom strings enable This bit controls the ability to write to the Manufacturer String Length, Manufacturer String, Product String Length, Product String, and Language ID registers 0 = The Manufacturer String Length, Manufacturer String, Product String Length, Product String, and Language ID registers are read only. 1 = The Manufacturer String Length, Manufacturer String, Product String Length, Product String, and Language ID registers can be loaded by EEPROM or written by SMBus. The default value of this bit is 0.
6	customSernum	RW	0	Custom serial number enable This bit controls the ability to write to the serial number registers. 0 = The Serial Number String Length and Serial Number String registers are read only. 1 = Serial Number String Length and Serial Number String registers can be loaded by EEPROM or written by SMBus. The default value of this bit is 0.
5	RSVD	RW	0	Reserved.
4	RSVD	R	1	Reserved. This bit is reserved and returns 1 when read.
3	ganged	RW	X	Ganged This bit is loaded at the deassertion of reset with the value of the GANGED/SMBA2/HS_UP pin. 0 = Each port is individually power switched and enabled by the PWRCTL[4:1]/BATEN[4:1] pins. 1 = The power switch control for all ports is ganged and enabled by the PWRCTL[4:1]/BATEN1 pin. When the TUSB4041I-Q1 device is in I^2C mode, the TUSB4041I-Q1 device loads this bit from the contents of the EEPROM. When the TUSB4041I-Q1 device is in SMBUS mode, the value can be overwritten by an SMBus host.

Table 8-7. Device Configuration Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	fullPwrMgmtz	RW	X	Full power management This bit is loaded at the deassertion of reset with the value of the FULLPWRMGMTz/SMBA1 pin. 0 = Port power switching status reporting is enabled 1 = Port power switching status reporting is disabled When the TUSB4041I-Q1 device is in I^2C mode, the TUSB4041I-Q1 device loads this bit from the contents of the EEPROM. When the TUSB4041I-Q1 device is in SMBUS mode, the value can be overwritten by an SMBus host.
1	RSVD	RW	0	Reserved This field is reserved and should not be altered from the default.
0	RSVD	R	0	Reserved This field is reserved and returns 0 when read.

8.8 Battery Charging Support Register

Offset = 6h

Figure 8-7. Battery Charging Support Register

7	6	5	4	3	2	1	0
RSVD				batEn[3:0]			
R-0				RW-X			

Table 8-8. Battery Charging Support Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RSVD	R	0	Reserved Read only, returns 0 when read.
3:0	batEn[3:0]	RW	X	Battery Charger Support. The bits in this field indicate whether the downstream port implements the charging port features. 0 = The port is not enabled for battery charging support features 1 = The port is enabled for battery charging support features Each bit corresponds directly to a downstream port, that is batEn0 corresponds to downstream port 1, and batEN1 corresponds to downstream port 2. The default value for these bits are loaded at the deassertion of reset with the value of PWRCTL/BATEN[3:0]. When in I^2C/SMBus mode the bits in this field can be overwritten by EEPROM contents or by an SMBus host.

8.9 Device Removable Configuration Register

Offset = 7h

Figure 8-8. Device Removable Configuration Register

7	6	5	4	3	2	1	0
customRmbl	RSVD			rmbl[3:0]			
RW-0	R-0			RW-X			

Table 8-9. Device Removable Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
7	customRmbl	RW	0	Custom removable This bit controls the ability to write to the port removable bits. 0 = rmbl[3:0] are read only, and the values are loaded from the OTP ROM. 1 = rmbl[3:0] are R/W and can be loaded by EEPROM or written by SMBus. This bit can be written simultaneously with rmbl[3:0].
6:4	RSVD	R	0	Reserved Read only, returns 0 when read

Table 8-9. Device Removable Configuration Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	rmbl[3:0]	RW	X	Removable The bits in this field indicate whether a device attached to downstream ports 4 through 1 are removable or permanently attached. 0 = The device attached to the port is not removable. 1 = The device attached to the port is removable. Each bit corresponds directly to a downstream port n + 1, For example: rmbl0 corresponds to downstream port 1, rmbl1 corresponds to downstream port 2, and so on. This field is read only unless the customRmbl bit is set to 1. Otherwise, the value of this field reflects the inverted values of the OTP ROM non_rmb[3:0] field.

8.10 Port Used Configuration Register

Offset = 8h

Figure 8-9. Port Used Configuration Register

7	6	5	4	3	2	1	0
RSVD				used[3:0]			
R-0				RW-1			

Table 8-10. Port Used Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RSVD	R	0	Reserved Read only
3:0	used[3:0]	RW	1	Used The bits in this field indicate whether a port is enabled. 0 = The port is disabled. 1 = The port is enabled. Each bit corresponds directly to a downstream port. For example: used0 corresponds to downstream port 1, used1 corresponds to downstream port 2, and so on. All combinations are supported with the exception of both ports 1 and 3 marked as disabled.

8.11 Device Configuration Register 2

Offset = Ah

Figure 8-10. Device Configuration Register 2

7	6	5	4	3	2	1	0
RSVD	customBCfeatures	pwrctlPol	HiCurAcpModeEn	cpdEN	RSVD	autoModeEnz	RSVD
R-0	RW-0	RW-X	R/RW-0	R/RW-0	RW-0	RW-X	R-0

Table 8-11. Device Configuration Register 2 Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0	Reserved Read only, returns 0 when read.
6	customBCfeatures	RW	0	Custom battery charging feature enable This bit controls the ability to write to the battery charging feature configuration controls. 0 = The HiCurAcpModeEn and cpdEN bits are read only and the values are loaded from the OTP ROM. 1 = The HiCurAcpModeEn and cpdEN, bits are R/W and can be loaded by EEPROM or written by SMBus from this register. This bit can be written simultaneously with HiCurAcpModeEn and cpdEN.

Table 8-11. Device Configuration Register 2 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	pwrctlPol	RW	X	Power enable polarity This bit is loaded at the deassertion of reset with the value of the PWRCTL_POL pin. 0 = PWRCTL polarity is active low. 1 = PWRCTL polarity is active high. When the TUSB4041I-Q1 device is in I^{2}C mode, the TUSB4041I-Q1 device loads this bit from the contents of the EEPROM. When the TUSB4041I-Q1 device is in SMBUS mode, the value can be overwritten by an SMBus host.
4	HiCurAcpModeEn	R/RW	0	High-current ACP mode enable This bit enables the high-current tablet charging mode when the automatic battery charging mode is enabled for downstream ports. 0 = High-current divider mode disabled. Legacy current divider mode enabled. 1 = High-current divider mode enabled This bit is read only unless the customBCfeatures bit is set to 1. If customBCfeatures is 0, the value of this bit reflects the value of the OTP ROM HiCurAcpModeEn bit.
3	cpdEN	RRW	0	Enable device attach detection This bit enables device attach detection (such as a cell-phone detect) when auto mode is enabled. 0 = Device attach detect is disabled in auto mode. 1 = Device attach detect is enabled in auto mode. This bit is read only unless the customBCfeatures bit is set to 1. If customBCfeatures is 0, the value of this bit reflects the value of the OTP ROM cpdEN bit.
2	RSVD	RW	0	Reserved
1	autoModeEnz	RW	X	Automatic mode enable(1) This bit is loaded at the deassertion of reset with the value of the AUTOENz/HS_SUSPEND pin. The automatic mode only applies to downstream ports with battery charging enabled when the upstream port is not connected. Under these conditions: 0 = Automatic mode battery charging features are enabled. 1 = Automatic mode is disabled; only battery-charging DCP mode is supported.
0	RSVD	R	0	Reserved Read only, returns 0 when read.

(1) When the upstream port is connected, battery charging 1.2 CDP mode is supported on all ports that are enabled for battery charging support regardless of the value of this bit, with the exception of port 1. CDP on port 1 is not supported when automatic mode is enabled.

8.12 USB 2.0 Port Polarity Control Register

Offset = Bh

Figure 8-11. USB 2.0 Port Polarity Control Register

7	6	5	4	3	2	1	0
customPolarity	RSVD		p4_usb2pol	p3_usb2pol	p2_usb2pol	p1_usb2pol	p0_usb2pol
RW-0	R-0		R/RW-0	R/RW-0	R/RW-0	R/RW-0	R/RW-0

Table 8-12. USB 2.0 Port Polarity Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7	customPolarity	RW	0	Custom USB 2.0 polarity This bit controls the ability to write the p[4:0]_usb2pol bits. 0 = The p[4:0]_usb2pol bits are read only, and the values are loaded from the OTP ROM. 1 = The p[4:0]_usb2pol bits are R/W and can be loaded by EEPROM or written by SMBus from this register. This bit can be written simultaneously with the p[4:0]_usb2pol bits
6:5	RSVD	R	0	Reserved Read only, returns 0 when read
4	p4_usb2pol	R/RW	0	Downstream port 4 DM/DP polarity This bit controls the polarity of the port. 0 = USB 2.0 port polarity is as shown in the pinout. 1 = USB 2.0 port polarity is swapped from that shown in the pinout (that is, DM becomes DP, and DP becomes DM). This bit is read only unless the customPolarity bit is set to 1. If customPolarity is 0, the value of this bit reflects the value of the OTP ROM p4_usb2pol bit.
3	p3_usb2pol	R/RW	0	Downstream port 3 DM/DP polarity This bit controls the polarity of the port. 0 = USB 2.0 port polarity is as shown in the pinout. 1 = USB 2.0 port polarity is swapped from that shown in the pinout (that is, DM becomes DP, and DP becomes DM). This bit is read only unless the customPolarity bit is set to 1. If customPolarity is 0, the value of this bit reflects the value of the OTP ROM p3_usb2pol bit.
2	p2_usb2pol	R/RW	0	Downstream port 2 DM/DP polarity This bit controls the polarity of the port. 0 = USB 2.0 port polarity is as shown in the pinout. 1 = USB 2.0 port polarity is swapped from that shown in the pinout (that is, DM becomes DP, and DP becomes DM). This bit is read only unless the customPolarity bit is set to 1. If customPolarity is 0, the value of this bit reflects the value of the OTP ROM p2_usb2pol bit.

Table 8-12. USB 2.0 Port Polarity Control Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	p1_usb2pol	RRW	0	Downstream port 1 DM/DP polarity This bit controls the polarity of the port. 0 = USB 2.0 port polarity is as shown in the pinout. 1 = USB 2.0 port polarity is swapped from that shown in the pinout (that is, DM becomes DP, and DP becomes DM). This bit is read only unless the customPolarity bit is set to 1. If customPolarity is 0, the value of this bit reflects the value of the OTP ROM p1_usb2pol bit.
0	p0_usb2pol	R/RW	0	Upstream port DM/DP polarity This bit controls the polarity of the port. 0 = USB 2.0 port polarity is as shown in the pinout. 1 = USB 2.0 port polarity is swapped from that shown in the pinout (that is, DM becomes DP, and DP becomes DM). This bit is read only unless the customPolarity bit is set to 1. If customPolarity is 0, the value of this bit reflects the value of the OTP ROM p0_usb2pol bit.

8.13 UUID Byte N Register

Offset = 10h-1Fh

Figure 8-12. UUID Byte N Register

7	6	5	4	3	2	1	0
uuidByte[n]							
R-X							

Table 8-13. UUID Byte N Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	uuidByte[n]	R	X	UUID byte N The UUID returned in the Container ID descriptor. The value of this register is provided by the device and meets the UUID requirements of the Internet Engineering Task Force (IETF) RFC 4122 A UUID URN Namespace.

8.14 Language ID LSB Register

Offset = 20h, reset = 09h

Figure 8-13. Language ID LSB Register

7	6	5	4	3	2	1	0
langIdLsb[7:4]				langIdLsb[3]	langIdLsb[2:1]		langIdLsb[0]
R/RW-0				R/RW-1	R/RW-0		R/RW-1

Table 8-14. Language ID LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	langIdLsb[7:4]	R/RW	0	Language ID least significant byte This register contains the value returned in the LSB of the LANGID code in string index 0. The TUSB4041I-Q1 device only supports one language ID. The default value of this register is 09h representing the LSB of the LangID 0409h indicating English United States. When the customStrings bit is set to 1, this field can be overwritten by the contents of an attached EEPROM or by an SMBus host.
3	langIdLsb[3]	R/RW	1	
2:1	langIdLsb[2:1]	R/RW	0	
0	langIdLsb[0]	R/RW	1	

8.15 Language ID MSB Register

Offset = 21h, reset = 04h

Figure 8-14. Language ID MSB Register

7	6	5	4	3	2	1	0
langIdMsb[7:3]					langIdMsb[2]	langIdMsb[1:0]	
R/RW-0					R/RW-1	R/RW-0	

Table 8-15. Language ID MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	langIdMsb[7:3]	R/RW	0	Language ID most significant byte This register contains the value returned in the MSB of the LANGID code in string index 0. The TUSB4041I-Q1 device only supports one language ID. The default value of this register is 04h representing the MSB of the LangID 0409h indicating English United States. When the customStrings bit is set to 1, this field can be overwritten by the contents of an attached EEPROM or by an SMBus host.
2	langIdMsb[2]	R/RW	1	
1:0	langIdMsb[1:0]	R/RW	0	

8.16 Serial Number String Length Register

Offset = 22h

Figure 8-15. Serial Number String Length Register

7	6	5	4	3	2	1	0
RSVD		serNumStringLen[5]	serNumStringLen[4:3]		serNumStringLen[2:0]		
R-0		R/RW-0	R/RW-1		R/RW-0		

Table 8-16. Serial Number String Length Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RSVD	R	0	Reserved Read only, returns 0 when read.
5	serNumStringLen[5]	R/RW	0	Serial number string length The string length in bytes for the serial number string. The default value is 18h indicating that a 24-byte serial number string is supported. The maximum string length is 32 bytes. When the customSernum bit is set to 1, this field can be overwritten by the contents of an attached EEPROM or by an SMBus host. When the field is non-zero, a serial number string of serNumbStringLen bytes is returned at string index 1 from the data contained in the Serial Number String registers.
4:3	serNumStringLen[4:3]	R/RW	1	
2:0	serNumStringLen[2:0]	R/RW	0	

8.17 Manufacturer String Length Register

Offset = 23h

Figure 8-16. Manufacturer String Length Register

7	6	5	4	3	2	1	0
RSVD	mfgStringLen						
R-0	R/RW-0						

Table 8-17. Manufacturer String Length Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0	Reserved Read only, returns 0 when read
6:0	mfgStringLen	R/RW	0	Manufacturer string length The string length in bytes for the manufacturer string. The default value is 0, indicating that a manufacturer string is not provided. The maximum string length is 64 bytes. When the customStrings bit is set to 1, this field can be overwritten by the contents of an attached EEPROM or by an SMBus host. When the field is non-zero, a manufacturer string of mfgStringLen bytes is returned at string index 3 from the data contained in the Manufacturer String registers.

8.18 Product String Length Register

Offset = 24h

Figure 8-17. Product String Length Register

7	6	5	4	3	2	1	0
RSVD	prodStringLen						
R-0	R/RW-0						

Table 8-18. Product String Length Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0	Reserved Read only, returns 0 when read.
6:0	prodStringLen	R/RW	0	Product string length The string length in bytes for the product string. The default value is 0, indicating that a product string is not provided. The maximum string length is 64 bytes. When the customStrings bit is set to 1, this field can be overwritten by the contents of an attached EEPROM or by an SMBus host. When the field is non-zero, a product string of prodStringLen bytes is returned at string index 3 from the data contained in the Product String registers.

8.19 Serial Number String Registers

Offset = 30h-4Fh

Figure 8-18. Serial Number String Registers

7	6	5	4	3	2	1	0
serialNumber[n]							
R/RW-X							

Table 8-19. Serial Number String Registers Field Descriptions

Bit	Field	Type	Reset	Description
7:0	serialNumber[n]	R/RW	X	Serial Number byte N The serial number returned in the Serial Number string descriptor at string index 1. The default value of these registers is assigned by TI. When customSernum is 1, these registers can be overwritten by EEPROM contents or by an SMBus host.

8.20 Manufacturer String Registers

Offset = 50h-8Fh

Figure 8-19. Manufacturer String Registers

7	6	5	4	3	2	1	0
mfgStringByte[n]							
R/W-0							

Table 8-20. Manufacturer String Registers Field Descriptions

Bit	Field	Type	Reset	Description
7:0	mfgStringByte[n]	R/W	0	Manufacturer string byte N These registers provide the string values returned for string index 3 when mfgStringLen is greater than 0. The number of bytes returned in the string is equal to mfgStringLen. The programmed data must be in UNICODE UTF-16LE encodings as defined by the Unicode Standard, Worldwide Character Encoding, Version 5.0.

8.21 Product String Byte N Register

Offset = 90h-CFh

Figure 8-20. Product String Byte N Register

7	6	5	4	3	2	1	0
prodStringByte[n]							
R/RW-0							

Table 8-21. Product String Byte N Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	prodStringByte[n]	R/RW	0	Product string byte N These registers provide the string values returned for string index 2 when prodStringLen is greater than 0. The number of bytes returned in the string is equal to prodStringLen. The programmed data must be in UNICODE UTF-16LE encodings as defined by the Unicode Standard, Worldwide Character Encoding, Version 5.0.

8.22 Additional Feature Configuration Register

Offset = F0h

Figure 8-21. Additional Feature Configuration Register

7	6	5	4	3	2	1	0
RSVD			stsOutputEn	pwronTime			RSVD
R-0			R/RW-0	R/W-0			R/W-0

Table 8-22. Additional Feature Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RSVD	R	0	Reserved Read only, returns 0 when read.
4	RSVD	R/RW	0	Reserved.
3:1	pwronTime	RW	0	Power-on delay time When OTP ROM pwronTime field is all 0, this field sets the delay time from the removal disable of PWRCTL to the enable of PWRCTL when transitioning battery charging modes. For example, when disabling the power on a transition from a custom charging mode to dedicated charging port mode. The nominal timing is defined as follows: TPWRON_EN = (pwronTime + 1) x 200ms (1) This field can be overwritten by EEPROM contents or by an SMBus host.
0	RSVD	RW	0	Reserved

8.23 Device Status and Command Register

Offset = F8h

Figure 8-22. Device Status and Command Register

7	6	5	4	3	2	1	0
RSVD						smbusRst	cfgActive
R-0						W1S-0	W1C-0

Table 8-23. Device Status and Command Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RSVD	R	0	Reserved Read only, returns 0 when read
1	smbusRst	W1S	0	SMBus interface reset This bit loads the registers back to the GRSTz values. This bit is set by writing a 1 and is cleared by hardware on completion of the reset. A write of 0 has no effect.
0	cfgActive	W1C	0	Configuration active This bit indicates that configuration of the TUSB4041I-Q1 device is currently active. The bit is set by hardware when the device enters the I^2C or SMBus mode. The TUSB4041I-Q1 device does not connect on the upstream port while this bit is 1. When in the SMBus mode, this bit must be cleared by the SMBus host to exit the configuration mode and allow the upstream port to connect. The bit is cleared by a writing 1. A write of 0 has no effect.

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Selection and Specification of Crystals for Texas Instruments USB 2.0 Devices* application note
- Texas Instruments, *TPS2561 Dual-Channel Precision Adjustable Current-limited Power Switches* data sheet
- Texas Instruments, *TUSB4041PAP Evaluation Module* user guide

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

PowerPAD™ and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (July 2024) to Revision D (June 2026)	Page
• Updated Global Reset Mode current in *Hub Input Supply Current*	11

Changes from Revision B (January 2016) to Revision C (July 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed all instances of legacy terminology to controller and target where I^2C is mentioned	1
• Added maximum junction temperature to the *Absolute Maximum Ratings* table	9

Changes from Revision A (September 2015) to Revision B (January 2016)	Page
• Changed the configuration of the PWRCTL_POL pin (R17) in the *Clock, Reset, and Miscellaneous* section	22

Changes from Revision * (July 2015) to Revision A (September 2015)	Page
• Changed pin number for USB_DP_DN1 and USB_DP_DN2 in the *Pin Functions* table	4

11 Mechanical, Packaging, and Orderable Information

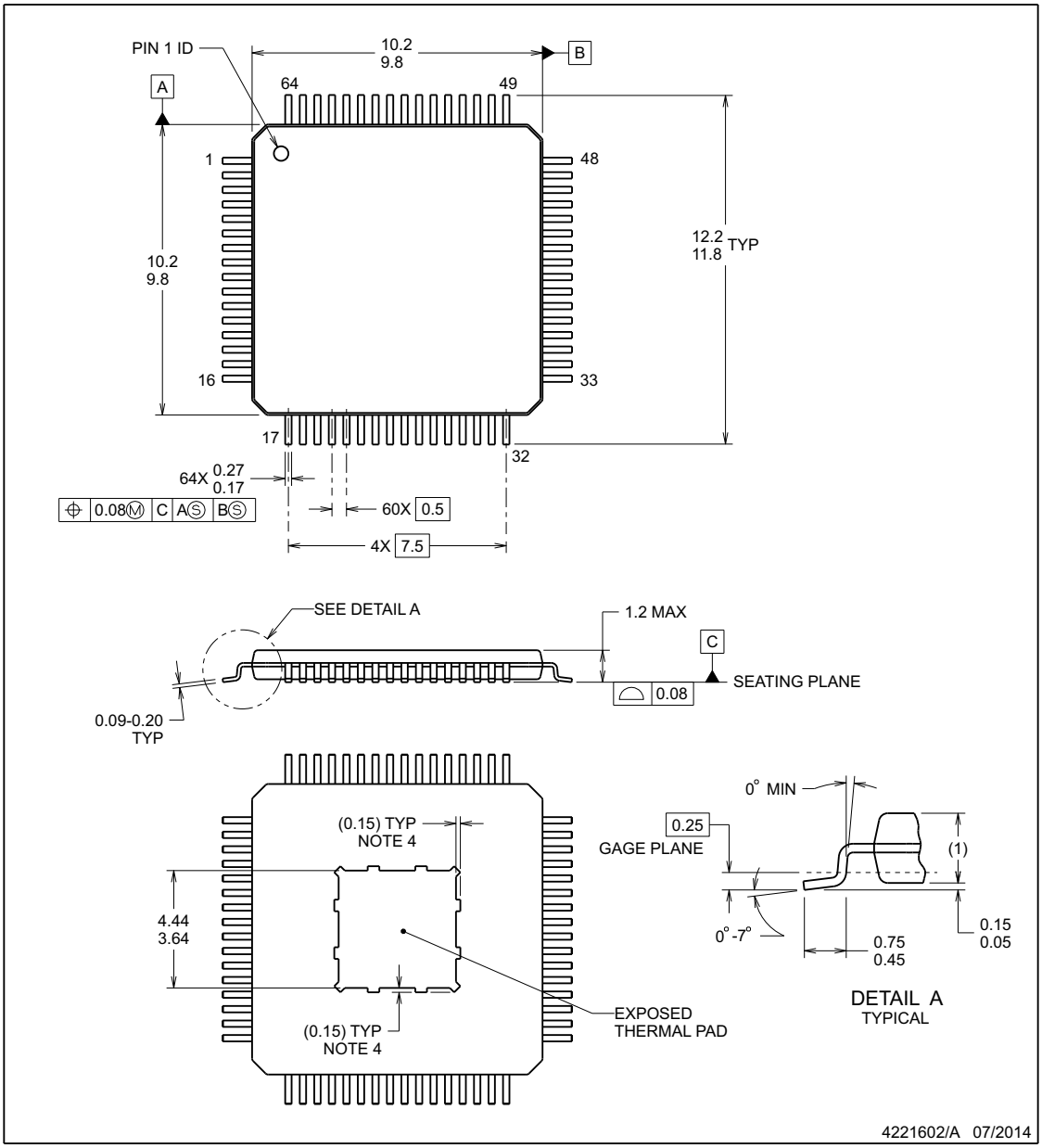
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

PAP0064M

PowerPAD ™ - 1.2 mm max height

PLASTIC QUAD FLAT PACK



PowerPAD is a trademark of Texas Instruments.

NOTES:

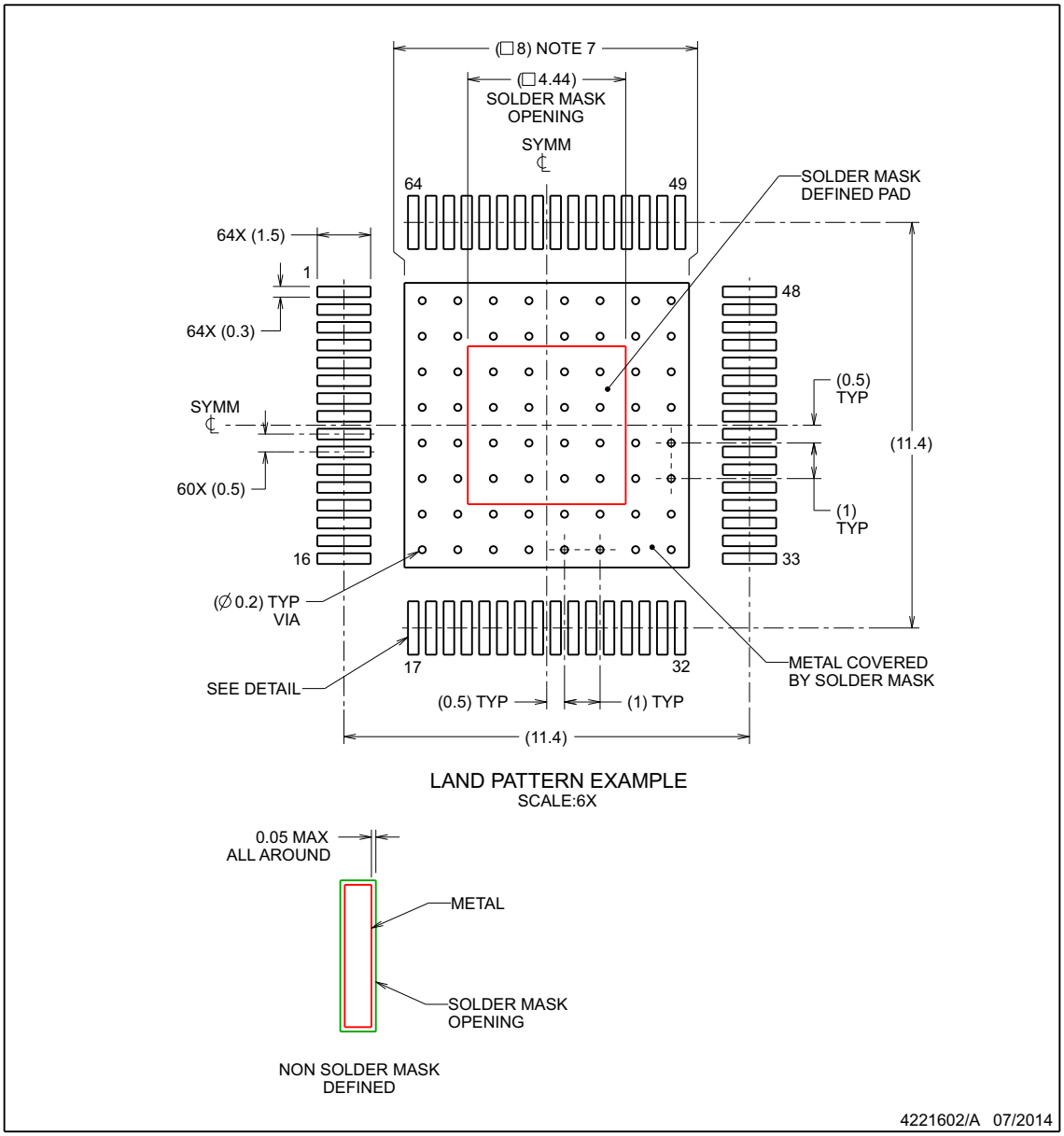
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026, variation ACD.
4. Strap features may not be present,

EXAMPLE BOARD LAYOUT

PAP0064M

PowerPAD ™ - 1.2 mm max height

PLASTIC QUAD FLATPACK



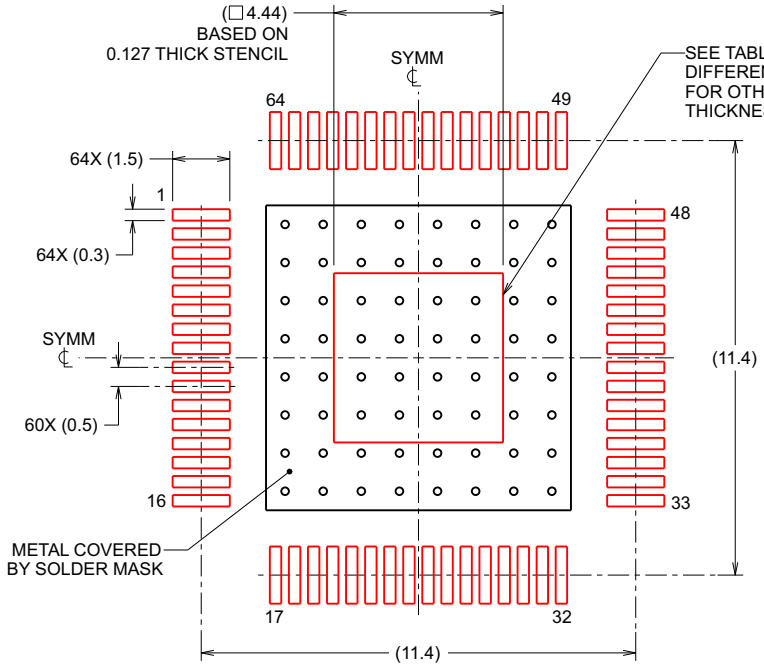
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
8. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

PAP0064M — **PowerPAD™ - 1.2 mm max height**

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	5 X 5
0.127	4.44 X 4.44 (SHOWN)
0.152	4.06 X 4.06
0.178	3.75 X 3.75

4221602/A 07/2014

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TUSB4041IPAPQ1	Active	Production	HTQFP (PAP) | 64	160 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TUSB4041I Q1
TUSB4041IPAPQ1.A	Active	Production	HTQFP (PAP) | 64	160 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TUSB4041I Q1
TUSB4041IPAPRQ1	Active	Production	HTQFP (PAP) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TUSB4041I Q1
TUSB4041IPAPRQ1.A	Active	Production	HTQFP (PAP) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TUSB4041I Q1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TUSB4041I-Q1 :

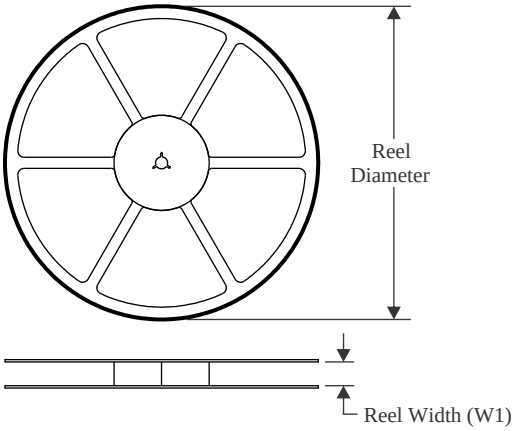
- Catalog : TUSB4041I

NOTE: Qualified Version Definitions:

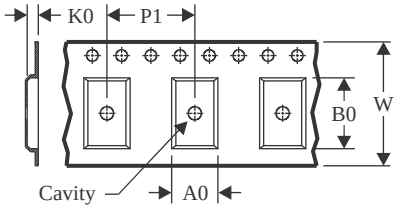
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

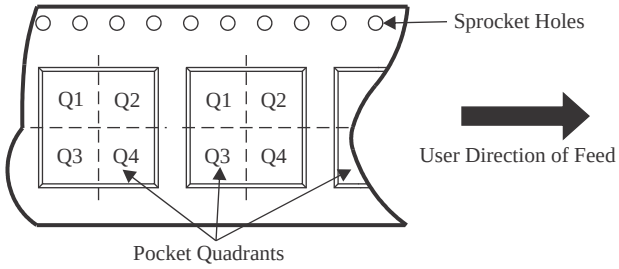


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

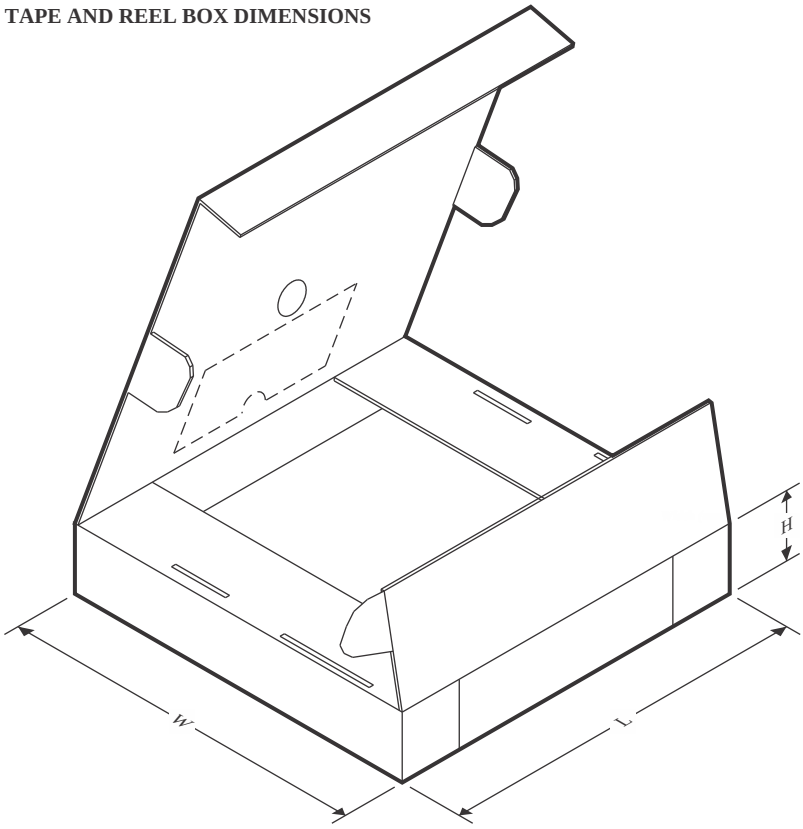
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB4041IPAPRQ1	HTQFP	PAP	64	1000	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2

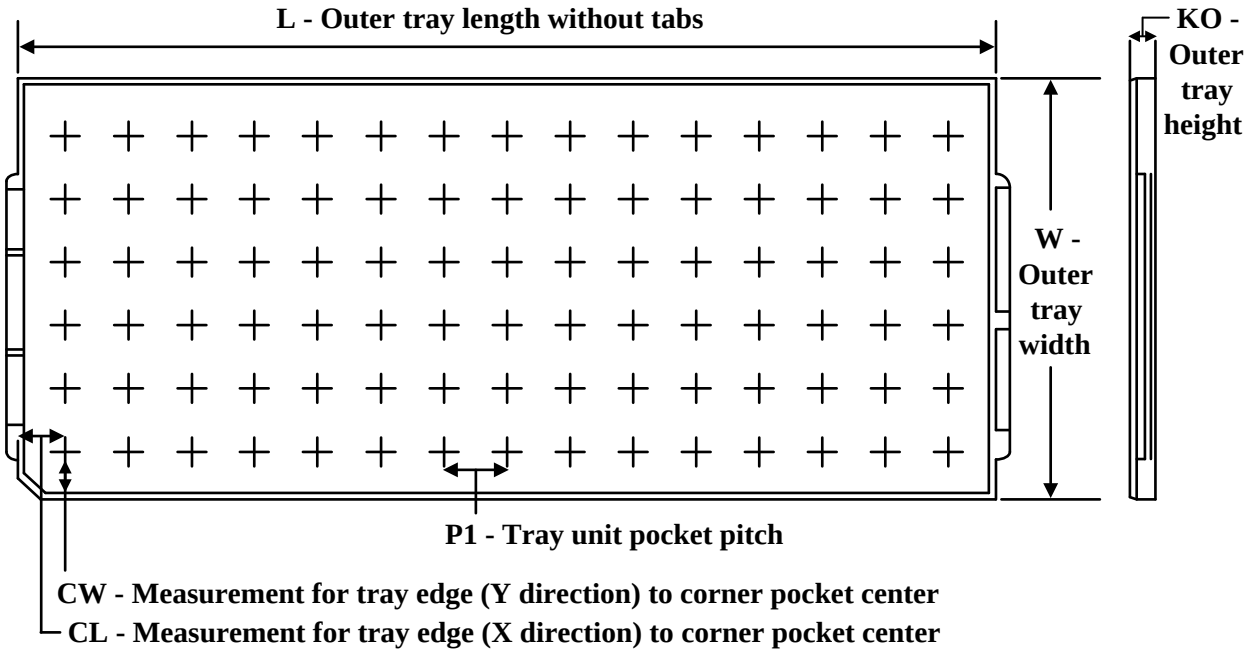
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB4041IPAPRQ1	HTQFP	PAP	64	1000	367.0	367.0	55.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TUSB4041IPAPQ1	PAP	HTQFP	64	160	8 X 20	150	322.6	135.9	7620	15.2	13.1	13
TUSB4041IPAPQ1.A	PAP	HTQFP	64	160	8 X 20	150	322.6	135.9	7620	15.2	13.1	13

GENERIC PACKAGE VIEW

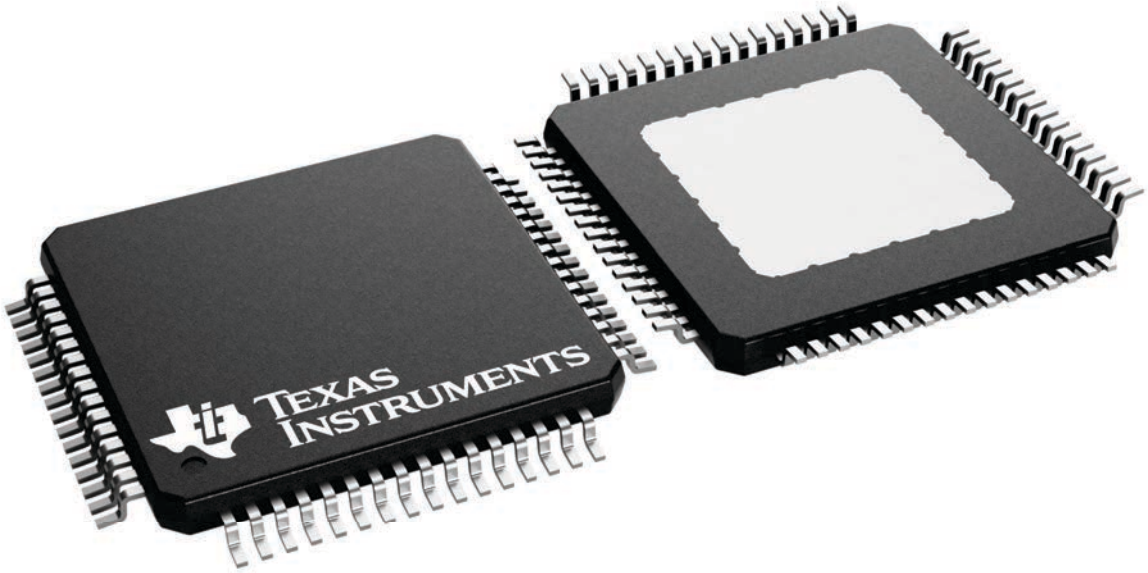
PAP 64

HTQFP - 1.2 mm max height

10 x 10, 0.5 mm pitch

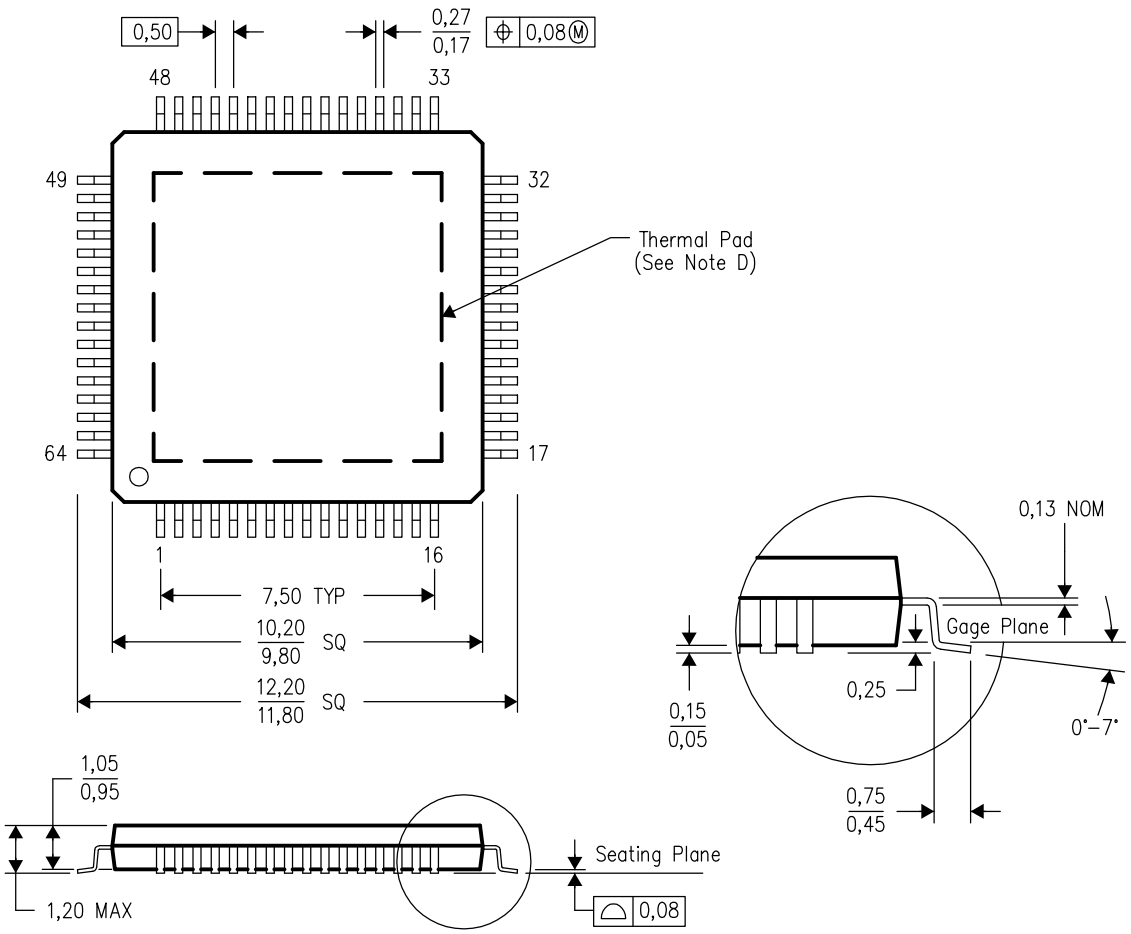
QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4226442/A

PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

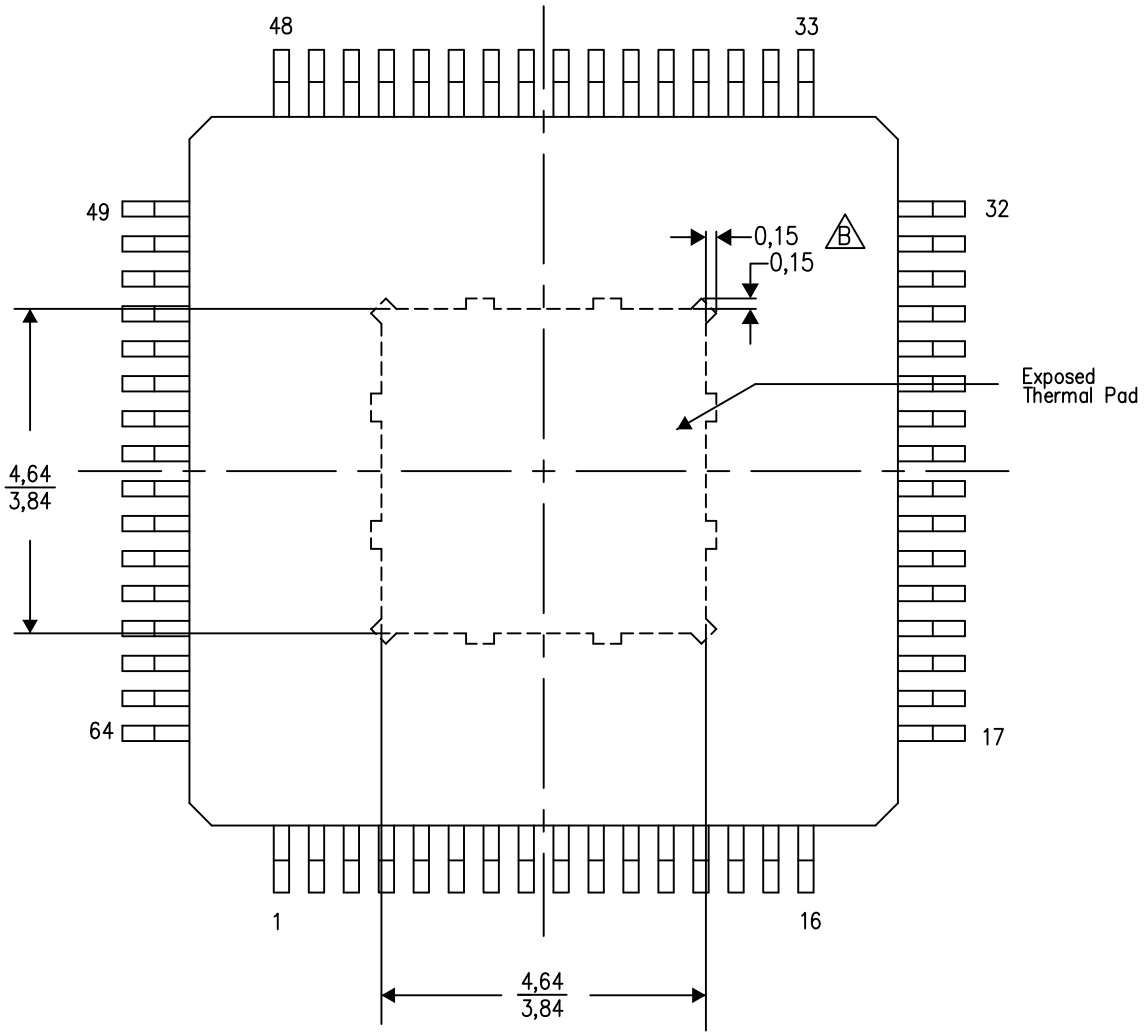
PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206326–14/P 05/14

NOTES: A. All linear dimensions are in millimeters

B. Tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025