

TXU0101 Dual-Bit Fixed Direction Voltage-Level Translator with Schmitt-Trigger Inputs and 3-State Outputs

1 Features

- Fully configurable dual-rail design allows each port to operate from 1.1V to 5.5V
- Up to 200Mbps support for 3.3V to 5.0V
- Schmitt-trigger inputs allows for slow and noisy inputs
- Inputs with integrated static pull-down resistors** prevent channels from floating
- High drive strength (up to 12mA at 5V)
- Low power consumption:
 - 2.5 μ A maximum (25°C)
 - 6 μ A maximum (-40°C to 125°C)
- V_{CC} isolation and V_{CC} disconnect (I_{off} -float) feature**
 - If either V_{CC} input is <100mV or disconnected, all outputs are disabled and become high-impedance
- I_{off} supports partial-power-down mode operation
- Control logic (OE) with $V_{CC(MIN)}$ circuitry** allows for control from either A or B port
- Pinout compatible with TXB family level shifters
- Operating temperature from -40°C to +125°C
- Latch-up performance exceeds 100mA per JESD 78, class II
- ESD protection exceeds JESD 22:
 - 2500-V human-body model
 - 1500-V charged-device model

2 Applications

- Eliminate slow or noisy input signals
- Driving indicator LEDs or buzzers
- Debouncing a mechanical switch
- General purpose I/O level shifting
- Push-pull level shifting (UART, SPI, JTAG, and so forth)

3 Description

TXU0101 is a 1-bit, dual-supply noninverting fixed direction voltage level translation device. A pin is referenced to V_{CCA} logic level, OE pin can be referenced to either V_{CCA} or V_{CCB} logic levels, and B pin is referenced to V_{CCB} logic level. The A port is able to accept input voltages ranging from 1.1V to 5.5V, while the B port can also accept input voltages from 1.1V to 5.5V. Fixed direction data transmission can occur from A to B when OE is set to high in reference to either supply. When OE is set to low, all output pins are in the high-impedance state. See *Device Functional Modes* for a summary of the operation of the control logic.

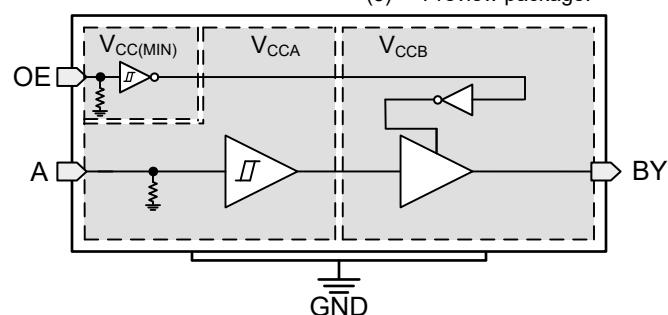
Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
TXU0101	DBV (SOT-23, 6)	2.9mm × 2.8mm
	DCK (SC70, 6)	2mm × 2.1mm
	DRL (SOT-5X3, 6) ⁽³⁾	1.6mm × 1.6mm
	DRY (SON, 6)	1.45mm × 1mm
	DTQ (X2SON, 6)	1mm × 0.8mm

(1) For more information, see [Section 11](#)

(2) The package size (length × width) is a nominal value and includes pins, where applicable.

(3) Preview package.



TXU0101 Functional Block Diagram



An **IMPORTANT NOTICE** at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. UNLESS OTHERWISE NOTED, this document contains **PRODUCTION DATA**.

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4 Pin Configuration and Functions—TXU0101

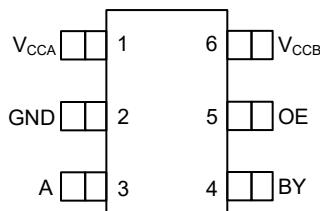


Figure 4-1. DBV Package, 6-Pin SOT-23 Transparent (Top View)

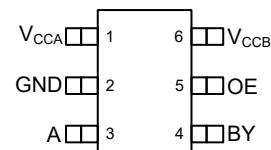


Figure 4-2. DCK Package, 6-Pin SC70 Transparent (Top View)

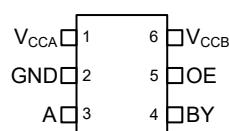


Figure 4-3. DRL Package, 6-Pin SOT-5X3 Transparent (Top View)

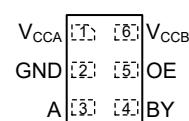


Figure 4-4. DRY Package, 6-Pin SON Transparent (Top View)

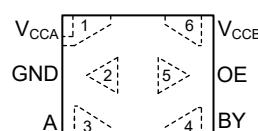


Figure 4-5. DTQ Package, 6-Pin X2SON Transparent (Top View)

Table 4-1. TXU0101 Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
V _{CCA}	1	—	A-port supply voltage. $1.1V \leq V_{CCA} \leq 5.5V$
GND	2	—	Ground
A	3	I	Input A. Referenced to V _{CCA} .
BY	4	O	Output B. Referenced to V _{CCB} .
OE	5	I	Output Enable. Pull to GND to place all outputs in high-impedance mode. Pull to V _{CCA} or V _{CCB} to enable all outputs.
V _{CCB}	6	—	B-port supply voltage. $1.1V \leq V_{CCB} \leq 5.5V$

(1) I = input, O = output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V_{CCA}	Supply voltage A		-0.5	6.5	V
V_{CCB}	Supply voltage B		-0.5	6.5	V
V_I	Input Voltage ⁽²⁾	I/O Ports (A Port)	-0.5	6.5	V
		I/O Ports (B Port)	-0.5	6.5	
		OE	-0.5	6.5	
V_O	Voltage applied to any output in the high-impedance or power-off state ⁽²⁾	A Port	-0.5	6.5	V
		B Port	-0.5	6.5	
V_O	Voltage applied to any output in the high or low state ^{(2) (3)}	A Port	-0.5 $V_{CCA} + 0.5$		V
		B Port	-0.5 $V_{CCB} + 0.5$		
I_{IK}	Input clamp current	$V_I < 0$	-20		mA
I_{OK}	Output clamp current	$V_O < 0$	-20		mA
I_O	Continuous output current		-25	25	mA
	Continuous current through V_{CC} or GND		-100	100	mA
T_j	Junction Temperature			150	°C
T_{stg}	Storage temperature		-65	150	°C

- (1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The output positive-voltage rating may be exceeded up to 6.5V maximum if the output current rating is observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾	±2500	V
		Charged device model (CDM), per AEC Q100-011	±1500	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) ^{(1) (2) (3)}

			MIN	MAX	UNIT
V_{CCA}	Supply voltage A		1.08	5.5	V
V_{CCB}	Supply voltage B		1.08	5.5	V
I_{OH}	High-level output current	$V_{CCO} = 1.1V$		-1.5	mA
		$V_{CCO} = 1.4V$		-3	
		$V_{CCO} = 1.65V$		-4.5	
		$V_{CCO} = 2.3V$		-8	
		$V_{CCO} = 3V$		-10	
		$V_{CCO} = 4.5V$		-12	
I_{OL}	Low-level output current	$V_{CCO} = 1.1V$		1.5	mA
		$V_{CCO} = 1.4V$		3	
		$V_{CCO} = 1.65V$		4.5	
		$V_{CCO} = 2.3V$		8	
		$V_{CCO} = 3V$		10	
		$V_{CCO} = 4.5V$		12	
V_I	Input voltage ⁽³⁾		0	5.5	V
V_O	Output voltage	Active State	0	V_{CCO}	V
		Tri-State	0	5.5	
T_A	Operating free-air temperature		-40	125	°C

(1) V_{CCI} is the V_{CC} associated with the input port.

(2) V_{CCO} is the V_{CC} associated with the output port.

(3) All control inputs and data I/Os of this device have weak pulldowns so that the line is not floating when undefined external to the device. The input leakage from these weak pulldowns is defined by the I_I specification indicated under [Electrical Characteristics](#).

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TXU0101-Q1			UNIT
		DCK (SC70)	DRL (SOT-5X3)	DRY (SON)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	215.9	TBD	279.2	°C/W
$R_{\theta JC(\text{top})}$	Junction-to-case (top) thermal resistance	143.2	TBD	172.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	76.6	TBD	154.6	°C/W
Y_{JT}	Junction-to-top characterization parameter	58.6	TBD	22.1	°C/W
Y_{JB}	Junction-to-board characterization parameter	76.2	TBD	153.8	°C/W
$R_{\theta JC(\text{bottom})}$	Junction-to-case (bottom) thermal resistance	N/A	TBD	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

PARAMETER	TEST CONDITIONS	V _{CCA}	V _{CCB}	Operating free-air temperature (T _A)						UNIT	
				25°C			−40°C to 85°C				
				MIN	TYP	MAX	MIN	TYP	MAX		
V _{T+}	Positive-going input-threshold voltage	Data Inputs (Ax, Bx) (Referenced to V _{CCI})	1.1V	1.1V			0.44	0.88	0.44	0.88	V
			1.4V	1.4V			0.60	0.98	0.60	0.98	
			1.65V	1.65V			0.76	1.13	0.76	1.13	
			2.3V	2.3V			1.08	1.56	1.08	1.56	
			3V	3V			1.48	1.92	1.48	1.92	
			4.5V	4.5V			2.19	2.74	2.19	2.74	
			5.5V	5.5V			2.65	3.33	2.65	3.33	
	OE (Referenced to V _{CCA} or V _{CCB})	OE (Referenced to V _{CCA} or V _{CCB})	1.1V	1.1V			0.44	0.88	0.44	0.88	V
			1.4V	1.4V			0.60	0.98	0.60	0.98	
			1.65V	1.65V			0.76	1.13	0.76	1.13	
			2.3V	2.3V			1.08	1.56	1.08	1.56	
			3V	3V			1.48	1.92	1.48	1.92	
			4.5V	4.5V			2.19	2.74	2.19	2.74	
			5.5V	5.5V			2.65	3.33	2.65	3.33	
V _{T-}	Negative-going input-threshold voltage	Data Inputs (Ax, Bx) (Referenced to V _{CCI})	1.1V	1.1V			0.17	0.48	0.17	0.48	V
			1.4V	1.4V			0.28	0.59	0.28	0.59	
			1.65V	1.65V			0.35	0.69	0.35	0.69	
			2.3V	2.3V			0.56	0.97	0.56	0.97	
			3V	3V			0.89	1.5	0.89	1.5	
			4.5V	4.5V			1.51	1.97	1.51	1.97	
			5.5V	5.5V			1.88	2.4	1.88	2.4	
	OE (Referenced to V _{CCA} or V _{CCB})	OE (Referenced to V _{CCA} or V _{CCB})	1.1V	1.1V			0.17	0.48	0.17	0.48	V
			1.4V	1.4V			0.28	0.59	0.28	0.59	
			1.65V	1.65V			0.35	0.69	0.35	0.69	
			2.3V	2.3V			0.56	0.97	0.56	0.97	
			3V	3V			0.89	1.5	0.89	1.5	
			4.5V	4.5V			1.51	1.97	1.51	1.97	
			5.5V	5.5V			1.88	2.46	1.88	2.46	
ΔV _T	Input-threshold hysteresis (V _{T+} – V _{T-})	Data Inputs (Ax, Bx) (Referenced to V _{CCI})	1.1V	1.1V			0.2	0.4	0.2	0.4	V
			1.4V	1.4V			0.25	0.5	0.25	0.5	
			1.65V	1.65V			0.3	0.55	0.3	0.55	
			2.3V	2.3V			0.38	0.65	0.38	0.65	
			3V	3V			0.46	0.72	0.46	0.72	
			4.5V	4.5V			0.58	0.93	0.58	0.93	
			5.5V	5.5V			0.69	1.06	0.69	1.06	
	OE (Referenced to V _{CCA} or V _{CCB})	OE (Referenced to V _{CCA} or V _{CCB})	1.1V	1.1V			0.15	0.41	0.15	0.41	V
			1.4V	1.4V			0.2	0.5	0.2	0.5	
			1.65V	1.65V			0.23	0.55	0.23	0.55	
			2.3V	2.3V			0.32	0.65	0.32	0.65	
			3V	3V			0.39	0.72	0.39	0.72	
			4.5V	4.5V			0.57	0.97	0.57	0.97	
			5.5V	5.5V			0.69	1.18	0.69	1.18	

5.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

PARAMETER	TEST CONDITIONS	V _{CCA}	V _{CCB}	Operating free-air temperature (T _A)						UNIT	
				25°C			-40°C to 85°C				
				MIN	TYP	MAX	MIN	TYP	MAX		
V _{OH}	High-level output voltage ⁽³⁾	I _{OH} = -0.1mA	1.1V – 5.5V	1.1V – 5.5V			V _{CCO} – 0.1		V _{CCO} – 0.1	V	
		I _{OH} = -0.5mA	1.1V	1.1V			0.82		0.82		
		I _{OH} = -3mA	1.4V	1.4V			1		1		
		I _{OH} = -4.5mA	1.65V	1.65V			1.2		1.2		
		I _{OH} = -8mA	2.3V	2.3V			1.7		1.7		
		I _{OH} = -10mA	3V	3V			2.2		2.2		
		I _{OH} = -12mA	4.5V	4.5V			3.7		3.7		
V _{OL}	Low-level output voltage ⁽⁴⁾	I _{OL} = 0.1mA	1.1V – 5.5V	1.1V – 5.5V				0.1	0.1	V	
		I _{OL} = 0.5mA	1.1V	1.1V				0.27	0.27		
		I _{OL} = 3mA	1.4V	1.4V				0.35	0.35		
		I _{OL} = 4.5mA	1.65V	1.65V				0.45	0.45		
		I _{OL} = 8mA	2.3V	2.3V				0.7	0.7		
		I _{OL} = 10mA	3V	3V				0.8	0.8		
		I _{OL} = 8mA	4.5V	4.5V				0.55	0.55		
		I _{OL} = 12mA	4.5V	4.5V				0.8	0.8		
I _I	Input leakage current	OE V _I = V _{CC} or GND	1.1V – 5.5V	1.1V – 5.5V	-0.1	1.5	-0.1	1.5	-0.1	2	µA
		Data Inputs (Ax, Bx) V _I = V _{CCI} or GND	1.1V – 5.5V	1.1V – 5.5V	-0.1	1.5	-0.1	1.5	-2	2	µA
I _{off}	Partial power down current	A Port or B Port V _I or V _O = 0V – 5.5V	0V	1.1V – 5.5V	-1.5	1.5	-2	2	-2.5	2.5	µA
			1.1V – 5.5V	0V	-1.5	1.5	-2	2	-2.5	2.5	
I _{off-float}	Floating supply Partial power down current	A Port or B Port V _I or V _O = GND	Floating ⁽⁵⁾	1.1V – 5.5V	-1.5	1.5	-2	2	-2.5	2.5	µA
			0V – 5.5V	Floating ⁽⁵⁾	-1.5	1.5	-2	2	-2.5	2.5	
I _{OZ}	Tri-state output current	A or B Port: V _I = V _{CCI} or GND V _O = V _{CCO} or GND OE = GND	1.1V – 5.5V	1.1V – 5.5V	-0.3	0.3	-1	1	-2	2	µA
I _{CCA}	V _{CCA} supply current	V _I = V _{CCI} or GND I _O = 0	1.1V – 5.5V	1.1V – 5.5V			1.5		2.5	6	µA
			0V	5.5V	-0.3		-1		-1		
		V _I = GND I _O = 0	5.5V	0V			1		1.5	3	
I _{CCB}	V _{CCB} supply current	V _I = V _{CCI} or GND I _O = 0	5.5V	Floating ⁽⁵⁾			1.5		7	15	µA
			1.1V – 5.5V	1.1V – 5.5V			1.5		2.5	6	
			0V	5.5V			1		1.5	3	
			5.5V	0V	-0.3		-1		-1		
I _{CCA} + I _{CCB}	Combined supply current	V _I = V _{CCI} or GND I _O = 0	Floating ⁽⁵⁾	5.5V			1.5		7	15	µA
			1.1V – 5.5V	1.1V – 5.5V			2.5		3	6	µA
C _i	Control Input Capacitance	V _I = 3.3V or GND	3.3V	3.3V			2.75		3	3.5	pF

5.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

PARAMETER	TEST CONDITIONS	V _{CCA}	V _{CCB}	Operating free-air temperature (T _A)						UNIT	
				25°C			-40°C to 85°C				
				MIN	TYP	MAX	MIN	TYP	MAX		
C _{io}	Data I/O Capacitance	OE = GND, V _O = 1.65V DC +1MHz -16 dBm sine wave	3.3V	3.3V	3		4		4	pF	

- (1) V_{CCI} is the V_{CC} associated with the input port.
- (2) V_{CCO} is the V_{CC} associated with the output port.
- (3) Tested at V_I = V_{T+(MAX)}.
- (4) Tested at V_I = V_{T-(MIN)}.
- (5) Floating is defined as a node that is both not actively driven by an external device and has leakage not exceeding 10 nA.

5.6 Switching Characteristics, $V_{CCA} = 1.2 \pm 0.1V$

See [Figure 6-1](#) and [Table 6-1](#) for test circuit and loading. See [Figure 6-2](#), [Figure 6-3](#), and [Figure 6-4](#) for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})												UNIT			
					1.2 \pm 0.1V			1.5 \pm 0.1V			1.8 \pm 0.15V			2.5 \pm 0.2V			3.3 \pm 0.3V			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	3.3	96	0.5	43	0.5	37	0.5	32	0.5	30	0.5	31	ns			
				-40°C to 125°C	5.7	60	3.0	39	1.4	33	0.5	28	0.5	27	0.5	26				
		B	A	-40°C to 85°C	3.3	95	1.9	80	0.5	75	0.5	70	0.5	69	0.5	69				
				-40°C to 125°C	5.7	60	4.1	51	2.9	48	1.8	45	1.5	44	1.3	44				
t_{dis}	Disable time	OE	A	-40°C to 85°C	28.8	133	28.5	130	28.4	133	28.8	137	28.4	143	18.7	211	ns			
				-40°C to 125°C	43.3	133	43.3	130	43.7	130	44.7	131	45.4	134	31.8	140				
		OE	B	-40°C to 85°C	32.5	150	27.6	117	25.8	110	22.5	104	22.1	112	20.1	181				
				-40°C to 125°C	48.3	149	43.2	120	40.8	113	36.8	104	36.5	107	33.8	111				
t_{en}	Enable time	OE	A	-40°C to 85°C	24.1	237	22.1	229	21.4	230	21.3	232	21.7	235	22.7	244	ns			
				-40°C to 125°C	34.9	156	33.3	167	32.0	169	31.7	173	32.0	177	34.2	187				
		OE	B	-40°C to 85°C	21.3	237	14.3	152	11.2	140	8.8	130	8.2	130	8.4	132				
				-40°C to 125°C	29.8	143	23.0	116	18.6	107	15.4	97	14.5	97	14.8	103				

5.7 Switching Characteristics, $V_{CCA} = 1.5 \pm 0.1V$

See [Figure 6-1](#) and [Table 6-1](#) for test circuit and loading. See [Figure 6-2](#), [Figure 6-3](#), and [Figure 6-4](#) for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})												UNIT	
					1.2 \pm 0.1V			1.5 \pm 0.1V			1.8 \pm 0.15V			2.5 \pm 0.2V				
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{pd}	Propagation delay	A	B	-40°C to 85°C	1.9	80	0.5	31	0.5	25	0.5	19	0.5	17	0.5	15	ns	
				-40°C to 125°C	4.1	51	1.6	31	0.5	25	0.5	20	0.5	18	0.5	16		
		B	A	-40°C to 85°C	0.5	43	0.5	31	0.5	28	0.5	26	0.5	25	0.5	24		
				-40°C to 125°C	3.0	39	1.6	31	0.5	28	0.5	26	0.5	25	0.5	24		
t_{dis}	Disable time	OE	A	-40°C to 85°C	20.0	91	19.0	82	18.8	81	19.2	82	19.6	83	12.2	87	ns	
				-40°C to 125°C	34.9	95	32.6	86	32.8	85	33.4	87	34.2	88	24.6	92		
		OE	B	-40°C to 85°C	27.4	127	21.7	91	19.9	82	16.3	71	15.9	71	13.7	70		
				-40°C to 125°C	44.4	130	36.7	95	34.7	86	30.2	75	29.8	75	26.6	74		
t_{en}	Enable time	OE	A	-40°C to 85°C	14.9	102	14.4	86	13.5	88	12.7	90	12.6	92	13.2	97	ns	
				-40°C to 125°C	25.5	102	25.2	89	24.1	91	22.8	93	22.8	96	23.5	100		
		OE	B	-40°C to 85°C	17.9	175	12.7	80	9.1	69	6.1	57	4.9	53	4.5	54		
				-40°C to 125°C	26.6	135	21.0	81	16.8	71	12.5	60	10.8	56	10.4	57		

5.8 Switching Characteristics, $V_{CCA} = 1.8 \pm 0.15V$

See [Figure 6-1](#) and [Table 6-1](#) for test circuit and loading. See [Figure 6-2](#), [Figure 6-3](#), and [Figure 6-4](#) for measurement waveforms.

PARAMETER	FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})												UNIT			
				1.2 \pm 0.1V			1.5 \pm 0.1V			1.8 \pm 0.15V			2.5 \pm 0.2V			3.3 \pm 0.3V			
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C		0.5	75	0.5	28	0.5	22	0.5	17	0.5	14	0.5	12	ns	
				-40°C to 125°C		2.9	48	0.5	28	0.5	23	0.5	17	0.5	15	0.5	13		
		B	A	-40°C to 85°C		0.5	37	0.5	25	0.5	22	0.5	19	0.5	19	0.5	18		
				-40°C to 125°C		1.4	33	0.5	25	0.5	23	0.5	20	0.5	19	0.5	19		
t_{dis}	Disable time	OE	A	-40°C to 85°C		17.2	79	14.7	67	14.5	65	14.3	65	14.4	66	8.5	68	ns	
				-40°C to 125°C		30.9	83	28.0	71	26.6	69	27.5	70	27.2	71	20.0	73		
		OE	B	-40°C to 85°C		25.4	121	18.7	81	16.5	71	12.8	60	12.5	58	9.8	55		
				-40°C to 125°C		41.7	123	34.0	86	30.3	76	26.2	64	25.3	62	21.8	59		
t_{en}	Enable time	OE	A	-40°C to 85°C		10.9	88	9.5	66	9.4	63	8.6	65	8.2	66	8.1	69	ns	
				-40°C to 125°C		20.3	87	19.0	69	18.9	67	17.6	68	17.1	70	17.1	73		
		OE	B	-40°C to 85°C		16.7	177	10.4	75	8.1	58	4.9	46	3.3	42	2.2	39		
				-40°C to 125°C		25.1	135	18.7	77	15.5	60	11.0	49	8.7	44	7.3	42		

5.9 Switching Characteristics, $V_{CCA} = 2.5 \pm 0.2V$

See [Figure 6-1](#) and [Table 6-1](#) for test circuit and loading. See [Figure 6-2](#), [Figure 6-3](#), and [Figure 6-4](#) for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})												UNIT
					1.2 \pm 0.1V			1.5 \pm 0.1V			1.8 \pm 0.15V			2.5 \pm 0.2V			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN
t_{pd}	Propagation delay	A	B	-40°C to 85°C	0.5	70	0.5	26	0.5	20	0.5	14	0.5	12	0.5	9	ns
				-40°C to 125°C	1.8	45	0.5	26	0.5	20	0.5	14	0.5	12	0.5	10	
		B	A	-40°C to 85°C	0.5	32	0.5	19	0.5	17	0.5	14	0.5	13	0.5	13	
				-40°C to 125°C	0.5	28	0.5	20	0.5	17	0.5	14	0.5	13	0.5	13	
t_{dis}	Disable time	OE	A	-40°C to 85°C	12.9	65	10.5	51	9.0	51	8.1	43	8.4	44	5.0	45	ns
				-40°C to 125°C	24.9	68	21.8	55	19.7	50	18.2	47	18.6	48	15.0	49	
		OE	B	-40°C to 85°C	23.2	112	16.5	74	14.0	61	9.0	46	9.1	44	6.4	39	
				-40°C to 125°C	38.7	115	30.9	79	27.1	66	21.6	51	20.5	48	16.8	43	
t_{en}	Enable time	OE	A	-40°C to 85°C	7.9	80	5.9	50	5.1	44	4.7	39	4.4	40	3.7	41	ns
				-40°C to 125°C	15.6	74	13.5	53	12.4	47	12.0	42	11.5	43	10.8	44	
		OE	B	-40°C to 85°C	16.3	183	9.2	74	6.0	54	4.0	36	2.1	31	0.5	27	
				-40°C to 125°C	24.4	139	17.2	76	13.0	57	9.8	38	7.1	33	4.7	29	

5.10 Switching Characteristics, $V_{CCA} = 3.3 \pm 0.3V$

See [Figure 6-1](#) and [Table 6-1](#) for test circuit and loading. See [Figure 6-2](#), [Figure 6-3](#), and [Figure 6-4](#) for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})												UNIT			
					1.2 \pm 0.1V			1.5 \pm 0.1V			1.8 \pm 0.15V			2.5 \pm 0.2V			3.3 \pm 0.3V			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	0.5	69	0.5	25	0.5	19	0.5	13	0.5	11	0.5	8	ns			
				-40°C to 125°C	1.5	44	0.5	25	0.5	19	0.5	13	0.5	11	0.5	9				
		B	A	-40°C to 85°C	0.5	30	0.5	17	0.5	14	0.5	12	0.5	11	0.5	10				
				-40°C to 125°C	0.5	27	0.5	18	0.5	15	0.5	12	0.5	11	0.5	10				
t_{dis}	Disable time	OE	A	-40°C to 85°C	12.9	62	10.1	47	8.7	42	6.9	39	6.6	39	6.9	40	ns			
				-40°C to 125°C	24.0	65	20.6	51	18.4	46	15.7	40	15.3	39	15.9	40				
		OE	B	-40°C to 85°C	22.7	109	15.7	71	13.2	59	8.5	42	7.6	38	4.7	34				
				-40°C to 125°C	37.6	111	29.5	75	25.4	63	19.2	46	18.5	42	14.2	36				
t_{en}	Enable time	OE	A	-40°C to 85°C	6.6	85	4.2	45	3.0	37	2.4	31	2.2	30	1.7	30	ns			
				-40°C to 125°C	13.6	72	10.9	47	9.3	40	8.2	33	8.1	32	7.5	33				
		OE	B	-40°C to 85°C	16.3	192	8.9	76	5.4	55	2.6	34	1.8	27	0.5	22				
				-40°C to 125°C	24.3	144	16.7	78	12.2	57	8.0	36	6.6	29	3.7	24				

5.11 Switching Characteristics, $V_{CCA} = 5.0 \pm 0.5V$

See [Figure 6-1](#) and [Table 6-1](#) for test circuit and loading. See [Figure 6-2](#), [Figure 6-3](#), and [Figure 6-4](#) for measurement waveforms.

PARAMETER	FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})												UNIT			
				1.2 \pm 0.1V			1.5 \pm 0.1V			1.8 \pm 0.15V			2.5 \pm 0.2V			3.3 \pm 0.3V			
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	0.5	69	0.5	24	0.5	18	0.5	13	0.5	10	0.5	8	ns		
				-40°C to 125°C	1.3	44	0.5	24	0.5	19	0.5	13	0.5	11	0.5	8			
		B	A	-40°C to 85°C	0.5	31	0.5	15	0.5	12	0.5	9	0.5	8	0.5	8			
				-40°C to 125°C	0.5	26	0.5	16	0.5	13	0.5	10	0.5	9	0.5	8			
t_{dis}	Disable time	OE	A	-40°C to 85°C	10.8	60	7.7	42	5.9	36	4.2	31	3.4	30	2.8	26	ns		
				-40°C to 125°C	20.8	62	17.0	46	14.5	40	11.8	33	10.4	31	9.6	29			
		OE	B	-40°C to 85°C	9.7	109	5.9	69	13.2	56	8.4	40	6.9	36	3.7	30			
				-40°C to 125°C	37.4	111	29.2	73	24.6	60	18.1	43	16.4	39	12.2	33			
t_{en}	Enable time	OE	A	-40°C to 85°C	6.0	102	2.8	44	1.2	33	0.5	25	0.5	22	0.5	21	ns		
				-40°C to 125°C	12.4	81	8.8	46	6.5	36	4.7	27	4.2	24	4.4	23			
		OE	B	-40°C to 85°C	16.7	212	8.8	82	4.8	58	1.6	35	0.5	26	0.5	19			
				-40°C to 125°C	24.8	158	16.7	83	11.7	60	6.9	37	4.7	28	3.5	21			

5.12 Operating Characteristics

$T_A = 25^\circ\text{C}$ ⁽¹⁾

PARAMETER	Test Conditions	Supply Voltage ($V_{CCB} = V_{CCA}$)						UNIT
		$1.2 \pm 0.1\text{V}$	$1.5 \pm 0.1\text{V}$	$1.8 \pm 0.15\text{V}$	$2.5 \pm 0.2\text{V}$	$3.3 \pm 0.3\text{V}$	$5.0 \pm 0.5\text{V}$	
		TYP	TYP	TYP	TYP	TYP	TYP	
C_{pdA} ⁽²⁾	A to B: outputs enabled	A Port CL = 0, RL = Open $f = 10\text{MHz}$ $t_{rise} = t_{fall} = 1\text{ ns}$	2	2	2	2	2	3
	A to B: outputs disabled		2	2	2	2	2	3
	B to A: outputs enabled		12	12	12	13	13	16
	B to A: outputs disabled		2	2	2	2	2	3
C_{pdB} ⁽³⁾	A to B: outputs enabled	B Port CL = 0, RL = Open $f = 10\text{MHz}$ $t_{rise} = t_{fall} = 1\text{ ns}$	12	12	12	13	13	16
	A to B: outputs disabled		2	2	2	2	2	3
	B to A: outputs enabled		2	2	2	2	2	3
	B to A: outputs disabled		2	2	2	2	2	3

(1) See the [CMOS Power Consumption and \$C_{pd}\$ Calculation](#) application report for additional information about how power dissipation capacitance affects power consumption.

(2) A-Port power dissipation capacitance per transceiver.

(3) B-Port power dissipation capacitance per transceiver.

5.13 Typical Characteristics

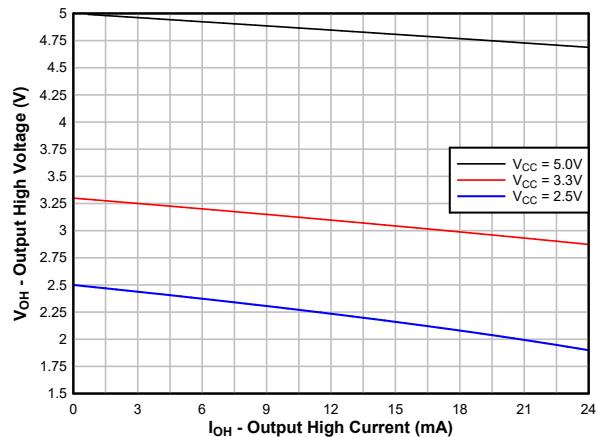


Figure 5-1. Typical ($T_A=25^\circ\text{C}$) Output High Voltage (V_{OH}) vs Source Current (I_{OH})

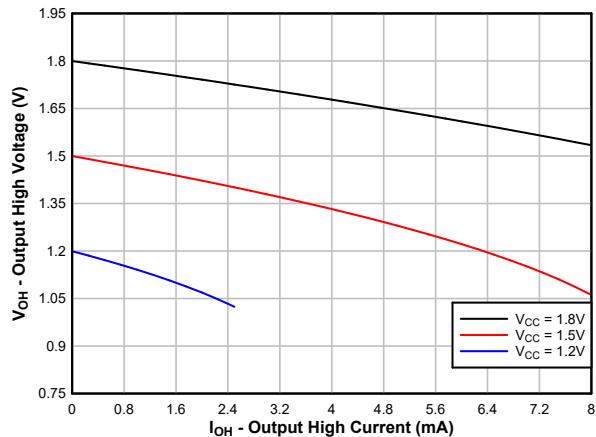


Figure 5-2. Typical ($T_A=25^\circ\text{C}$) Output High Voltage (V_{OH}) vs Source Current (I_{OH})

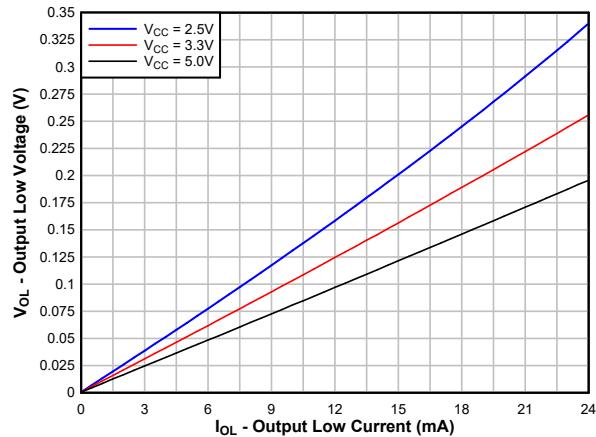


Figure 5-3. Typical ($T_A=25^\circ\text{C}$) Output Low Voltage (V_{OL}) vs Sink Current (I_{OL})

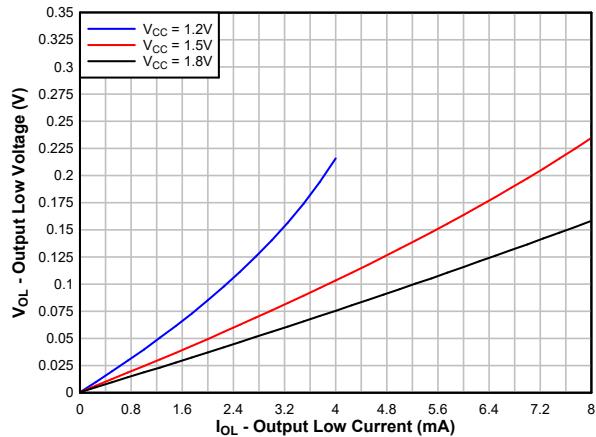


Figure 5-4. Typical ($T_A=25^\circ\text{C}$) Output Low Voltage (V_{OL}) vs Sink Current (I_{OL})

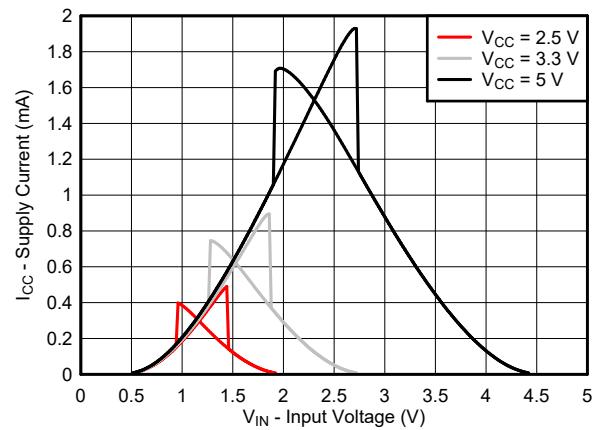


Figure 5-5. Typical ($T_A=25^\circ\text{C}$) Supply Current (I_{CC}) vs Input Voltage (V_{IN})

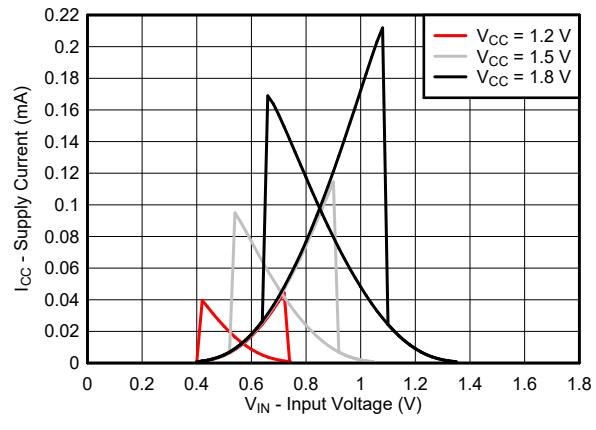


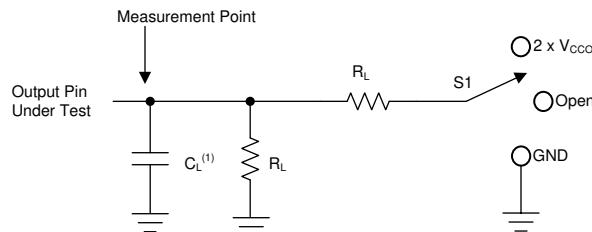
Figure 5-6. Typical ($T_A=25^\circ\text{C}$) Supply Current (I_{CC}) vs Input Voltage (V_{IN})

6 Parameter Measurement Information

6.1 Load Circuit and Voltage Waveforms

Unless otherwise noted, generators supply all input pulses that have the following characteristics:

- $f = 1\text{MHz}$
- $Z_O = 50\Omega$
- $\Delta t/\Delta V \leq 1\text{ns/V}$

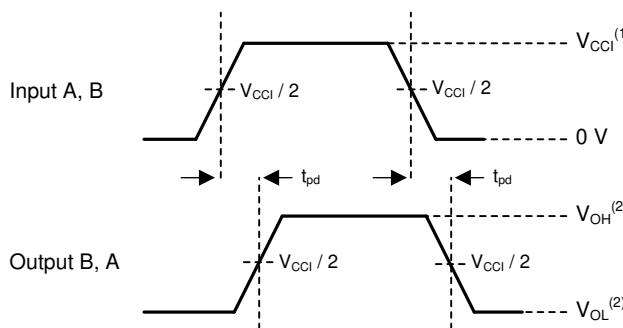


A. C_L includes probe and jig capacitance.

Figure 6-1. Load Circuit

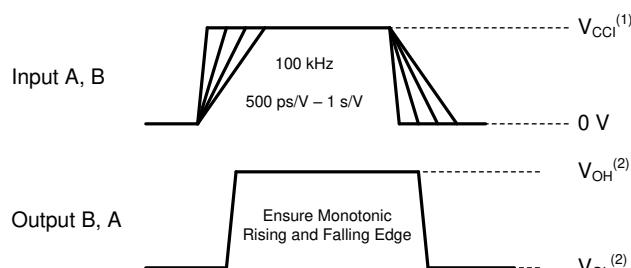
Table 6-1. Load Circuit Conditions

Parameter	V_{CCO}	R_L	C_L	S_1	V_{TP}
t_{pd} Propagation (delay) time	1.1V – 5.5V	10k Ω	5pF	Open	N/A
t_{en}, t_{dis} Enable time, disable time	1.1V – 1.6V	10k Ω	5pF	2 $\times V_{CCO}$	0.1V
	1.65V – 2.7V	10k Ω	5pF	2 $\times V_{CCO}$	0.15V
	3.0V – 5.5V	10k Ω	5pF	2 $\times V_{CCO}$	0.3V
t_{en}, t_{dis} Enable time, disable time	1.1V – 1.6V	10k Ω	5pF	GND	0.1V
	1.65V – 2.7V	10k Ω	5pF	GND	0.15V
	3.0V – 5.5V	10k Ω	5pF	GND	0.3V



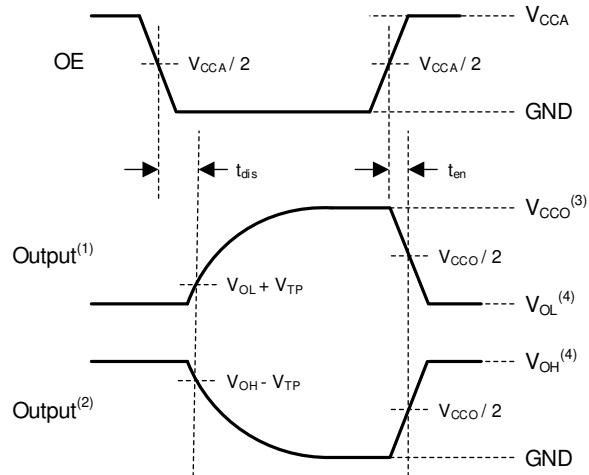
1. V_{CC1} is the supply pin associated with the input port.
2. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L , C_L , and S_1

Figure 6-2. Propagation Delay



1. V_{CC1} is the supply pin associated with the input port.
2. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L , C_L , and S_1

Figure 6-3. Input Transition Rise and Fall Rate



1. Output waveform on the condition that input is driven to a valid Logic Low.
2. Output waveform on the condition that input is driven to a valid Logic High.
3. V_{CCO} is the supply pin associated with the output port.
4. V_{OH} and V_{OL} are typical output voltage levels with specified R_L , C_L , and S_1 .

Figure 6-4. Enable Time And Disable Time

7 Detailed Description

7.1 Overview

The TXU0101 is a 4-bit translating transceiver that uses two individually configurable power-supply rails. The device is operational with V_{CCA} and V_{CCB} supplies as low as 1.1V and as high as 5.5V. Additionally, the device can be operated with $V_{CCA} = V_{CCB}$. The A port is designed to track V_{CCA} , and the B port is designed to track V_{CCB} .

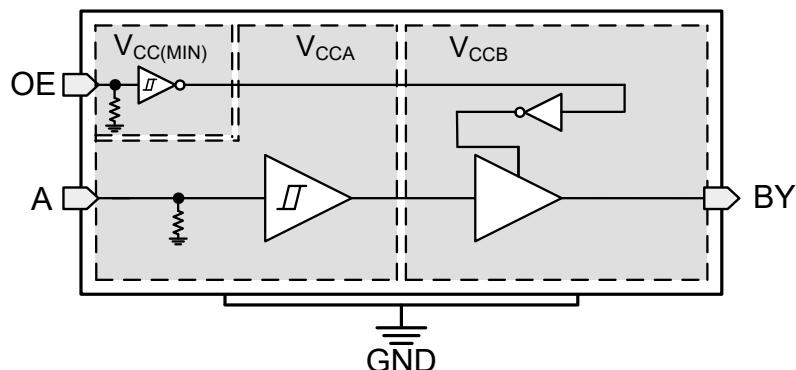
The TXU0101 device is designed for asynchronous communication between data buses, and transmits data with fixed direction from the A bus to the B bus. The output-enable input (OE) is used to disable the outputs so the buses are effectively isolated. The output-enable pin of the TXU0101 (OE) can be referenced to either V_{CCA} or V_{CCB} . The OE pin can be left floating or externally pulled down to ground so that the high-impedance state of the level shifter outputs during power up or power down.

This device is fully specified for partial-power-down applications using the I_{off} current. The I_{off} protection circuitry is designed so that no excessive current is drawn from or sourced into an input or output while the device is powered down.

The V_{CC} isolation or V_{CC} disconnect feature is designed so that if either V_{CC} is less than 100mV or disconnected with the complementary supply within the recommended operating conditions, then the outputs are disabled and set to the high-impedance state while the supply current is maintained. The $I_{off\text{-float}}$ circuitry is designed so that no excessive current is drawn from or sourced into an input or output while the supply is floating.

Glitch-free power supply sequencing allows either supply rail to be powered on or off in any order while providing robust power sequencing performance.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 CMOS Schmitt-Trigger Inputs with Integrated Pulldowns

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the [Electrical Characteristics](#). The worst case resistance is calculated with the maximum input voltage, given in the [Absolute Maximum Ratings](#), and the maximum input leakage current, given in the [Electrical Characteristics](#), using ohm's law ($R = V \div I$).

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the [Electrical Characteristics](#), which makes this device extremely tolerant to slow or noisy inputs. Driving the inputs slowly will increase dynamic current consumption of the device. See [Understanding Schmitt Triggers](#) for additional information regarding Schmitt-trigger inputs.

7.3.1.1 Inputs with Integrated Static Pull-Down Resistors

This device has 5 MΩ typical integrated weak pull-downs for each input. This feature allows all inputs to be left floating without the concern for unstable outputs or increased current consumption. This also helps to reduce external component count for applications where not all channels are used or need to be fixed low. If an external pull-up is required, it should be no larger than 1 MΩ to avoid contention with the 5 MΩ internal pull-down.

7.3.2 Control Logic (OE) with $V_{CC(MIN)}$ Circuitry

The output-enable input (OE) is used to disable the outputs so the buses are effectively isolated. The output-enable pin of the TXU0x04 has $V_{CC(MIN)}$ circuitry, which allows the OE pin to operate with the lower supply voltage. The [Over-Voltage Tolerant Inputs](#) feature allows the OE pin to operate with the higher supply voltage. This combination means that the enable pin can be referenced to either V_{CCA} or V_{CCB} supply. Multiple permutations of each device are possible since the controller can be placed on either the A or B port and can still control the enable pin.

7.3.3 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. [Absolute Maximum Ratings](#) defines the electrical and thermal limits that must be followed at all times.

7.3.4 VCC Isolation and V_{CC} Disconnect

The outputs for this device are disabled and enter a high-impedance state when either supply is <100mV or left floating (disconnected), with the complementary supply within recommended operating conditions. It is recommended that the inputs are kept low before floating (disconnecting) either supply.

The $I_{CCx(floating)}$ in the [Electrical Characteristics](#) specifies the maximum supply current. The $I_{off(float)}$ in the [Electrical Characteristics](#) specifies the maximum leakage into or out of any input or output pin on the device.

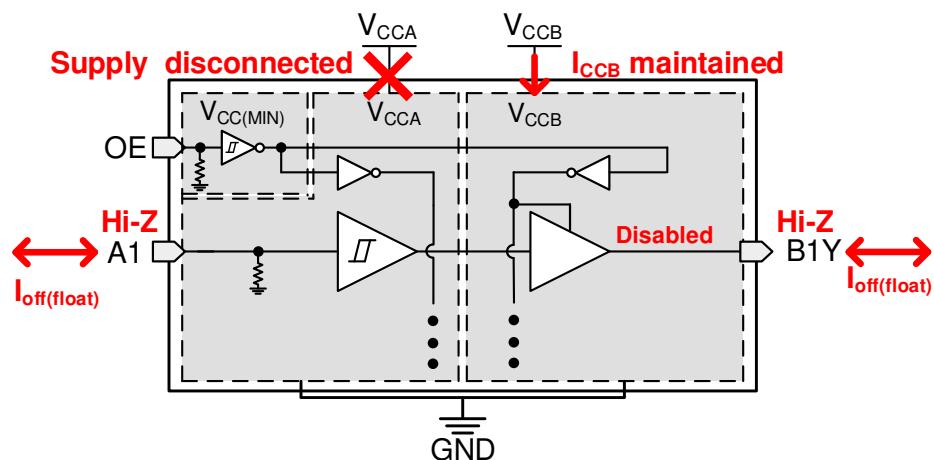


Figure 7-1. V_{CC} Disconnect Feature

7.3.5 Over-Voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the [Recommended Operating Conditions](#).

7.3.6 Glitch-Free Power Supply Sequencing

Either supply rail may be powered on or off in any order without producing a glitch on the inputs or outputs (that is, where the output erroneously transitions to VCC when it should be held low or vice versa). Glitches of this nature can be misinterpreted by a peripheral as a valid data bit, which could trigger a false device reset of the peripheral, a false device configuration of the peripheral, or even a false data initialization by the peripheral.

7.3.7 Negative Clamping Diodes

Figure 7-2 shows the inputs and outputs to this device that have negative clamping diodes.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

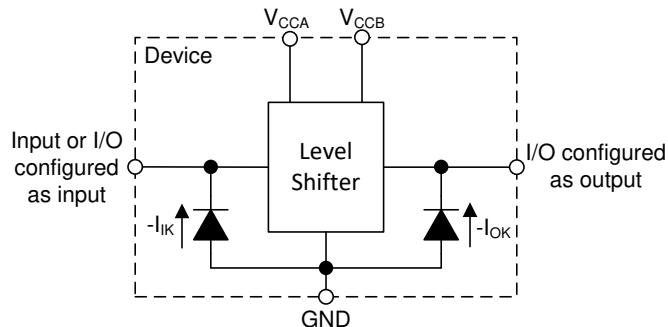


Figure 7-2. Electrical Placement of Clamping Diodes for Each Input and Output

7.3.8 Fully Configurable Dual-Rail Design

The V_{CCA} and V_{CCB} pins can be supplied at any voltage from 1.1V to 5.5V, making the device suitable for translating between any of the voltage nodes (1.2V, 1.5V, 1.8V, 3.3V, and 5.0V).

7.3.9 Supports High-Speed Translation

The TXU0101 device can support high data-rate applications. The translated signal data rate can be up to 200Mbps when the signal is translated from 3.3V to 5.0V.

7.4 Device Functional Modes

Table 7-1. Function Table

CONTROL INPUTS		Port Status		OPERATION
OE		Input	Output	
H		L	L	Unidirectional non-inverting voltage translation
H		H	H	Unidirectional non-inverting voltage translation
L		X	Hi-Z	Isolation

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TXU0101 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The TXU0101 device is ideal for use in applications where a push-pull driver is connected to the data Inputs. The maximum data rate can be up to 200Mbps when device translates a signal from 3.3V to 5.0V.

8.2 Typical Application

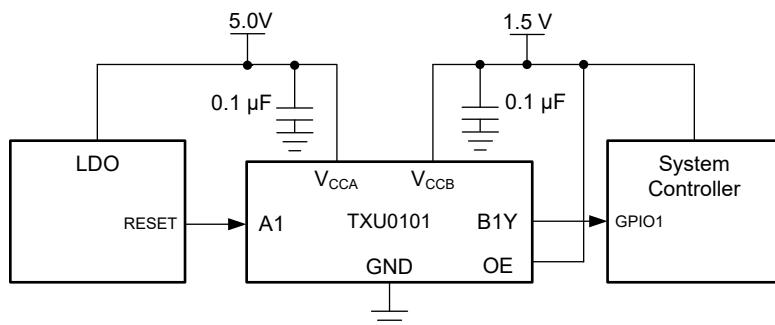


Figure 8-1. TXU0101 LDO Reset Application

8.2.1 Design Requirements

Use the parameters listed in [Table 8-1](#) for this design example.

Table 8-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input voltage range	1.1V to 5.5V
Output voltage range	1.1V to 5.5V

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
 - Use the supply voltage of the device that is driving the TXU0101 device to determine the input voltage range. For a valid logic-high, the value must exceed the positive-going input-threshold voltage (V_{T+}) of the input port. For a valid logic low the value must be less than the negative-going input-threshold voltage (V_{T-}) of the input port.
- Output voltage range
 - Use the supply voltage of the device that the TXU0101 device is driving to determine the output voltage range.

8.2.3 Application Curve

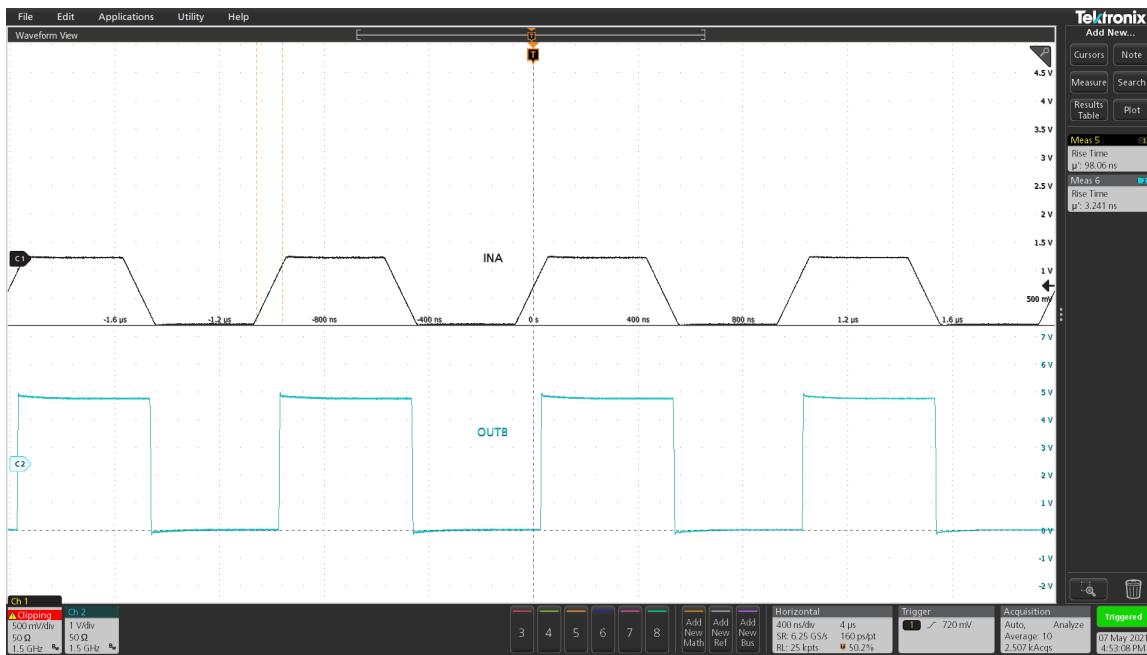


Figure 8-2. Up Translation at 1MHz (1.2V to 5V)

8.3 Power Supply Recommendations

Always apply a ground reference to the GND pins first. This device is designed for glitch free power sequencing without any supply sequencing requirements such as ramp order or ramp rate.

Glitch-Free Power Supply Sequencing describes how this device was designed with various power supply sequencing methods in mind to help prevent unintended triggering of downstream devices.

8.4 Layout

8.4.1 Layout Guidelines

For device reliability, it is recommended to follow common printed-circuit board layout guidelines such as follows:

- Use bypass capacitors on the power supply pins and place them as close to the device as possible. A $0.1\mu\text{F}$ capacitor is recommended, but transient performance can be improved by having $1\mu\text{F}$ and $0.1\mu\text{F}$ capacitors in parallel as bypass capacitors.
- The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing.

8.4.2 Layout Example

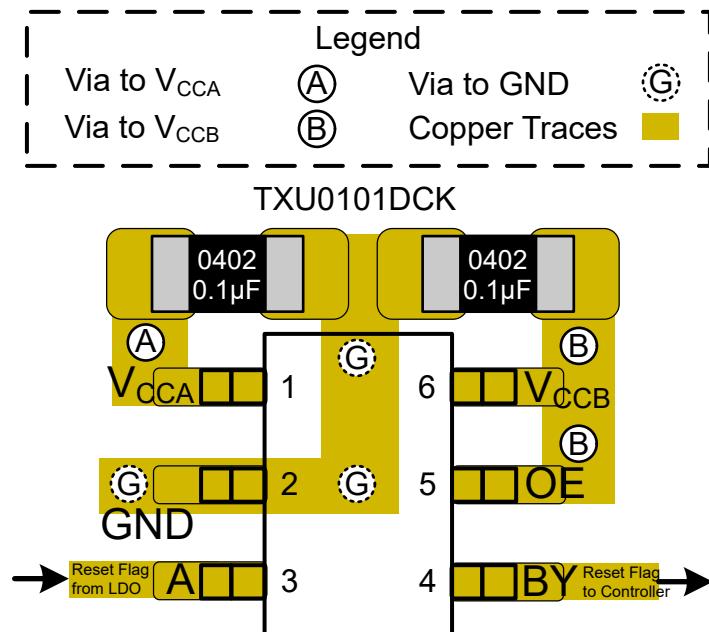


Figure 8-3. Layout Example – TXU0101

9 Device and Documentation Support

9.1 Device Support

9.1.1 Regulatory Requirements

No statutory or regulatory requirements apply to this device.

There are no special characteristics for this product.

9.2 Documentation Support

9.2.1 Related Documentation

- Texas Instruments, [Understanding Schmitt Triggers](#) application report
- Texas Instruments, [CMOS Power Consumption and \$C_{pd}\$ Calculation](#) application report

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

9.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (February 2022) to Revision A (May 2024)	Page
• Updated the low power consumption specification in the <i>Features</i> section.....	1
• Updated the device design features in the <i>Overview</i> section.....	19
• Updated the layout example figure in the <i>Layout Example</i> section.....	25

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TXU0101DBVR	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2T9H
TXU0101DBVR.A	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2T9H
TXU0101DCKR	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1LQ
TXU0101DCKR.A	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1LQ
TXU0101DRYR	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MO
TXU0101DRYR.A	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MO
TXU0101DTQR	Active	Production	X2SON (DTQ) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MN
TXU0101DTQR.A	Active	Production	X2SON (DTQ) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MN

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

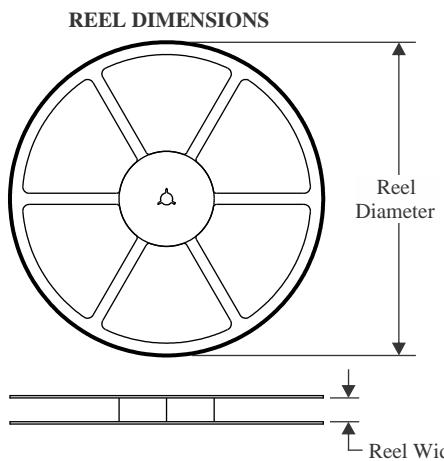
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TXU0101 :

- Automotive : [TXU0101-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

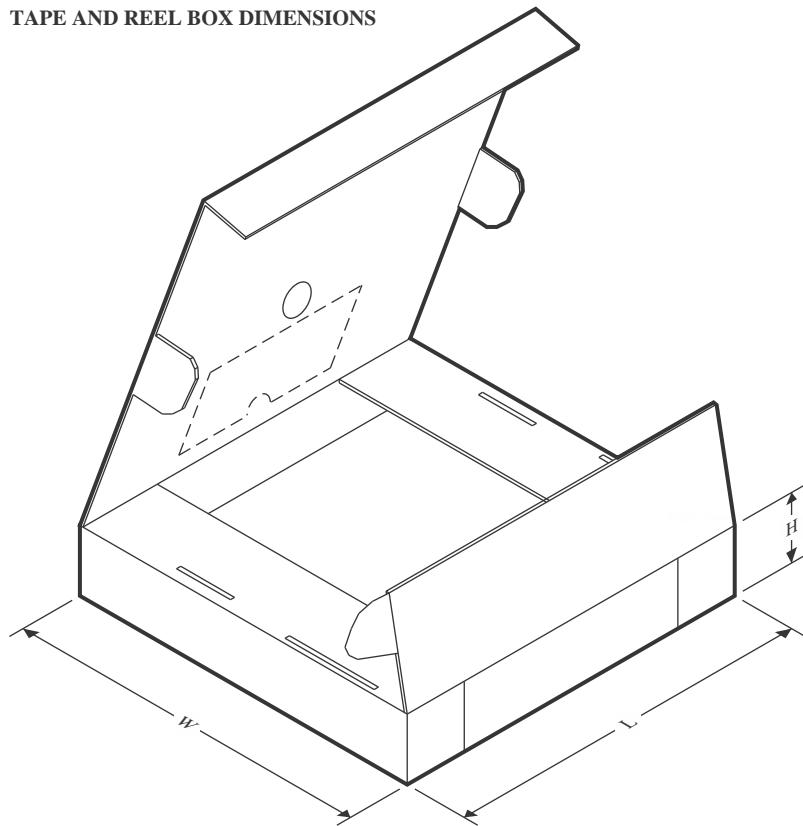
TAPE AND REEL INFORMATION


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXU0101DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TXU0101DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TXU0101DCKR	SC70	DCK	6	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
TXU0101DCKR	SC70	DCK	6	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
TXU0101DRYR	SON	DRY	6	5000	180.0	9.5	1.2	1.65	0.7	4.0	8.0	Q1
TXU0101DTQR	X2SON	DTQ	6	3000	180.0	9.5	0.94	1.13	0.5	2.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXU0101DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TXU0101DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TXU0101DCKR	SC70	DCK	6	3000	210.0	185.0	35.0
TXU0101DCKR	SC70	DCK	6	3000	208.0	191.0	35.0
TXU0101DRYR	SON	DRY	6	5000	189.0	185.0	36.0
TXU0101DTQR	X2SON	DTQ	6	3000	189.0	185.0	36.0

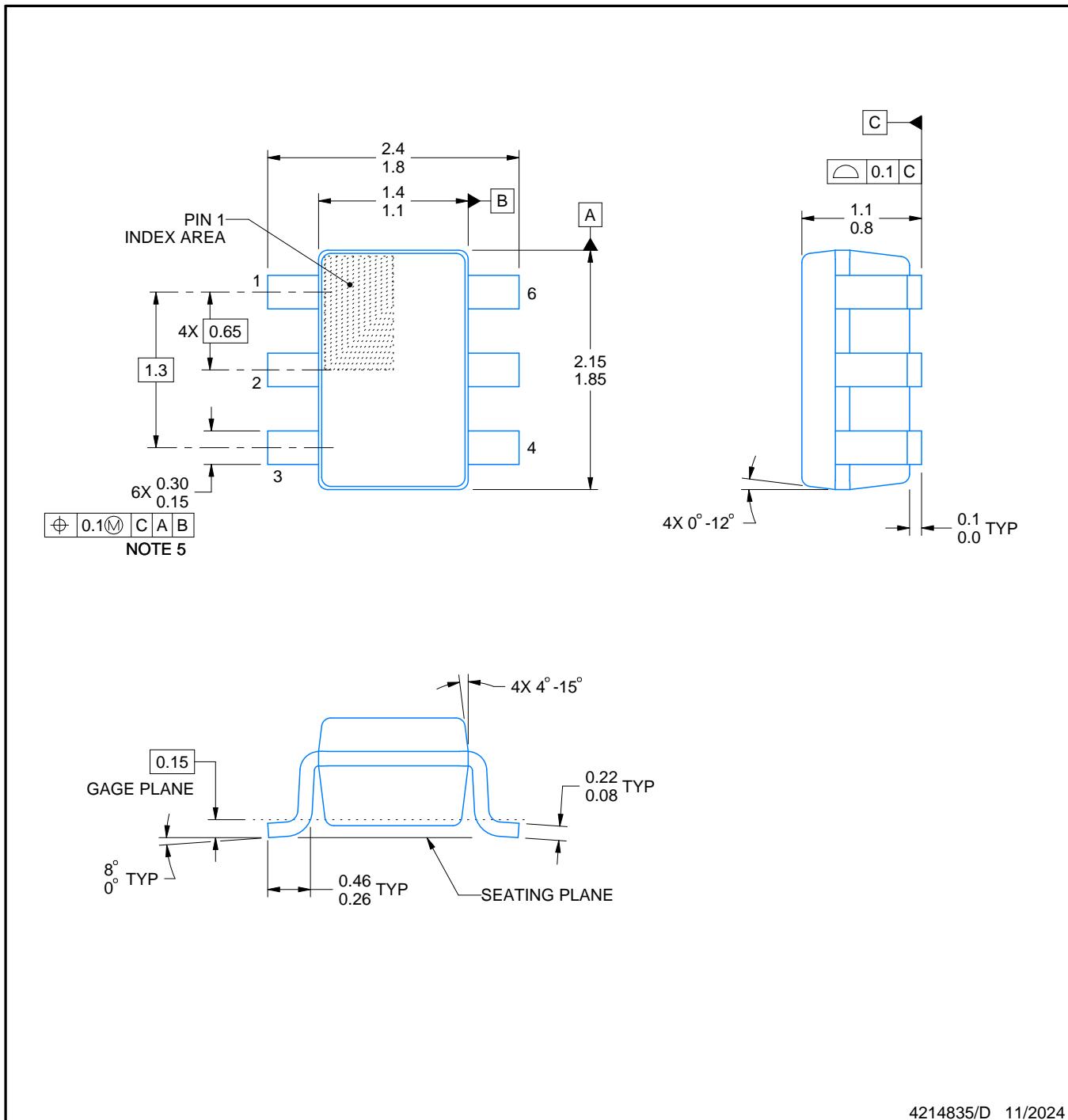
PACKAGE OUTLINE

DCK0006A



SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214835/D 11/2024

NOTES:

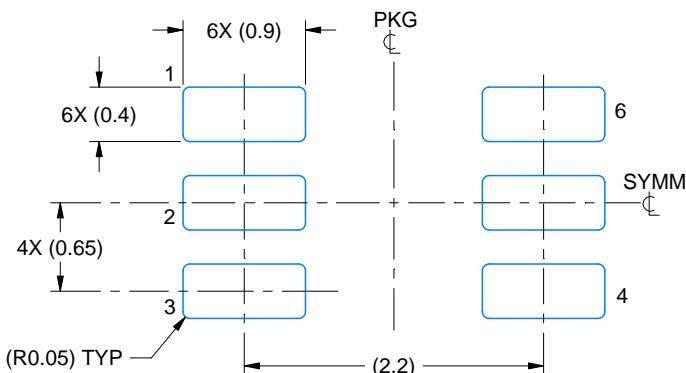
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.

EXAMPLE BOARD LAYOUT

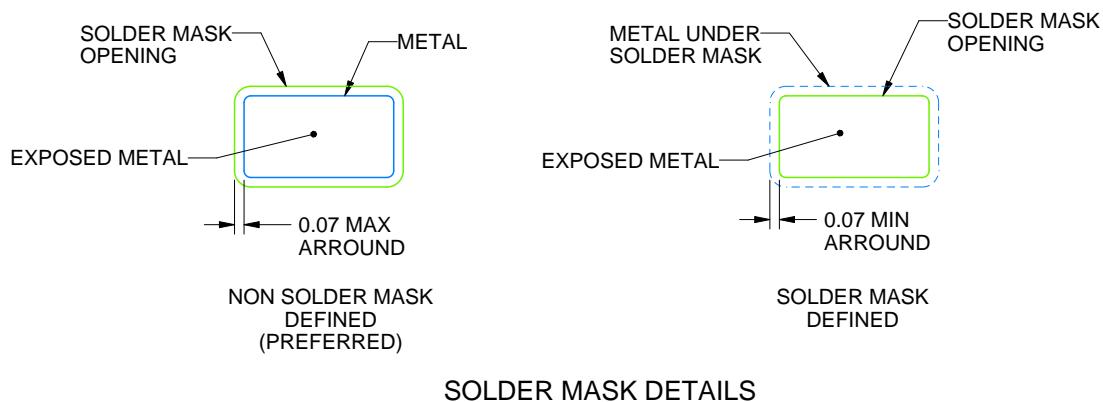
DCK0006A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



4214835/D 11/2024

NOTES: (continued)

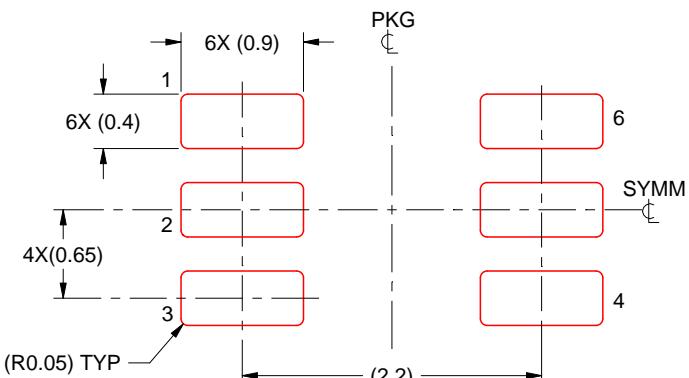
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0006A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DRY 6

GENERIC PACKAGE VIEW

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

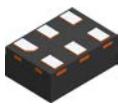


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4207181/G

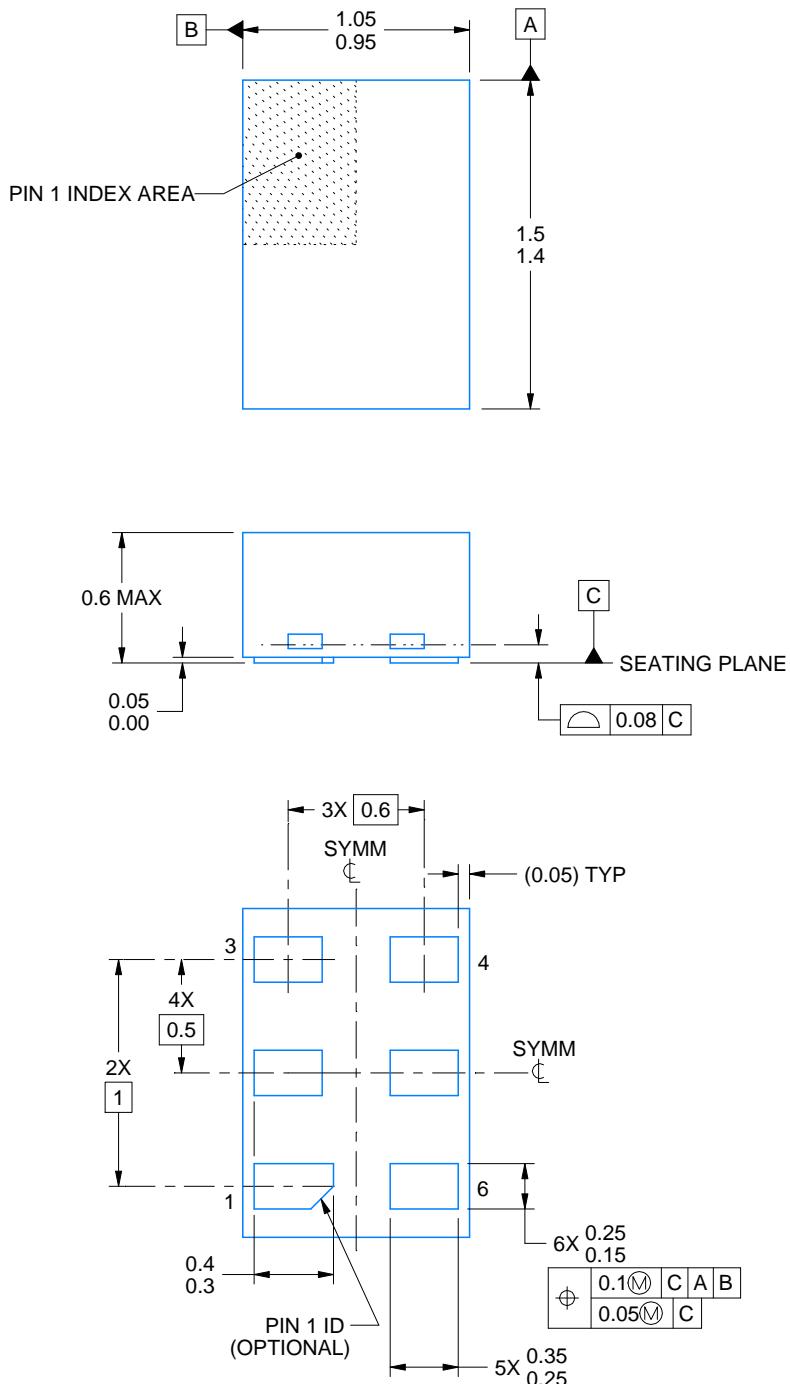
PACKAGE OUTLINE

DRY0006A



USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4222894/A 01/2018

NOTES:

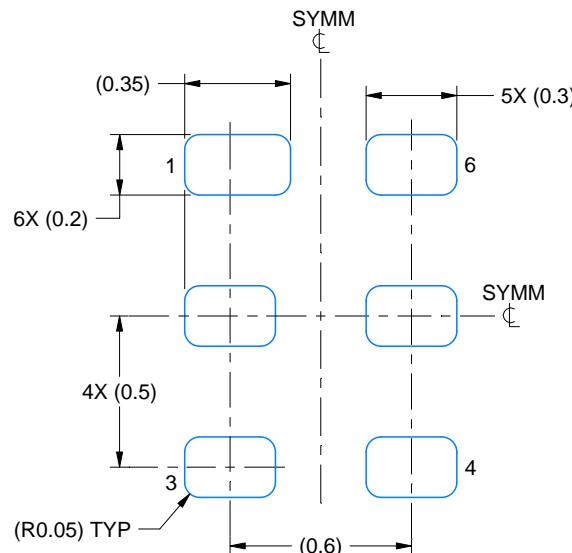
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

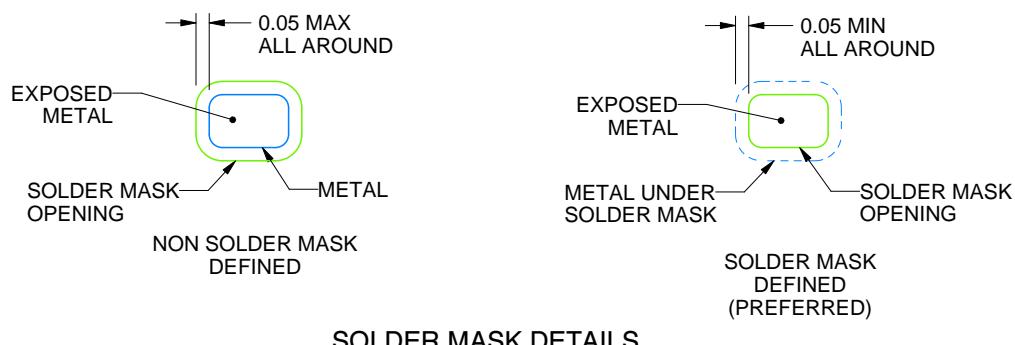
DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

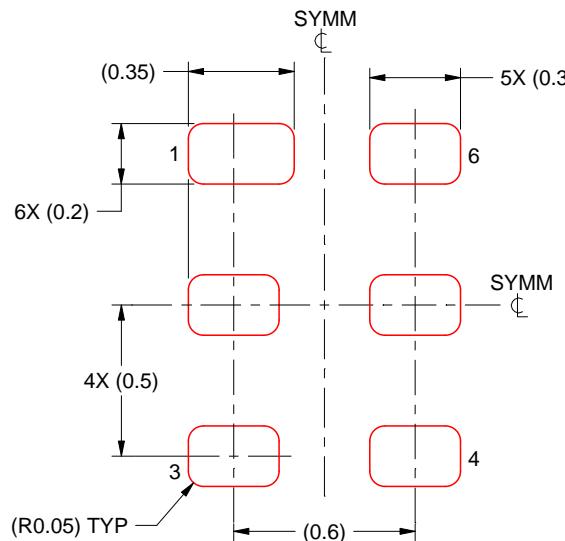
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

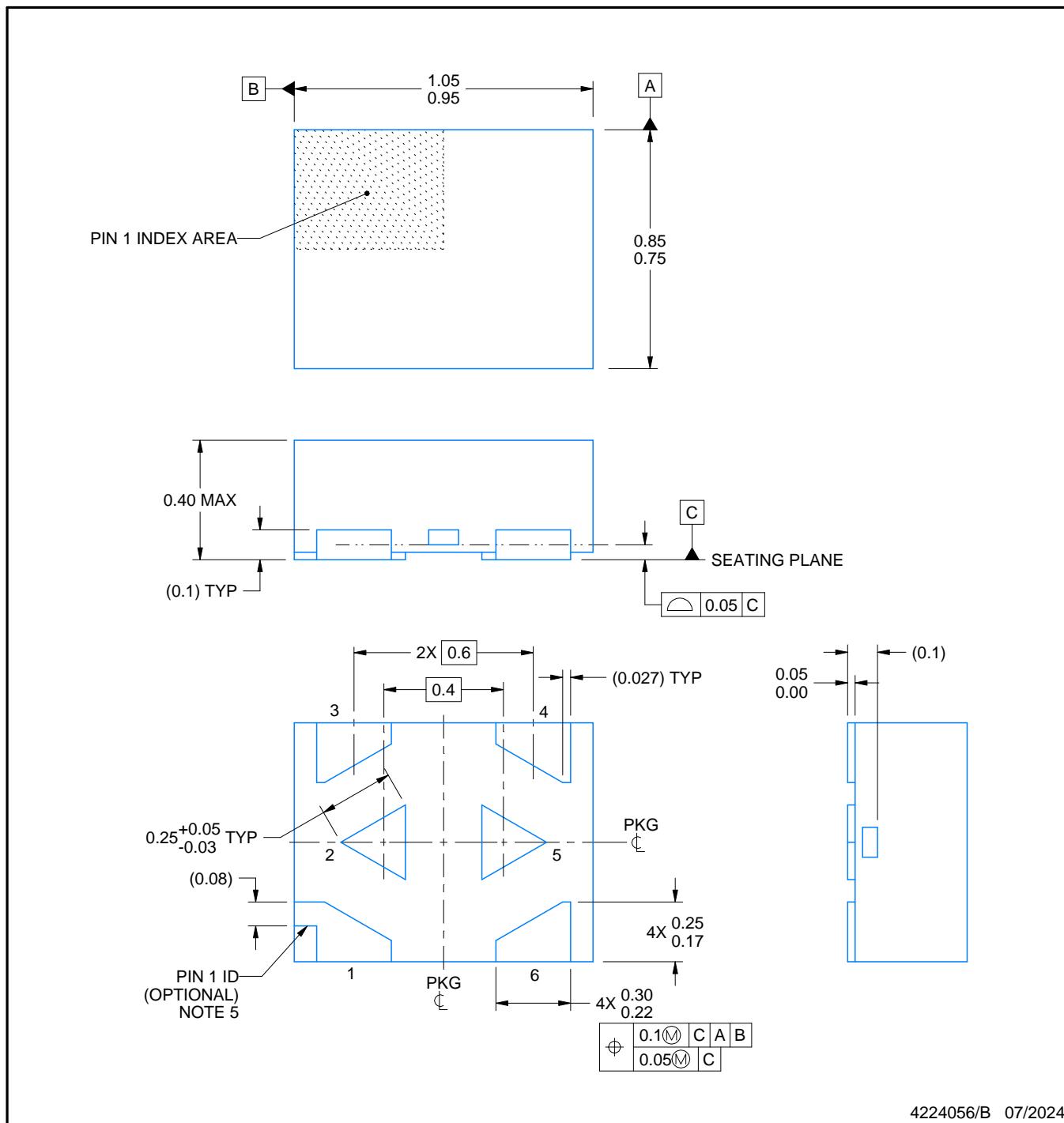
PACKAGE OUTLINE

DTQ0006A



X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4224056/B 07/2024

NOTES:

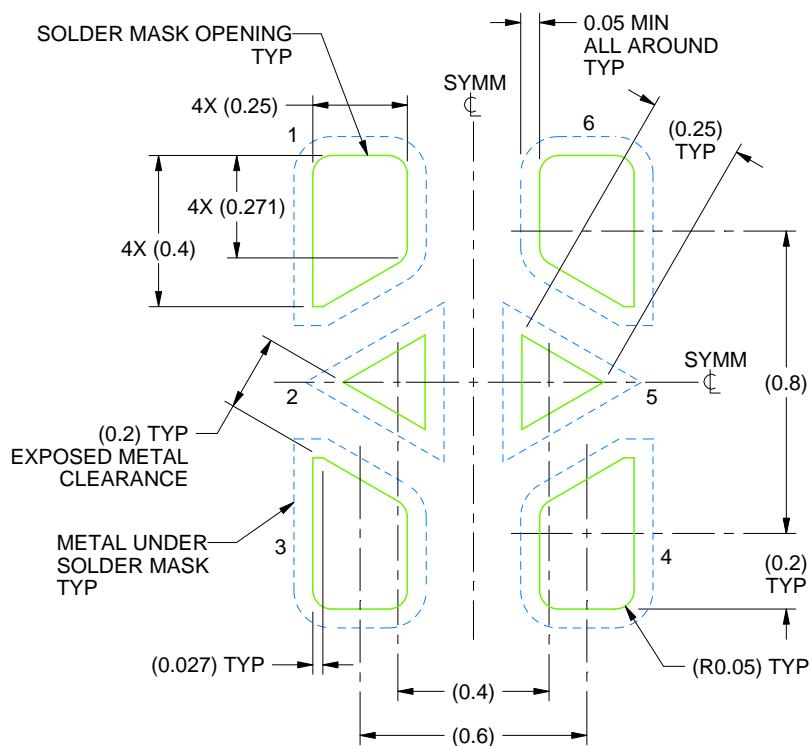
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. The size and shape of this feature may vary.
5. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.

EXAMPLE BOARD LAYOUT

DTQ0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:50X

4224056/B 07/2024

NOTES: (continued)

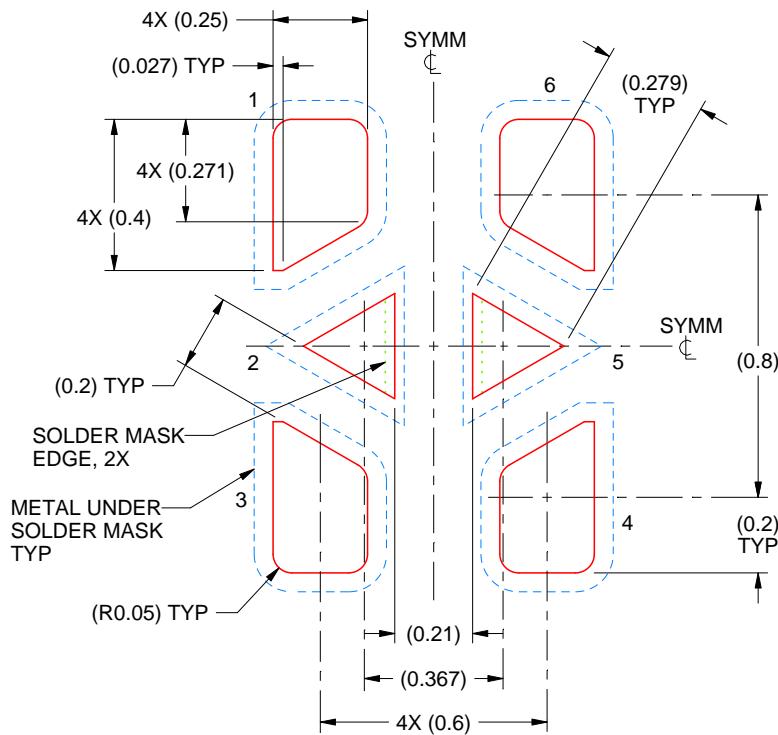
6. This package is designed to be soldered to a thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
7. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DTQ0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.07 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:50X

4224056/B 07/2024

NOTES: (continued)

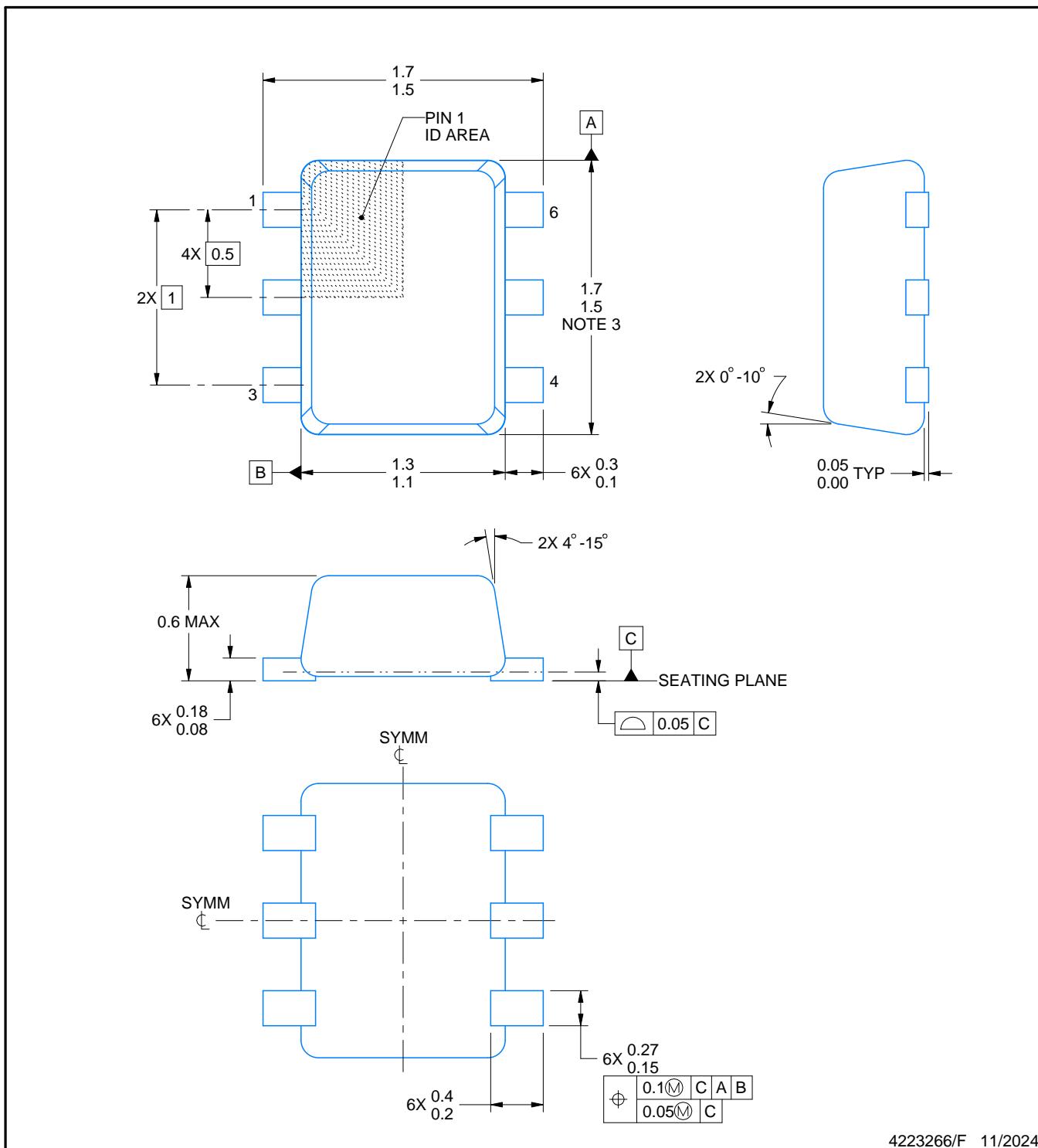
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE

DRL0006A



4223266/F 11/2024

NOTES:

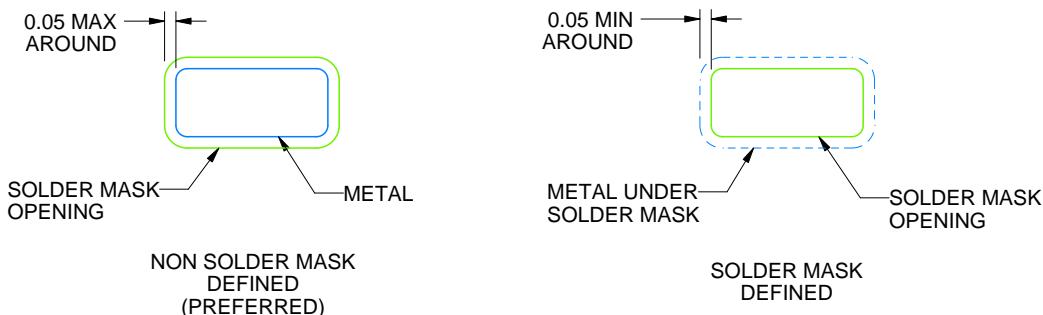
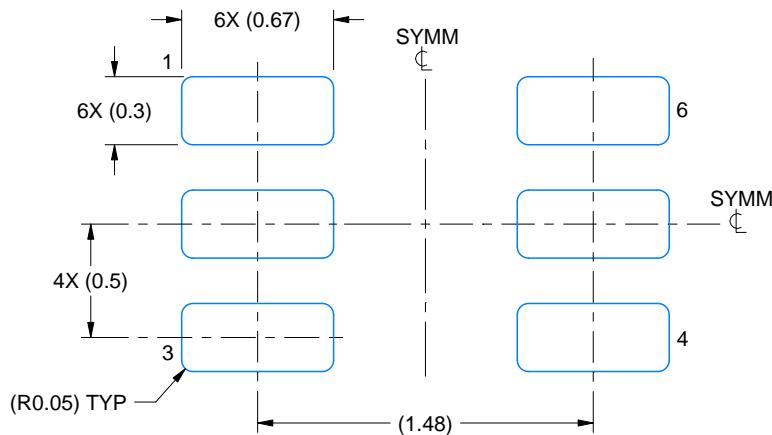
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



4223266/F 11/2024

NOTES: (continued)

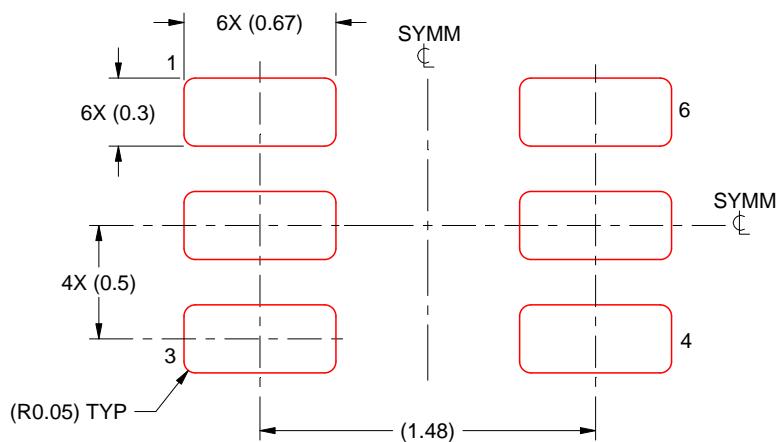
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/F 11/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

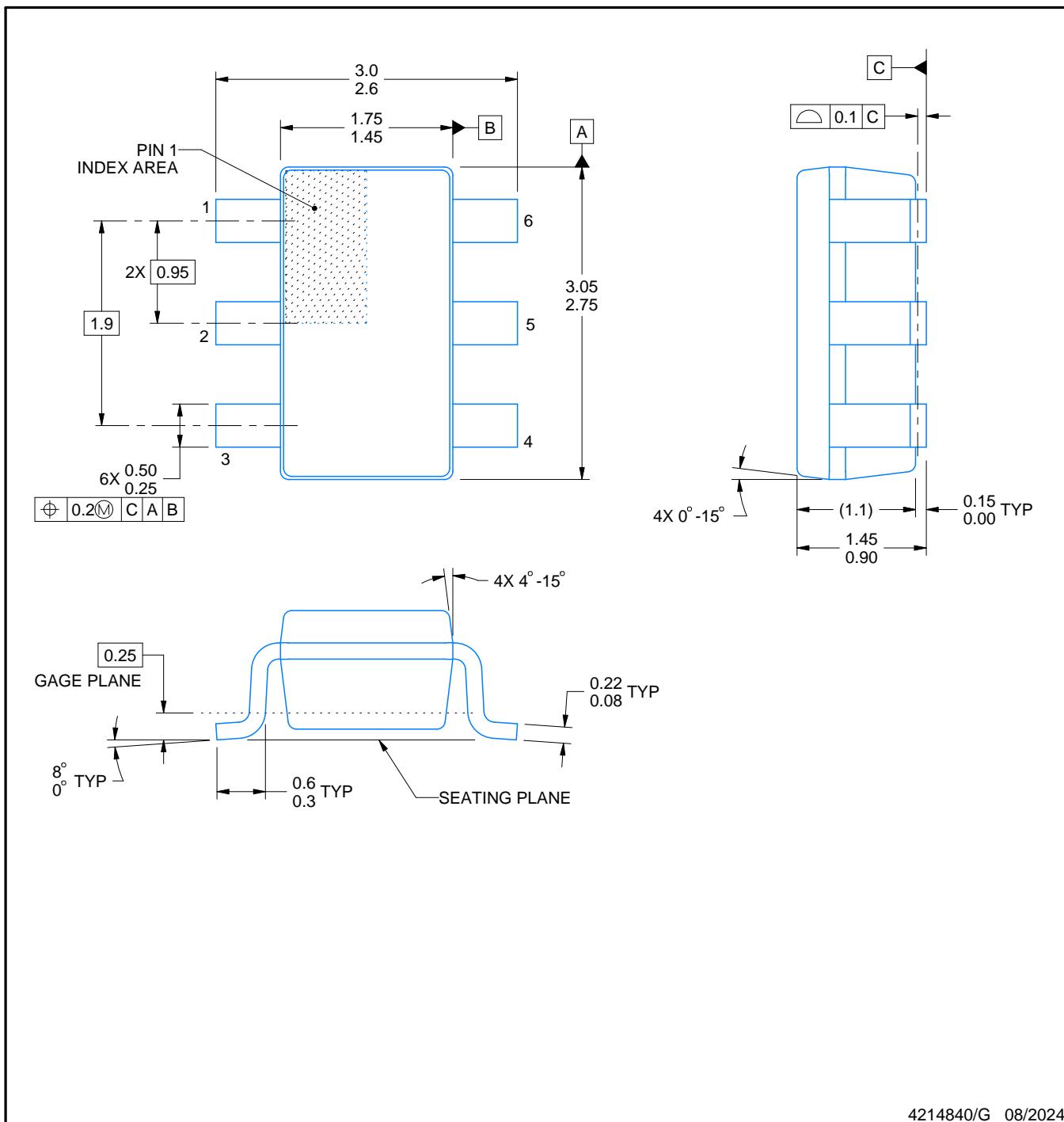
PACKAGE OUTLINE

DBV0006A



SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



NOTES:

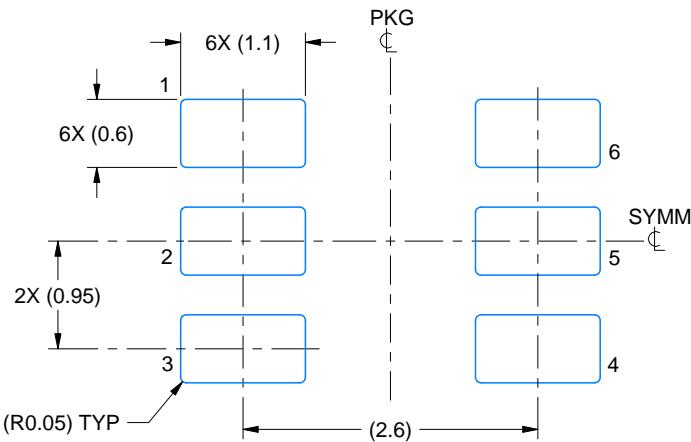
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

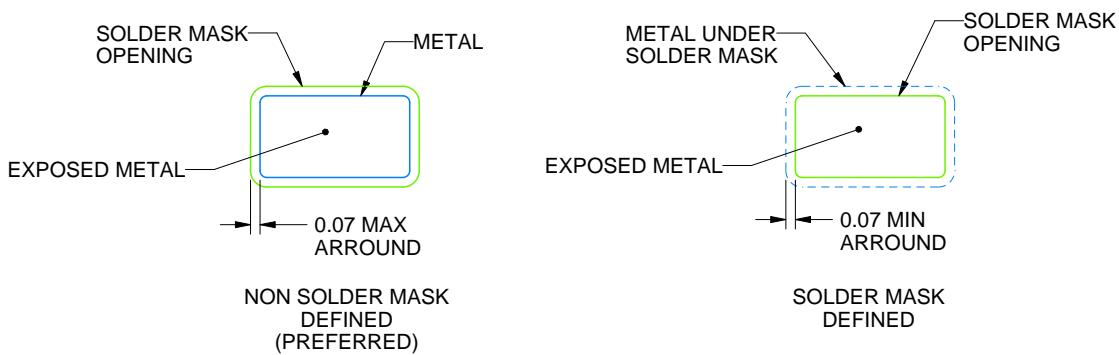
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

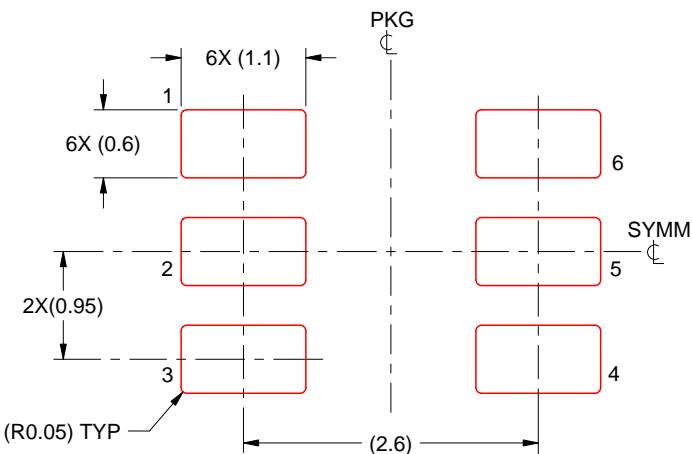
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025