

Improved Current Mode PWM Controller

FEATURES

- Pin-for-Pin Compatible With the UC3846
- 65ns Typical Delay From Shutdown to Outputs, and 50ns Typical Delay From Sync to Outputs
- Improved Current Sense Amplifier With Reduced Noise Sensitivity
- Differential Current Sense with 3V Common Mode Range
- Trimmed Oscillator Discharge Current for Accurate Deadband Control
- Accurate 1V Shutdown Threshold
- High Current Dual Totem Pole Outputs (1.5A peak)
- TTL Compatible Oscillator SYNC Pin Thresholds
- 4kV ESD Protection

DESCRIPTION

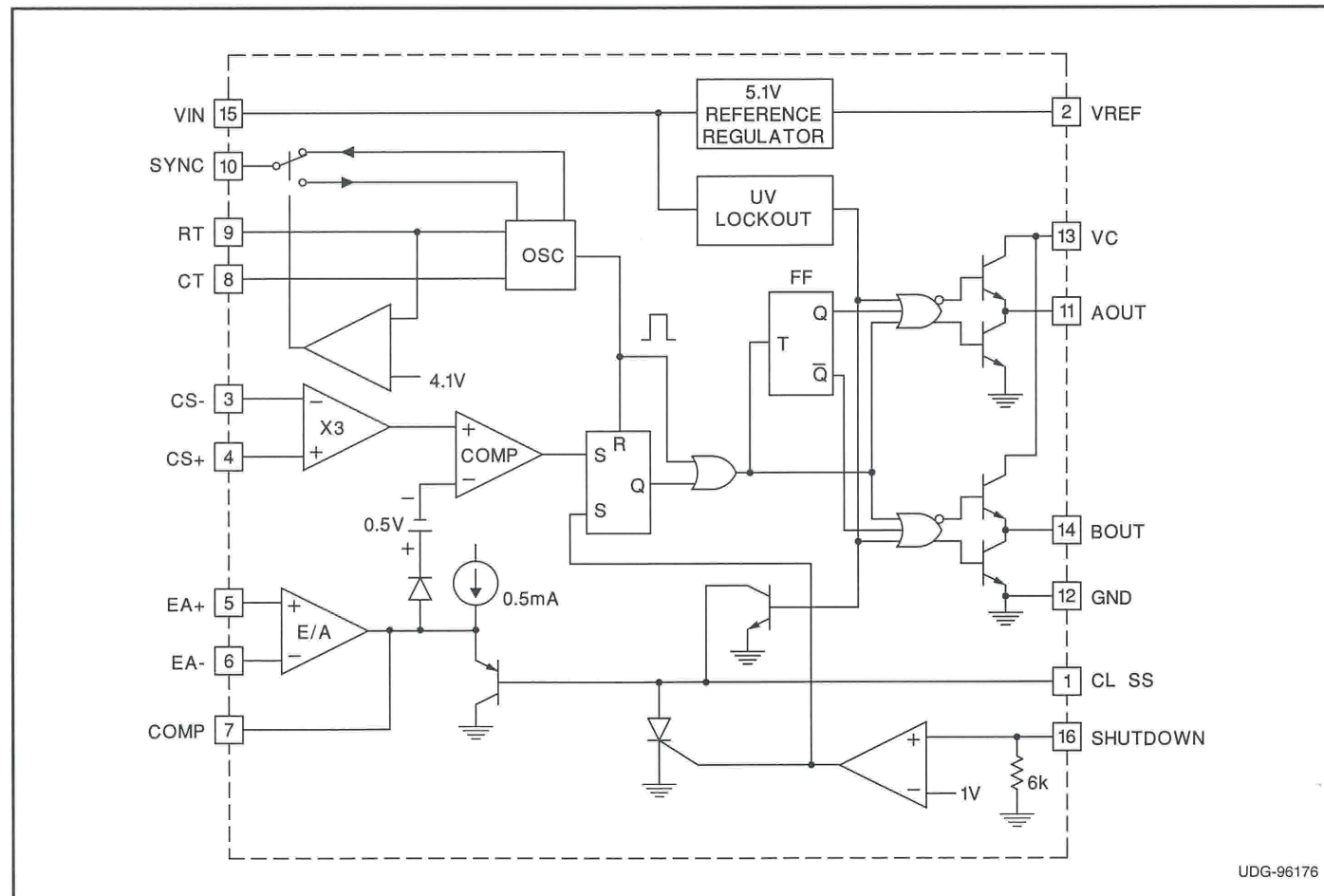
The UC3856 is a high performance version of the popular UC3846 series of current mode controllers, and is intended for both design upgrades and new applications where speed and accuracy are important. All input to output delays have been minimized, and the current sense output is slew rate limited to reduce noise sensitivity. Fast 1.5A peak output stages have been added to allow rapid switching of power FETs.

A low impedance TTL compatible sync output has been implemented with a tri-state function when used as a sync input.

Internal chip grounding has been improved to minimize internal "noise" caused when driving large capacitive loads. This, in conjunction with the improved differential current sense amplifier results in enhanced noise immunity.

Other features include a trimmed oscillator current (8%) for accurate frequency and dead time control; a 1V, 5% shutdown threshold; and 4kV minimum ESD protection on all pins.

BLOCK DIAGRAM



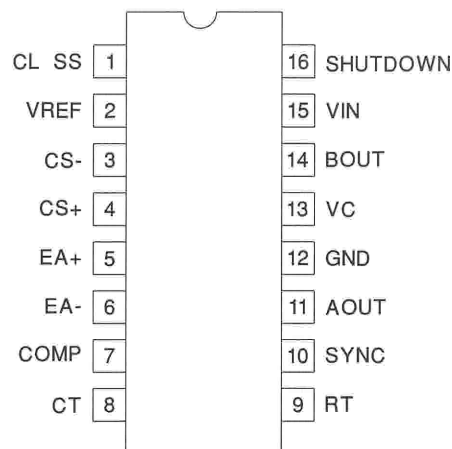
ABSOLUTE MAXIMUM RATINGS

| | |
|---|---------------------------|
| Supply Voltage | +40V |
| Collector Supply Voltage | +40V |
| Output Current, Source or Sink | |
| DC | 0.5A |
| Pulse (0.5μs) | 2.0A |
| Error Amp Inputs | −0.3V to +V _{IN} |
| Shutdown Input | −0.3V to +10V |
| Current Sense Inputs | −0.3V to +3V |
| SYNC Output Current | ±10mA |
| Error Amplifier Output Current | −5mA |
| Soft Start Sink Current | 50mA |
| Oscillator Charging Current | 5mA |
| Power Dissipation at T _A = 25°C (Note 2) | 1000mW |
| Power Dissipation at T _C = 25°C (Note 2) | 2000mW |
| Junction Temperature | −55°C to +150°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | +300°C |

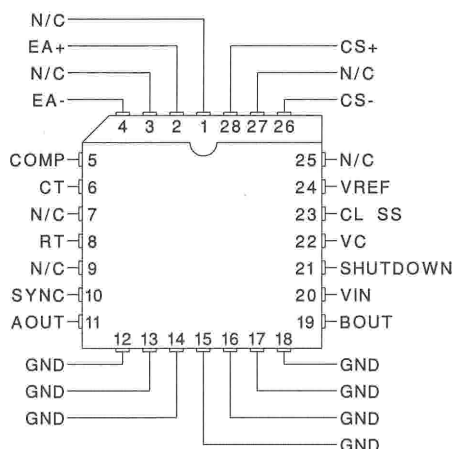
All voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal. Consult packaging section of databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

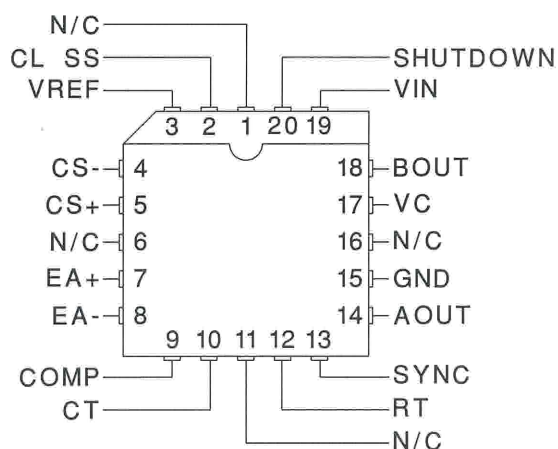
**DIL-16, SOIC-16 (Top View)
J or N, DW PACKAGE**



**PLCC-28 (Top View)
QP PACKAGE**



**PLCC-20 (Top View)
Q PACKAGE**



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = −55°C to +125°C for UC1856; −40°C to +85°C for the UC2856; and 0°C to +70°C for the UC3856, V_{IN} = 15V, R_T = 10k, C_T = 1nF, T_A = T_J.

| PARAMETER | TEST CONDITIONS | UC1856/UC2856 | | | UC3856 | | | UNITS |
|------------------------|---|---------------|------|------|--------|------|------|-------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| Reference Section | | | | | | | | |
| Output Voltage | T _J = 25°C, I _O = 1mA | 5.05 | 5.10 | 5.15 | 5.00 | 5.10 | 5.20 | V |
| Line Regulation | V _{IN} = 8V to 40V | | | 20 | | | 20 | mV |
| Load Regulation | I _O = −1mA to −10mA | | | 15 | | | 15 | mV |
| Total Output Variation | Line, Load, and Temperature | 5.00 | | 5.20 | 4.95 | | 5.25 | V |
| Output Noise Voltage | 10Hz < f < 10kHz, T _J = 25°C | | 50 | | | 50 | | μV |
| Long Term Stability | T _J = 125°C, 1000 Hrs (Note 2) | | 5 | 25 | | 5 | 25 | mV |
| Short Circuit Current | VREF = 0V | −25 | −45 | −65 | −25 | −45 | −65 | mA |
| Oscillator Section | | | | | | | | |
| Initial Accuracy | T _J = 25°C | 180 | 200 | 220 | 180 | 200 | 220 | kHz |
| | Over Operating Range | 170 | | 230 | 170 | | 230 | kHz |

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ for UC1856; -40°C to $+85^{\circ}\text{C}$ for the UC2856; and 0°C to $+70^{\circ}\text{C}$ for the UC3856, $V_{IN} = 15\text{V}$, $R_T = 10\text{k}$, $C_T = 1\text{nF}$, $T_A = T_J$.

| PARAMETER | TEST CONDITIONS | UC1856/UC2856 | | | UC3856 | | | UNITS |
|---|---|---------------|------|-------|--------|------|-------|-------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| Oscillator Section (cont.) | | | | | | | | |
| Voltage Stability | VIN = 8V to 40V | | | 2 | | | 2 | % |
| Discharge Current | TJ = 25°C, VCT = 2V | 7.5 | 8.0 | 8.8 | 7.5 | 8.0 | 8.8 | mA |
| | VCT = 2V | 6.7 | 8.0 | 8.8 | 6.7 | 8.0 | 8.8 | mA |
| Sync Output High Level | IO = −1mA | 2.4 | 3.6 | | 2.4 | 3.6 | | V |
| Sync Output Low Level | IO = +1mA | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| Sync Input High Level | CT = 0V, RT = VREF | 2.0 | 1.5 | | 2.0 | 1.5 | | V |
| Sync Input Low Level | CT = 0V, RT = VREF | | 1.5 | 0.8 | | 1.5 | 0.8 | V |
| Sync Input Current | CT = 0V, RT = VREF VSYNC = 5V | | 1 | 10 | | 1 | 10 | μA |
| Sync Delay to Outputs | CT = 0V, RT = VREF VSYNC = 0.8V to 2V | | 50 | 100 | | 50 | 100 | ns |
| Error Amplifier Section | | | | | | | | |
| Input Offset Voltage | VCM = 2V | | | 5 | | | 10 | mV |
| Input Bias Current | | | | −1 | | | −1 | μA |
| Input Offset Current | | | | 500 | | | 500 | nA |
| Common Mode Range | VIN = 8V to 40V | 0 | | VIN-2 | 0 | | VIN-2 | V |
| Open Loop Gain | VO = 1.2V to 3V | 80 | 100 | | 80 | 100 | | dB |
| Unity Gain Bandwidth | TJ = 25°C | 1 | 1.5 | | 1 | 1.5 | | MHz |
| CMRR | VCM = 0V to 38V, VIN = 40V | 75 | 100 | | 75 | 100 | | dB |
| PSRR | VIN = 8V to 40V | 80 | 100 | | 80 | 100 | | dB |
| Output Sink Current | VID = −15mV, VCOMP = 1.2V | 5 | 10 | | 5 | 10 | | mA |
| Output Source Current | VID = 15mV, VCOMP = 2.5V | −0.4 | −0.5 | | −0.4 | −0.5 | | mA |
| Output High Level | VID = 50mV, RL (COMP) = 15k | 4.3 | 4.6 | 4.9 | 4.3 | 4.6 | 4.9 | V |
| Output Low Level | VID = −50mV, RL (COMP) = 15k | | 0.7 | 1 | | 0.7 | 1 | V |
| Current Sense Amplifier Section | | | | | | | | |
| Amplifier Gain | VCS− = 0V, CL SS Open (Notes 3,4) | 2.5 | 2.75 | 3.0 | 2.5 | 2.75 | 3.0 | V/V |
| Maximum Differential Input Signal (VCS+ - VCS−) | CL SS Open (Note 3) RL (COMP) = 15k | 1.1 | 1.2 | | 1.1 | 1.2 | | V |
| Input Offset Voltage | VCL SS = 0.5VCOMP Open (Note 3) | | 5 | 35 | | 5 | 35 | mV |
| CMRR | VCM = 0V to 3V | 60 | | | 60 | | | dB |
| PSRR | VIN = 8V to 40V | 60 | | | 60 | | | dB |
| Input Bias Current | VCL SS = 0.5V, COMP Open (Note 3) | −1 | | 1 | −1 | | 1 | μA |
| Input Offset Current | VCL SS = 0.5V, COMP Open (Note 3) | −1 | | 1 | −1 | | 1 | μA |
| Input Common Mode Range | | 0 | | 3 | 0 | | 3 | V |
| Delay to Outputs | VEA+ = VREF, EA− = 0V CS+ − CS− = 0V to 1.5V | | 120 | 250 | | 120 | 250 | ns |
| Current Limit Adjust Section | | | | | | | | |
| Current Limit Offset | VCS− = 0V VCS+ = 0V, COMP = Open (Note 3) | 0.43 | 0.5 | 0.57 | 0.43 | 0.5 | 0.57 | V |
| Input Bias Current | VEA+ = VREF, VEA− = 0V | | −10 | −30 | | −10 | −30 | μA |
| Shutdown Terminal Section | | | | | | | | |
| Threshold Voltage | | 0.95 | 1.00 | 1.05 | 0.95 | 1.00 | 1.05 | V |
| Input Voltage Range | | 0 | | 5 | 0 | | 5 | V |

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ for UC1856; -40°C to $+85^\circ\text{C}$ for the UC2856; and 0°C to $+70^\circ\text{C}$ for the UC3856, $V_{IN} = 15\text{V}$, $R_T = 10\text{k}$, $C_T = 1\text{nF}$, $T_A = T_J$.

| PARAMETER | TEST CONDITIONS | UC1856/UC2856 | | | UC3856 | | | UNITS |
|--|---|---------------|------|-----|--------|------|-----|-------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| Shutdown Terminal Section (cont.) | | | | | | | | |
| Minimum Latching Current (I _{CL SS}) | (Note 5) | 3 | 1.5 | | 3 | 1.5 | | mA |
| Maximum Non-Latching Current (I _{CL SS}) | (Note 6) | | 1.5 | 0.8 | | 1.5 | 0.8 | mA |
| Delay to Outputs | V _{SHUTDOWN} = 0 to 1.3V | | 65 | 110 | | 65 | 110 | ns |
| Output Section | | | | | | | | |
| Collector-Emitter Voltage | | 40 | | | 40 | | | V |
| Off-State Bias Current | V _C = 40V | | | 250 | | | 250 | μA |
| Output Low Level | I _{OUT} = 20mA | | 0.1 | 0.5 | | 0.1 | 0.5 | V |
| | I _{OUT} = 200mA | | 0.5 | 2.6 | | 0.5 | 2.6 | V |
| Output High Level | I _{OUT} = -20mA | 12.5 | 13.2 | | 12.5 | 13.2 | | V |
| | I _{OUT} = -200mA | 12 | 13.1 | | 12 | 13.1 | | V |
| Rise Time | C1 = 1nF | | 40 | 80 | | 40 | 80 | ns |
| Fall Time | C1 = 1nF | | 40 | 80 | | 40 | 80 | ns |
| UVLO Low Saturation | V _{IN} = 0V, I _{OUT} = 20mA | | 0.8 | 1.5 | | 0.8 | 1.5 | V |
| PWM Section | | | | | | | | |
| Maximum Duty Cycle | | 45 | 47 | 50 | 45 | 47 | 50 | % |
| Minimum Duty Cycle | | | | 0 | | | 0 | % |
| Undervoltage Lockout Section | | | | | | | | |
| Startup Threshold | | | 7.7 | 8.0 | | 7.7 | 8.0 | V |
| Threshold Hysteresis | | | 0.7 | | | 0.7 | | V |
| Total Standby Current | | | | | | | | |
| Supply Current | | | 18 | 23 | | 18 | 23 | mA |

Note 1: All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal.

Note 2: This parameter, although guaranteed over the recommended operating conditions is not 100% tested in production.

Note 3: Parameter measured at trip point of latch with $V_{EA+} = V_{REF}$, $V_{EA-} = 0\text{V}$.

Note 4: Amplifier gain defined as:

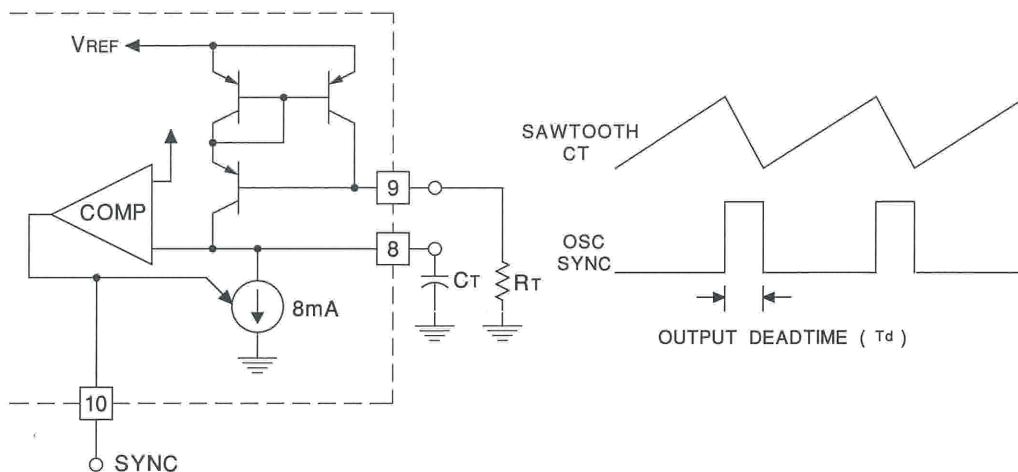
$$G = \frac{\Delta V_{COMP}}{\Delta V_{CS+}}; \quad \Delta V_{CS-} = 0\text{V TO } 1.0\text{V}$$

Note 5: Current into CL SS guaranteed to latch circuit into shutdown state.

Note 6: Current into CL SS guaranteed not to latch circuit into shutdown state.

APPLICATIONS INFORMATION

Oscillator Circuit



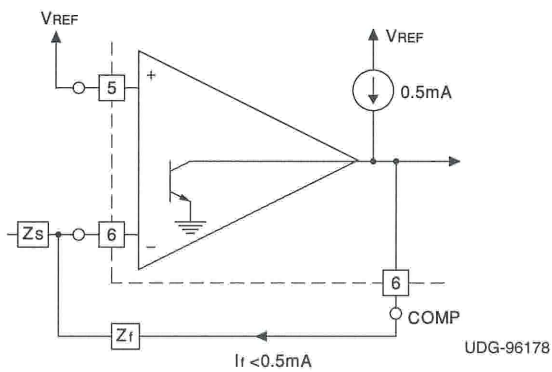
Output deadtime is determined by size of the external capacitor, C_T , according to the formula: $T_d = \frac{2C_T}{8mA - \frac{3.6}{R_T}}$

For large values of R_T : $T_d = 250C_T$

Oscillator frequency is approximated by the formula: $f_T = \frac{2}{R_T C_T}$

UDG-96177

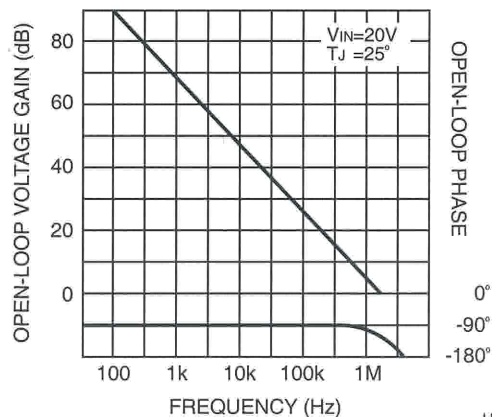
Error Amplifier Output Configuration



Error Amplifier can source up to 0.5mA.

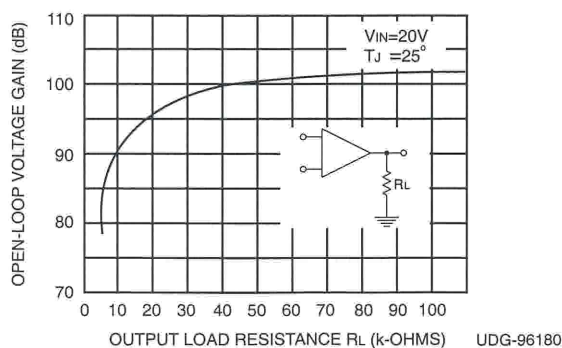
UDG-96178

Error Amplifier Gain and Phase vs Frequency



UDG-96179

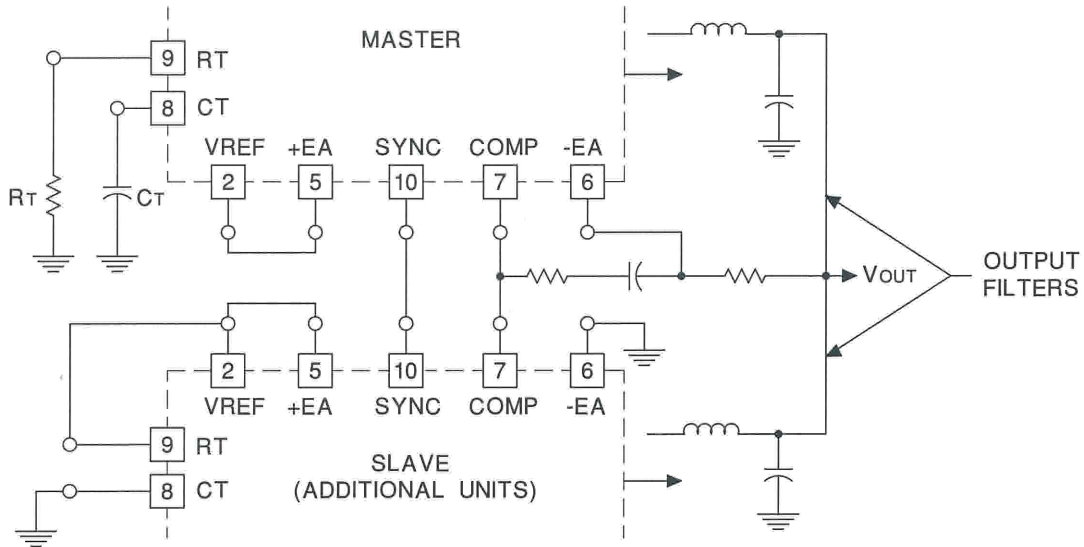
Error Amplifier Open-Loop D.C. Gain vs Load Resistance



UDG-96180

APPLICATIONS INFORMATION (cont.)

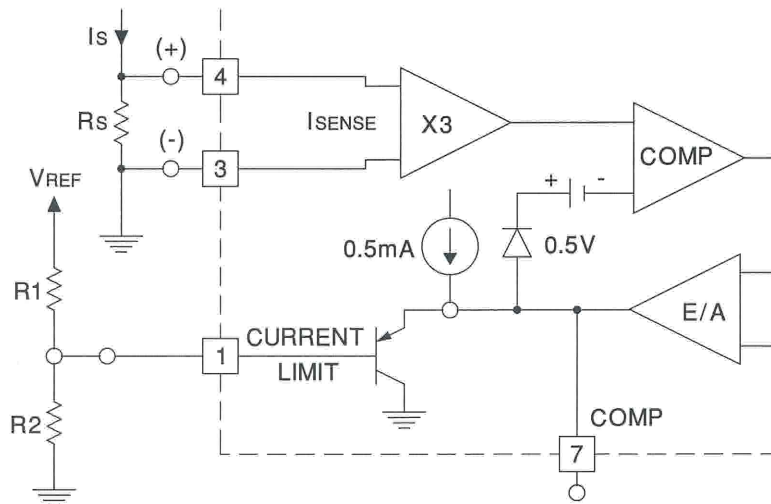
Parallel Operation



UDG-96181

Slaving allows parallel operation of two or more units with equal current sharing.

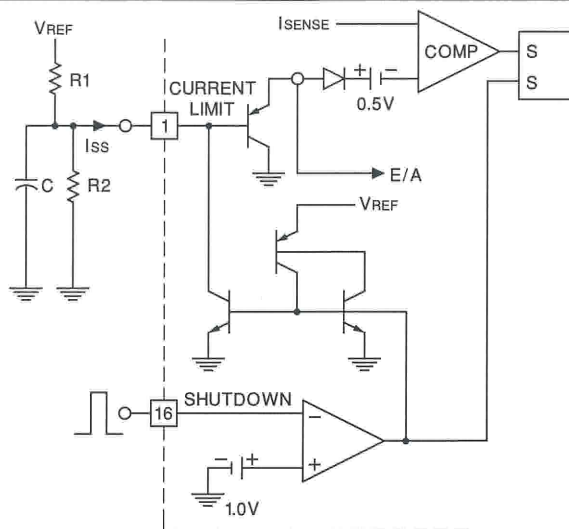
Pulse by Pulse Current Limiting



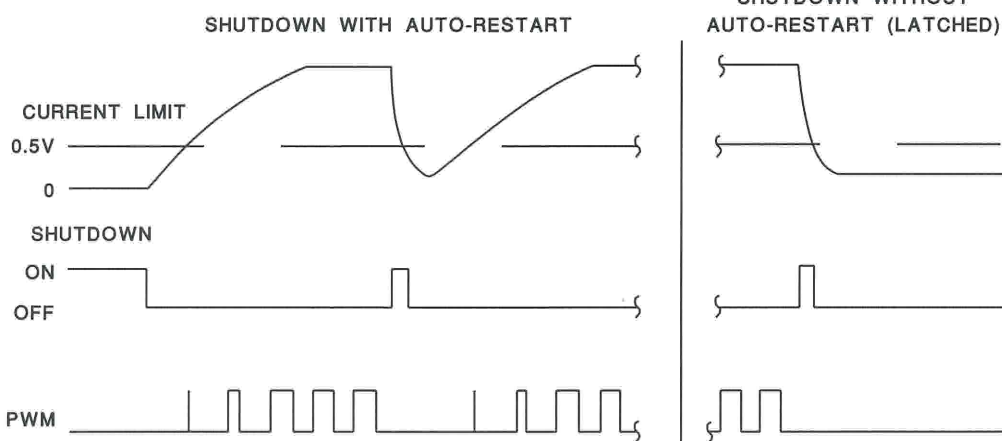
UDG-96182

Peak current (I_s) is determined by the formula:
$$I_s = \frac{\left(\frac{R_2 V_{REF}}{R_1 + R_2} \right) - 0.5}{3R_s}$$

APPLICATIONS INFORMATION (cont.)



UDG-96183

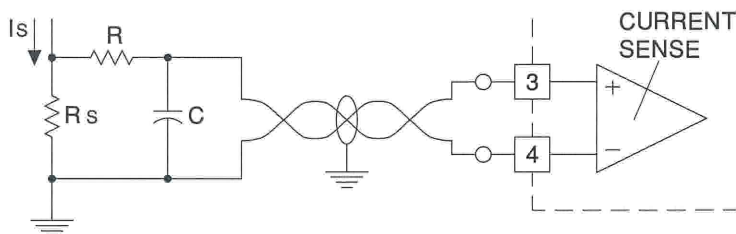


UDG-96184

If $\frac{V_{REF}}{R1} < 0.8\text{mA}$, the shutdown latch will commutate when $I_{ss} = 0.8\text{mA}$ and a restart cycle will be initiated.

If $\frac{V_{REF}}{R1} > 3\text{mA}$, the device will latch off until power is recycled.

Current Sense Amplifier Connections

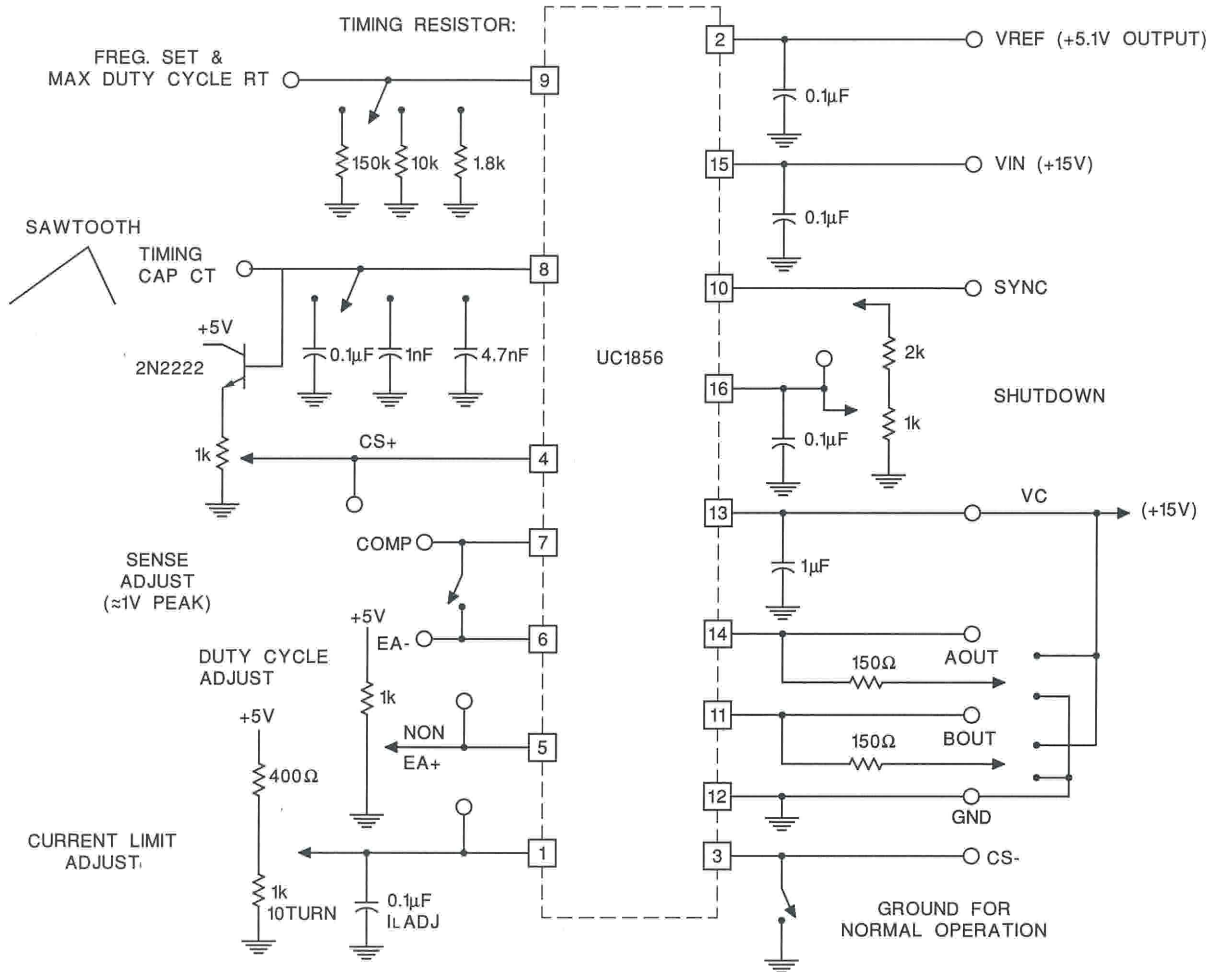


UDG-96185

A small RC filter may be required in some applications to reduce switch transients. Differential input allows remote, noise sensing.

APPLICATIONS INFORMATION (cont.)

UC1856 Open Loop Test Circuit



- BYPASS CAPS SHOULD BE LOW ESR & ESL TYPE
 - SHORT E/A- & COMP FOR UNITY GAIN TESTING
- THE USE OF A GROUND PLANE IS HIGHLY RECOMMENDED**

UDG-96186

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---|
| 5962-9453001M2A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 9453001M2A UC1856L20/ 883B |
| 5962-9453001MEA | Active | Production | CDIP (J) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9453001ME A UC1856J/883B |
| UC1856J | Active | Production | CDIP (J) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | UC1856J |
| UC1856J.A | Active | Production | CDIP (J) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | UC1856J |
| UC1856J883B | Active | Production | CDIP (J) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9453001ME A UC1856J/883B |
| UC1856J883B.A | Active | Production | CDIP (J) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9453001ME A UC1856J/883B |
| UC1856L20 | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | UC1856L20 |
| UC1856L20.A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | UC1856L20 |
| UC1856L20883B | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 9453001M2A UC1856L20/ 883B |
| UC1856L20883B.A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 9453001M2A UC1856L20/ 883B |
| UC2856DW | Obsolete | Production | SOIC (DW) 16 | - | - | Call TI | Call TI | -40 to 85 | UC2856DW |
| UC2856DWTR | Obsolete | Production | SOIC (DW) 16 | - | - | Call TI | Call TI | -40 to 85 | UC2856DW |
| UC2856J | Active | Production | CDIP (J) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -40 to 85 | UC2856J |
| UC2856J.A | Active | Production | CDIP (J) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -40 to 85 | UC2856J |
| UC2856N | Active | Production | PDIP (N) 16 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | UC2856N |
| UC2856N.A | Active | Production | PDIP (N) 16 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | UC2856N |
| UC3856DW | Active | Production | SOIC (DW) 16 | 40 TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | UC3856DW |
| UC3856DW.A | Active | Production | SOIC (DW) 16 | 40 TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | UC3856DW |

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|----------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| UC3856DWTR | Active | Production | SOIC (DW) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | UC3856DW |
| UC3856DWTR.A | Active | Production | SOIC (DW) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | UC3856DW |
| UC3856N | Active | Production | PDIP (N) 16 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | UC3856N |
| UC3856N.A | Active | Production | PDIP (N) 16 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | UC3856N |
| UC3856NG4 | Active | Production | PDIP (N) 16 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | UC3856N |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF UC1856, UC2856, UC2856M, UC3856 :

- Catalog : [UC3856](#), [UC2856](#)
- Automotive : [UC2856-Q1](#), [UC2856-Q1](#)
- Military : [UC2856M](#), [UC1856](#)
- Space : [UC1856-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| UC3856DWTR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| UC3856DWTR | SOIC | DW | 16 | 2000 | 353.0 | 353.0 | 32.0 |

TUBE



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-9453001M2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| UC1856L20 | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| UC1856L20.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| UC1856L20883B | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| UC1856L20883B.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| UC2856N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| UC2856N.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| UC3856DW | DW | SOIC | 16 | 40 | 507 | 12.83 | 5080 | 6.6 |
| UC3856DW.A | DW | SOIC | 16 | 40 | 507 | 12.83 | 5080 | 6.6 |
| UC3856N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| UC3856N.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| UC3856NG4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| PINS ** DIM | 14 | 16 | 18 | 20 |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



| PINS ** DIM | 14 | 16 | 18 | 20 |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS-001 VARIATION | AA | BB | AC | AD |



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

GENERIC PACKAGE VIEW

DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A



DW0016A

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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