

High Power Factor Preregulator

FEATURES

- Complete 8-pin Power Factor Solution
- Reduced External Components
- RMS Line Voltage Compensation
- Precision Multiplier/Squarer/Divider
- Internal 63kHz Synchronizable Oscillator
- Average Current Mode PWM Control
- Overvoltage Protection Comparator
- High Current, Clamped Gate Driver

DESCRIPTION

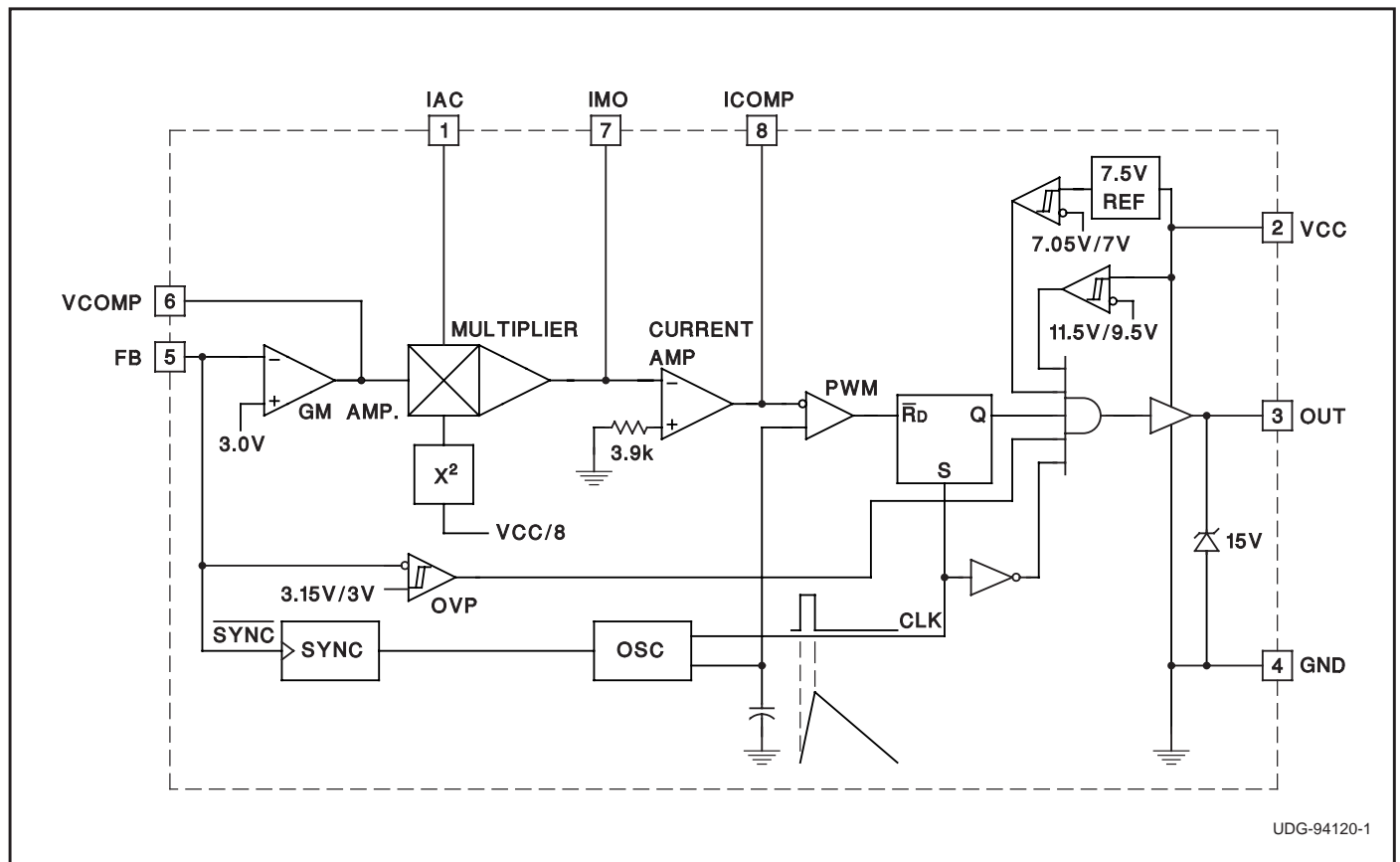
The UC2853A provides simple, yet high performance active power factor correction. Using the same control technique as the UC1854, this 8-pin device exploits a simplified architecture and an internal oscillator to minimize external component count. The UC2853A incorporates a precision multiplier/squarer/divider circuit, voltage and current loop error amplifiers, and a precision voltage reference to implement average current mode control with RMS line voltage compensation. This control technique maintains constant loop gain with changes in input voltage, which minimizes input line current distortion over the worldwide input voltage range.

The internal 63kHz oscillator includes an external clock input, allowing synchronization to downstream converters. Additionally, the device features an overvoltage protection comparator, a clamped MOSFET gate driver which self-biases low during undervoltage lockout, and low startup and supply current.

The UC2853A is identical to the UC2853 except the internal oscillator frequency has been reduced from 75kHz to 63kHz. The switching frequency is lowered in order to keep the second harmonic of the switching frequency below a 150kHz. For EMI specifications at 150kHz this makes it easier for a design to meet system requirements.

BLOCK DIAGRAM

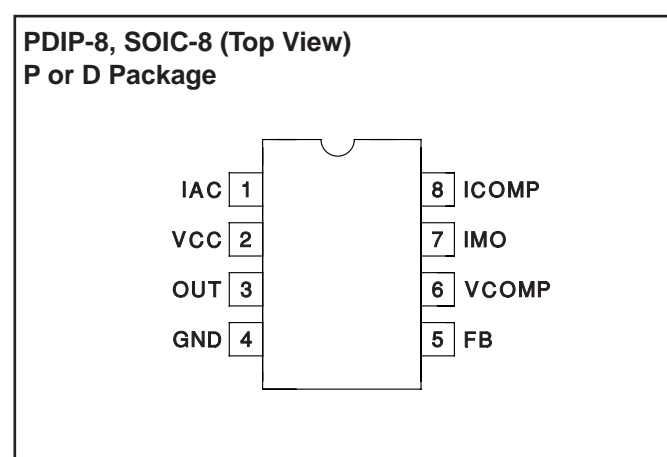
These devices are available in 8-pin PDIP (P) and SOIC (D) packages. The UC2853A is specified for operation from -40°C to 105°C .



ABSOLUTE MAXIMUM RATINGS

| | |
|---|-----------------|
| Supply Voltage (VCC) | 40V |
| Output Drive Current, | |
| Continuous | 0.125A |
| Peak | 0.5A |
| Output Minimum Voltage | -0.3V |
| IAC Maximum Input Current | 1mA |
| IMO Maximum Output Current | -2mA |
| IMO Minimum Voltage | -0.3V |
| FB Maximum Input Voltage | 5V |
| VCOMP Maximum Voltage | 6.2V |
| ICOMP Sourcing Current | Self-Limiting |
| ICOMP Sinking Current | 20mA |
| ICOMP Maximum Voltage | 7.2V |
| Storage Temperature | -65°C to +150°C |
| Junction Temperature | -55°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | +300°C |

All voltages with respect to GND. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM**ELECTRICAL CHARACTERISTICS**

Unless otherwise stated, these parameters apply for $T_A = -40^\circ\text{C}$ to 105°C for the UC2853A; $V_{CC} = 16\text{V}$, $V_{FB} = 3\text{V}$, $I_{AC} = 100\mu\text{A}$, $V_{VCOMP} = 3.75\text{V}$, $V_{ICOMP} = 3\text{V}$, $T_A = T_J$.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|-------|------|-------|-----------------|
| Undervoltage Lockout Section | | | | | |
| VCC Turn-on Threshold | V_{VCOMP} , V_{ICOMP} Open | | 11.5 | 13 | V |
| Hysteresis | | 1.5 | 1.8 | 2.1 | V |
| Supply Current Section | | | | | |
| I_{VCC} Startup | $V_{CC} = 8\text{V}$, $I_{AC} = 100\mu\text{A}$; V_{VCOMP} , V_{ICOMP} Open | | 250 | 500 | μA |
| I_{VCC} | $I_{AC} = 0\mu\text{A}$, $V_{ICOMP} = 0\text{V}$ | | 10 | 15 | mA |
| Voltage Loop Error Amplifier Section | | | | | |
| Transconductance | $I_{OUT} = \pm 20\mu\text{A}$ 0-70C | 300 | 450 | 575 | μmho |
| | Temperature | 135 | | 640 | μmho |
| Input Voltage | 0-70C | 2.925 | 3 | 3.075 | V |
| | Temperature | 2.9 | | 3.1 | V |
| AVOL | $V_{VCOMP} = 1\text{V} - 4\text{V}$ | 50 | 60 | | dB |
| Output Sink Current | $V_{FB} = 3.2\text{V}$, $V_{VCOMP} = 3.75\text{V}$ | 20 | 50 | | μA |
| Output Source Current | $V_{FB} = 2.8\text{V}$, $V_{VCOMP} = 3.75\text{V}$ | | -50 | -20 | μA |
| Output Voltage High | | 5.5 | 6 | | V |
| Output Voltage Low | | | 0.6 | 0.9 | V |
| Current Loop Error Amplifier Section | | | | | |
| Offset Voltage | | 0 | | 6 | mV |
| Voltage Gain | $V_{ICOMP} = 1\text{V} - 4\text{V}$ | | 70 | | dB |
| Sink Current | $V_{IMO} = 100\text{mV}$, $V_{ICOMP} = 3\text{V}$ | 1 | | | mA |
| Source Current | $V_{IMO} = -0.1\text{V}$, $V_{ICOMP} = 3\text{V}$ | | -150 | -80 | μA |
| Output High | $I_{ICOMP} = -50\text{mA}$ | 6 | 6.8 | | V |
| Output Low | $I_{ICOMP} = 50\mu\text{A}$ | | 0.3 | 0.8 | V |
| PWM Modulator Gain | $V_{ICOMP} = 2\text{V} - 3\text{V}$ (Note 1) | | 20 | | %/V |

ELECTRICAL CHARACTERISTICS
(continued)

Unless otherwise stated, these parameters apply for $T_A = -40^{\circ}\text{C}$ to 105°C for the UC2853A; $V_{CC} = 16\text{V}$, $V_{FB} = 3\text{V}$, $I_{AC} = 100\mu\text{A}$, $V_{VCOMP} = 3.75\text{V}$, $V_{ICOMP} = 3\text{V}$, $T_A = T_J$.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------------|--|-------|------|-------|-----------------|
| Multiplier Section | | | | | |
| Output Current – IAC Limited | $V_{CC} = 11\text{V}$, $V_{VCOMP} = 6\text{V}$ | -230 | -200 | -170 | μA |
| Output Current – Zero | $I_{AC} = 0\mu\text{A}$ | -2 | -0.2 | 2 | μA |
| Output Current – Power Limited | $V_{CC} = 12\text{V}$, $V_{VCOMP} = 5.5\text{V}$ | -236 | -178 | -168 | μA |
| Output Current | $V_{CC} = 12\text{V}$, $V_{VCOMP} = 2\text{V}$ | | -22 | | μA |
| | $V_{CC} = 12\text{V}$, $V_{VCOMP} = 5\text{V}$ | | -156 | | μA |
| | $V_{CC} = 40\text{V}$, $V_{VCOMP} = 2\text{V}$ | | -2 | | μA |
| | $V_{CC} = 40\text{V}$, $V_{VCOMP} = 5\text{V}$ | | -14 | | μA |
| Multiplier Gain Constant | $V_{CC} = 12\text{V}$, $V_{VCOMP} = 5.5\text{V}$ (Note 2) | -1.05 | -0.9 | -0.75 | V^{-1} |
| Oscillator Section | | | | | |
| Oscillator Initial Frequency | $T_A = 25^{\circ}\text{C}$ | 56 | 63 | 70 | kHz |
| Oscillator Frequency | Line, Load, Temperature | 50 | 63 | 74 | kHz |
| Synchronization Frequency Range | | | | 100 | kHz |
| Synchronization Pulse Amplitude | Pulse slew rate = $100\text{V}/\mu\text{sec}$ (Note 3) | | 2 | | V |
| Output Driver Section | | | | | |
| Maximum Output Voltage | 0mA load, $V_{CC} = 20\text{V}$ | 12 | 15 | 17.5 | V |
| Output High | 0mA load, $V_{CC} = 12\text{V}$, ref. to VCC | -2.7 | -1.7 | | V |
| | -50mA load, $V_{CC} = 12\text{V}$, ref. to VCC | -3 | -2.2 | | V |
| Output Low (Device Inactive) | $V_{CC} = 0\text{V}$, 20mA load (Sinking) | | 0.9 | 2.0 | V |
| Output Low (Device Active) | 50mA load (Sinking) | | 0.5 | 1 | V |
| OUT Rise Time | 1nF from OUT to GND | | 55 | 100 | ns |
| OUT Fall Time | 1nF from OUT to GND | | 35 | 100 | ns |
| OUT Maximum Duty Cycle | $V_{ICOMP} = 0\text{V}$ | 88 | 93 | | % |
| OVP Comparator Section | | | | | |
| Threshold Voltage | Volts Above EA Input V | 90 | 150 | | mV |
| Hysteresis | | | 80 | | mV |

Note 1:

$$1\text{PWM modulator gain} = \frac{\Delta\text{DutyCycle}}{\Delta V_{ICOMP}}$$

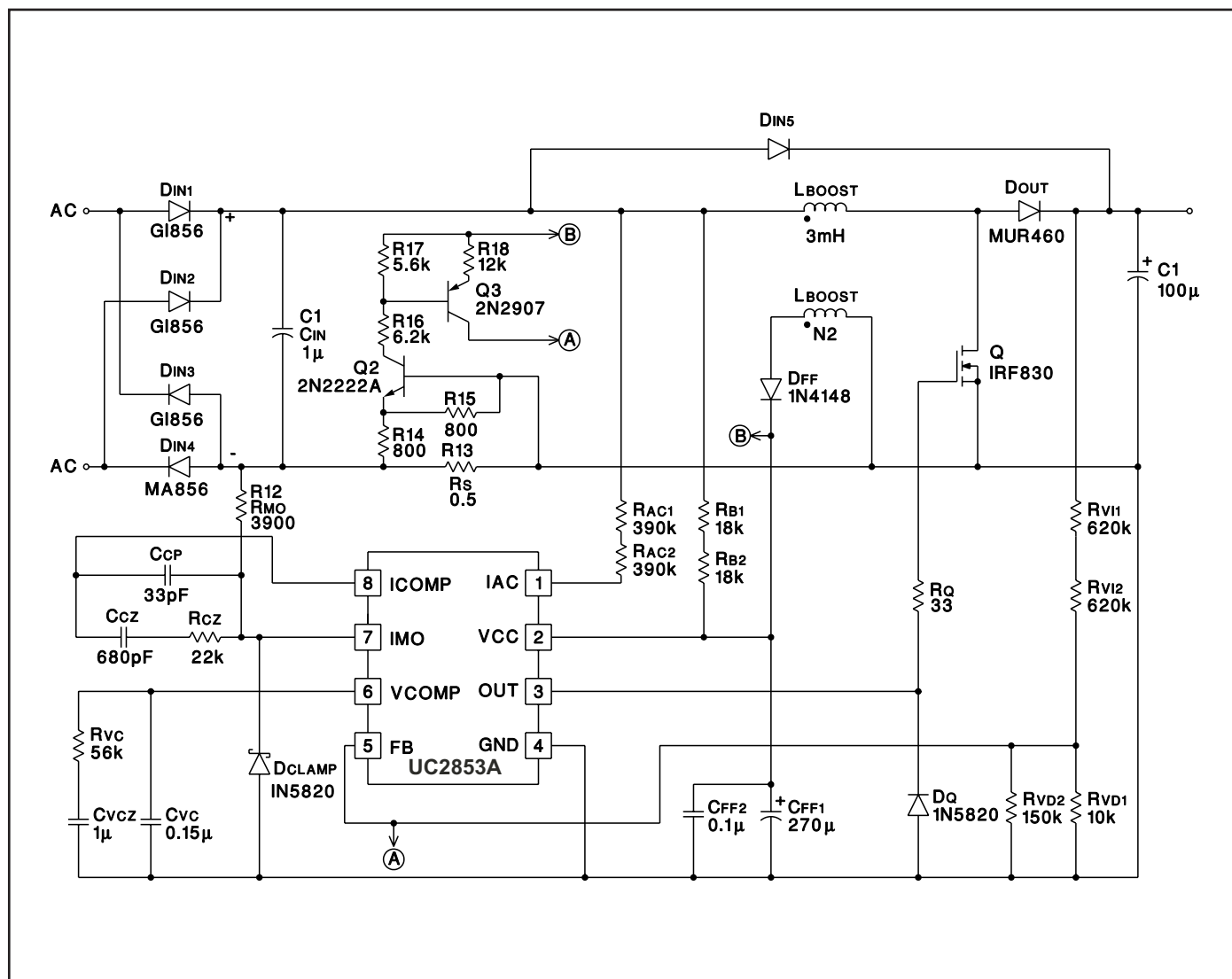
Note 2:

$$\text{Gain constant (K)} = \frac{I_{AC} \cdot (V_{COMP} - 1.5\text{V})}{I_{MO} \cdot V_{CC} \cdot \frac{V_{CC}}{64}}, \text{VCC} = 12\text{V}.$$

Note 3.

Synchronization is accomplished with a falling edge of 2V magnitude and $100\text{V}/\mu\text{sec}$ slew rate.

UC2853A TYPICAL APPLICATION



Note: the application circuit shown is a 100W, 63kHz design. Additional application information can be found in Application Note U-159 (TI literature Number SLUA080) and Design Note DN-78.

PIN DESCRIPTIONS

FB: Voltage Amplifier Inverting Input, Overvoltage Comparator Input, Sync Input. This pin serves three functions. FB accepts a fraction of the power factor corrected output voltage through a voltage divider, and is nominally regulated to 3V. FB voltages 5% greater than nominal will trip the overvoltage comparator, and shut down the output stage until the output voltage drops 5%. The internal oscillator can be synchronized through FB by injecting a 2V clock signal through a capacitor. To prevent false tripping of the overvoltage comparator, the clock signal must have a fast falling edge, but a slow rising edge. See Application Note U-159 for more information.

GND: Ground. All voltages are measured with respect to GND. The VCC bypass capacitor should be connected to ground as close to the GND pin as possible.

IAC: AC Waveform Input. This input provides voltage waveform information to the multiplier. The current loop will try to produce a current waveform with the same shape as the IAC signal. IAC is a low impedance input, nominally at 2V, which accepts a current proportional to the input voltage. Connect a resistor from the rectified input line to IAC which will conduct 500 μ A at maximum line voltage.

IMO: Multiplier Output and Current Sense Inverting Input. The output of the multiplier and the inverting input of the current amplifier are connected together at IMO. Avoid bringing this input below -0.5 V to prevent the internal protection diode from conducting. The multiplier output is a current, making this a summing node and allowing a differential current error amplifier configuration to reject ground noise. The input resistance at this node should be 3.9k to minimize input bias current induced offset voltage. See the Applications section for the recommended circuit configuration.

OUT: Gate Driver Output. OUT provides high current gate drive for the external power MOSFET. A 15V clamp pre-

vents excessive MOSFET gate-to-source voltage so that the UC2853A can be operated with VCC and high as 40V. A series gate resistor of at least 5 ohms should be used to minimize clamp voltage overshoot. In addition, a Schottky diode such as a 1N5818 connected between OUT and GND may be necessary to prevent parasitic substrate diode conduction.

ICOMP: Current Loop Error Amplifier Output. The current loop error amplifier is a conventional operational amplifier with a 150 μ A current source class A output stage. Compensate the current loop by placing an impedance between ICOMP and IMO. This output can swing above the oscillator peak voltage, allowing zero duty cycle when necessary.

VCC: Input Supply Voltage. This pin serves two functions. It supplies power to the chip, and an input voltage level signal to the squarer circuit. When this input is connected to a DC voltage proportional to the AC input RMS voltage, the voltage loop gain is reduced by

$$\frac{64}{V_{CC}^2}$$

This configuration maintains constant loop gain. The UC2853A input voltage range extends from 12V to 40V, allowing an AC supply voltage range in excess of 85VAC to 265VAC. Bypass VCC with at least a 0.1 μ F ceramic capacitor to ensure proper operation. See the Applications section for the recommended circuit configuration.

VCOMP: Voltage Loop Error Amplifier Output. The voltage loop error amplifier is a transconductance type operational amplifier. A feedback impedance between VCOMP and FB for loop compensation must be avoided to maintain proper operation of the overvoltage protection comparator. Instead, compensate the voltage loop with an impedance between VCOMP and GND. When VCOMP is below 1.5V, the multiplier output current is zero.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|----------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| UC2853AD | NRND | Production | SOIC (D) 8 | 75 TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | UC2853A |
| UC2853AD.A | NRND | Production | SOIC (D) 8 | 75 TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | UC2853A |
| UC2853ADTR | NRND | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | UC2853A |
| UC2853ADTR.A | NRND | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | UC2853A |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| UC2853ADTR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| UC2853ADTR | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| UC2853AD | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| UC2853AD.A | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |

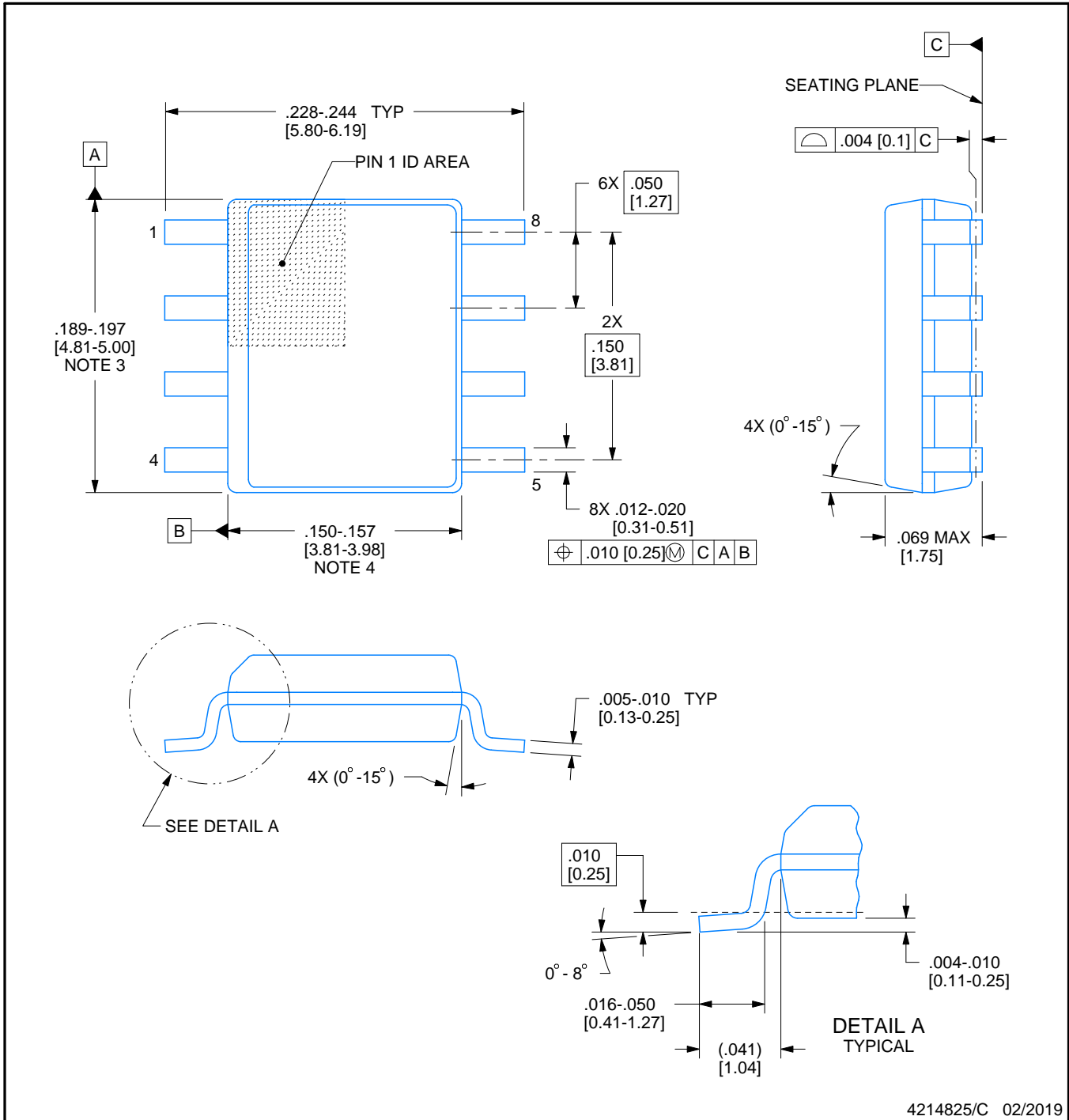


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



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NOTES:

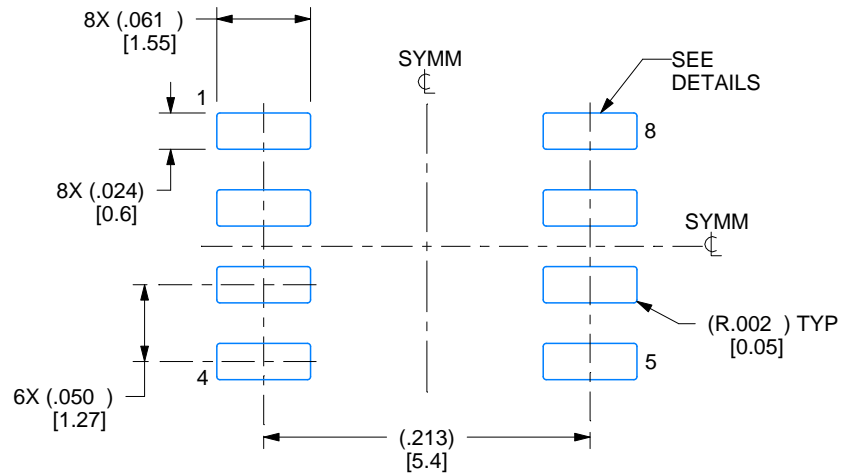
- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

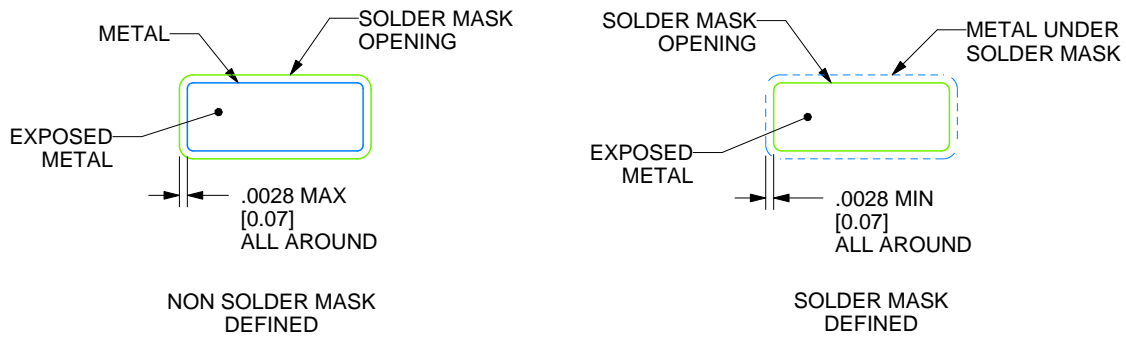
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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