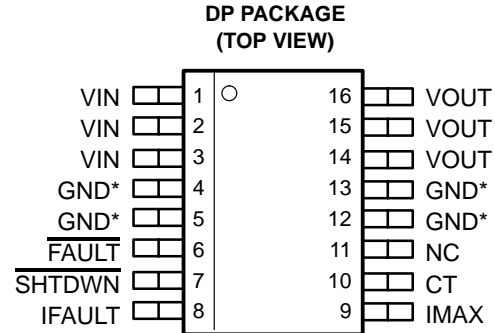


- **Integrated 0.075-Ω Power MOSFET**
- **3 V to 6 V Operation**
- **External Analog Control of Fault Current from 0 A to 4 A**
- **Independent Analog Control of Current Limit Up to 5 A**
- **Fast Overload Protection**
- **Unidirectional Switch**
- **Minimal External Components**
- **1-μA I_{CC} When Disabled**
- **Programmable On Time**
- **Programmable Start Delay**
- **Fixed 3% Duty Cycle**



Pin 5 serves as the lowest impedance to the electrical ground. Pins 4, 12, and 13, serve as heat sink/ground. These pins should be connected to large etch PCB areas to help dissipate heat.

description

The UCC3918 low on-resistance hot swap power manager provides complete power management, hot swap capability, and circuit breaker functions. The only components needed to operate the device, other than supply bypassing, are a timing capacitor, and two programming resistors. All control and housekeeping functions are integrated, and externally programmable. These include the fault current level, maximum output sourcing current, maximum fault time, and startup delay. In the event of a constant fault, the internal fixed 3% duty cycle ratio limits the average output power. The IFAULT pin allows linear programming of the fault level current from 0 A to 4 A.

Fast overload protection is accomplished by an additional overload comparator. Its threshold is internally set above the maximum sourcing current limit setting. In the event of a short circuit or extreme current condition, this comparator is tripped, shutting down the output. This function is needed since the maximum sourcing current limit loop has a finite bandwidth.

When the output current is below the fault level, the output MOSFET is switched on with a nominal resistance of 0.075 Ω. When the output current exceeds the fault level or the maximum sourcing level, the output remains on, but the fault timer starts charging a capacitor connected to the CT pin (C_T). Once C_T charges to a preset threshold, the switch is turned off, and remains off for 30 times the programmed fault time. When the output current reaches the maximum sourcing level, the MOSFET transitions from a switch to a constant current source.

The UCC3918 is designed for unidirectional current flow, emulating an ideal diode in series with the power switch. This feature is particularly attractive in applications where many devices are powering a common bus, such as with SCSI termination power (Term_{pwr}). The UCC3918 can also be put into the sleep mode, drawing only 1 μA of supply current.

Other features include an open-drain fault output indicator, thermal shutdown, undervoltage lockout, 3 V to 6 V operation, and a low thermal resistance small-outline power package.



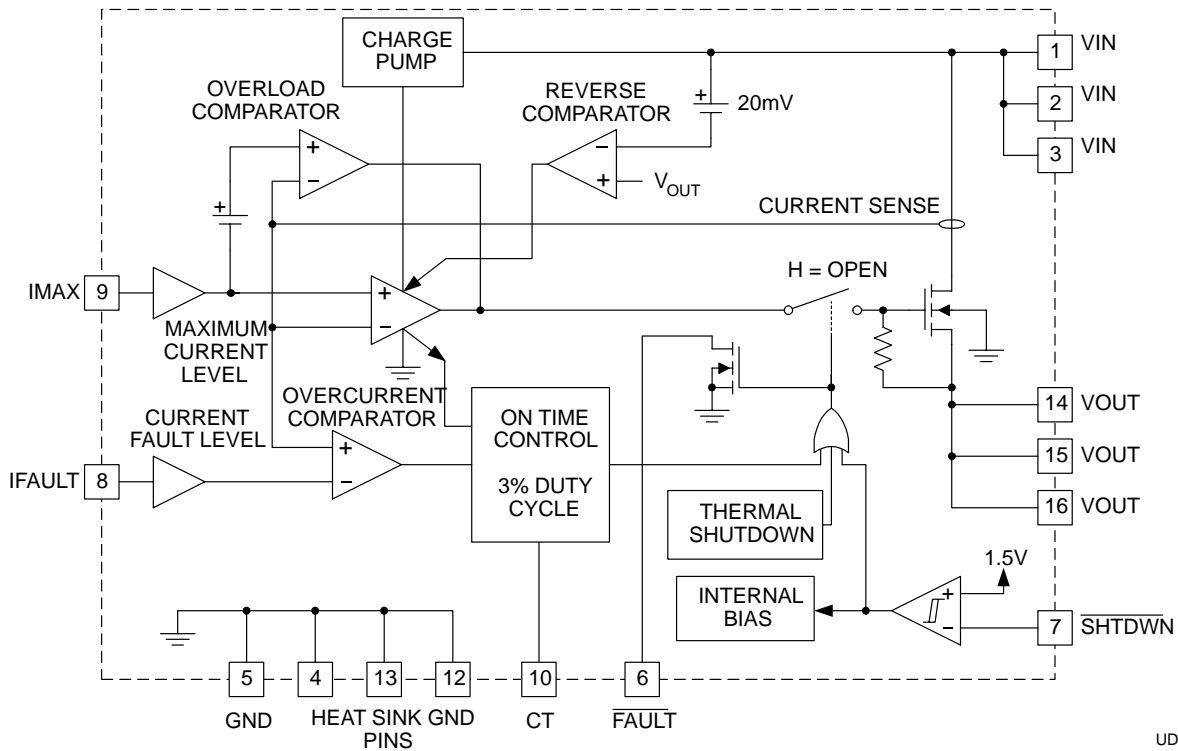
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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

UCC3918 LOW ON-RESISTANCE HOT SWAP POWER MANAGER

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functional block diagram



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absolute maximum ratings over operating free-air temperature (unless otherwise noted)^{†‡}

Input Voltage	8 V
SOIC Power dissipation	2.5 W
Fault output sink current	50 mA
Fault output voltage	VIN
Output Current (dc)	Internally Limited
Input Voltage <u>SHTDWN</u> , IFault, IMAX	-0.3 V to VIN
Storage temperature range T _{stg}	-65°C to 150°C
Operating virtual junction temperature T _J	-55°C to 150°C
Lead temperature (soldering, 10 seconds)	300°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[‡] Unless otherwise indicated, voltages are reference to ground and currents are positive into, negative out of the specified terminal. Pulsed is defined as a less than 10% duty cycle with a maximum duration of 500 μ s. Consult *Packaging Section* of Databook for thermal limitations and considerations of package.

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electrical characteristics at $T_A = 0^\circ\text{C}$ to 70°C , $V_{IN} = 5\text{ V}$, $R_{I\text{MAX}} = 42.2\text{ k}\Omega$, $R_{I\text{FAULT}} = 52.3\text{ k}\Omega$, $\overline{\text{SHTDWN}} = 2.4\text{ V}$, $T_A = T_J$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Section					
Voltage input range, V_{IN}		3	5	6	V
VDD supply current	No load		1	2	mA
Sleep mode current	$\overline{\text{SHTDWN}} = 0.2\text{ V}$		0.5	5	μA
Output Section					
$R_{DS(on)}$	$I_{OUT} = 1\text{ A to }4\text{ A}$, $V_{IN} = 5\text{ V}$, $T_A = 25^\circ\text{C}$		0.075	0.095	Ω
	$I_{OUT} = 1\text{ A to }4\text{ A}$, $V_{IN} = 3\text{ V}$, $T_A = 25^\circ\text{C}$		0.09	0.116	Ω
	$I_{OUT} = 1\text{ A to }4\text{ A}$, $V_{IN} = 5\text{ V}$		0.075	0.125	Ω
	$I_{OUT} = 1\text{ A to }4\text{ A}$, $V_{IN} = 3\text{ V}$		0.09	0.154	Ω
Reverse leakage current	$\overline{\text{SHTDWN}} = 0\text{ V}$, $V_{IN} = 0\text{ V}$, $V_{OUT} = 5\text{ V}$			20	μA
Initial startup time	See Note 1		100		μs
Thermal shutdown	$V_{IN} = 5\text{ V}$, See Note 1		170		$^\circ\text{C}$
Thermal hysteresis	See Note 1		10		$^\circ\text{C}$
Output leakage	$\overline{\text{SHTDWN}} = 0.2\text{ V}$, $V_{OUT} = 0\text{ V}$			20	μA
Trip current	$R_{I\text{FAULT}} = 105\text{ k}\Omega$	0.75	1	1.25	A
	$R_{I\text{FAULT}} = 52.3\text{ k}\Omega$	1.7	2	2.3	A
	$R_{I\text{FAULT}} = 34.8\text{ k}\Omega$	2.5	3	3.5	A
	$R_{I\text{FAULT}} = 25.5\text{ k}\Omega$	3.3	4	4.7	A
Maximum output current	$R_{I\text{MAX}} = 118\text{ k}\Omega$	0.3	1	1.7	A
	$R_{I\text{MAX}} = 60.4\text{ k}\Omega$	1	2	3	A
	$R_{I\text{MAX}} = 42.2\text{ k}\Omega$	2	3	4	A
	$R_{I\text{MAX}} = 33.2\text{ k}\Omega$	2.5	3.8	5.1	A
	$R_{I\text{MAX}} = 27.4\text{ k}\Omega$	3.0	4.6	6.2	A
Fault Section					
C_T charge current	$V_{CT} = 1\text{ V}$	-50	-36	-22	μA
C_T discharge current	$V_{CT} = 1\text{ V}$	0.5	1.2	2.0	μA
Output duty cycle	$V_{OUT} = 0\text{ V}$	1.5	3	6	%
C_T fault threshold		0.8	1.3	1.8	V
C_T reset threshold		0.25	0.5	0.75	V
Shutdown Section					
Shutdown threshold		1.1	1.5	2.0	V
Shutdown hysteresis			100		mV
Input low current	$\overline{\text{SHTDWN}} = 0\text{ V}$	-500	0	500	nA
Input high current	$\overline{\text{SHTDWN}} = 2\text{ V}$	-2	-1	-0.5	μA
Open Drain Fault Output Section					
High level output current				1	μA
Low level output voltage	$I_{OUT} = 1\text{ mA}$		0.4	0.9	V

NOTE 1: Ensured by design. Not production tested.

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pin descriptions

CT: A capacitor connected to this pin sets the maximum fault time. The maximum time must be greater than the time to charge external load capacitance. The nominal fault time is defined as:

$$T_{\text{FAULT}} = 22.2 \times 10^3 \times C_T \quad (1)$$

Once the fault time is reached the output shuts down for a time given by:

$$T_{\text{SD}} = 0.667 \times 10^6 \times C_T \quad (2)$$

This equates to a 3% duty cycle. The recommended minimum value for the C_T capacitor is 0.1 μF .

FAULT: Open-drain output, which pulls low on any condition that causes the output to open; Fault, Thermal Shutdown, Shutdown, and maximum sourcing current greater than the fault time.

GND: This is the most negative voltage in the circuit. All 4 ground pins should be used, and properly heat sunk on the PCB.

IFault: A resistor connected from this pin to ground sets the fault threshold. The resistor versus fault current is set by the formula

$$R_{\text{FAULT}} = \frac{105 \text{ k}\Omega}{I_{\text{TRIP}}} \quad (3)$$

IMAX: A resistor connected from this pin to ground sets the maximum sourcing current. The resistor vs the output sourcing current is set by the formula:

$$R_{\text{IMAX}} = \frac{126 \text{ k}\Omega}{\text{Maximum Sourcing Current}} \quad (4)$$

SHTDWN: When this pin is brought low, the IC is put into sleep mode. The input threshold is hysteretic, allowing the user to program a startup delay with an external RC circuit.

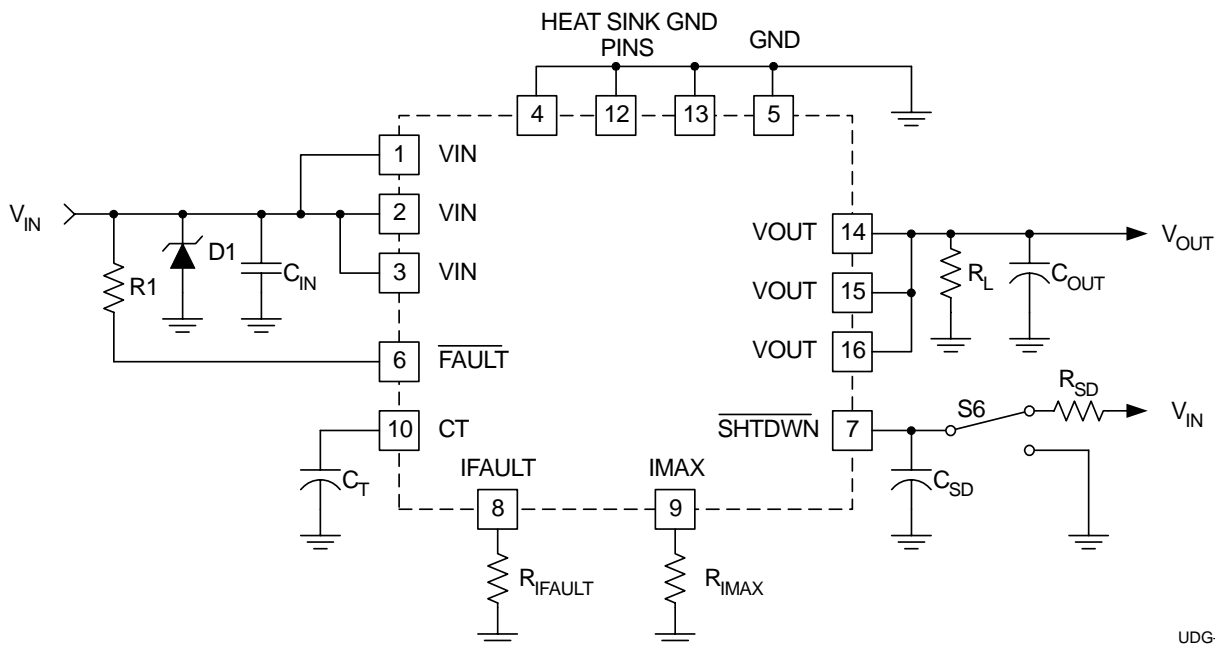
VIN: This is the input voltage to the UCC3918. The recommended operating voltage range is 3V to 6V. All VIN pins should be connected together and to the power source.

VOUT: Output voltage for the circuit breaker. When switched the output voltage will be approximately:

$$V_{\text{OUT}} = V_{\text{IN}} - 0.075\Omega \times I_{\text{OUT}} \quad (5)$$

All VOUT pins should be connected together and to the load.

APPLICATION INFORMATION



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Figure 1. Typical Application

protecting the UCC3918 from voltage transients

The parasitic inductance associated with the power distribution can cause a voltage spike at V_{IN} if the load current is suddenly interrupted by the UCC3918. *It is important to limit the peak of this spike to less than 6 V to prevent damage to the UCC3918.* This voltage spike can be minimized by:

- Reducing the power distribution inductance (e.g., twist the positive “+” and negative “-” leads of the power supply feeding V_{IN} , locate the power supply close to the UCC3918 or use a PCB ground plane).
- Decoupling V_{IN} with a capacitor, C_{IN} (refer to Figure 1), located close to the V_{IN} pin. This capacitor is typically less than 1 μF to limit the inrush current.
- Clamping the voltage at V_{IN} below 6 V with a Zener diode, D1 (refer to Figure 1), located close to the V_{IN} pin.

estimating maximum load capacitance

For circuit breaker applications, the rate at which the total output capacitance can be charged depends on the maximum output current available and the nature of the load. For a constant-current current-limited circuit breaker, the output comes up if the load requires less than the maximum available short-circuit current.

To ensure recovery of a duty-cycle of the current-limited circuit breaker from a short-circuited load condition, there is a maximum total output capacitance that can be charged for a given unit ON time (fault time). The design value of ON or fault time can be adjusted by changing the timing capacitor C_T .

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APPLICATION INFORMATION

estimating maximum load capacitance

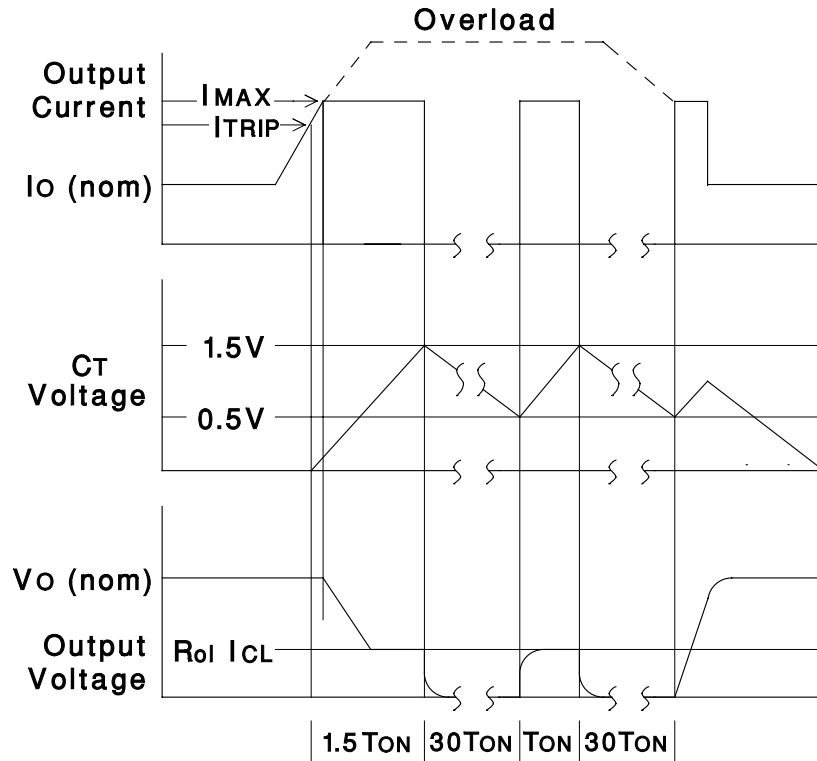
For worst-case constant-current load of value just less than the trip limit; $C_{OUT(max)}$ can be estimated from:

$$C_{OUT(max)} = (I_{MAX} - I_{LOAD}) \left(\frac{22 \times 10^3 \times C_T}{V_{OUT}} \right) \quad (6)$$

Where V_{OUT} is the output voltage and I_{MAX} is the maximum sourcing current.

For a resistive load of value R_{LOAD} , the value of $C_{OUT(max)}$ can be estimated from:

$$C_{OUT(max)} = \left[\frac{22 \times 10^3 \times C_T}{R_{LOAD} \times \ln \left[\frac{1}{1 - \frac{V_{OUT}}{I_{MAX} \times R_{LOAD}}} \right]} \right] \quad (7)$$



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Figure 2. Load Current, Timing Capacitor Voltage and Output Voltage of the UCC3918 Under Fault

TYPICAL CHARACTERISTICS

**REVERSE VOLTAGE COMPARATOR
RESPONSE TIME**

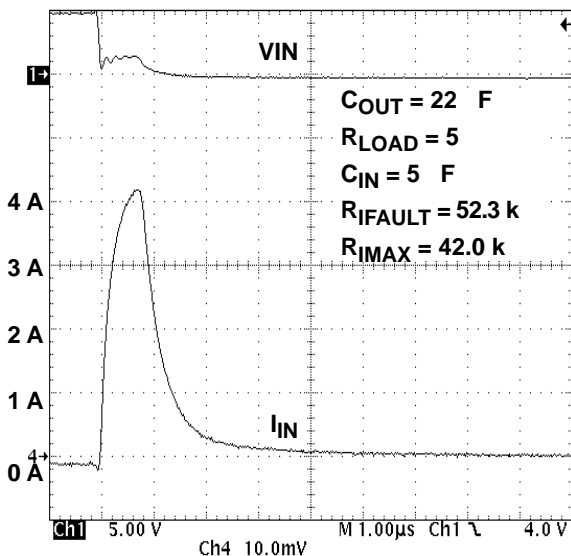


Figure 3

FAULT TIMING WAVEFORMS

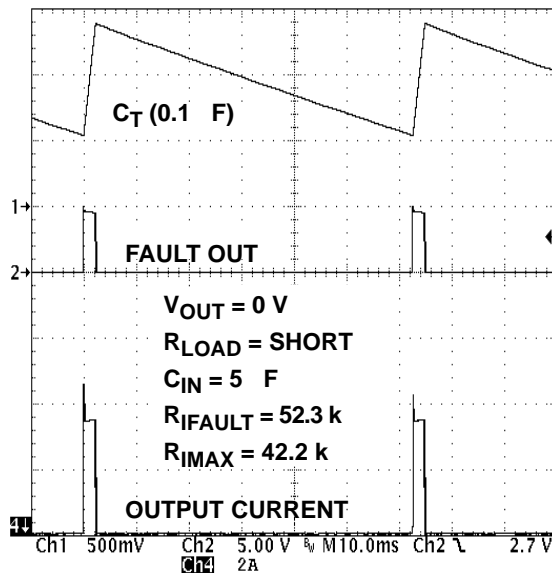


Figure 4

INRUSH CURRENT LIMITING

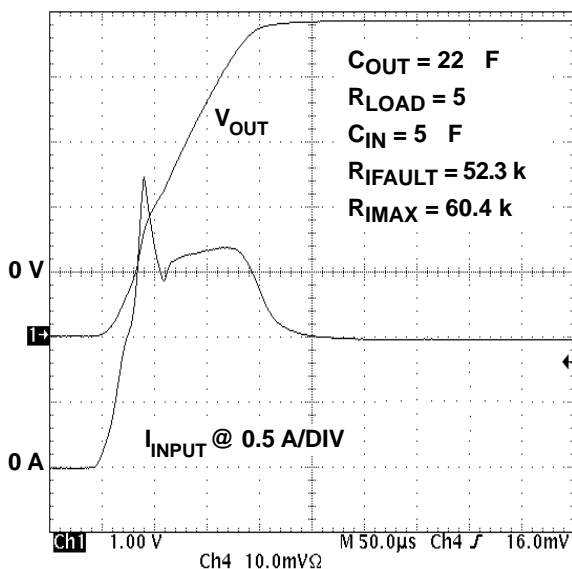


Figure 5

**FAULT AND OUTPUT TURN-OFF
DELAY FROM CT FAULT
THRESHOLD**

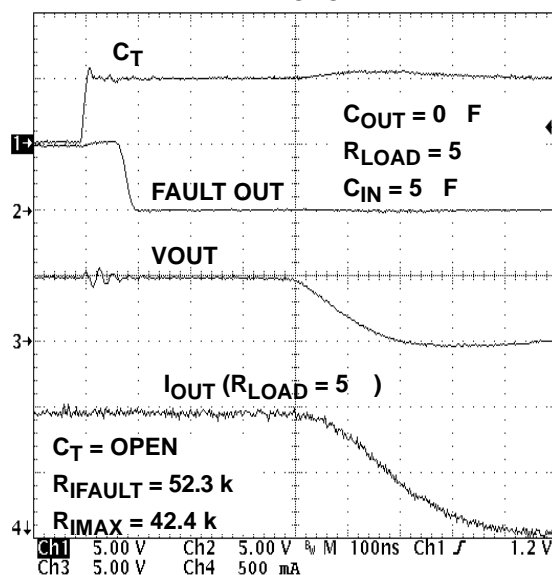


Figure 6

UCC3918 LOW ON-RESISTANCE HOT SWAP POWER MANAGER

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TYPICAL CHARACTERISTICS

PROPAGATION DELAY
SHUTDOWN TO FAULT AND
OUTPUT RAMP-DOWN

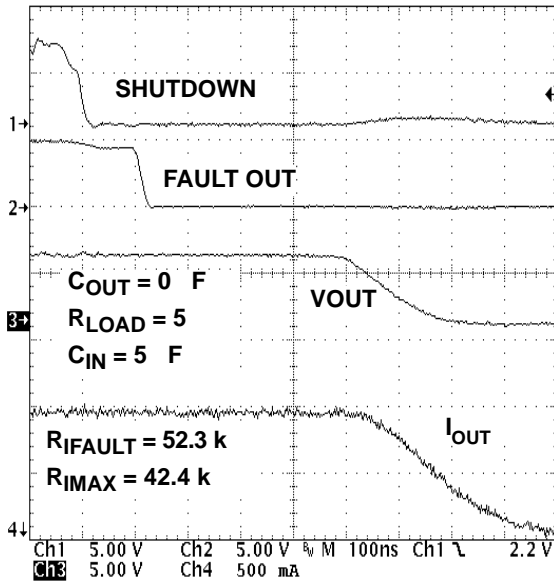


Figure 7

PROPAGATION DELAY
ENABLE TO FAULT AND
OUTPUT RAMP-UP

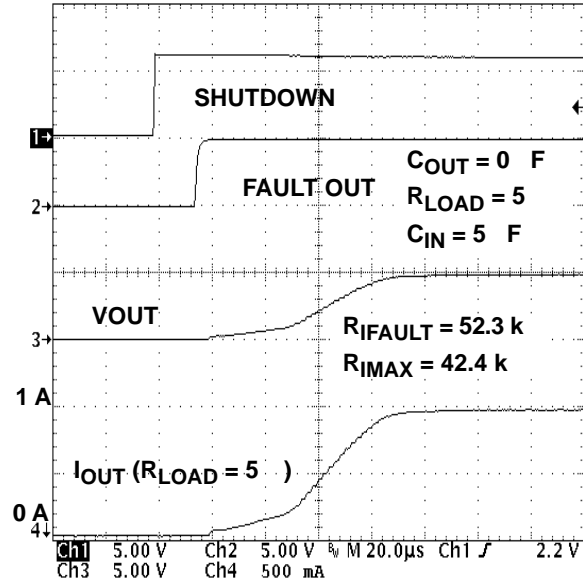


Figure 8

ON-STATE RESISTANCE
vs
OUTPUT CURRENT

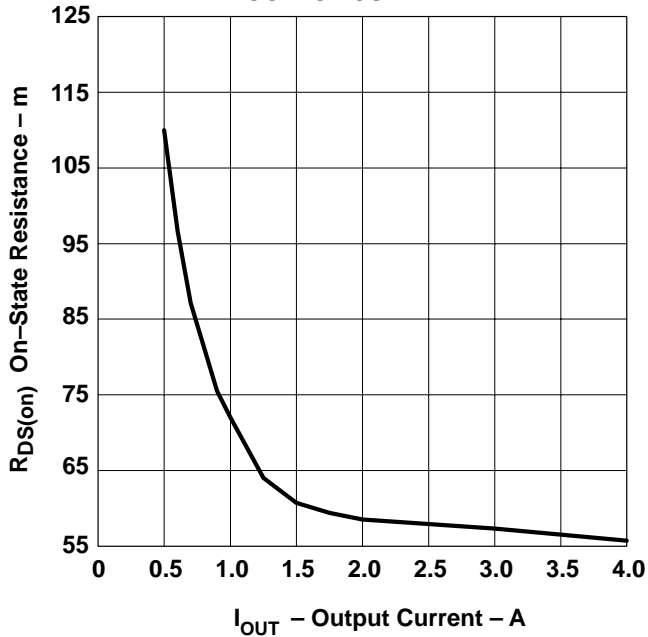


Figure 9

ON-STATE RESISTANCE
vs
TEMPERATURE

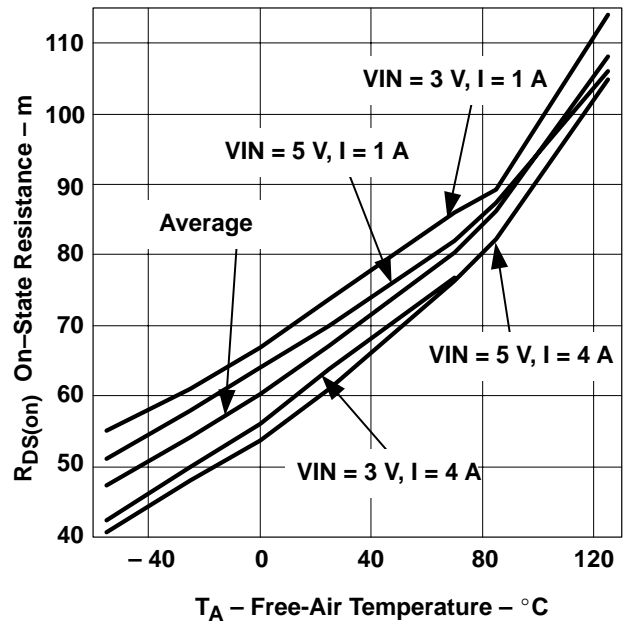


Figure 10

APPLICATION INFORMATION

safety considerations

Although the UCC3918 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UCC3918 is intended for use in safety critical applications where UL[®] or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the power device. The UCC3918 prevents the fuse from blowing for virtually all fault conditions, increasing system reliability and reducing maintenance cost, in addition to providing the hot swap benefits of the device.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC3918DP	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3918DP
UCC3918DP.A	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3918DP
UCC3918DPG4	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3918DP
UCC3918DPTR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3918DP
UCC3918DPTR.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3918DP

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC3918DPTR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC3918DPTR	SOIC	D	16	2500	353.0	353.0	32.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
UCC3918DP	D	SOIC	16	40	506.6	8	3940	4.32
UCC3918DP.A	D	SOIC	16	40	506.6	8	3940	4.32
UCC3918DPG4	D	SOIC	16	40	506.6	8	3940	4.32

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