UCC5714x-Q1 High-Speed, Low-Side Gate Drivers With Overcurrent Protection for Automotive Applications

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified
  - Device Temperature Grade 1
- Typical 3A sink 3A source output currents
- -250mV over current protection (OCP) threshold
- Single pin for fault output and enable
- Programmable fault clear time and over current detection response time
- Absolute maximum VDD voltage: 30V
- Tight UVLO threshold for bias flexibility
- Typical 26ns propagation delay
- Self-protected driver with thermal shutdown function at 180°C
- Available in 2.9mm x 1.6mm SOT-23 package
- Operating junction temperature range of –40°C to 150°C

2 Applications

- Digital controlled PFC
- Air conditioner
- Home appliances
- Motor drives
- General purpose low-side gate driver for single-ended topologies

3 Description

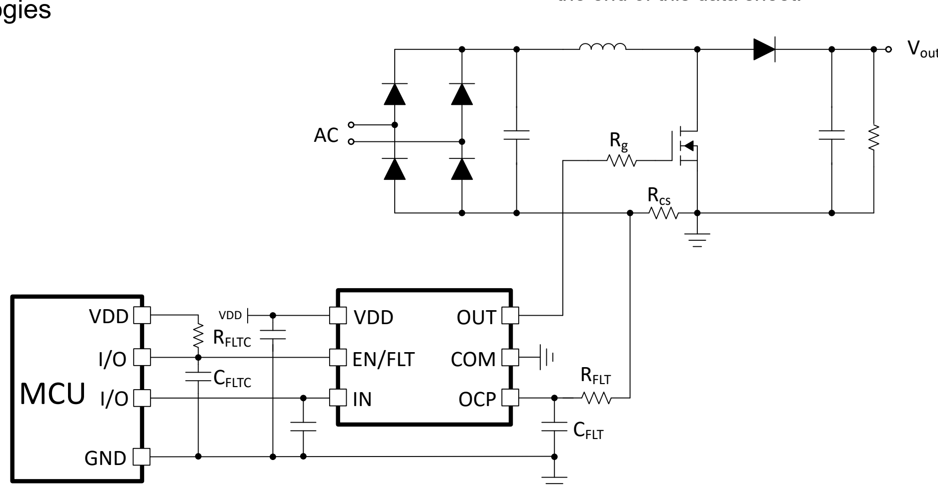
The UCC5714x-Q1 is a single channel, high-performance, low-side gate driver capable of effectively driving MOSFET, IGBT, and SiC power switches. The UCC5714x-Q1 has a typical peak drive strength of 3A.

The UCC5714x-Q1 provides overcurrent protection with the OCP pin. When the overcurrent signal is detected on the OCP pin, the internal circuit pulls down the EN/$\overline{FLT}$ pin to report a fault and force OUT to low stage. An external pullup circuit on the EN/$\overline{FLT}$ pin is required during normal operation of the driver. Pulling the EN/$\overline{FLT}$ pin low disables the driver. The EN/$\overline{FLT}$ pin also reports the undervoltage lock out (UVLO) fault on VDD and the overtemperature fault. The UCC5714x-Q1 provides both 8V and 12V UVLO options for SiC and IGBT applications.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
UCC57142-Q1	DBV (SOT-23 6)	2.90mm x 2.80mm
UCC57148-Q1	DBV (SOT-23 6)	2.90mm x 2.80mm

(1) For all available packages, see the orderable addendum at the end of this data sheet.



Simplified Application Diagram

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4 Pin Configuration and Functions

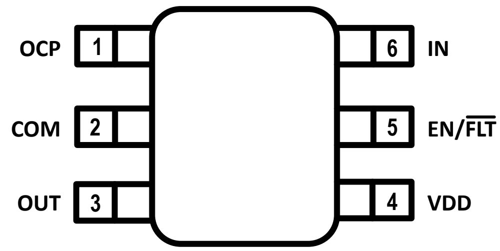


Figure 4-1. 6-Pin SOT-23 DBV Package (top view)

Table 4-1. Pin Functions

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
OCP	1	I	Current sense input
COM	2	G	Device ground
OUT	3	O	Output of the driver
VDD	4	P	Driver bias supply
EN/$\overline{\text{FLT}}$	5	I/O	Enable and fault report
IN	6	I	Input of the driver

(1) I/O = Digital input/output, I = Input, O= Output, P = Power connection, G=Ground

5 Specifications

5.1 Absolute Maximum Ratings

All the voltages are with respect to COM. Over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
VDD	Positive power supply	–0.3	30	V
OUT	Output signal DC voltage	COM–0.3	VDD+0.3	V
	Outout signal transient voltage for 200ns	COM–2	VDD+3	V
VOCP	Voltage at current sense pin (OCP)	–10	12	V
V_{IN}	IN signal DC voltage	–5	30	V
$V_{EN/\overline{FLT}}$	EN/$\overline{FLT}$ signal DC voltage	–0.3	30	V
T_J	Junction temperature	–40	150	℃
T_{stg}	Storage temperature	–65	150	℃

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 [1]	±2000	V
		Charged device model (CDM), per AEC Q100-011	±1000	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

All voltages are with reference to COM. Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Positive Power Supply (8V UVLO Option)	8.5		26	V
VDD	Positive Power Supply (12V UVLO Option)	14.5		26	V
V_{OUT}	Output Voltage	COM		VDD	V
V_{OCP}	Voltage at current sense pin	-5		10	V
V_{IN}	IN signal DC voltage	-2		26	V
$V_{EN/\overline{FLT}}$	EN signal DC voltage	0		26	V
T_J	Junction temperature	–40		150	℃

5.4 Thermal Information

THERMAL METRIC[1]		UCC5713x	UNIT
		D	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	126.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	75.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	15.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	74.8	°C/W

5.4 Thermal Information (continued)

THERMAL METRIC[(1)]		UCC5713x D 8 PINS	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	na	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

VDD = 15V, 1µF capacitor from VDD to COM, TJ = –40°C to +150°C, CL = 0pF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS						
I_{VDDQ}	VDD quiescent supply current	V_{IN} = 3.3V, EN = 5V, VDD = 6.5V			1.3	mA
I_{VDD}	VDD static supply current	V_{IN} = 3.3V, EN = 5V		0.7	1.5	mA
I_{VDD}	VDD static supply current	V_{IN} = 0V, EN = 5V		0.7	1.1	mA
I_{VDDO}	VDD dynamic operating current	f_{SW} = 1MHz, EN = 5V, VDD=15V, C_L=1.8nF			30	mA
I_{DIS}	VDD disable current	V_{IN} = 3.3V, EN = 0V		0.8	1.1	mA
VDD UNDERVOLTAGE THRESHOLDS AND DELAY						
V_{VDD_ON}	VDD UVLO Rising Threshold	8V UVLO Option	7.65	8	8.35	V
V_{VDD_OFF}	VDD UVLO Falling Threshold		6.65	7	7.35	V
V_{VDD_HYS}	VDD UVLO Threshold Hysteresis			1		V
$t_{UVLO2FLT}$	Propagation delay from UVLO to $\overline{FLT}$			2		µs
V_{VDD_ON}	VDD UVLO Rising Threshold	12V UVLO Option	12.8	13.5	14.2	V
V_{VDD_OFF}	VDD UVLO Falling Threshold		11.8	12.5	13.2	V
V_{VDD_HYS}	VDD UVLO Threshold Hysteresis			1		V
IN, EN/$\overline{FLT}$						
V_{INH}	Input High Threshold Voltage		1.8	2.2	2.6	V
V_{INL}	Input Low Threshold Voltage		0.8	1.2	1.6	V
V_{IN_HYS}	Input-threshold Hysteresis			1		V
R_{IND}	IN Pin Pull Down Resistance			115		kΩ
V_{ENH}	Enable High Threshold Voltage		1.8	2.2	2.6	V
V_{ENL}	Enable Low Threshold Voltage		0.8	1.2	1.6	V
V_{EN_HYS}	Enable Threshold Hysteresis			1		V
R_{ENU}	EN Pin Pull Up Resistance			2		MΩ
$I_{\overline{FLT}th}$	$\overline{FLT}$ threshold	$V_{\overline{FLT}\text{-sink}}$ = 400mV, Tj=25°C	18			mA
OC DETECTION						
t_{OCFIL} [(1)]	OC deglitch filter (8V-UVLO version)			70		ns
t_{OCFIL} [(1)]	OC deglitch filter (12V-UVLO version)			190		ns
t_{OC2OUT} [(1)]	OC propagation delay to 90% of OUT (8V-UVLO version)			115	145	ns
t_{OC2OUT} [(1)]	OC propagation delay to 90% of OUT (12V-UVLO version)			230	350	ns
t_{OC2FLT} [(1)]	OC propagation delay to 90% of EN/$\overline{FLT}$ low(8V-UVLO version)			115	150	ns
t_{OC2FLT} [(1)]	OC propagation delay to 90% of EN/$\overline{FLT}$ low(12V-UVLO version)			220	320	ns

5.5 Electrical Characteristics (continued)

VDD = 15V, 1µF capacitor from VDD to COM, TJ = –40°C to +150°C, CL = 0pF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OCLEB} (1)	OC Leading edge blanking time(8V-UVLO version)			60	80	ns
t_{OCLEB} (1)	OC Leading edge blanking time(12V-UVLO version)			180	250	ns
OVERTEMPERATURE PROTECTION						
T_{SD} (1)	Overtemperature threshold			180		℃
T_{HYS} (1)	Overtemperature protection hysteresis			30		℃
$t_{OTP2FLT}$ (1)	Propagation delay from overtemperature shutdown to $\overline{FLT}$	Over temperature shutdown to 90% of $\overline{FLT}$, Cl=10pF		8		us
OUTPUT DRIVER STAGE						
I_{SRCPK} (1)	Peak Output Source Current	C_{VDD} = 10µF, C_L = 0.1µF, f = 1kHz		-3		A
I_{SNKPK} (1)	Peak Output Sink Current	C_{VDD} = 10µF, C_L = 0.1µF, f = 1kHz		3		A
R_{OH}	Pull up resistance	I_{OUT} = –500mA		5		Ω
R_{OL}	Pull down resistance	I_{OUT} = 50mA		1		Ω

(1) Parameter are not tested in production

5.6 Switching Characteristics

VDD = 15V, 1µF capacitor from VDD to COM, TJ = –40°C to +150°C, CL = 0pF, unless otherwise noted. (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_R	Output Rise Time	C_L=1.8nF, 10% to 90%, Vin = 0 to 3.3V		8	18	ns
t_F	Output Fall Time	C_L=1.8nF, 90% to 10%, Vin = 0 to 3.3V		14	32	ns
t_{D2}	Propagation Delay – Input falling to output falling	C_L=1.8nF, from 1V falling on Vin to 90% of output fall, Vin=0 - 3.3V, Fsw=500kHz, 50% duty cycle		28	50	ns
t_{D1}	Propagation Delay – Input rising to output rising	C_L=1.8nF, from 2V rising on Vin to 10% of output rise, Vin=0 - 3.3V, Fsw=500kHz, 50% duty cycle		26	50	ns
t_{PD_DIS}	DIS Response Delay	C_L=1.8nF, from 1V falling on EN to 90% of output fall, EN=0 - 3.3V		27	45	ns
t_{PWD}	Pulse Width Distortion	Input Pulse Width = 100ns, 500kHz $\lvert t_{D2\_1} - t_{D1\_1} \rvert$	-10		10	ns

(1) Switching parameters are not tested in production.

5.7 Timing Diagram

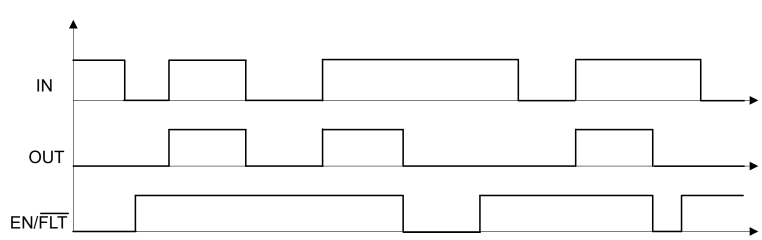
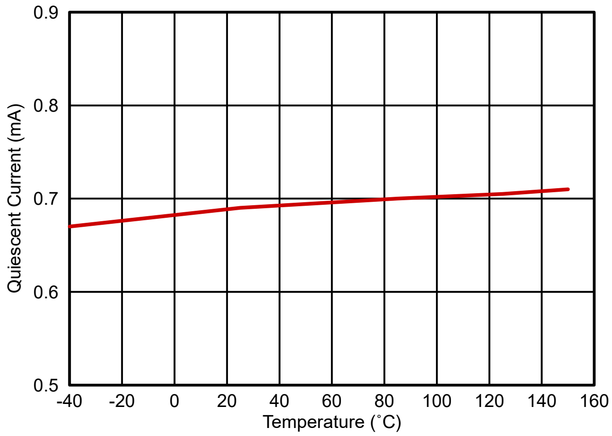


Figure 5-1. Input/Output/Enable Timing Diagram, IN = PWM

5.8 Typical Characteristics

Unless otherwise specified, VDD=15V, IN=3.3V, EN=5V, T_J = 25 °C, No load



V_{DD} = 6.5V

Figure 5-2. Quiescent Current

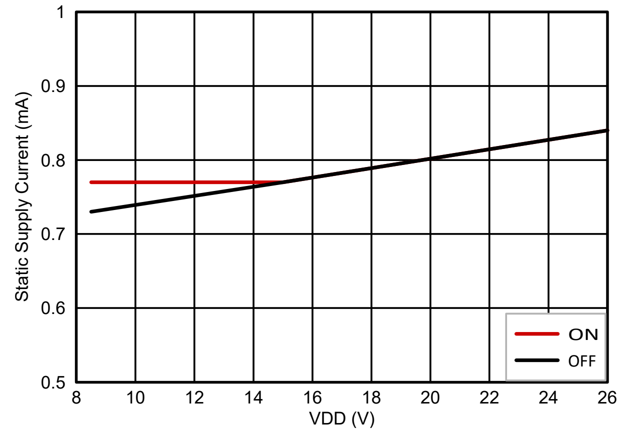


Figure 5-3. Operating Static Supply Current

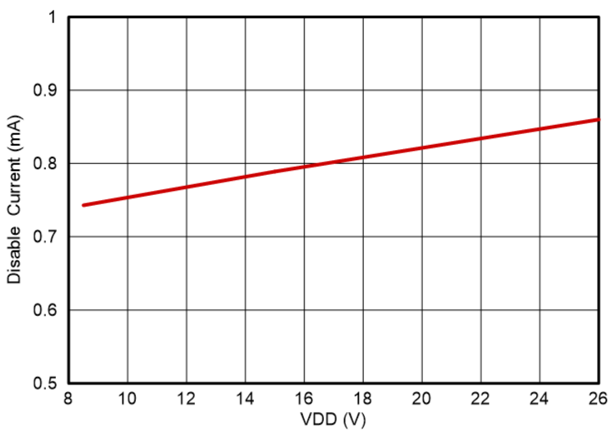
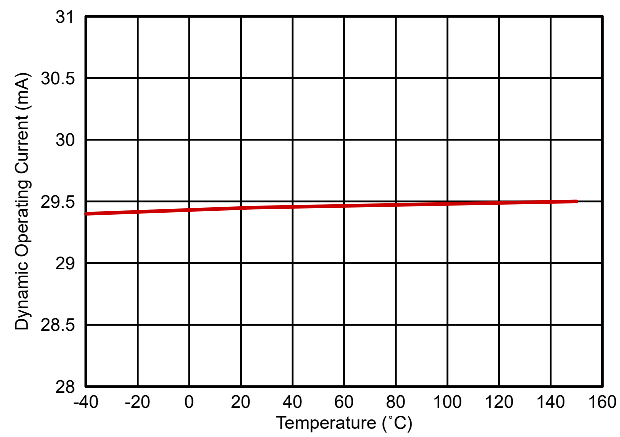


Figure 5-4. Disable Current



C_{LOAD} = 1.8nF

Figure 5-5. Operating Supply Current

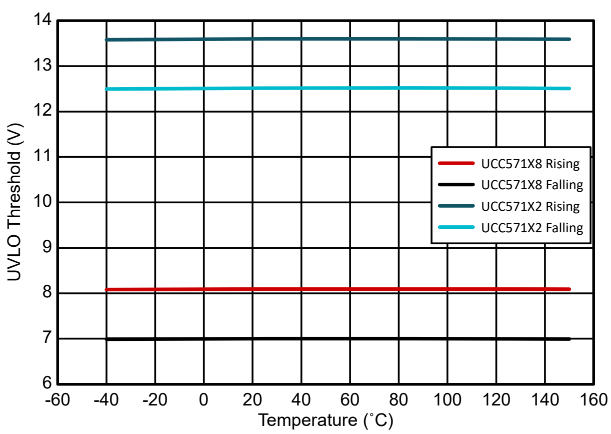


Figure 5-6. UVLO Threshold

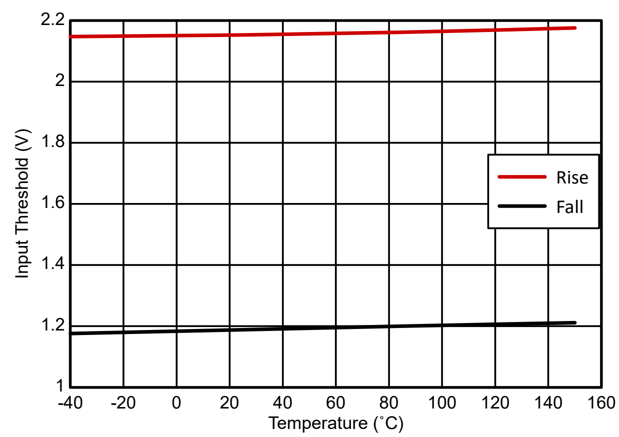


Figure 5-7. Input Threshold

5.8 Typical Characteristics (continued)

Unless otherwise specified, VDD=15V, IN=3.3V, EN=5V, T_J = 25 °C, No load

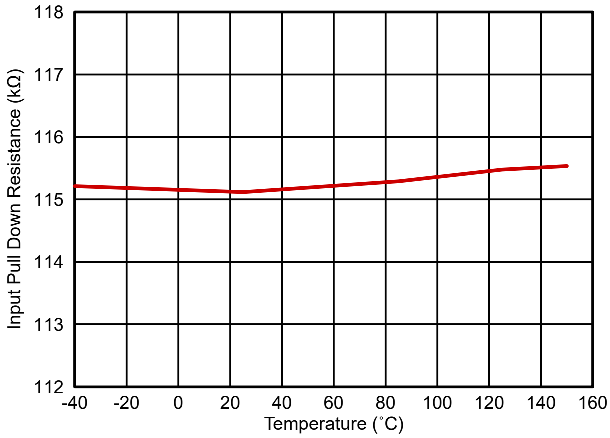


Figure 5-8. Input Pulldown Resistance

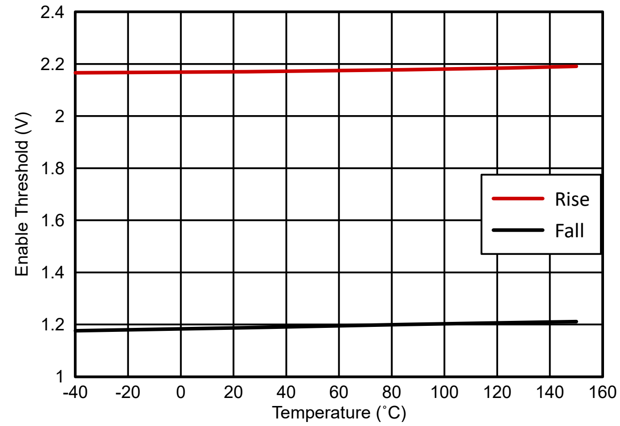


Figure 5-9. Enable Threshold

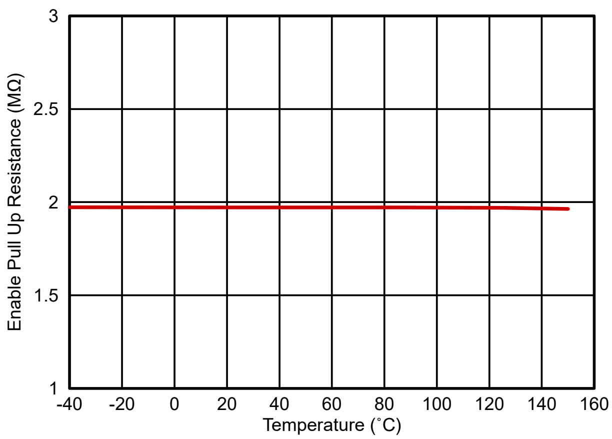


Figure 5-10. Enable Pullup Resistance

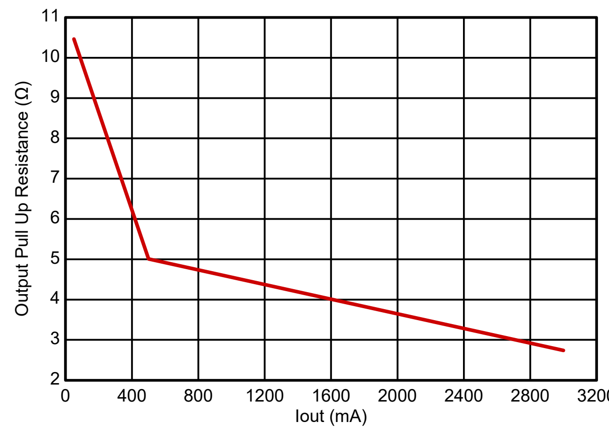


Figure 5-11. Output Pullup Resistance vs VDD

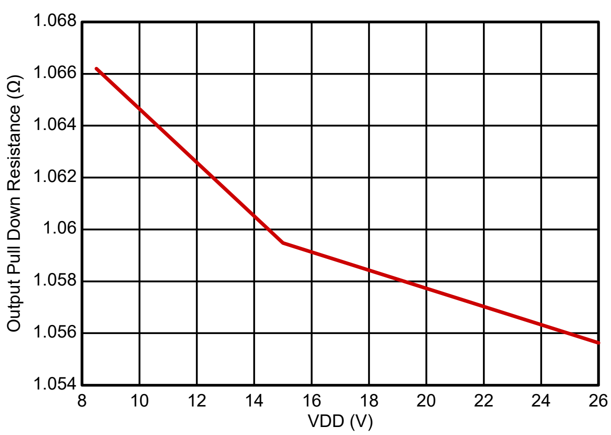


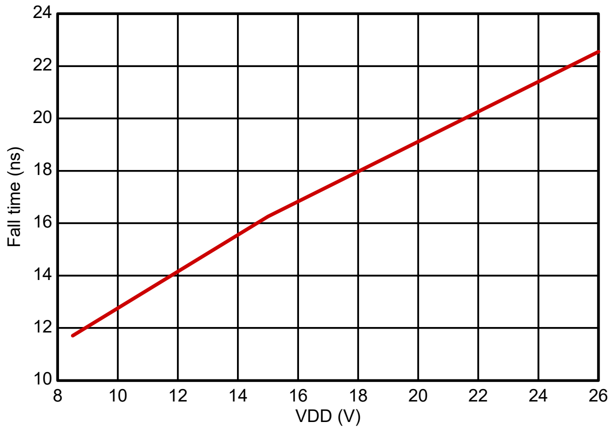
Figure 5-12. Output Pulldown Resistance

C_{LOAD} = 1.8nF

Figure 5-13. Output Rise Time

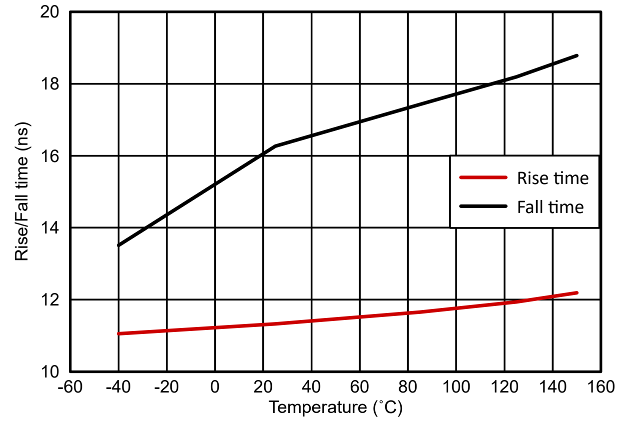
5.8 Typical Characteristics (continued)

Unless otherwise specified, VDD=15V, IN=3.3V, EN=5V, T_J = 25 °C, No load



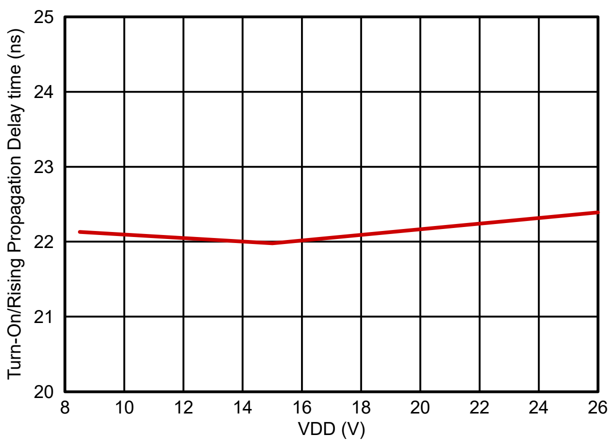
C_{LOAD} = 1.8nF

Figure 5-14. Output Fall Time



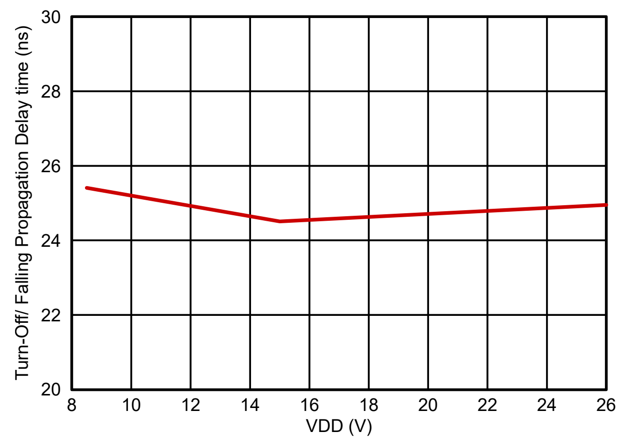
C_{LOAD} = 1.8nF

Figure 5-15. Output Rise and Fall Time



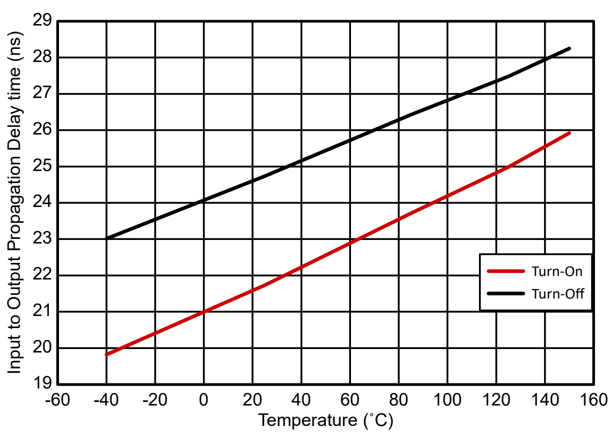
C_{LOAD} = 1.8nF

Figure 5-16. Input to Output Rising (Turnon) Propagation Delay



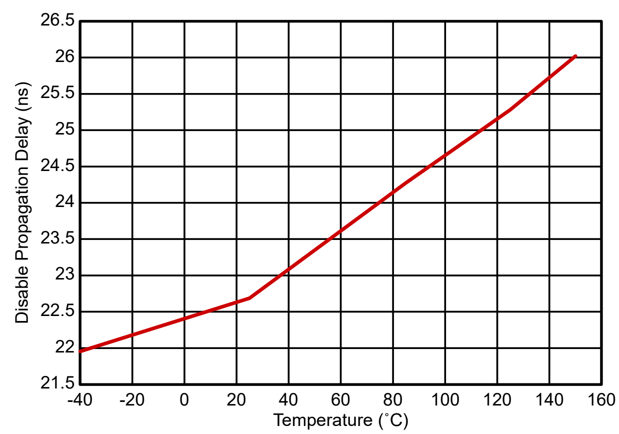
C_{LOAD} = 1.8nF

Figure 5-17. Input to Output Falling (Turnoff) Propagation Delay



C_{LOAD} = 1.8nF

Figure 5-18. Input Propagation Delay



C_{LOAD} = 1.8nF

Figure 5-19. Disable Propagation Delay

5.8 Typical Characteristics (continued)

Unless otherwise specified, VDD=15V, IN=3.3V, EN=5V, T_J = 25 °C, No load

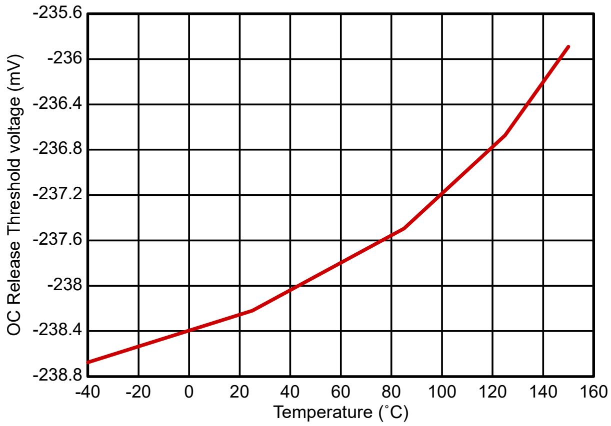


Figure 5-20. OC Threshold

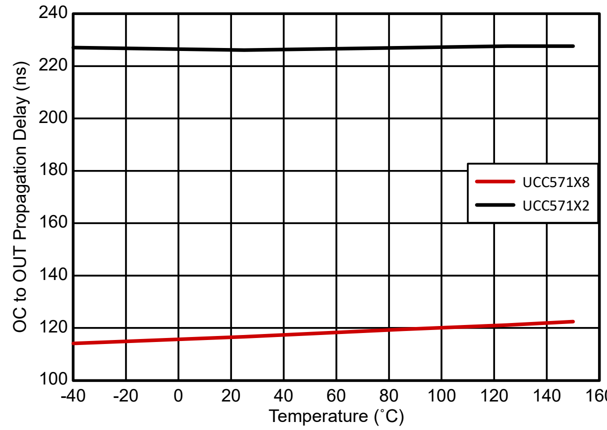


Figure 5-21. OC to Output Propagation Delay

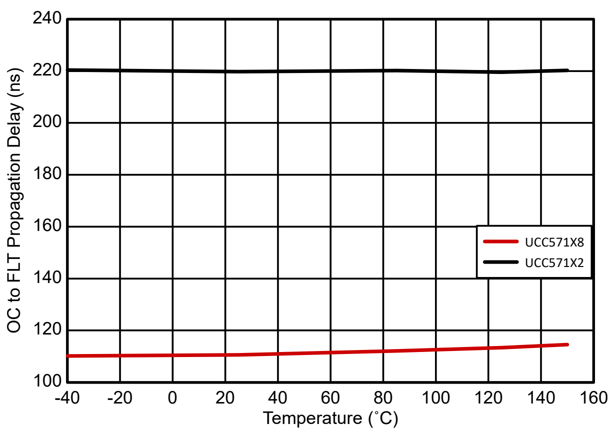
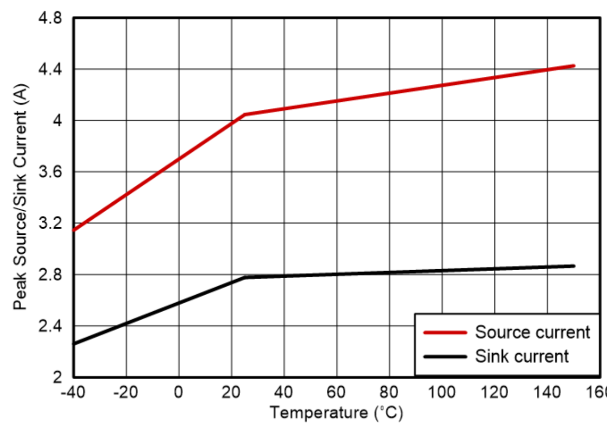


Figure 5-22. OC to Fault Propagation Delay



C_{LOAD} = 1µF

Figure 5-23. Peak Source and Sink Current

6 Detailed Description

6.1 Overview

The UCC5714x-Q1 device is a single-channel, high-speed, gate driver capable of effectively driving MOSFET, SiC, and IGBT power switches with 3A source and 3A sink (symmetrical drive) peak currents. The driver has a good transient handling capability on its output, as well as rail-to-rail drive capability and a small propagation delay, typically 26ns. The device has an overcurrent detection and fault reporting function to the low voltage side DSP/MCU. When the overcurrent signal is detected on the OCP pin, the internal circuit pulls down the EN/$\overline{FLT}$ pin to report a fault and force OUT to low stage.

The input threshold of the UCC5714x-Q1 is compatible to TTL low-voltage logic, which is fixed and independent of VDD supply voltage. The driver can also work with CMOS based controllers as long as the threshold requirement is met. The 1V typical hysteresis offers noise immunity.

External pullup circuit on the EN/$\overline{FLT}$ pin is required during normal operation of the driver. Pulling EN/$\overline{FLT}$ low disables the driver. EN/$\overline{FLT}$ also reports the undervoltage lockout (UVLO) fault on VDD and the overtemperature fault.

6.2 Functional Block Diagram

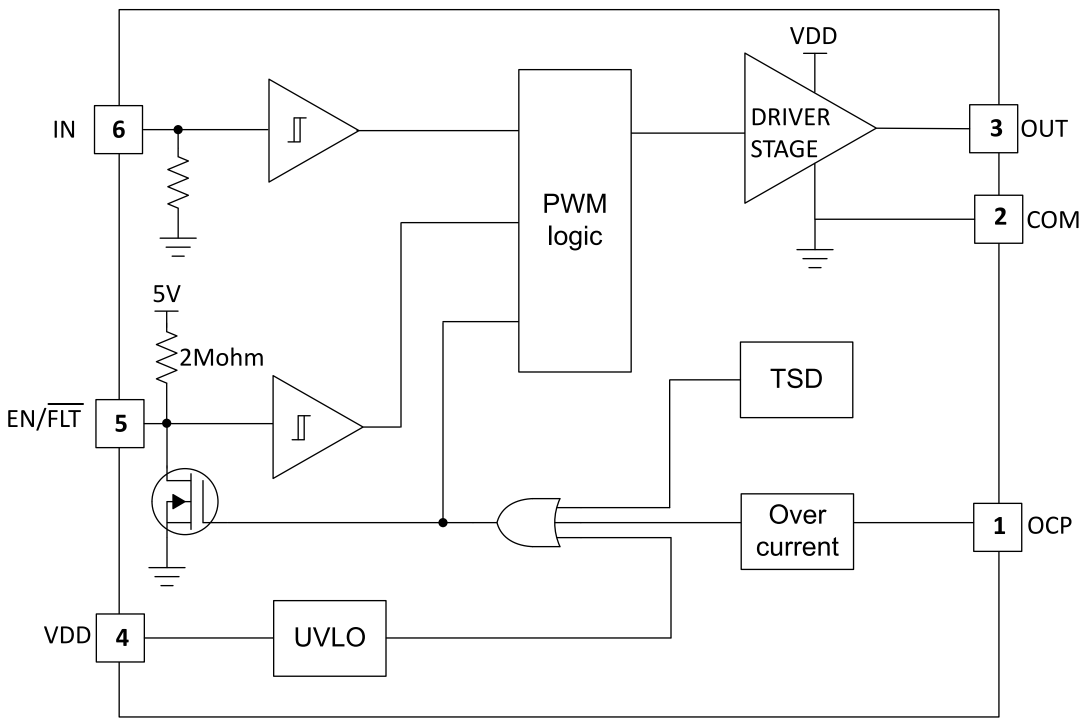


Figure 6-1. UCC5714x-Q1 Simplified Functional Block Diagram

6.3 Feature Description

6.3.1 Input Stage

The inputs of the UCC5714x-Q1 device are compatible with TTL based threshold logic and the inputs are independent of the VDD supply voltage. Wider hysteresis (typically 1V) offers enhanced noise immunity compared to traditional TTL logic implementations. This device also features tight control of the input pin threshold voltage levels which eases system design considerations and ensures stable operation across temperature.

The device features an important protection function wherein, whenever the input pin is in a floating condition, the output is held in the low state. This is achieved with internal pulldown resistors on the input pins as shown in the simplified functional block diagrams. In some applications, due to difference in bias supply sequencing, different ICs power-up at different times. This may cause output of the controller to be in tri-state. This output of the controller gets connected to the input of the driver IC. If the driver IC does not have a pulldown resistor then the output of the driver may go high erroneously and damage the switching power device.

The input stage of the driver should preferably be driven by a signal with a short rise or fall time. Caution must be exercised whenever the driver is used with slowly varying input signals, especially in situations where the device is located in a separate daughter board or PCB layout has long input connection traces:

- High dI/dt current from the driver output coupled with board layout parasitics can cause ground bounce. Because the device features just one COM pin which may be referenced to the power ground, this may interfere with the differential voltage between Input pins and COM and trigger an unintended change of output state. Because of fast 26ns propagation delay, this can ultimately result in high-frequency oscillations, which increases power dissipation and poses risk of damage.
- 1V Input threshold hysteresis boosts noise immunity compared to most other industry standard drivers.

An external resistance is highly recommended between the output of the driver and the power device instead of adding delays on the input signal. This also limits the rise or fall times to the power device which reduces the EMI. The external resistor has the additional benefit of reducing part of the gate charge related power dissipation in the gate driver device package and transferring it into the external resistor itself.

Finally, because of the unique input structure that allows negative voltage capability on the input caution must be used and limit the input pin slew rate less than 1V/ns.

6.3.2 Enable/Fault (EN/$\overline{\text{FLT}}$)

The EN/$\overline{\text{FLT}}$ pin of the UCC5714x-Q1 can report a fault signal to the DSP/MCU with the adjustable fault clear time. When a fault is detected through the OCP pin, internal TSD, or the UVLO, the EN/$\overline{\text{FLT}}$ pin is pulled down to COM internally. The EN/$\overline{\text{FLT}}$ pin will stay low until the fault is removed and the internal pulldown FET turns off, the voltage on the pin charged up with external pull-up voltage. The t_{FLTC} is determinded by the exponential charging characteristics of the capacitor where the time constant is set by R_{FLTC} and C_{FLTC} as shown in Simplified Application Diagram, the R_{FLTC} is pulled up to external VDD. C_{FLTC} is connected from EN/$\overline{\text{FLT}}$ to COM. EN/$\overline{\text{FLT}}$is weakly pulled up to 5V internally through a R_{ENU}. The t_{FLTC} can be calculated by the folumla below if it is pullup to 5V rail.

$$t_{FLTC} = -\left(\frac{R_{FLTC} \times R_{ENU}}{R_{FLTC} + R_{ENU}}\right) \times C_{FLTC} \times \ln\left(1 - \frac{V_{ENH}}{V_{DD}}\right) \quad (1)$$

The UCC5714x-Q1 provides an enable function that can allow shutdown or enable the output. When the EN/$\overline{\text{FLT}}$ is pulled up above the V_{ENH}, the output is following IN, when it is pulled down below V_{ENL}, the output will stay low. The relationship for input, output and enable can be found in Timing Diagram.

6.3.3 Driver Stage

The device has a ±3A peak drive strength and is suitable for driving Si MOSFET/ IGBT/SiC. The driver features an important safety function wherein, when the input pins are in a floating condition, the output is held in the LOW state. The driver has rail-to-rail output by implementing an NMOS pullup with intrinsic bootstrap gate drive. Under DC conditions, a PMOS is used to keep OUT tied to VDD as shown in the following figure. The low pullup impedance of the NMOS results in strong drive strength during the turn-on transient, which shortens the charging time of the input capacitance of the power semiconductor and reduces the turn on switching loss.

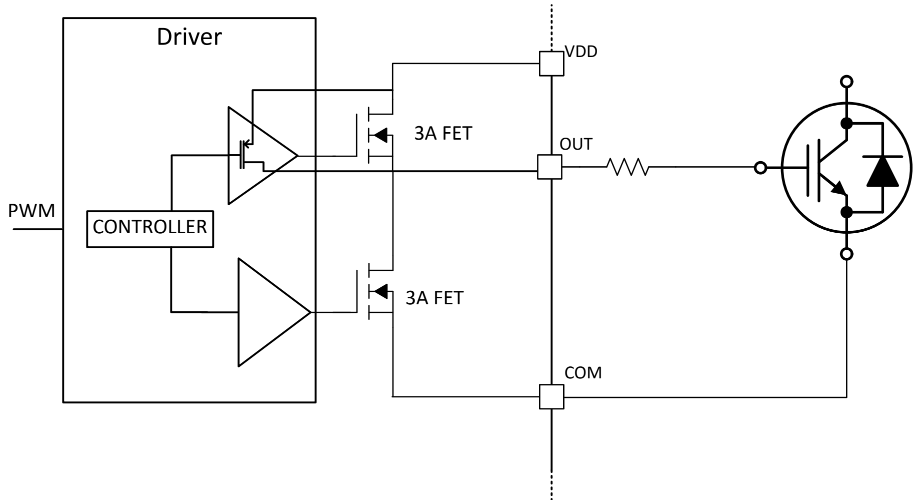


Figure 6-2. Gate Driver Output Stage

6.3.4 Overcurrent (OC) Protection

The UCC5714x-Q1 implements a fast overcurrent protection feature to protect the MOSFET/IGBT from catastrophic breakdown during a fault throught the OCP pin. The voltage at OCP pin sensed the negative voltage drop across the system sense resistor. The pin can handle up to -10V negative DC voltage. The relationship for input, output and enable can be found in OC Protection Timing Diagram shows the typical operating conditions for the OC protection. The device features an internal leading edge blanking time t_{OCLEB} that is actived at eaching raising edge of the input. During the t_{OCLEB}, the driver will disable overcurrent fault detection. For noisy systems, additional RC filter is recommended to avoid the false fault report. After the device exits t_{OCLEB} and the OCP pin voltage is above V_{OCTH}, the OUT will go low after t_{OC2OUT} and the EN/$\overline{FLT}$ will be pulled down. Once the OCP pin voltage goes above V_{OCTL}, the EN/$\overline{FLT}$ is pulled up and the OUT stays low until the next input raising edge.

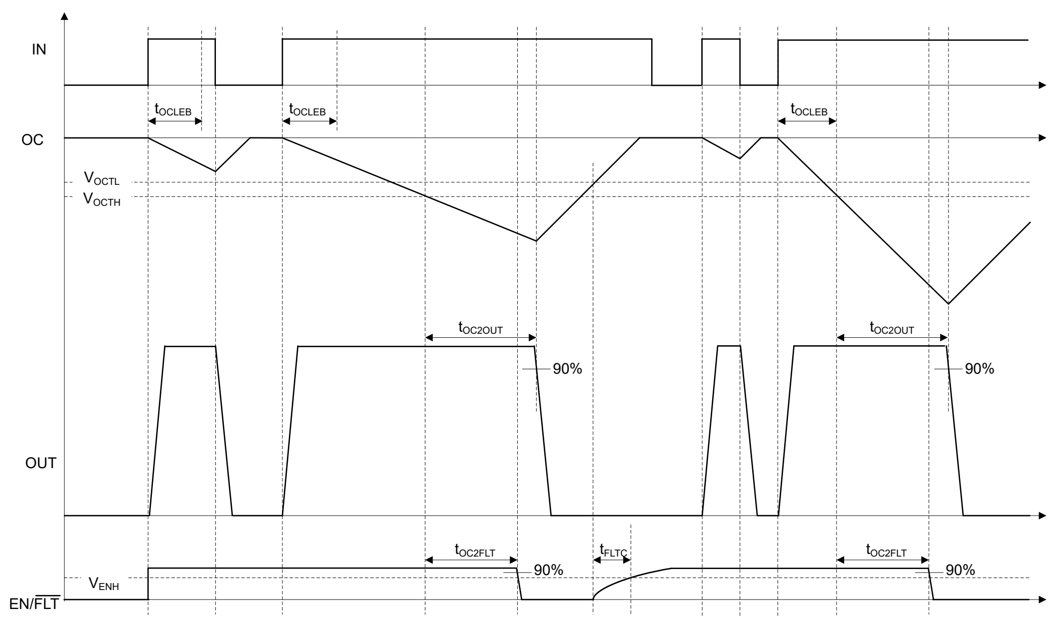


Figure 6-3. OC Protection Timing Diagram

6.3.5 Thermal Shutdown

The UCC5714x-Q1 device provides a thermal shutdown function that can protect the driver when the internal temperature goes above the threshold. When the device exceeds the overtemperature threshold, the EN/$\overline{FLT}$ is pulled low after the $t_{OTP2FLT}$ propagation delay. The device activates again once the temperature falls below the threshold after t_{FLTC} .

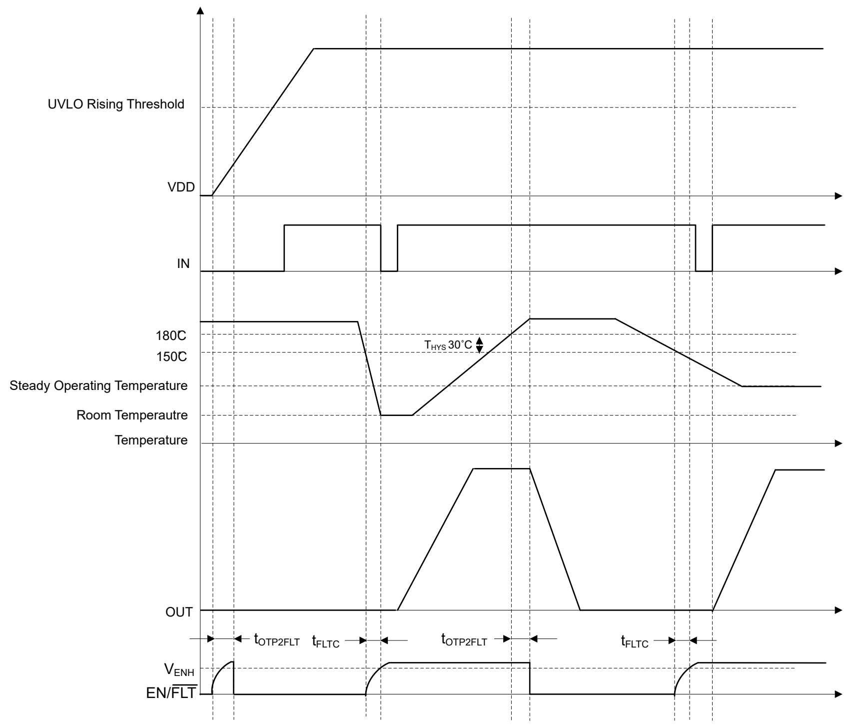


Figure 6-4. Thermal Shutdown Timing Diagram

6.4 Device Functional Modes

The UCC5714x-Q1 devices operate in normal mode and UVLO mode (see Section 7.2.1.2.1 for information on UVLO operation). In normal mode, the table below shows the output state in different states of the device and the input pins.

Table 6-1. UCC5714x-Q1 Truth Table

IN	EN/$\overline{FLT}$	OCP (1)	UVLO (2)	INTERNAL TSD (3)	OUT
H	H	L	L	L	H
L	H	L	L	L	L
Any	L	H	Any	Any	L
Any	L	Any	H	Any	L
Any	L	Any	Any	H	L

(1) H refers to the over current protection being triggered.
(2) H refers to the UVLO protection being triggered.
(3) H refers to the thermal shutdown protection being triggered.

7 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

High-current gate driver devices are required in switching power applications for a variety of reasons. To enable fast switching of power devices and reduce associated switching power losses, a powerful gate driver can be employed between the PWM output of controllers or signal isolation devices and the gates of the power semiconductor devices. Further, gate drivers are indispensable when sometimes it is just not feasible to have the PWM controller directly drive the gates of the switching devices. The situation will be often encountered because the PWM signal from a digital controller or signal isolation device is often a 3.3V or 5V logic signal which is not capable of effectively turning on a power switch. A level-shifting circuitry is needed to boost the logic-level signal to the gate-drive voltage in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar, (or P- N-channel MOSFET), transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate for this because they lack level-shifting capability and low-drive voltage protection. Gate drivers effectively combine both the level-shifting, buffer drive and UVLO functions. Gate drivers also find other needs such as minimizing the effect of switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses into itself.

The UCC5714x-Q1 is very flexible in this role with a strong drive current capability and wide recommended supply voltage range from UVLO to 26V. This allows the driver to be used in 5V bias logic level very high frequency MOSFET applications.

These requirements, coupled with the need for low propagation delays and availability in compact, and low-inductance packages with good thermal capability, make gate driver devices such as the UCC5714x-Q1 extremely important components in switching power combining benefits of high-performance, low cost, low component count, board space reduction and simplified system design.

7.2 Typical Application

7.2.1 Driving MOSFET/IGBT/SiC MOSFET

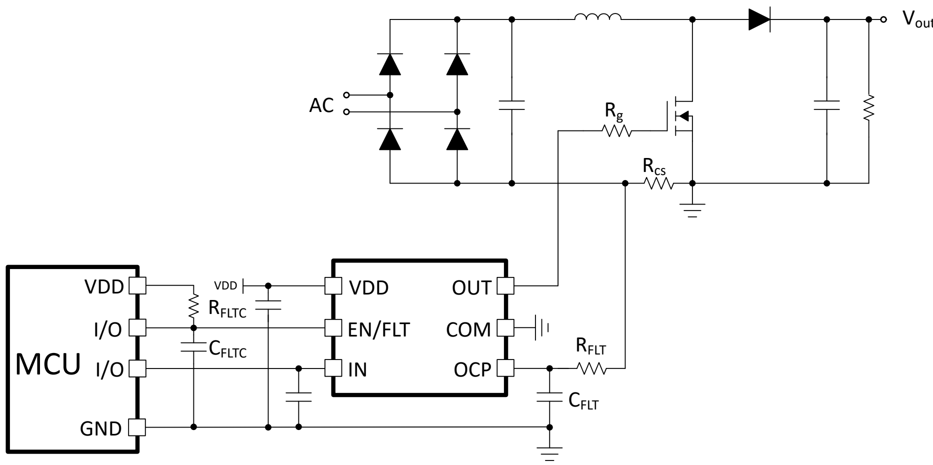


Figure 7-1. Driving a MOSFET/IGBT/SiC MOSFET in a Boost Converter

7.2.1.1 Design Requirements

When selecting the gate driver device for an end application, some design considerations must be evaluated in order to make the most appropriate selection. Following are some of the design parameters that should be used when selecting the gate driver device for an end application: input-to-output configuration, the input threshold type, bias supply voltage levels, peak source and sink currents, availability of independent enable and disable functions, propagation delay, power dissipation, and package type. See the example design parameters and requirements in Table 7-1.

Table 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input to output logic	Noninverting
Input threshold type	TTL
Bias supply voltage levels	+18V
Enable function	Yes
Disable function	N/A
Propagation delay	<30ns
Power dissipation	<1W
Package type	SOT-23

7.2.1.2 Detailed Design Procedure

7.2.1.2.1 VDD Undervoltage Lockout

The UCC57142-Q1 device provides an undervoltage lockout threshold of 12V and the UCC57148-Q1 device provides an undervoltage lockout threshold of 8V. The UVLO hysteresis range helps to avoid any chattering due to the presence of noise on the bias supply. 1V of typical UVLO hysteresis is expected. 2µs of turnon delay is expected due to the UVLO feature during startup or when the supply voltage exceeds the rising thresholds. The UVLO turn-off delay is also minimized as much as possible to 3µs maximum. The UVLO delay is designed to minimize chattering that may occur due to very fast transients that may appear on VDD. When the bias supply is below UVLO thresholds, the outputs are held actively low irrespective of the state of the input pins. When exiting the UVLO, the EN/$\overline{FLT}$ is charged by external pullup circuit. The fault clear time is depended on the time constant of the R_{FLTC} and C_{FLTC}. After exit the UVLO longer than the fault clear time and UVLO turn on delay, the OUT follow the IN after the first rising edge of the IN.

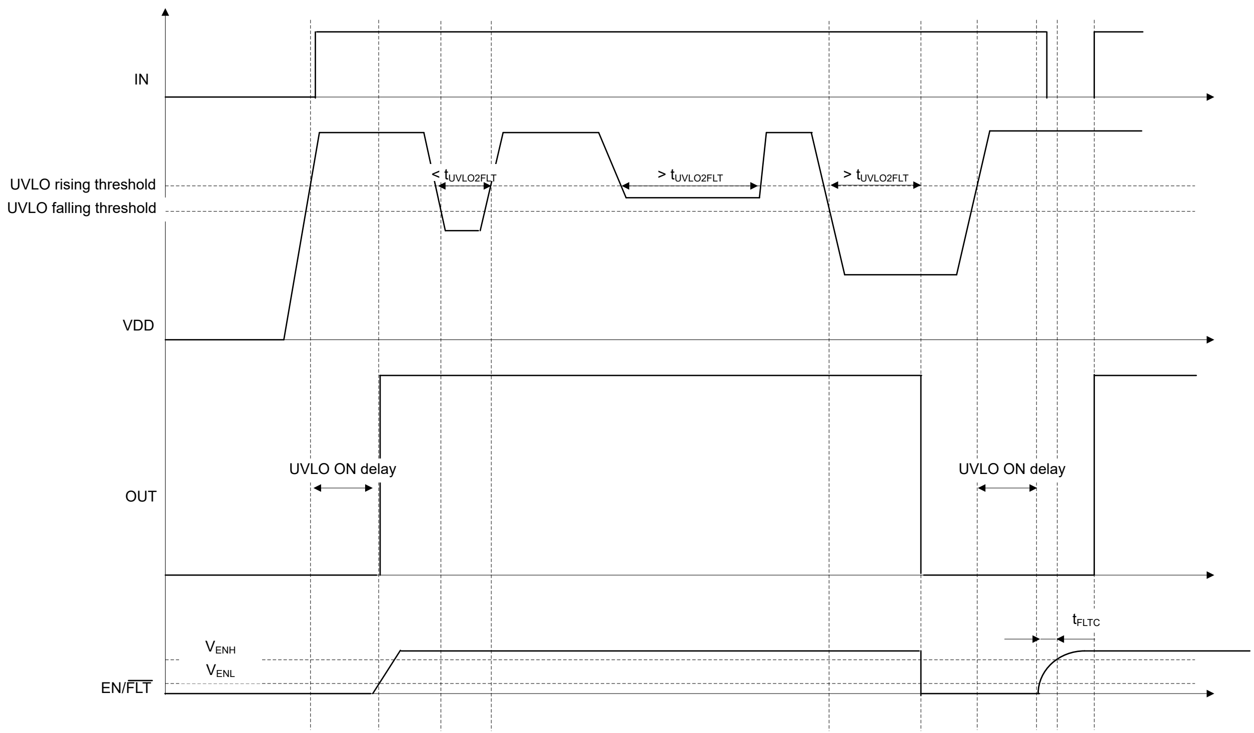


Figure 7-2. UVLO Timing Diagram

7.2.1.2.2 Power Dissipation

Power dissipation of the gate driver has two portions as shown in equation below:

$$P_{DISS} = P_{DC} + P_{SW} \tag{2}$$

The DC portion of the power dissipation is P_{DC} = I_Q× VDD where I_Q is the quiescent current for the driver. The quiescent current is the current consumed by the device to bias all internal circuits such as input stage, reference voltage, logic circuits, protections,and so on, and any current associated with switching of internal devices when the driver output changes state (such as charging and discharging of internal parasitic capacitances, parasitic shoot-through). The UCC5714x-Q1 contains internal logic to minimize any shoot-through (PMOS to NMOS and vice versa) in the output driver stage. Thus, the effect of the P_{DC} on the total power dissipation within the gate driver can be assumed to be negligible. In practice this is the power consumed by driver when its output is disconnected from the gate of power switch.

As explained in earlier sections, the output stage of the gate driver is based on PMOS and NMOS. These NMOS and PMOS are designed in such a way that they offer very low resistance during switching. And therefore they have very low drop-out. The power dissipated in the gate driver package during switching (P_{SW}) depends on the following factors:

- Gate charge required of the power device (usually a function of the drive voltage V_G, which is very close to input bias supply voltage VDD due to low V_{Ox} drop-out)
- Switching frequency
- Power MOSFET internal and external gate resistor

When a driver device is tested with a discrete, capacitive load it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by:

$$E_G = \frac{1}{2} C_{LOAD} V_{DD}^2 \tag{3}$$

where

- C_{LOAD} is load capacitor and V_{DD} is bias voltage feeding the driver.

There is an equal amount of energy dissipated when the capacitor is discharged. During turnoff the energy stored in capacitor is fully dissipated in drive circuit. This leads to a total power loss during switching cycle given by the following:

$$P_G = C_{LOAD} V_{DD}^2 f_{sw} \quad (4)$$

where

- f_{SW} is the switching frequency

The switching load presented by a power FET and IGBT can be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications of typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_g, one can determine the power that must be dissipated when charging a capacitor. This is done by using the equivalence, $Q_g = C_{LOAD}V_{DD}$, to provide the following equation for power:

$$P_G = C_{LOAD} V_{DD}^2 f_{sw} = Q_g V_{DD} f_{sw} \quad (5)$$

This power P_G is dissipated in the resistive elements of the circuit when the MOSFET and IGBT is being turned on or off. Half of the total power is dissipated when the load capacitor is charged during turnon, and the other half is dissipated when the load capacitor is discharged during turn-off. When no external gate resistor is employed between the driver IC and MOSFET/IGBT, this power is completely dissipated inside the driver IC. With the use of external gate drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor in accordance to the ratio of the resistances (more power dissipated in the higher resistance component). Based on this simplified analysis, the driver power dissipation during switching is calculated as shown in following equation. This primarily applies to those applications where total external gate resistor is significantly large to limit the peak current of the gate driver.

$$P_{SW} = 0.5 \times Q_g \times V_{DD} \times f_{sw} \left(\frac{R_{OFF}}{(R_{OFF} + R_{GATE})} + \frac{R_{ON}}{(R_{ON} + R_{GATE})} \right) \quad (6)$$

where

- $R_{OFF} = R_{OL}$ and R_{ON} (effective resistance of pullup structure)

7.2.1.3 Application Curves

The figures below show the typical switching characteristics of the UCC5714x-Q1 device with a 1nF capacitor load.

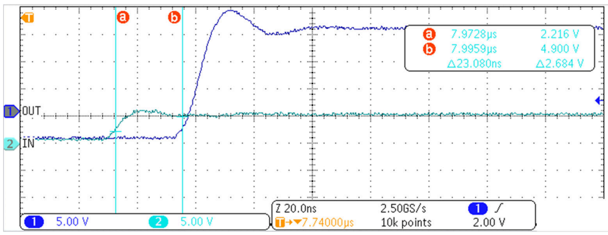


Figure 7-3. UCC5714x-Q1 Rising (Turn-On) Propagation Delay

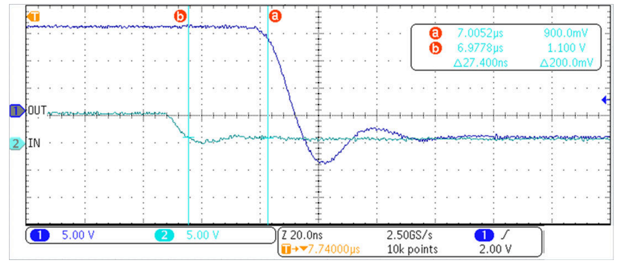


Figure 7-4. UCC5714x-Q1 Falling (Turn-Off) Propagation Delay

7.3 Power Supply Recommendations

The bias supply voltage range for which the UCC5714x-Q1 devices are recommended to operate is from UVLO to 26V. The lower end of this range is governed by the internal UVLO protection feature on the VDD pin supply circuit blocks. Whenever the driver is in UVLO condition when the VDD pin voltage is below the $V_{(ON)}$ supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 26V recommended maximum voltage rating of the VDD pin of the device. The absolute maximum voltage for the VDD pin is 30V.

The UVLO protection feature also involves a hysteresis function. This means that when the VDD pin bias voltage has exceeded the threshold voltage and device begins to operate, and if the voltage drops, then the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification. Therefore, ensuring that, while operating at or near the UVLO, the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device is important to avoid triggering device shutdown.

During system shutdown, the device operation continues until the VDD pin voltage has dropped below the VDD UVLO falling threshold which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system start-up, the device does not begin operation until the VDD pin voltage has exceeded above the VDD UVLO rising threshold. The quiescent current consumed by the internal circuit blocks of the device is supplied through the VDD pin. Although this fact is well known, recognizing that the charge for source current pulses delivered by the OUT pin is also supplied through the same VDD pin is important. As a result, every time a current is sourced out of the output pin (OUT), a corresponding current pulse is delivered into the device through the VDD pin. Thus ensuring that local bypass capacitors are provided between the VDD and GND pins and located as close to the device as possible for the purpose of decoupling is important. A low-ESR, ceramic surface-mount capacitor is needed. TI recommends having two capacitors; a 100nF ceramic surface-mount capacitorplaced less than 1mm from the VDD pin of the device and another ceramic surface-mount capacitor of a few microfarads (≥1µF) added in parallel.

If the gate driver is placed far from the switching power device such as MOSFET then that may create large inductive loop. This large inductive loop may cause excessive ringing on any and all pins of the gate driver. This may result in stress exceeding device recommended rating. Therefore, it is recommended to place the gate driver as close to the switching power device as possible. It is also advisable to use an external gate resistor to damp any ringing due to the high switching currents and board parasitic elements.

7.4 Layout

7.4.1 Layout Guidelines

Proper PCB layout is extremely important in a high-current, fast-switching circuit to provide appropriate device operation and design robustness. The UCC5714x-Q1 gate driver incorporates short propagation delays and powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of power switch to facilitate voltage transitions very quickly. Very high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. The following circuit layout guidelines are recommended when designing with these high-speed drivers.

- Place the driver device as close as possible to power device to minimize the length of high-current traces between the driver output pins and the gate of the power switch device.
- Place the bypass capacitors between VDD pin and the COM pin as close to the driver pins as possible to minimize trace length for improved noise filtering. TI recommends having two capacitors; a 100nF ceramic surface-mount capacitor placed less than 1mm from the VDD pin of the device and another ceramic surface-mount capacitor of few microfarads added in parallel. These capacitors support high peak current being drawn from VDD during turnon of power switch. The use of low inductance surface-mount components such as chip capacitors is highly recommended.
- The turnon and turn-off current loop paths (driver device, power switch and VDD bypass capacitor) should be minimized as much as possible in order to keep the stray inductance to a minimum. High di/dt is established in these loops at two instances – during turnon and turn-off transients, which induces significant voltage transients on the output pins of the driver device and gate of the power switch.
- Wherever possible, parallel the source and return traces of a current loop, taking advantage of flux cancellation
- Separate power traces and signal traces, such as output and input signals.
- To minimize switch node transients and ringing, adding some gate resistance and/or snubbers on the power devices may be necessary. These measures may also reduce EMI.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The COM of the driver should be connected to the other circuit nodes such as source of power switch, ground of PWM controller, and so forth, at a single point. The connected paths should be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at OUT pin may corrupt the input signals during transitions. The ground plane must not be a conduction path for any current loop. Instead the ground plane should be connected to the star-point with one trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well.
- Place OCP filter capacitor to the driver OCP pin as close as possible. Also minimize the current sense loop will help with noise immunity. The sense resisitor should be placeed close to the IGBT emmiter or source of the MOSFET to decrease the parasitic inductance. A low ESL film resistor is recommened for sense resistor.

7.4.2 Layout Example

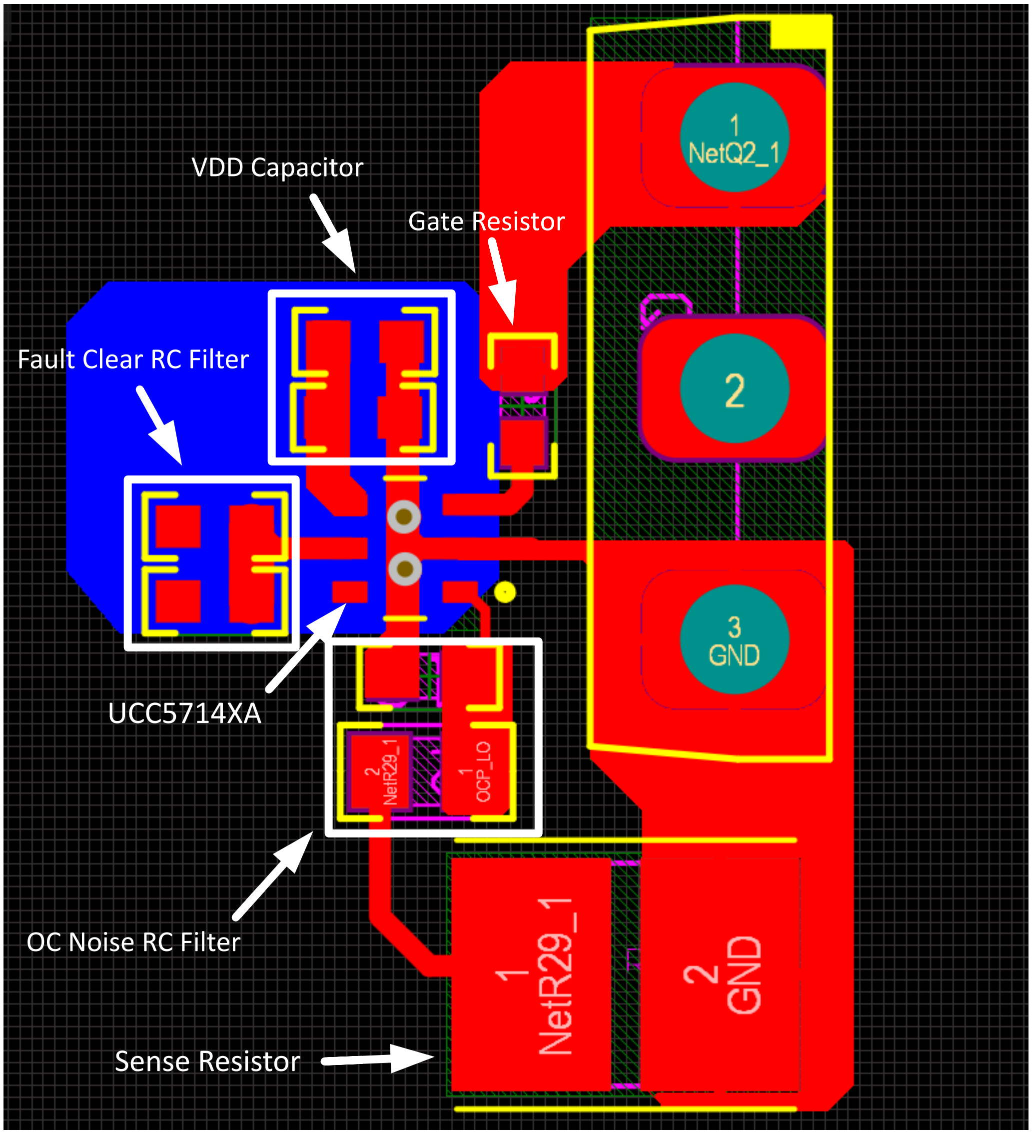


Figure 7-5. Layout Example: UCC5714x-Q1D

7.4.3 Thermal Consideration

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the package. In order for a gate driver to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The thermal metrics for the driver package is summarized in the Thermal Characteristics section of the datasheet. For detailed information regarding the thermal information table, refer to *IC Package Thermal Metrics Application Note* (SPRA953).

8 Device and Documentation Support

8.1 Third-Party Products Disclaimer

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (July 2025) to Revision A (October 2025) — **Page**

- Updated data sheet status from *Advanced Information* to *Production Data* 1

DATE	REVISION	NOTES
July 2025	*	Advance Information Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC57142AQDBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	U42Q
UCC57148AQDBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	U48Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UCC57142-Q1, UCC57148-Q1 :

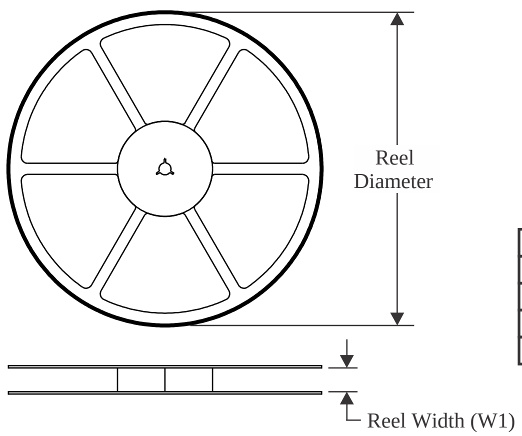
- Catalog : UCC57142, UCC57148

NOTE: Qualified Version Definitions:

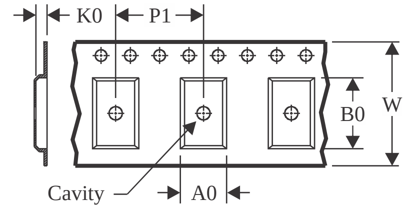
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

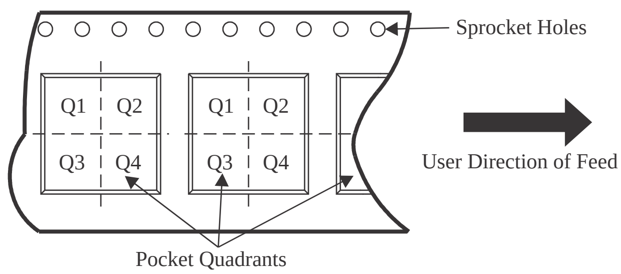


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

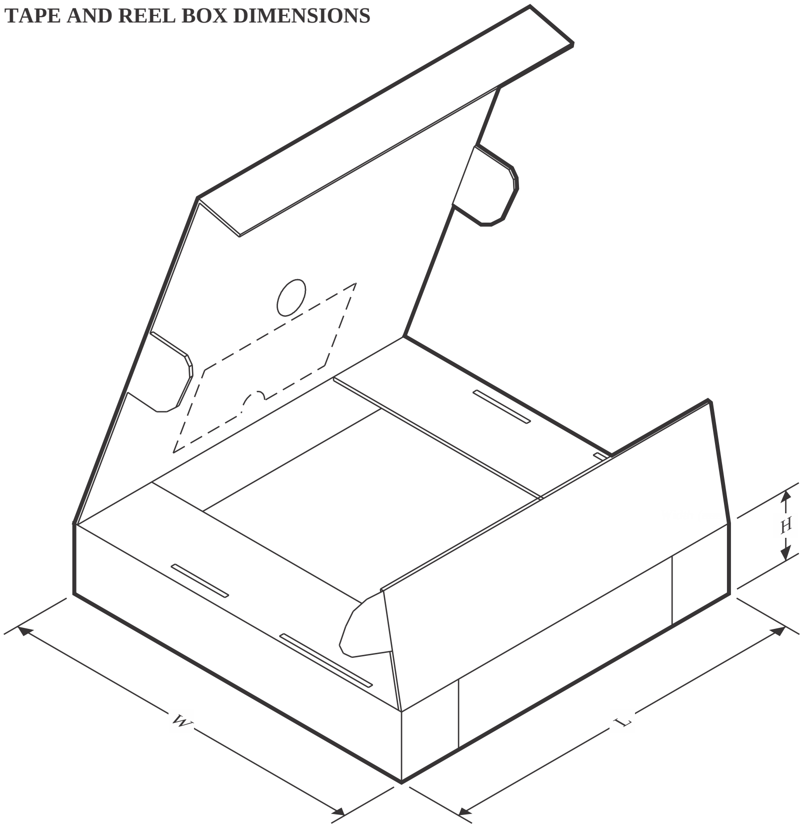
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

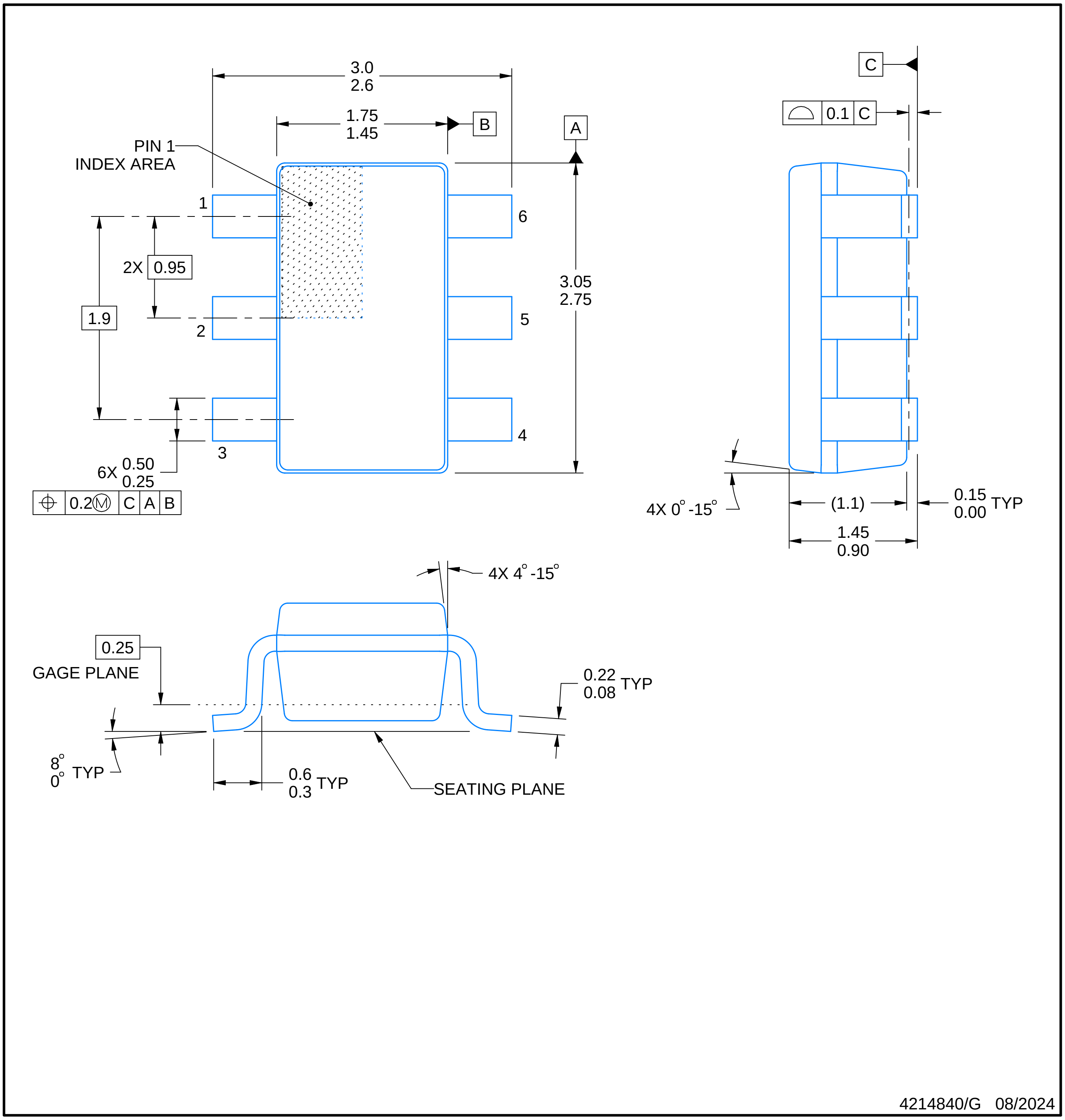
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC57142AQDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
UCC57148AQDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



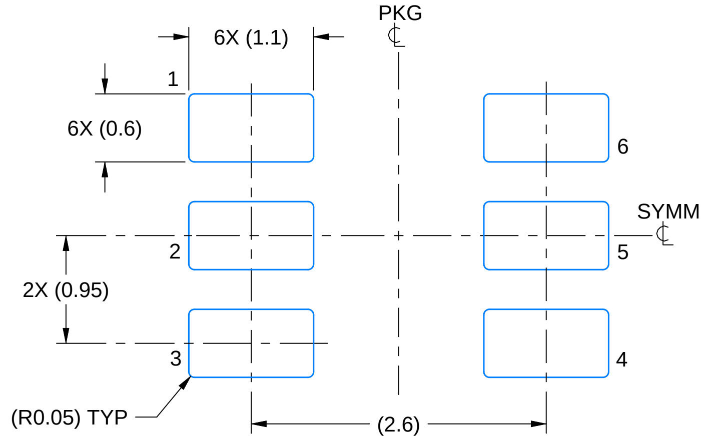
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC57142AQDBVRQ1	SOT-23	DBV	6	3000	210.0	185.0	35.0
UCC57148AQDBVRQ1	SOT-23	DBV	6	3000	210.0	185.0	35.0

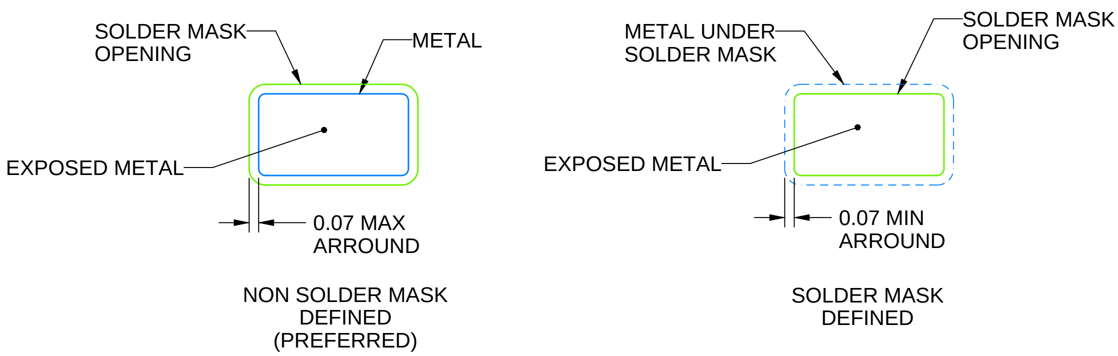


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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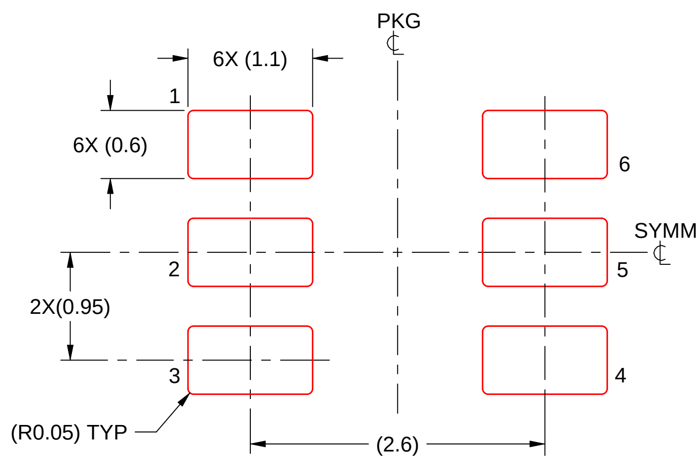
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.