UCC5880-Q1 Isolated 20A Adjustable Gate Drive IGBT/SiC MOSFET Gate Driver With Advanced Protection Features For Automotive Applications

1 Features

- Dual-output driver with real time variable drive strength
  - ±15A and ±5A drive current outputs
  - Digital input pins (GD*) for drive strength adjustment without SPI
  - 3 resistor settings R1, R2, or R1||R2
  - Integrated 4A active Miller clamp or optional external drive for Miller clamp transistor
- Primary-side and secondary-side active short circuit (ASC) support
- Under-voltage and over-voltage protection on internal and external supplies
- Driver die temperature sensing and over temperature protection
- Short-circuit protection:
  - 110ns response time to DESAT event
  - DESAT protection – selections up to 14V
  - Shunt resistor based short-circuit (SC) and over-current (OC) protection
  - Configurable protection threshold values and blanking times
  - Programmable soft turn-off (STO) and two-level soft turn-off (2STO) current
- Integrated 10-bit ADC
  - Able to measure power switch temperature, DC Link voltage, driver die temperature, DESAT pin voltage, VCC2 voltage
  - Programmable digital comparators
- Advanced VCE/VDS clamping circuit
- Functional Safety-Compliant
  - Developed for functional safety applications
  - Documentation available to aid ISO 26262 system design up to ASIL D
- Integrated diagnostics:
  - Built in self-test (BIST) for protection comparators
  - Gate threshold voltage measurement for power device health monitoring
  - INP to transistor gate path integrity
  - Internal clock monitoring
  - Fault alarm and warning outputs (nFLT*)
  - ISO communication data integrity check
- SPI based device reconfiguration, verification, supervision, and diagnosis
- 150V/ns CMTI
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: -40°C to +125°C ambient operating temperature
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C2b

2 Applications

- EV and HEV traction inverter
- EV and HEV power modules

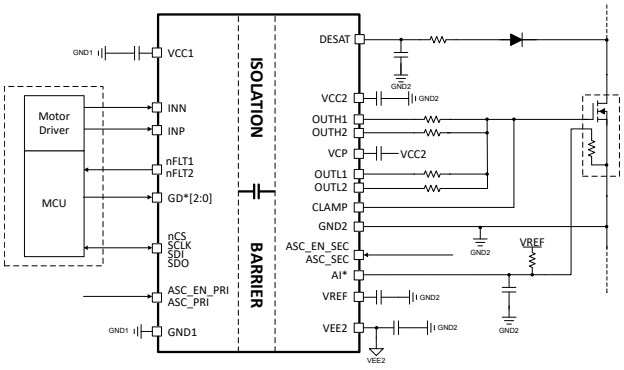
3 Description

The UCC5880-Q1 device is an isolated, highly configurable adjustable drive strength gate driver targeted to drive high power SiC MOSFETs and IGBTs in EV/HEV applications. Power transistor protections are included, such as shunt resistor based over-current, over-temperature (PTC, NTC, or diode), and DESAT detection, with selectable soft turn-off or two-level soft turn-off during these faults. An integrated 10-bit ADC enables monitoring of up to 2 analog inputs, VCC2, DESAT, and the gate driver temperature for enhanced system management. Diagnostics and detection functions are integrated to simplify the design of ASIL compliant systems. The parameters and thresholds for these features are configurable using the SPI, which allows the device to be used with nearly any SiC MOSFET or IGBT.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE (NOM)
UCC5880-Q1	DFC (SSOP, 32)	10.3mm × 10.3mm	10.5mm x 7.5mm

(1) For all available packages, see the Mechanical, Packaging, and Orderable Information section.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

Table of Contents

4 Pin Configuration and Functions

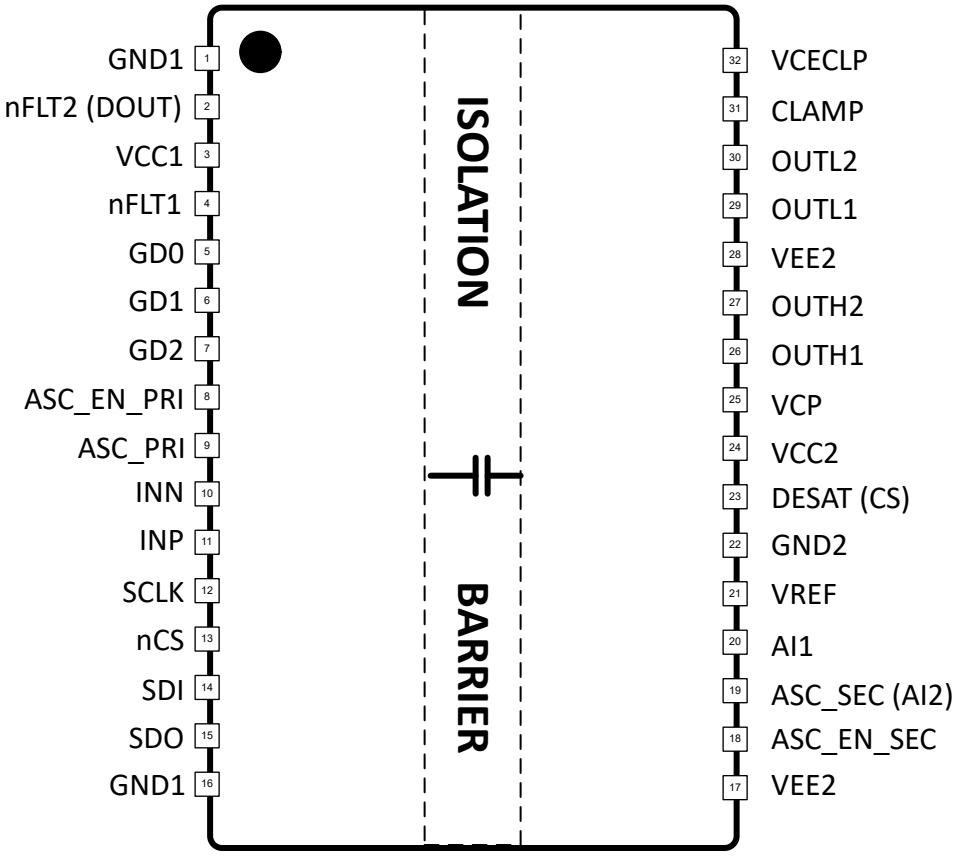


Figure 4-1. 32-Pin DFC SSOP Package Top View

Table 4-1. Pin Functions

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
GND1	1, 16	P	Primary Side Ground. Connect all GND1 pins together and to the PCB ground plane on the primary side. Prioritize pin 1 for supply and input filter decoupling.
nFLT2 (DOUT)	2	O	Fault Indicator Output 2. nFLT2 is used to interrupt the host when a fault occurs. Faults that are unmasked pull nFLT2 low when the fault occurs. nFLT2 is high when all faults are either non-existent or masked. It is recommended to add an external pull up resistor to VCC1 if faster rise time is needed. Additionally, nFLT2 may be configured as DOUT (push/pull) to provide the host controller a PWM signal with a duty cycle relative to the ADC input of interest.
VCC1	3	P	Primary Side Power Supply. Connect a 3V to 5.5V power supply to VCC1. Bypass VCC1 to GND1 with ceramic bulk capacitance as close to the VCC1 pin as possible.
nFLT1	4	O	Fault Indicator Output 1. nFLT1 is used to interrupt the host when a fault occurs. Faults that are unmasked pull nFLT1 low when the fault occurs. nFLT1 is high when all faults are either non-existent or masked. It is recommended to add an external pull up resistor to VCC1 if faster rise time is needed.
GD0	5	I	OUTL1/2 and OUTH1/2 Selector Inputs. GD* select combinations of OUT*1 and OUT*2 with user-selectable resistors. Drive all GD* high to force the gate of the power transistor low and reset all faults. See Adjustable Gate Drive Outputs (OUTL* OUTH*) for more details. Tie to GND1 if not used.
GD1	6	I	
GD2	7	I	
ASC_EN_PRI	8	I	Primary-side Active Short Circuit Enable Input. ASC_EN_PRI enables the ASC function and forces the output to follow the ASC_PRI pin input state. When ASC_EN_PRI is low, the OUT* pins follow the INP and INN pin logical truth table. Tie to GND1 if not used.
ASC_PRI	9	I	Primary-side Active Short Circuit Polarity Input. The OUT* pins follow the logic level at ASC_PRI when the ASC_EN_PRI input is driven high. See the ASC section for more details. Tie to GND1 if not used.
INN	10	I	Negative PWM Input. INN is connected to the INP from the opposite arm of the half-bridge. If INP and INN overlap, the Shoot Through Protection (STP) engages and forces output low. Tie to GND1 if not used.
INP	11	I	Positive PWM Input. INP drives the state of the driver output. With the driver enabled, when INP is high, OUTH* is pulled high. When INP is low, OUTL* is pulled low. CMOS input logic level determined by the VCC1 voltage. INP is connected to the INN of the opposite arm of the half-bridge. If INP and INN overlap, STP engages and forces output low.
SCLK	12	I	SPI Clock. SCLK is the clock signal for the main SPI interface. The SPI interface operates with clock rates up to 4MHz.
nCS	13	I	SPI Chip Selection Input. nCS is an active low input used to activate the SPI peripheral device. Drive nCS low during SPI communication. When nCS is high, SDO is set to disabled (high-impedance) and commands on SDI are ignored. Tie to VCC1 if not used.
SDI	14	I	SPI Data Input. SDI is the data input for the main SPI interface. Data is sampled on the falling edge of CLK, SDI must be in a stable condition to ensure proper communication.
SDO	15	O	SPI Data Output. SDO is the data output for the main SPI interface. Data is clocked out on the falling edge of CLK, SDO is changed with a rising edge of CLK.
VEE2	17, 28	P	Secondary Negative Power Supply. Connect all VEE2 supply inputs together. Connect a -12V to 0V power supply to VEE2. The total voltage rail from VCC2 to VEE2 must not exceed 30V. Bypass VEE2 to GND2 with at least 1uF of low-impedance ceramic capacitors as close to pin 28 as possible, to encourage gate current flow through pin 28.
ASC_EN_SEC	18	I	Secondary-side Active Short Circuit Enable Input. ASC_EN_SEC enables the ASC function, overriding the INP command and forcing the output of the driver to the defined safe state, set by CONTROL2[ASC_LEV_SEL] register. When ASC_EN_SEC is low, the output is controlled by primary side pins. Tie to GND2 if not used.
ASC_SEC	19	I	ASC_SEC (AI2) defaults to Active Short Circuit Polarity Input. When programmed as ASC_SEC, the OUT* pins follow the logic level at ASC_SEC when the ASC_EN_SEC input is driven high.
AI2		I	ASC_SEC (AI2) can be programmed as an ADC input that digitizes analog voltages up to 4.0V. Additionally, a programmable “digital comparator” is available to signal faults when the voltage is above/below (selectable) the programmed threshold. This is useful for monitoring the DC-LINK voltage or phase voltage during the switching cycle. Tie to GND2 if not used.

Table 4-1. Pin Functions (continued)

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
AI1	20	I	Analog Input 1. AI1 is an ADC input that digitizes analog voltages up to 4.0V. Additionally, a programmable “digital comparator” is available to signal faults when the voltage is above/ below (selectable) the programmed threshold. This is useful for monitoring the DC-LINK voltage or phase voltage during the switching cycle. Tie to GND2 if not used.
VREF	21	P	Internal ADC Voltage Regulator Output. VREF provides an external 5.0V reference voltage, which is internally scaled down to 4.0V for the ADC. Bypass VREF to GND2 with at least 1uF of ceramic capacitance.
GND2	22	P	Gate Drive Supply Reference. Connect GND2 to the power FET source/ IGBT emitter. ASC_EN_SEC, ASC_SEC (AI2), AI1, VREF, and DESAT are referenced to GND2.
DESAT	23	I	Current Sense Input/ Desaturation based Short Circuit Detection Input. DESAT (CS) is configurable to sense over-current conditions in resistor sense applications, or DESAT over-current in VCE/VDS sensing applications. For DESAT applications, bypass DESAT to GND2 with a ceramic capacitor and, in parallel, connect a Schottky diode with the cathode connected to the DESAT pin, and the anode connected to GND2. See the applications section for details on calculating the component values. Additionally, connect the DESAT pin to a resistor to the anode of a diode to the collector of the power FET. The DESAT pin detects a fault when the VDS/VCE voltage of the power FET exceeds the SPI programmable threshold while the power FET is on. Tie to GND2 if not used.
CS		I	Current Sense Positive Input/ Desaturation based Short Circuit Detection Input. CS (DESAT) is configurable to sense over-current and short-circuit conditions in resistor sense applications, or DESAT over-current in VCE/VDS sensing applications. For sense resistor based applications, connect DESAT (CS) pin to the positive side of the sense element through an RC. The current limit threshold is programmable via SPI. Tie to GND2 if not used.
VCC2	24	P	Secondary Positive Power Supply. Connect a 15V to 30V power supply to VCC2. The total voltage rail from VCC2 to VEE2 must not exceed 30V. Bypass VCC2 to GND2 and VCC2 to VEE2 with bulk ceramic capacitance as close to the VCC2 pin as possible. Additional capacitance may be needed depending on the gate charge of the power device.
VCP	25	P	High-side Drive Supply. VCP supplies power for the OUTH* drive. Bypass VCP to VCC2 with a ceramic capacitor between 10nF and 100nF, as close to the VCP pin as possible.
OUTH1	26	O	Gate driver source pins (OUTH1 = 15A_{PK}, OUTH2 = 5A_{PK}). When the driver is active and commanded high, OUTH* pins are used to source current to the gate of the power FET to drive the output high. Connect OUTH* pins to the gate of the power FET through individual gate resistors. The value of the gate resistor is chosen based on the slew rate required for the application. Different slew rates are programmed by using different resistor values for OUTH1 and OUTH2. The two outputs are enabled “on the fly” using the GD* inputs to set 3 different slew rates (OUTH1 only, OUTH2 only, and OUTH1 + OUTH2).
OUTH2	27	O	
OUTL1	29	O	Gate driver sink pins (OUTL1 = 15A_{PK}, OUTL2 = 5A_{PK}). When the driver is active and commanded low, OUTL* pins are used to sink current from the gate of the power FET to drive the gate low. Connect OUTL* pins to the gate of the power FET through individual gate resistors. The value of the gate resistor is chosen based on the slew rate required for the application. Different slew rates are programmed by using different resistor values for OUTL1 and OUTL2. The two outputs are enabled “on the fly” using the GD* inputs to set 3 different slew rates (OUTL1 only, OUTL2 only, and OUTL1 + OUTL2).
OUTL2	30	O	
CLAMP	31	O	Miller Clamp pin. The CLAMP pin is used to hold the gate of the power FET strongly to VEE2 while the power FET is "off". CLAMP is configurable as an internal Miller clamp, or to drive an external clamping circuit. When using the internal clamping function, connect CLAMP directly the power FET gate. When configured as an external clamp, connect CLAMP to the gate of an external pulldown MOSFET. Disable and tie to VEE2 if not used.
VCECLP	32	I	VCE Clamp Input. VCECLP clamps to a diode above the VCC2 rail and indicates a fault when the voltage at VCECLP is above the VCECLPth voltage. Bypass VCECLP to VEE2 with ceramic capacitor and, in parallel, connect a resistor. See the applications section for details on calculating the component values. Additionally, connect VCECLP to the anode of a zener diode to the collector/drain of the power FET. Tie to VEE2 if not used.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

5 Power Supply Recommendations

5.1 VCC1

VCC1 supports an input range of 3V to 5.5V in order to support both 3.3V and 5V controller signaling. VCC1 is monitored with both an undervoltage and overvoltage comparator circuit to ensure valid operation. UV and OV conditions of VCC1 are recorded in FAULT2[UVLO1_FAULT] and FAULT2[OVLO_FAULT1], respectively.

5.2 VCC2

VCC2 operates within an input range of 12V and 30V, allowing for use in IGBT and SiC applications. VCC2 is monitored with both an undervoltage and overvoltage comparator circuit to ensure valid operation. UV and OV conditions of VCC2 are recorded in FAULT2[UVLO2_FAULT] and FAULT2[OVLO2_FAULT], respectively.

5.3 VEE2

VEE2 operates with an input range of -12V to 0V, allowing a negative gate bias on the power FET during turn-off in both IGBT and SiC applications. This prevents the power FET from unintentionally turning on due to current inducted from the Miller effect. For operation with a unipolar supply, connect VEE2 to GND2. VEE2 is monitored with both an undervoltage and overvoltage comparator circuit to ensure valid operation. UV and OV conditions of VEE2 are recorded in FAULT2[UVLO3_FAULT] andFAULT2[OVLO3_FAULT], respectively.

6 Layout

6.1 Layout Guidelines

Layout best practices must be followed to achieve robust performance from UCC5880-Q1. Failure to follow best practices may lead to low noise immunity. Reach out to TI engineers for feedback during schematic phase, component placement phase, and trace/plane layout phase of board design.

6.1.1 Component Placement

- Low-ESR and low-ESL capacitors must be connected close to the device between the VCC1 and GND1 pins and between the VCC2, VEE2 and GND2 pins to support high peak currents when turning the external power transistor on and off.
- Place the VCP and VREF caps as close to the device as possible.

6.1.2 Grounding Considerations

- It is essential to confine the high peak currents that charge and discharge the transistor gates to a minimal physical area. This decreases the loop inductance and minimize noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.
- Ensure a small loop area/inductance between VCP and VCC2.
- Analog signals measured with the integrated ADC on AI1 and AI2 pins must be effectively isolated from high gate switching currents in GND2 net. It is recommended to create Kelvin connections for these measurements to reduce impact of ground bounce caused by high di/dt in the gate drive loop.

6.1.3 High-Voltage Considerations

- To ensure isolation performance between the primary and secondary side, one should avoid placing any PCB traces or copper below the driver device. A PCB cutout is recommended in order to prevent contamination that may compromise the UCC5880-Q1's isolation performance.
- For half-bridge, or high-side/low-side configurations, where the high-side and low-side drivers could operate with a DC-link voltage up to 1000 VDC, one should try to increase the creepage distance of the PCB layout between the high and low-side PCB traces.
- Conformal coating is commonly used in systems to limit pollution degree and enable shorter creepage/clearance distances.

6.1.4 Thermal Considerations

- The power dissipated in UCC5880-Q1 is directly proportional to the VCC1, VCC2, and VEE2 voltages, capacitive loading, and switching frequency. Proper PCB layout helps dissipate heat from the device to the PCB and minimize junction to board thermal impedance (θ_{JB}).
- Increasing the PCB copper connecting to VCC2 and VEE2 planes is recommended, with priority on maximizing the connection to VEE2.
- If there are multiple layers in the system, it is also recommended to connect the VCC2 and VEE2 to their respective internal planes using multiple vias of adequate size. However, it is still critical to ensure that there are not any traces/planes from different high voltage planes overlapping.

6.2 Layout Example

Please refer to UCC5880EVM-057 Evaluation Module (EVM) design for layout example.

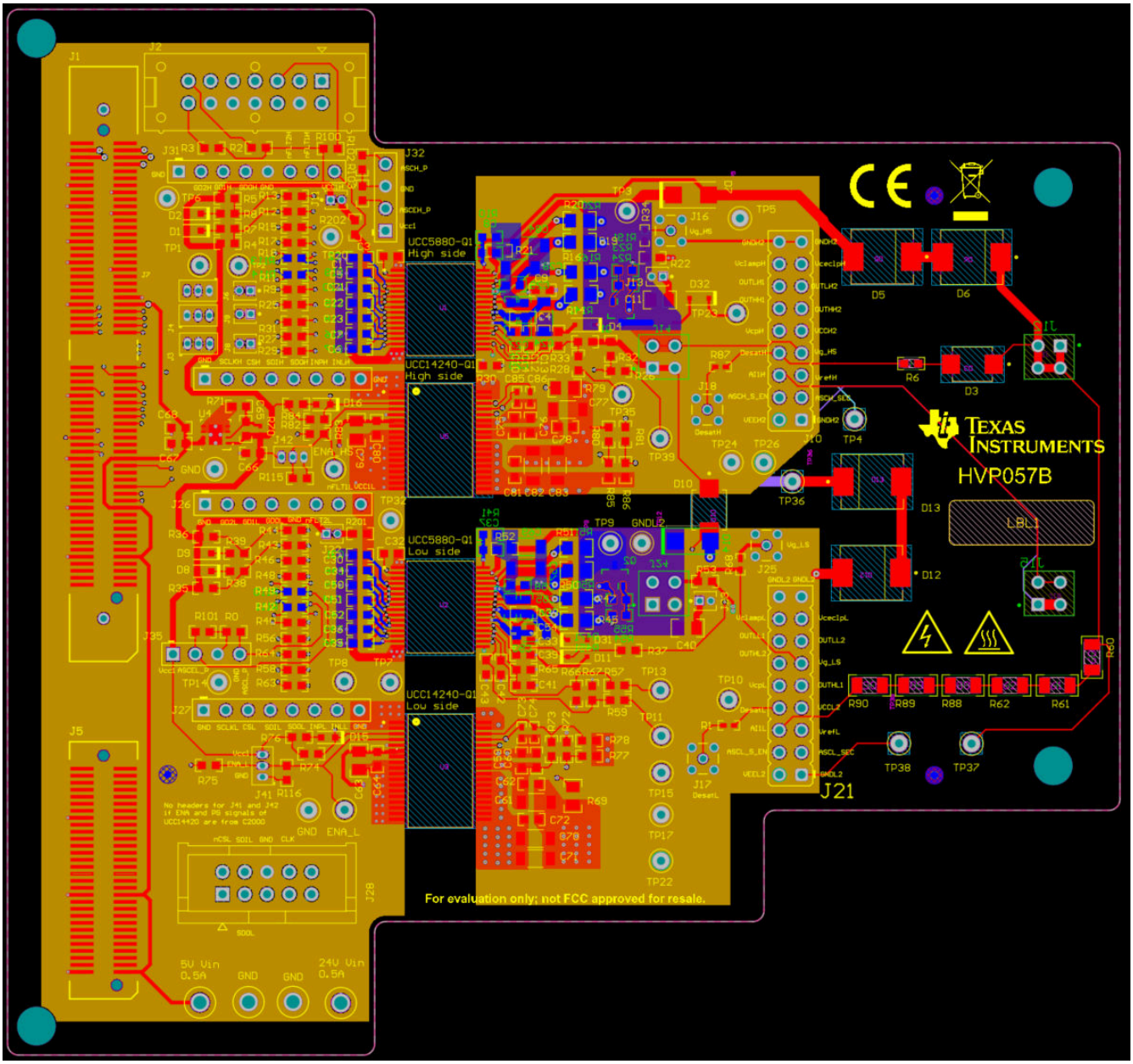


Figure 6-1. 2D Layout Example

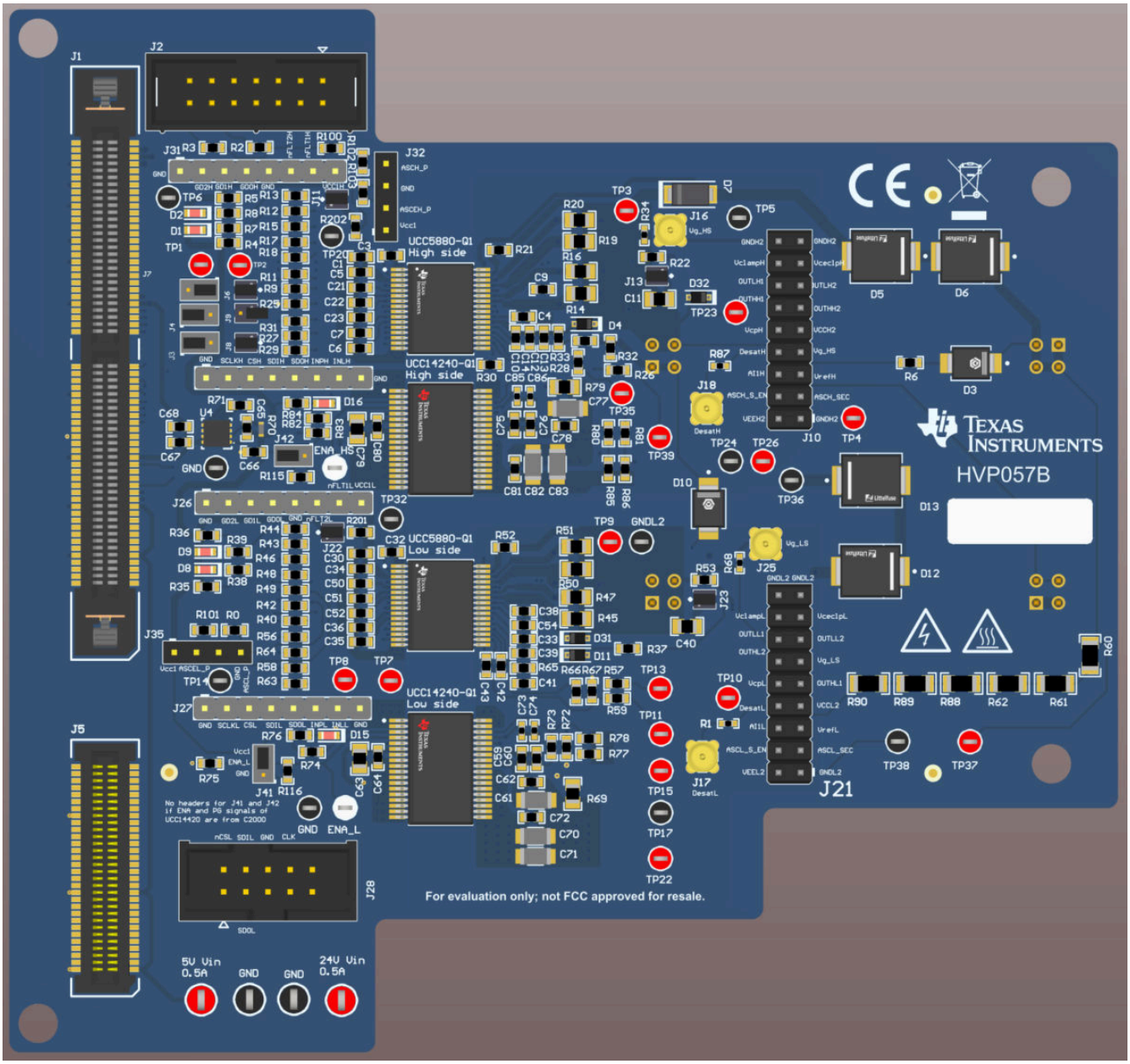


Figure 6-2. 3D Layout Example

7 Device and Documentation Support

7.1 Device Support

7.1.1 Third-Party Products Disclaimer

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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2022) to Revision A (February 2024)	Page
• Changed from Advance Information to Production Data	1

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC5880QDFCRQ1	Active	Production	SSOP (DFC) | 32	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCC5880Q
UCC5880QDFCRQ1.A	Active	Production	SSOP (DFC) | 32	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCC5880Q
UCC5880QDFCRQ1.B	Active	Production	SSOP (DFC) | 32	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

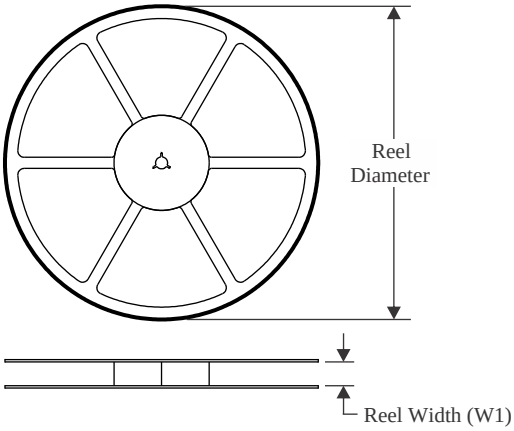
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

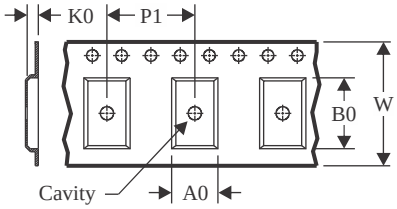
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

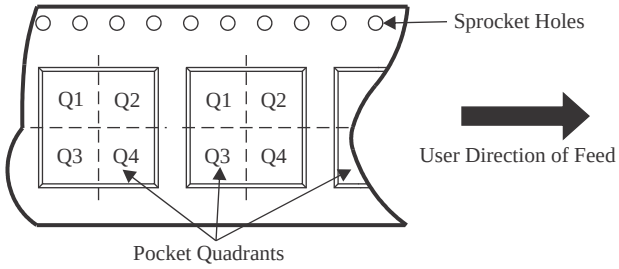


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

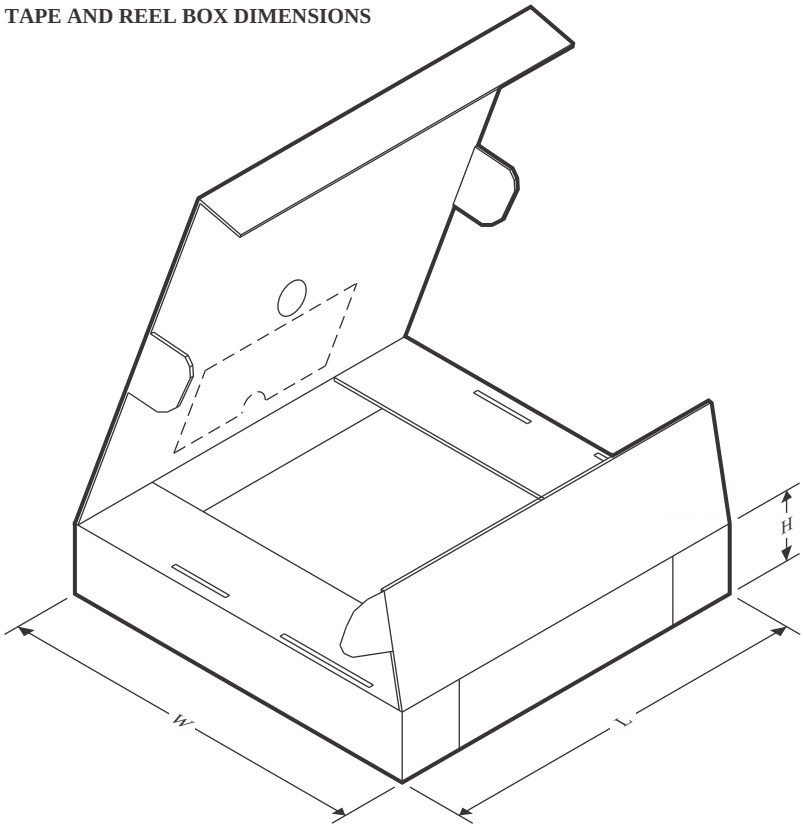
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC5880QDFCRQ1	SSOP	DFC	32	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

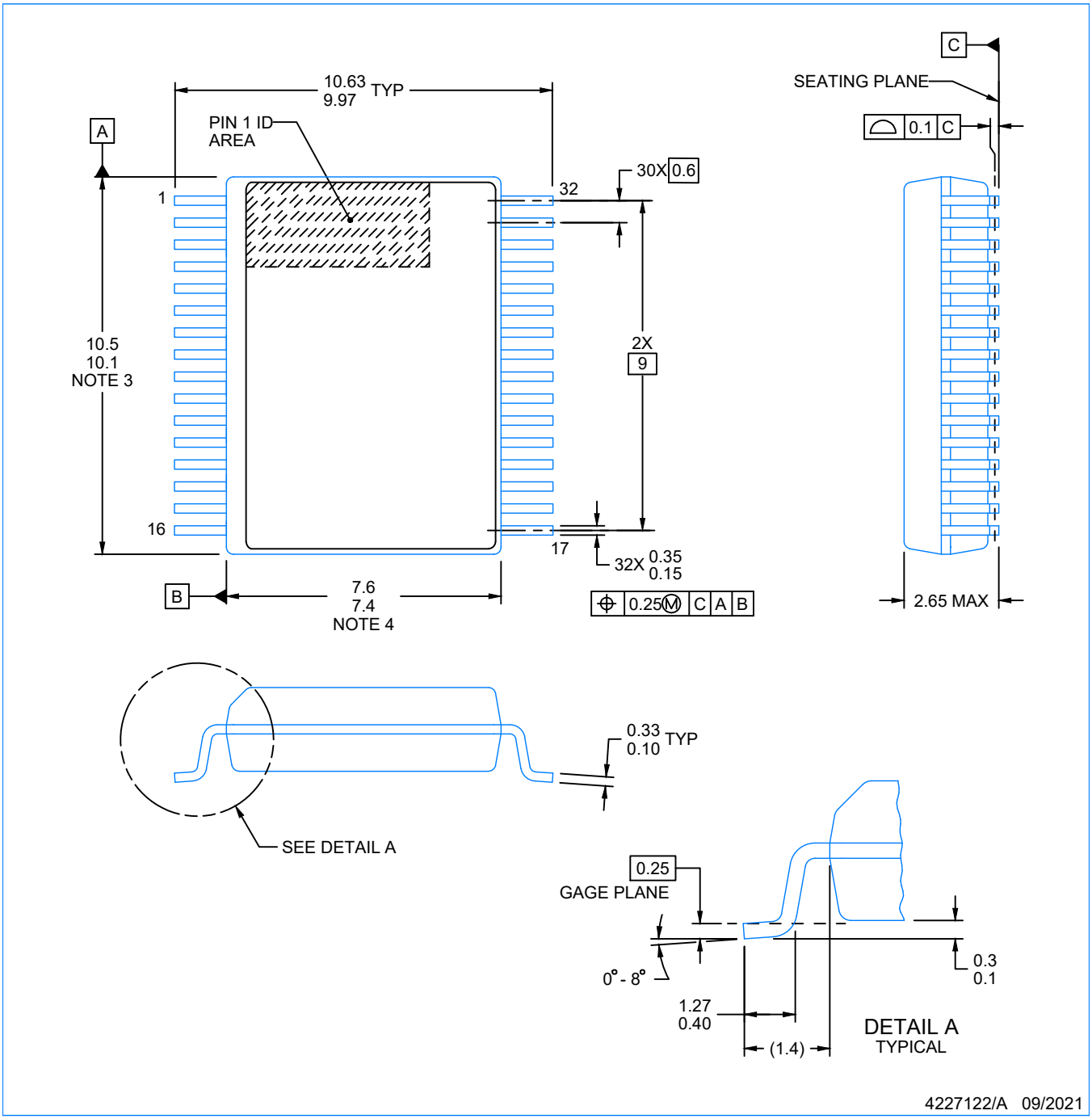
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC5880QDFCRQ1	SSOP	DFC	32	2000	350.0	350.0	43.0

PACKAGE OUTLINE

DFC0032A

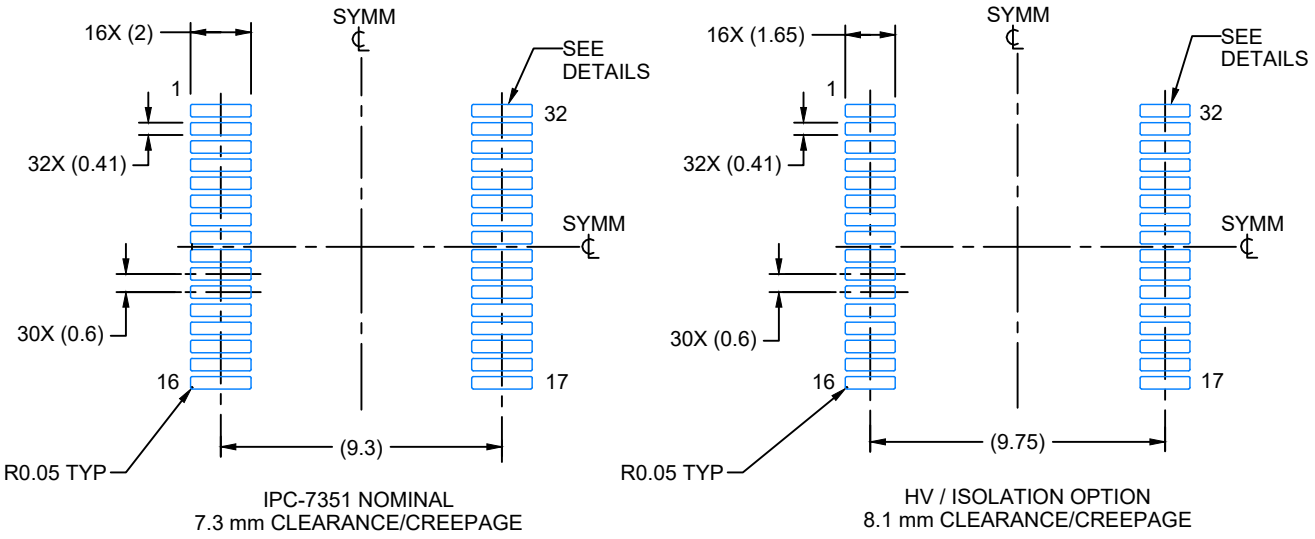
SSOP - 2.65 mm max height

SMALL OUTLINE PACKAGE

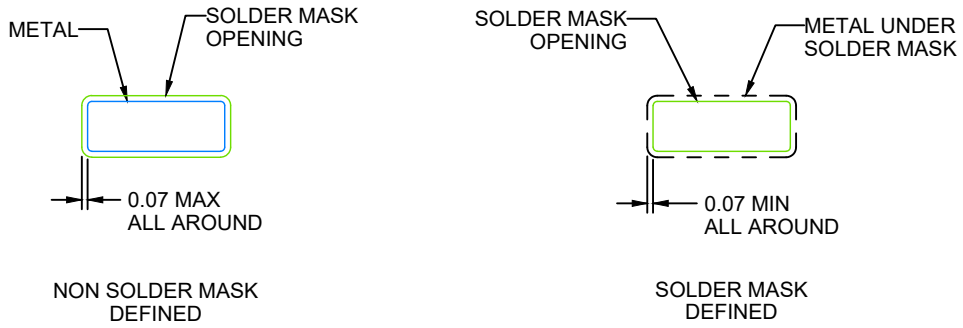


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:4X

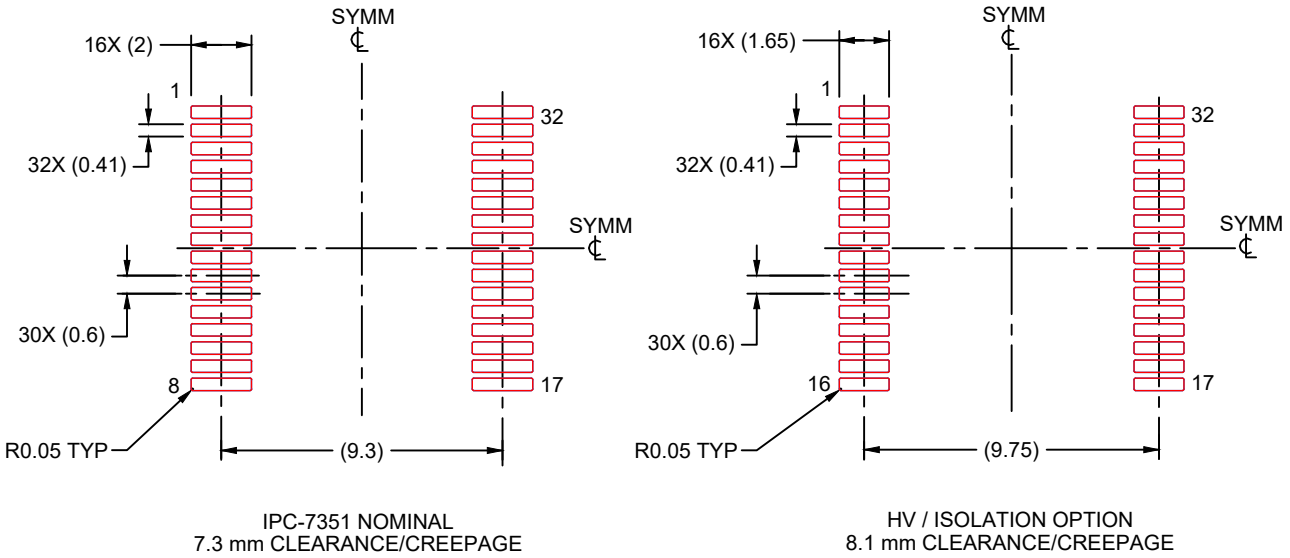


SOLDER MASK DETAILS

4227122/A 09/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4227122/A 09/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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