EVM User's Guide: ADS1285EVM-PDK

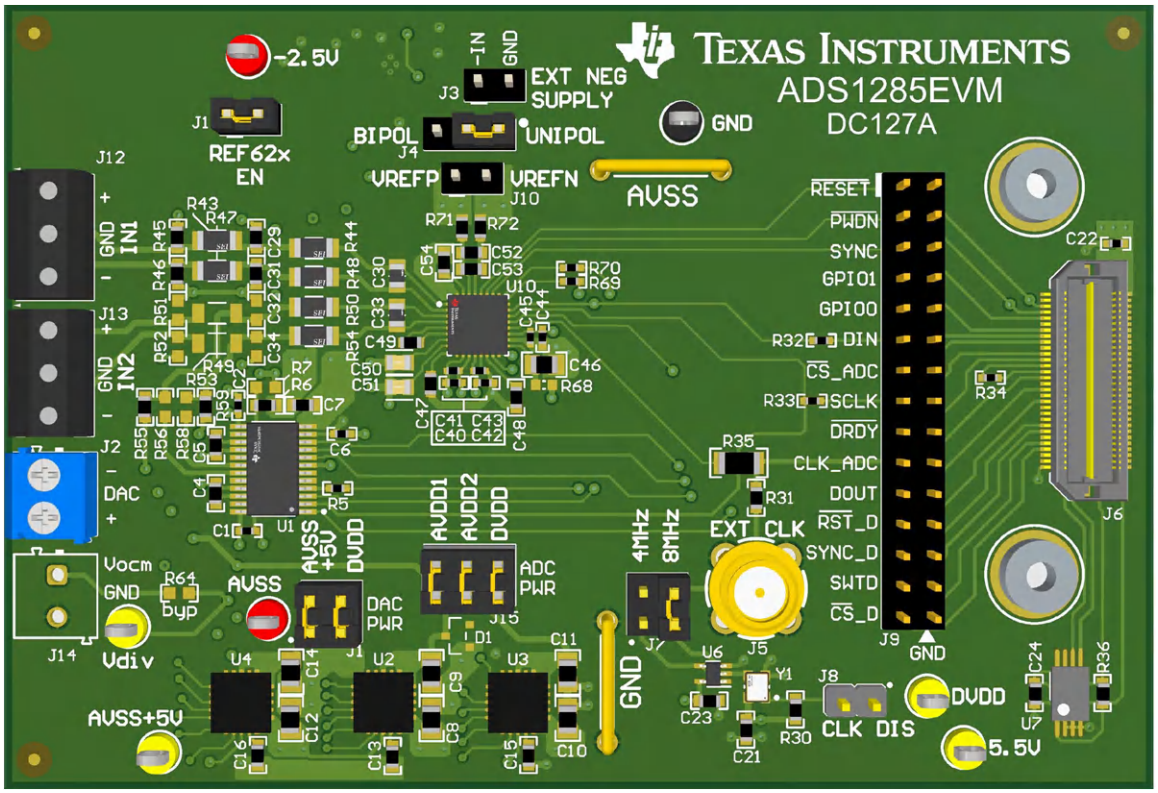
ADS1285EVM-PDK Evaluation Module

Description

The ADS1285 evaluation module (EVM) performance demonstration kit (PDK) is a platform that combines the ADS1285EVM-PDK and a precision host interface (PHI) controller board. The PHI controller board allows the ADS1285EVM to connect to a computer via a USB port. A downloadable GUI interfaces with ADS1285EVM-PDK for complete evaluation of the 32-bit ADS1285, a 32-bit delta-sigma analog-to-digital converter (ADC) for energy exploration applications.

Features

- Onboard DAC1282 for producing signals and calibration
- Onboard 5V and 3V unipolar analog supply, with options for external ±2.5-V bipolar analog supply
- Onboard 8.192-MHz crystal oscillator with divide-by-2 clock divider option
- Built-in analysis tools to plot transient behavior, fast Fourier transforms (FFT), and histograms
- USB powered; no external power supply required for unipolar



1 Evaluation Module Overview

1.1 Introduction

This user's guide describes the characteristics, operation, and use of the ADS1285EVM-PDK. This EVM allows the user to evaluate the performance of the ADS1285, a 32-bit, 4-kSPS, 2-channel delta-sigma ADC for energy exploration applications. Throughout this document, the terms *evaluation board*, *evaluation module*, and *EVM* are synonymous with the ADS1285EVM-PDK. Complete circuit descriptions, schematic diagrams, and bills of material are also included in this document.

The evaluation kit includes the ADS1285EVM-PDK board and the precision host interface (PHI) controller board. The PHI board enables the accompanying computer software to communicate with the ADC over the universal serial bus (USB) for data capture and analysis because the ADS1285EVM-PDK does not include a microprocessor on the board.

The PHI board primarily serves three functions:

- Provides a communication interface from the EVM to the computer through a USB port
- Provides the digital input and output signals necessary to communicate with the ADS1285EVM-PDK
- Supplies power to all active circuitry on the ADS1285EVM-PDK board

The following related documents are available for download through the Texas Instruments web site at www.ti.com.

Table 1-1. Related Documentation

Device	Literature Number
ADS1285	SBASAK6

1.2 Kit Contents

The ADS1285EVM-PDK includes the following features:

- Contains all support circuitry needed for the ADS1285
- USB powered: No external power supply is required
- Voltage reference options: External or onboard
- Clock options: External clock source or 8.192MHz onboard crystal oscillator with dividers for 4.096MHz
- Voltage supply options: Unipolar or bipolar support with adjustable AVDD1 low-dropout regulator (LDO) and externally sourced -2.5V LDO
- Communication signal header enables simple probing with a logic analyzer
- Built-in analysis tools including scope, FFT, histogram, and DAC configuration using the graphical user interface (GUI)

1.3 Specification

The following specifications are applicable to the ADS1285EVM board and the PHI board.

Table 1-2. ADS1285EVM-PDK Specifications

PARAMETER	CONDITIONS		VALUE
Temperature	Recommended operating free-air temperature range, T_A		15°C ≤ T_A ≤ 35°C
Power supply input current range (unipolar or bipolar)	Supply current range $\|I_s\|$		0.25A ≤ $\|I_s\|$ ≤ 0.5A
Power supply input voltage range (bipolar)	Recommended voltage input range for J3 (-IN) versus AGND		-6.5V ≤ -Vin ≤ -5.5V
Input voltage range	Absolute input voltage versus AGND for VINPx and VINNx	Buffer only	AVSS + 0.1V ≤ VINx ≤ AVDD1 - 0.1V
		PGA enabled	AVSS + 1.1V ≤ VINx ≤ AVDD1 - 0.85V
EXT clock	Recommended voltage range (V_{CLK}) versus DGND, external source applied to J5	Logic Level High (V_{CLKh})	0.8×IOVDD ≤ V_{CLKh}
		Logic Level Low (V_{CLKl})	V_{CLKl} ≤ 0.2×IOVDD
	Recommended frequency range (f_{CLK}), external source applied to J5		3MHz ≤ f_{CLK} ≤ 8.3MHz
External digital IO	External logic levels connected to header J9 versus DGND	Logic Level High (V_{IOh})	0.8×IOVDD ≤ V_{IOh}
		Logic Level Low (V_{IOl})	V_{IOl} ≤ 0.2×IOVDD
ADS1285 AVDD1 to AVSS	Recommended voltage range, external source applied to J15-2		3V ≤ AVDD1 ≤ 5.25V
ADS1285 AVDD1 to AGND	Recommended voltage range, external source applied to J15-2		2.375V ≤ AVDD1
ADS1285 AVSS to AGND	Recommended voltage range, external source applied to J3-1		-2.625V ≤ AVSS ≤ 0V
ADS1285 AVDD2 to AGND	Recommended voltage range, external source applied to J15-4		2.375V ≤ AVDD2 ≤ 5.25V
ADS1285 AVDD2 to AVSS	Recommended voltage range, external source applied to J15-4		AVDD2 ≤ 5.25V
ADS1285 IOVDD to DGND	Recommended voltage range, external source applied to J15-6	IOVDD not connected to CAPD pin	2.7V ≤ IOVDD ≤ 3.6V
		IOVDD connected to CAPD pin	1.65V ≤ IOVDD ≤ 1.95V
ADS1285 VREFN to AVSS	Recommended voltage range (R42 removed), external source applied to J10-2		AVSS-0.05V ≤ REFN
ADS1285 VREFP to AVSS	Recommended voltage range (R38 removed), external source applied to J10-1		REFP ≤ AVDD1+0.1V
ADS1285 VREF	Recommended voltage range (R38 and R42 removed), external differential source applied to J10	Reference voltage = 5V	4.9V ≤ VREF ≤ AVDD1-AVSS+0.1V
		Reference voltage = 4.096V	4V ≤ VREF ≤ 4.2V
		Reference voltage = 2.5V	2.4V ≤ VREF ≤ 2.6V

1.4 Device Information

For complete specifications, see ADS1285 data sheet.

Table 1-3. ADS1285 Specifications

DEVICE SPECIFICATION	VALUE
Package size	5.00mm x 5.00mm VQFN
Operating temperature range	-40°C to 85°C
AVDD1 to AVSS supply voltage	2.375V to 5.25V
AVDD2 to AGND supply voltage	2.375V to 5.25V
IOVDD to DGND supply voltage	2.7V to 3.6V (IOVDD not connected to CAPD)
	1.65V to 1.95V (IOVDD connected to CAPD)
Differential reference voltage inputs	Supports 2.5V, 4.096V, and 5V

1.5 Quick Start Guide

The following instructions are a step-by-step guide to connecting the ADS1285EVM-PDK to the computer and evaluating the performance of the ADS1285:

1. Review the default jumper settings in Section 4 and GUI software installation in Section 3.
2. Connect the ADS1285EVM to the PHI. Install the two screws as indicated in Figure 1-1.
3. Attach the micro USB to the PHI board and your PC. Three LEDs illuminate on the PHI board to indicate connectivity to the PC.
   a. LED D5 on the PHI lights up, indicating that the PHI is powered up.
   b. LEDs D1 and D2 on the PHI start blinking to indicate that the PHI is booted up and communicating with the PC. Figure 1-1 shows the resulting LED indicators.

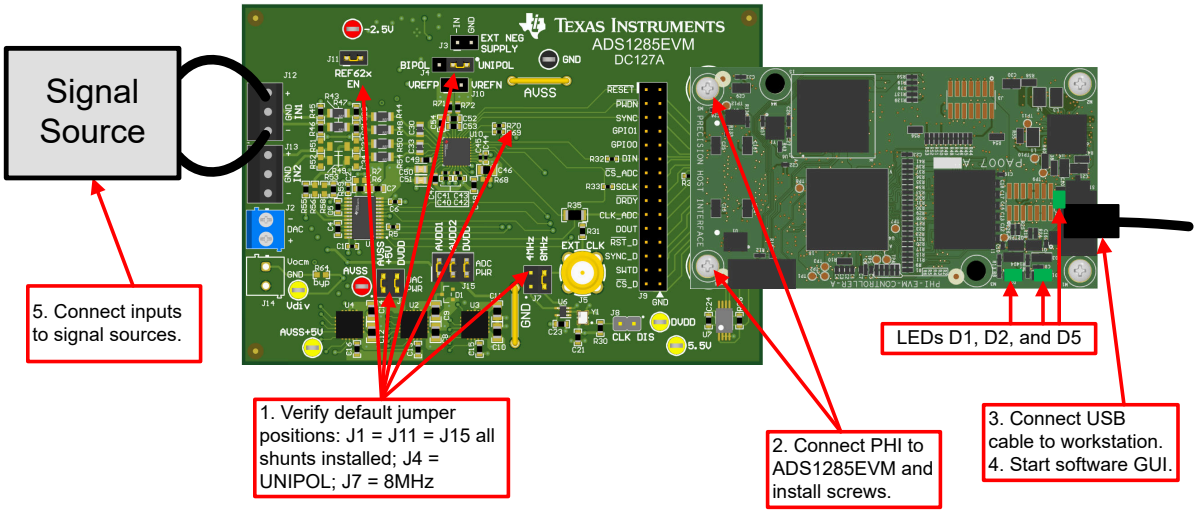


Figure 1-1. ADS1285EVM-PDK Hardware Setup and LED Indicators

4. Launch the ADS1285EVM-PDK GUI software and power can be supplied to the EVM.
   a. The default installation path is *C:\Program Files (x86)\Texas Instruments\ADS1285 EVM*.
5. As shown in Figure 1-2, use the *Configuration* section of the GUI for a specific clock input, desired data rate, and number of samples. Then, use the **Capture** button to collect data. Section 4.2.1 details the EVM GUI global input parameters and the various pages within the GUI.

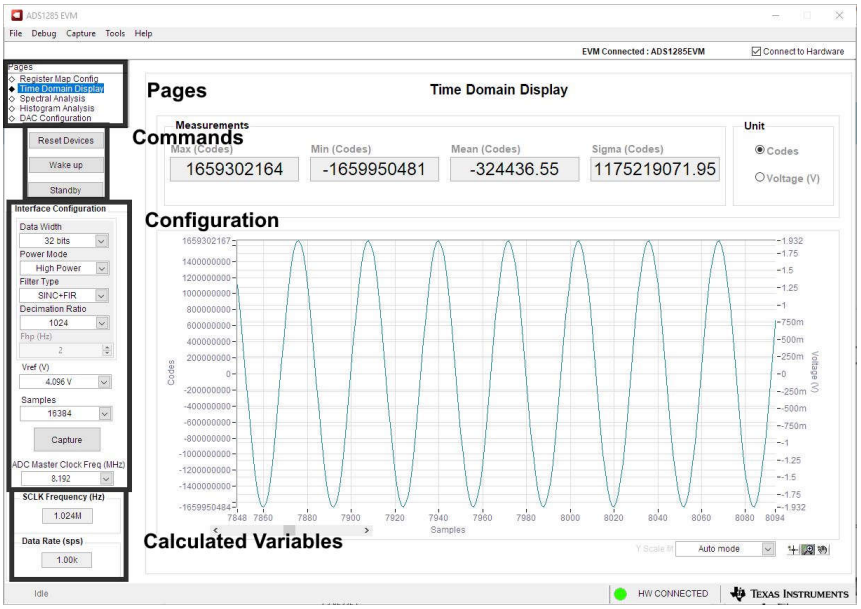


Figure 1-2. EVM GUI Global Input Parameters

2 Hardware

The ADS1285EVM-PDK is designed for easy interfacing with analog sources. This section details the front-end circuit, including jumper configuration for different input test signals and board connectors for signal sources.

2.1 ADC Analog Input Signal Path

Connect analog inputs to the EVM using the terminal blocks associated with each ADC channel. The screw terminal blocks (J12, and J13) can interface directly with the leads of an external sensor input. Figure 2-1 depicts the input path for each ADC channel on the EVM while Table 2-1 lists the supported input options.

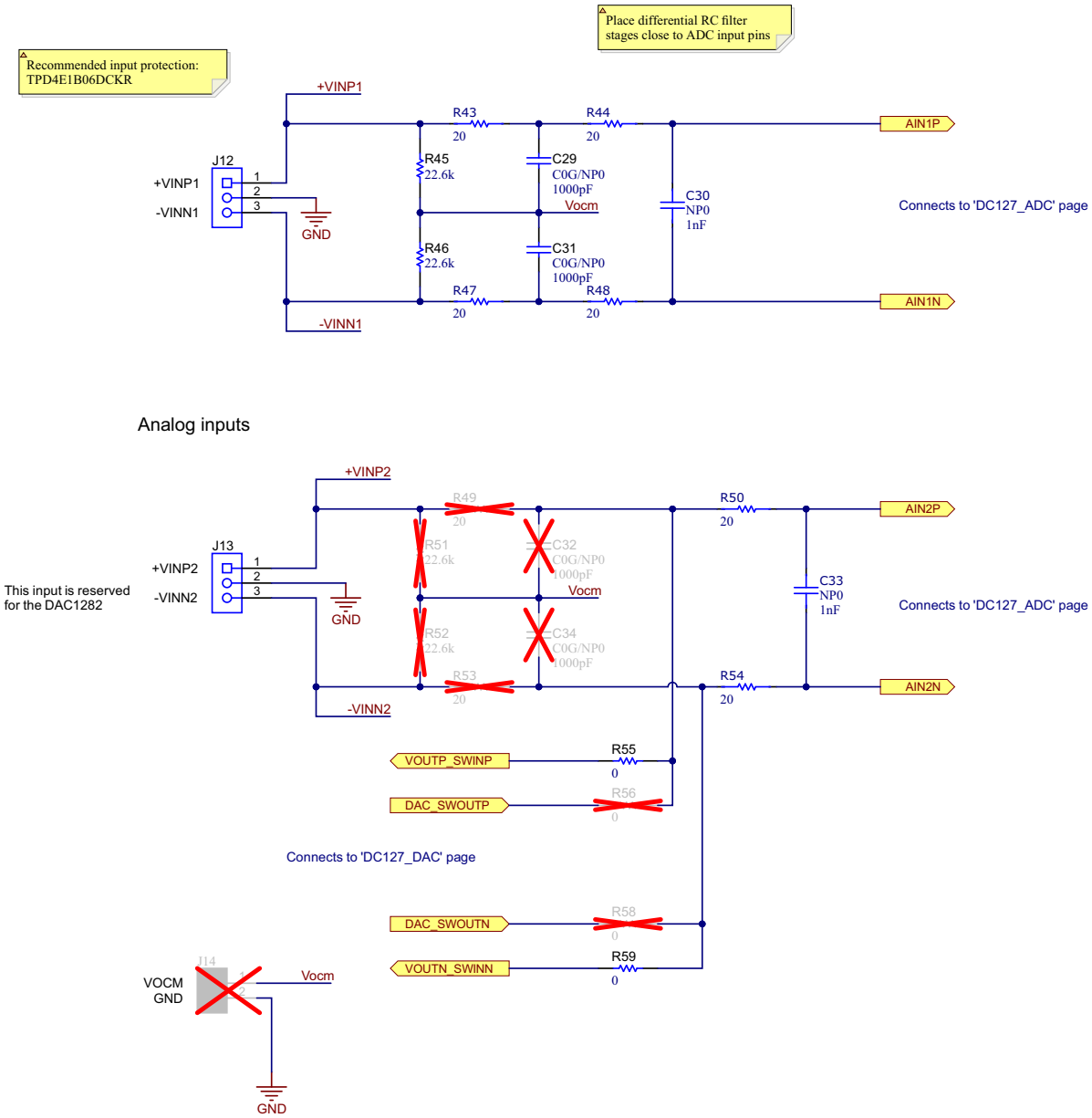


Figure 2-1. Input Terminal Blocks and Headers (Schematic)

Table 2-1. Analog Input Terminal Blocks (J12, J13)

Terminal Block	Pin	Function	ADS1285 Input Pin(s)
J12	1	Channel 1 positive input	+VINP1 (Eventually leading to AIN1P)
	2	GND	AGND and DGND
	3	Channel 1 negative input	–VINN1 (Eventually leading to AIN1N)
J13	1	Channel 2 positive input	+VINP2 (Eventually leading to AIN2P)
	2	GND	AGND and DGND
	3	Channel 2 negative input	–VINN2 (Eventually leading to AIN2N)

Do not apply an input such that the voltage on the input pins of the ADS1285 exceeds the absolute maximum ratings. For more details, see the *ADS1285 data sheet*.

R45 and R46 provide common-mode voltage paths for the channel 1 inputs. See Section 2.3 for more information. In addition, R43 and C29 (in combination with R47 and C31) provide the common-mode, low-pass filters for the positive and negative inputs, respectively. Furthermore, R44 and R40 in combination with C30 provides the differential low-pass filter used in antialiasing. The series impedance is kept relatively low to maintain adequate total harmonic distortion (THD) performance. Similar differential and common-mode, low-pass filter footprints are present on all inputs.

Specifically for channel 2, the default configuration is set up to use the DAC1282 on the input. As a result, the common-mode filters for this configuration are not populated, and R50, R54, and C33 are optimized for the output of the DAC. There are two options for connecting the DAC to the channel 2 of the ADS1285: using the direct output of the DAC1282 or the integrated switches of the DAC1282. By default, the direct output of the DAC1282 is used by populating R55 and R59. As a result, using the integrated switches is achieved by depopulating R55 and R59, populating R56 and R58, and configuring the DAC using the GUI as described in Section 2.5. For best THD performance (approximately a 1-dB difference), use the direct output. For maximum flexibility, use the integrated switches.

If necessary, use the Vocm circuit to bias a floating input (2-wire) sensor to the proper ADC input common mode level. Vocm is 2.5V with respect to GND using a unipolar power supply (AVDD1=5V, AVSS=0V with respect to GND). Vocm is 0V with respect to GND using a bipolar power supply (AVDD1=2.5V, AVSS=-2.5V with respect to GND). The Vocm voltage and buffer circuitry are installed by default on the EVM. The Vocm output header is not installed by default on the EVM. Refer to Figure 5-3 for the circuit schematic.

2.2 ADC Connections and Decoupling

Figure 2-2 shows all connections to the ADS1285 (U10). Each power supply connection has 0.1-µF and 1-µF decoupling capacitors. Make sure these capacitors are physically close to the device and have a good connection to the respective ground plane (GND or AVSS). The supply connections pass through a set of jumpers (J15). These jumpers enable power supply current measurements by the removing the shunt and inserting an ammeter between the supply power and the ADC pin. Alternatively, remove the shunts on jumper J15 and apply an external power source directly to the corresponding supply pin if desired. For more information about the required voltage and current levels for an external supply, see the Section 2.3, Table 1-2, and the ADC data sheet.

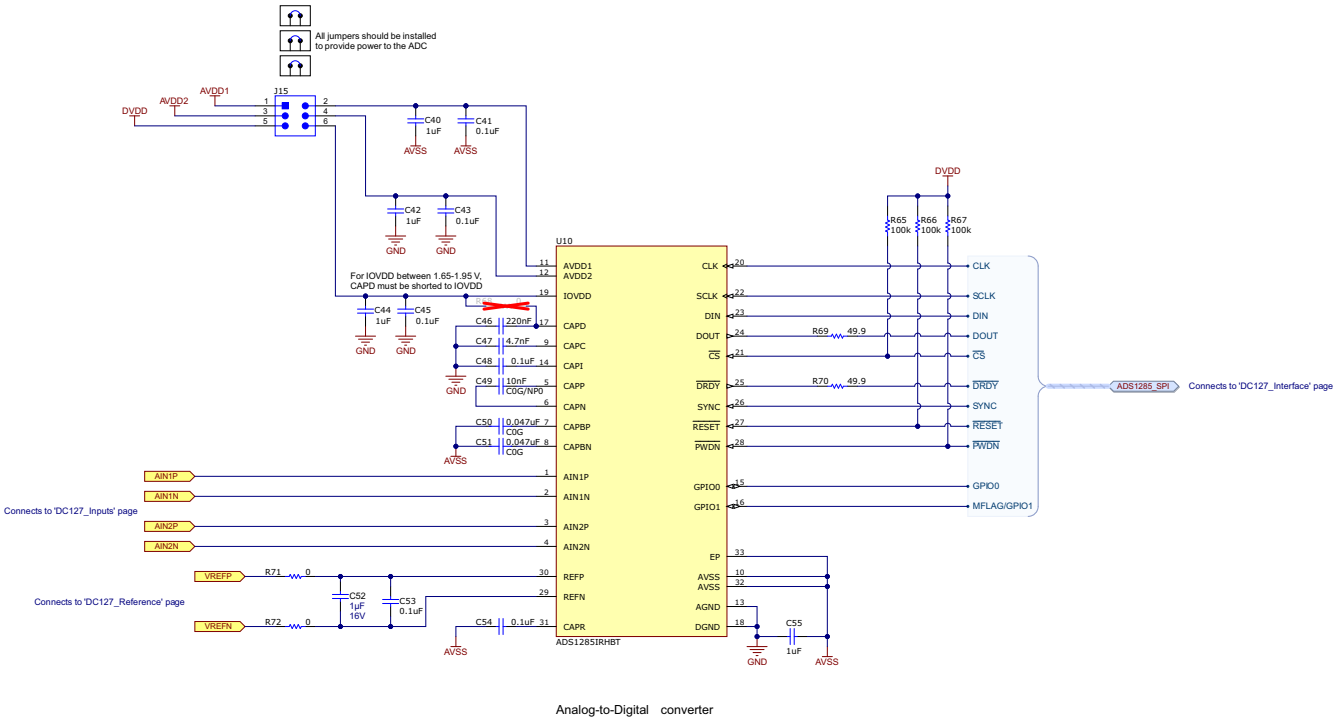


Figure 2-2. ADS1285 Connections and Decoupling

By default, the EVM IOVDD is configured for 3.3V operation. Install resistor R68 to connect IOVDD to CAPD and enable 1.8V operation. Do not use the PHI board when R68 is installed. The IOVDD absolute maximum voltage is 2.2V and the maximum operating voltage is 1.95V with R68 installed. Applying 3.3V with R68 installed causes permanent damage to the ADS1285.

Several digital pins have a 49.9Ω series resistor. These resistors smooth the edges of the digital signals to provide minimal overshoot and ringing. The $\overline{\text{CS}}$, $\overline{\text{PWDN}}$, and $\overline{\text{RESET}}$ pins each have a 100kΩ pull-up resistor. These resistors verify that the ADC powers up in a known state.

2.3 Power Supplies

The PHI provides multiple power-supply options for the EVM, derived from the USB supply of the computer that is routed to the 5.5V net on the ADS1285EVM-PDK on the board.

The EEPROM on the ADS1285EVM-PDK uses a 3.3V power supply, ID_PWR, generated directly by the PHI. The 3.3V supply to the digital section of the ADC (3V3_IOVDD) is provided directly by a separate LDO on the PHI.

Figure 2-3 and Table 2-2 describe the supply generation and programmable configurations, respectively.

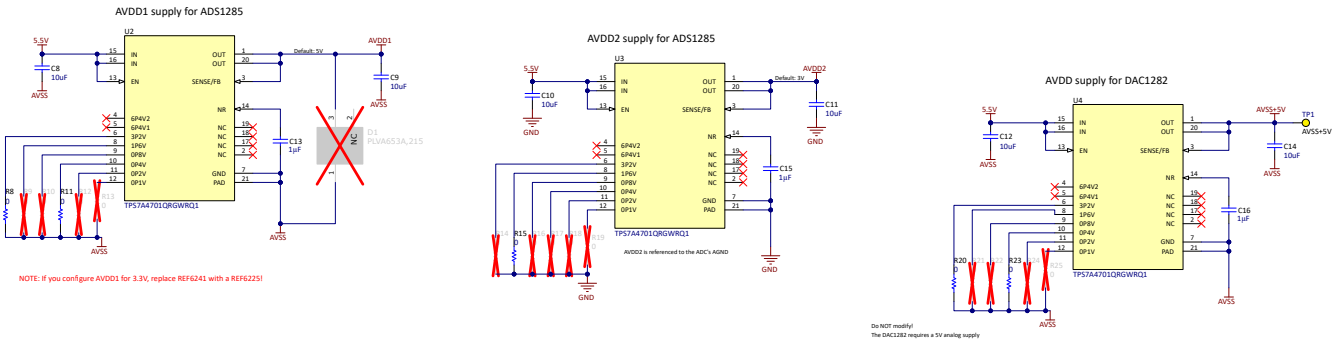


Figure 2-3. ADS1285EVM-PDK AVDD1, AVDD2, and AVSS+5V Supply Generation (Schematic)

Table 2-2. Programmable LDO Configurations

V_{OUT} (V)(2)	3P2V	1P6V	0P8V	0P4V	0P2V	0P1V
2.5	—	—	Installed(1)	—	Installed	Installed
3.0	—	Installed	—	—	—	—
3.3	—	Installed	—	—	Installed	Installed
4.5	—	Installed	Installed	Installed	Installed	Installed
5.0	Installed	—	—	Installed	—	—

(1) Installed = Solder a 0Ω jumper to GND/AVSS.
(2) V_{OUT} = 1.4V + Σ (all grounded pins).

The PGA positive analog supply of the ADC, AVDD1, is supplied by the TPS7A4701 (U2). The TPS7A4701 is a low-noise, configurable-output linear regulator that uses the PHI 5.5V output voltage to generate a clean 5V supply for AVDD1 by default. Install or remove resistors R8 to R13 to change the LDO output voltage if desired. This LDO (U2) is referenced to AVSS such that AVDD1 is the same level relative to AVSS using either a unipolar or bipolar power supply.

AVDD2 is the modulator analog supply that is also used by the ADC. As with AVDD1, AVDD2 is generated by another TPS7A4701 (U3). This LDO uses the PHI 5.5V output voltage to generate a clean 3V supply for AVDD2 by default. Install or remove resistors R14 to R19 to change the LDO output voltage if desired. However, this LDO (U3) is referenced to GND such that AVDD2 is a different level relative to AVSS using a unipolar power supply compared to using a bipolar power supply. Verify that the AVDD2 voltage is within data sheet specifications when operating the EVM in either mode. Additionally, increasing or decreasing the AVDD2 voltage results in higher or lower THD performance, respectively, in unipolar mode.

AVSS+5V is used for the analog supply of the DAC1282. This pin also uses a TPS7A470x (U4) onboard the EVM, which is a low-noise linear regulator that uses the 5.5V supply on the PHI to generate a cleaner 5V output. The DAC1282 requires a 5V supply so R20 to R25 must not be modified.

The user has the option to configure the EVM for unipolar supplies (AVSS = 0V) by placing a jumper to cover pins 1 and 2 of J4 (UNIPOL), or to configure the EVM for bipolar supplies (AVSS = –2.5V) by placing the jumper to cover pins 2 and 3 of J4 (BIPOL). The TPS7A3001 (U5) is an LDO with a V_{IN} range from –3V to –36V that provides a clean –2.5V output for the AVSS voltage. However, an external voltage is needed to supply the AVSS voltage, which can be supplied using J3. Figure 2-4 shows the supply selection and –2.5V generation circuit.

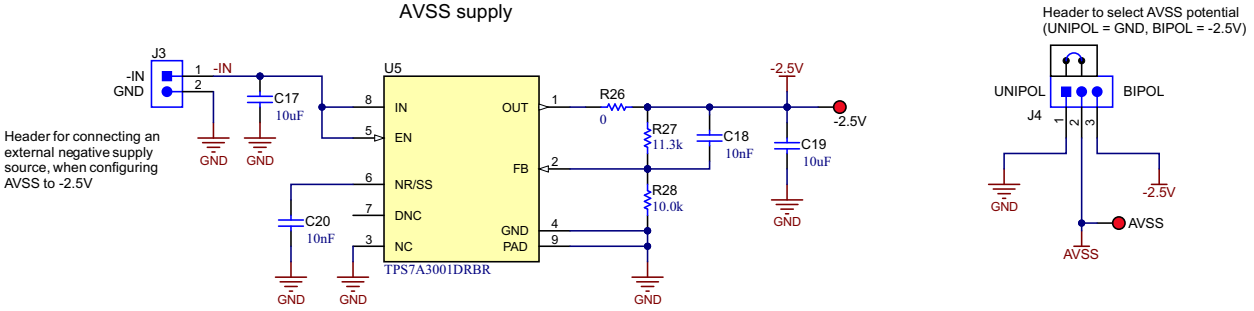


Figure 2-4. ADS1285EVM-PDK Negative LDO and Unipolar or Bipolar Supply Selection (Schematic)

AVDD1 is used as the supply for the REF6241, which is a high-precision voltage reference with an integrated high-bandwidth buffer in reference to AVSS. The voltage reference can be used to supply the positive reference, VREFP, for the ADC and DAC using resistor R38. Alternatively, remove resistors R38 and R42 to apply external positive and negative reference voltages using pins 1 and 2 of J10, respectively.

Figure 2-5 shows a schematic of the voltage reference.

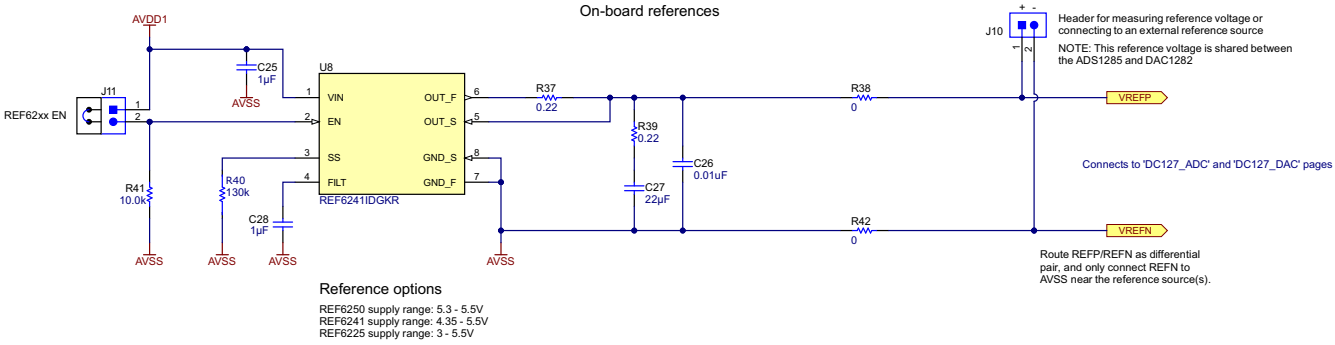


Figure 2-5. Voltage Reference (Schematic)

The power supply for each active component on the EVM is bypassed with a ceramic capacitor placed close to that component. Where possible, the EVM layout uses thick traces or large copper fill areas between bypass capacitors and their loads to minimize inductance along the load current path.

As mentioned previously in Section 1, power to the EVM is supplied by the PHI through connector J5. For information about PHI pins and the power connections, see Table 2-3.

With modifications, the user can use external supplies for any voltage supplies. Using the ADC PWR header (J26), DAC PWR header (J1), and the unipolar or bipolar select (J4); the shunts can be depopulated for direct access to the AVDD1, AVDD2, AVSS+5V, DVDD, and AVSS pins.

2.4 ADC Input Clock (CLK) Options

The main ADC clock signal (CLK) generates the ADS1285 modulator clock (f_{MOD}) in one of two ways:

- A crystal oscillator and the accompanying clock dividers can provide a selectable frequency for the entire range of the ADC.
  - The onboard crystal oscillator (Y1) provides the nominal 8.192MHz clock frequency (default)
  - The dividers (U6) step down the frequency to 4.096MHz
  - J8 allows the user to select between these frequencies and connect them directly to CLK by using a shunt
- Provide an external main clock to a subminiature version A (SMA) connector (J5) or to pins 4 or 2 of J7 when a shunt does not select the frequency from the crystal oscillator.
  - In this case, a shunt must not cover J7 so that CLK is connected to any of the crystal oscillator signals
  - Be sure to review the valid CLKIN input frequency in the data sheet

Note

All clock sources are sourced back to the PHI connector (J6) so that SCLK is synchronous to CLK.

Figure 2-6 shows a schematic for the clock source.

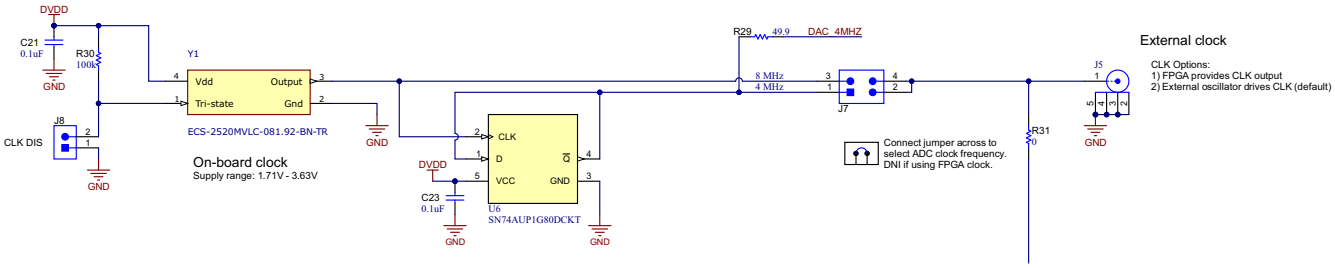


Figure 2-6. CLK Source (Schematic)

2.5 Digital-to-Analog Converter (DAC)

The ADS1285EVM-PDK includes a DAC1282, which is a fully integrated digital-to-analog converter (DAC) that provides a low-distortion, digital-synthesized voltage output designed for testing seismic equipment and the ADS128x family of devices. For more information, see the *DAC1282 Low Distortion Digital-to-Analog Converter for Seismic Data Sheet*. The DAC1282 can be used in combination with the GUI to directly supply an input voltage for testing and performance purposes. For more information on configuring the inputs to use the DAC1282, see Section 2.1.

The DAC output frequency in Sine mode is programmable from 0.5Hz to 250Hz and the magnitude is scaled by both analog and digital control. The analog gain is adjustable in 6-dB steps and the digital gain in 0.5-dB steps. The analog gain settings match those of the ADS1285 for high-resolution testing at all gains. Control the DAC1282 settings using the *DAC Configuration* page of the GUI as explained in Section 4.2.6.

The DAC1282 uses AVSS+5V and DVDD for the power supplies and shares the same reference as the ADS1285. This configuration minimizes potential errors from using separate references between the devices. However, most of the DAC1282 documentation is in reference to a 5V supply while the ADS1285EVM-PDK uses a 4.096V reference by default. As a result, the DAC output amplitude is scaled in reference to the 4.096V reference through the following equation:

$$V_{out\_peak} = V_{FSR\_peak} \times 10^{\frac{G_{DAC\_Dig(dB)}}{20}} \quad (1)$$

where:

- V_{out_peak} = Output amplitude of the DAC in Sine mode
- V_{FSR_peak} = Positive peak of the full-scale range calculation, which depends on voltage reference
- $G_{DAC\_Dig(dB)}$ = Digital gain of the DAC determined by the SINEG register

This equation and scaling is automatically calculated in the ADS1285EVM-PDK GUI; see Section 4.2.6.

2.6 Digital Interface

As noted in Section 1, the EVM interfaces with the PHI and communicates with the computer over the USB. There are two devices on the EVM with which the PHI communicates: the ADS1285 ADC (over SPI) and the EEPROM (over I2C). The EEPROM comes pre-programmed with the information required to configure and initialize the ADS1285EVM-PDK GUI. When the hardware is initialized, the EEPROM is no longer used.

2.7 Connection to the PHI

The ADS1285EVM-PDK board communicates with the PHI through a shrouded, 60-pin connector, J6. There are two round standoffs next to J6 with Phillips-head screws. Connect the PHI to the EVM by first removing the screws, then attaching the PHI to the EVM, and then installing the screws into the standoffs. The screws secure the EVM to the PHI and makes sure the connection between the boards.

Table 2-3 lists the different PHI connection and their functions.

Table 2-3. PHI Connector Pin Functions

PHI Connector Pin Name	PHI Connector Pin	Function
5.5V	J6[1]	Power-supply source for the analog section of the EVM
GND	J6[3]	Ground
~RESET	J6[6]	ADC reset pin, active low
~PWDN	J6[8]	ADC power-down pin, active low
SYNC	J6[10]	ADC synchronization, active high
DIN_PHI	J6[12]	SPI: DIN from the ADC, PICO, or serial interface data in (pre-RTM GUI revision compatibility)
GPIO1	J6[14]	General-purpose I/O 1 pin from the ADC
GPIO0	J6[16]	General-purpose I/O 0 pin from the ADC
DIN_PHI	J6[18]	SPI: DIN from the ADC, PICO, or serial interface data in (RTM GUI revision compatibility)
~CS_ADC	J6[22]	SPI: $\overline{CS}$, chip-select, or serial interface select, active low for the ADC
SCLK_PHI	J6[24]	SPI: Serial interface clock, or SCLK
CAPCLK_OUT	J6[26]	Output path for the PHI signal to synchronize captures with any delay from the EVM
CAPCLK_IN	J6[28]	Input path for the PHI signal to synchronize captures with any delay from the EVM
~DRDY	J6[30]	SPI: Data-ready signal for the ADS1285; active-low $\overline{DRDY}$
ADC_CLK (input)	J6[32]	Input for the PHI to sense CLK
ADC_CLK (output)	J6[34]	Possible output for the PHI to provide CLK (not supported on the ADS1285EVM-PDK)
DOUT	J6[38]	SPI: Serial data output for the ADS1285, or POCI
~RST/PWDN_DAC	J6[46]	Reset or power-down input pin for the DAC1282
SYNC_DAC	J6[48]	Synchronize input pin for the DAC1282
WP	J6[49]	Write protection for the EEPROM
DVDD	J6[50]	Power-supply source for the digital section of the EVM
SW/TD_DAC	J6[52]	Switch control input or bitstream input pin for the DAC1282
~CS_DAC	J6[54]	SPI: Serial port chip select, or $\overline{CS}$, for the DAC1282
SDA	J6[56]	I2C serial data for the EEPROM used to identify the EVM
SCL	J6[58]	I2C serial clock for the EEPROM used to identify the EVM
ID_PWR	J6[59]	Power-supply source for the EEPROM used to identify the EVM
GND	J6[60]	Ground

2.8 Digital Header

In addition to the PHI, the EVM has a header connected to the digital lines that can be used to connect a logic analyzer or oscilloscope. This placement allows for easy access to the digital communications. Header J9 is connected to the digital lines between the ADS1285 and the PHI connector. Table 2-4 describes the digital header pins.

Table 2-4. Digital Header Pins

Signal Name	Digital Header Pin
~RESET	J9[1]
~PWDN	J9[3]
SYNC	J9[5]
GPIO1	J9[7]
GPIO0	J9[9]
DIN_PHI	J9[11]
~CS_ADC	J9[13]
SCLK_PHI	J9[15]
~DRDY	J9[17]
ADC_CLK	J9[19]
DOUT	J9[21]
~RST/PWDN_DAC	J9[23]
SYNC_DAC	J9[25]
SW/TD_DAC	J9[27]
~CS_DAC	J9[29]

3 Software Installation

Download the latest version of the EVM GUI installer from the *Tools and Software* folder of the ADS1285EVM-PDK and run the GUI installer to install the EVM GUI software on your computer.

CAUTION

Manually disable any antivirus software running on the computer before downloading the EVM GUI installer onto the local hard disk. Depending on the antivirus settings, an error message can appear or the installer. The .exe file can be deleted.

Accept the license agreements and follow the on-screen instructions shown in Figure 3-1 to complete the installation.

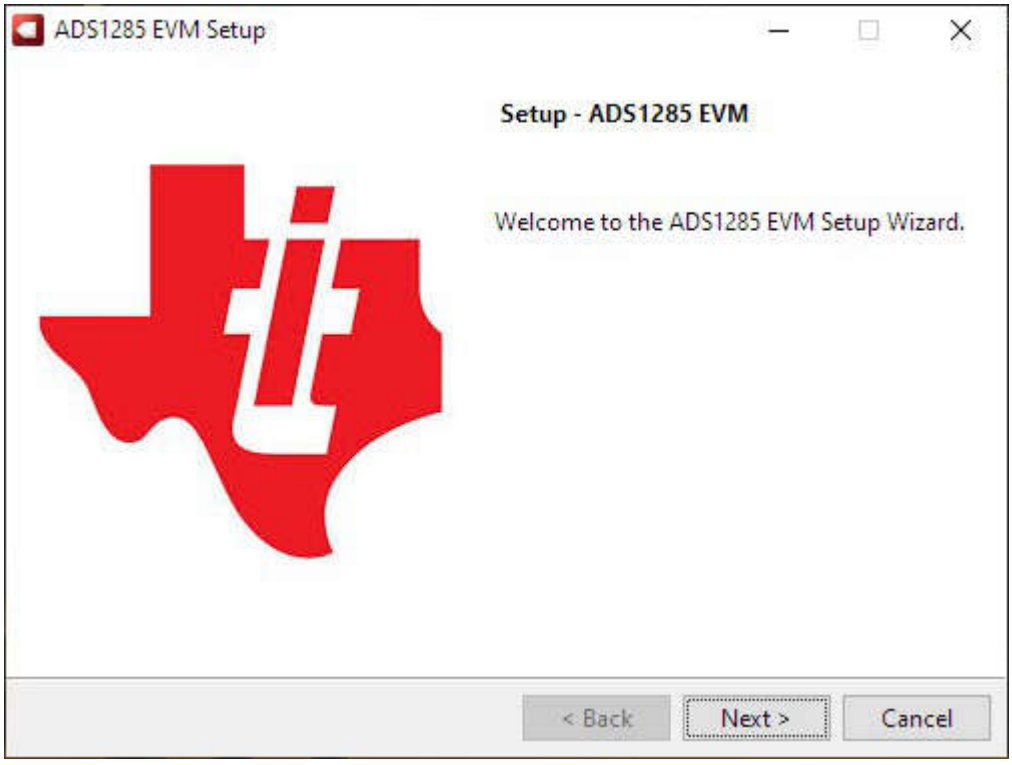


Figure 3-1. ADS1285 Software Installation Prompt

As part of the ADS1285EVM-PDK GUI installation, a prompt with a device driver installation (as shown in Figure 3-2) appears on the screen. Click *Next* to proceed.

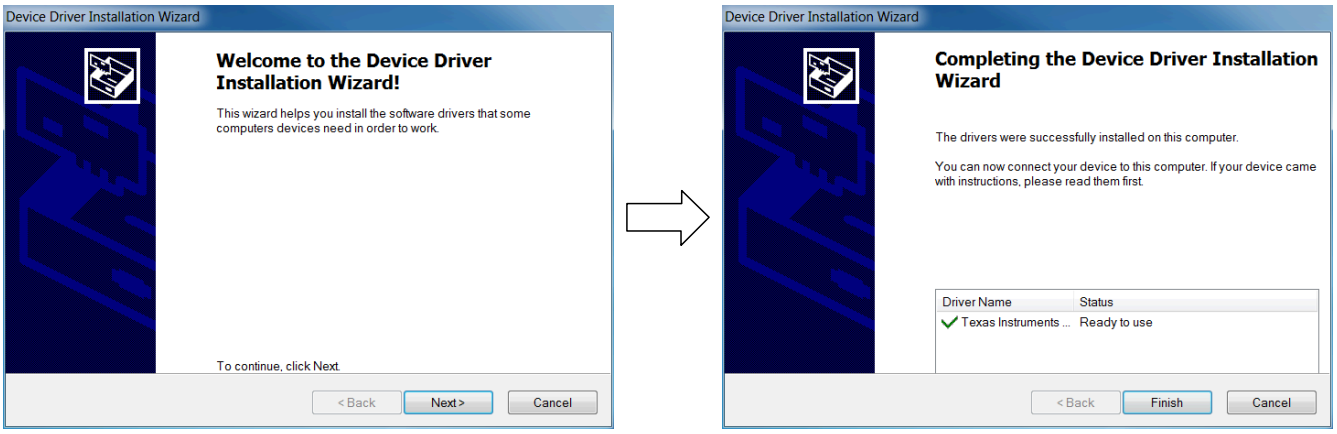


Figure 3-2. Device Driver Installation Wizard Prompts

Note

A notice can appear on the screen stating that Windows cannot verify the publisher of this driver software. Select *Install this driver software anyway*.

The ADS1285EVM-PDK requires the LabVIEW® run-time engine and can prompt for the installation of this software, as shown in Figure 3-3, if not already installed.

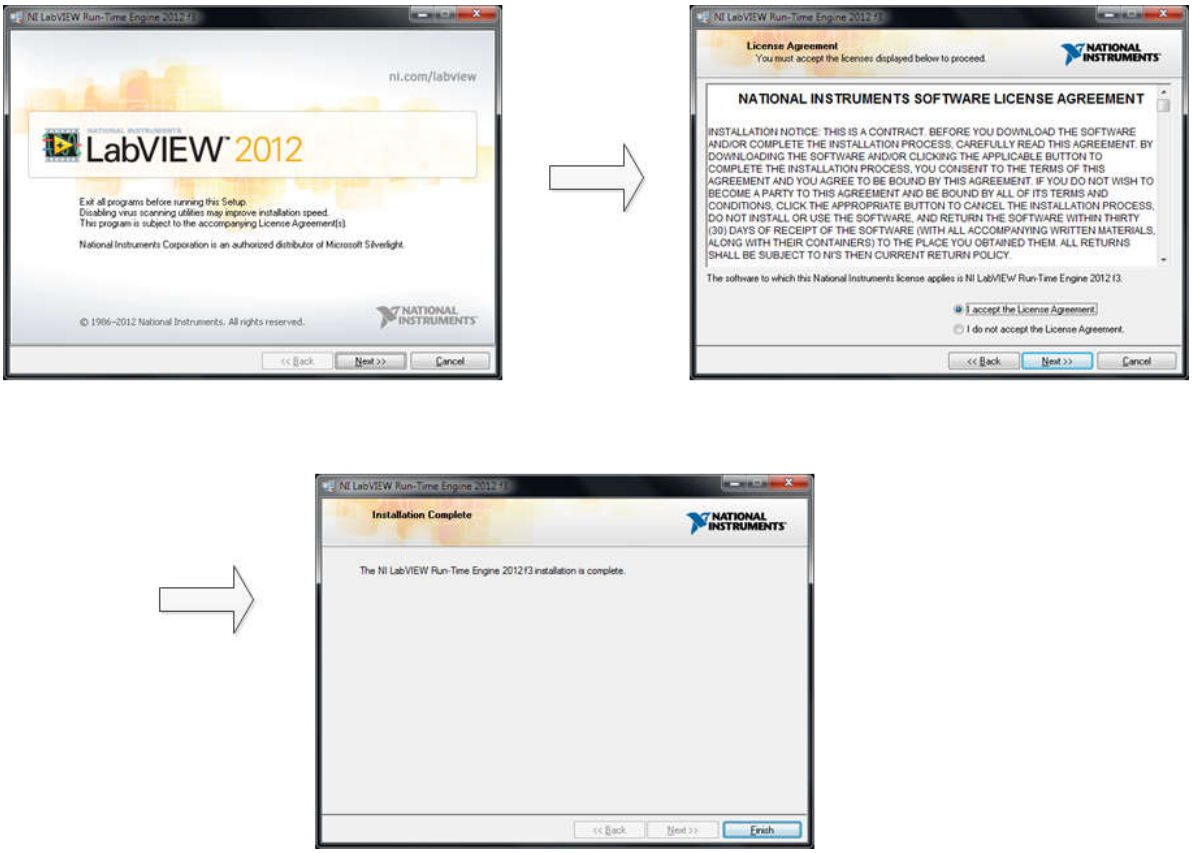


Figure 3-3. LabVIEW Run-Time Engine Installation

4 EVM Configuration and GUI Operation

This section explains the initial hardware setup as well as the GUI behavior so the user can successfully operate the ADS1285EVM-PDK.

4.1 EVM Configuration

After unpacking, the EVM is already configured with the default jumper settings. Figure 4-1 shows the locations for the default jumpers and Table 4-1 shows the functions of the default shunts.

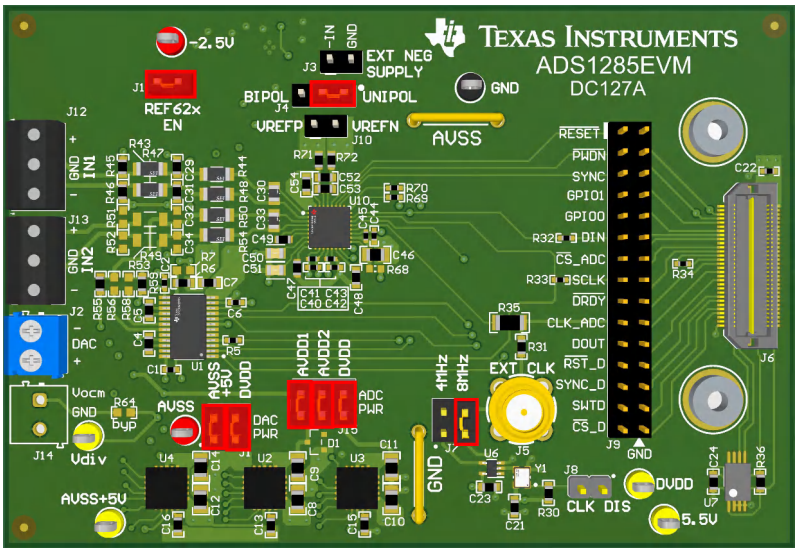


Figure 4-1. ADS1285EVM-PDK Jumper Default Settings

Table 4-1. Default Shunt Settings

Header Designator	Position	Function
J11	[1-2]	Enables the REF62x supply to VREFP
J4	[1-2]	Connects AVSS to GND for unipolar ADC supply mode
J7	[3-4]	Connects CLK to an 8.192-MHz source from the crystal oscillator
J10	Not installed	Header to supply the external reference voltage to VREFN and VREFP
J1	[1-2]	DAC PWR: Connects the output of the U4 LDO (AVSS+5V) to the DAC analog supply pin (AVDD)
J1	[3-4]	DAC PWR: Connects the PHI digital supply (DVDD) to the DAC digital supply pin (DVDD)
J15	[1-2]	ADC PWR: Connects the output of the U2 LDO (AVDD1) to the ADC analog supply 1 (AVDD1)
J15	[3-4]	ADC PWR: Connects the output of the U3 LDO (AVDD2) to the ADC analog supply 2 (AVDD2)
J15	[5-6]	ADC PWR: Connects the PHI digital supply (DVDD) to the ADC digital supply (IOVDD)
J3	Not installed	Header to supply the external input to U5 for the –2.5-V supply
J8	Not Installed	Disables 8.192-MHz crystal oscillator

Table 4-2 lists the nominal voltages that result from the default configuration.

Table 4-2. Nominal Voltages Resulting From a Default Configuration

Supply Name	Voltage (Referenced to GND)
AVSS	GND (0V)
AVSS+5V	5V
DVDD (IOVDD)	3.3V
AVDD1	5V
AVDD2	3V
5.5V	5.5V
REFP	4.096V
–2.5V	NA, external supply needed to generate –2.5V

4.2 GUI Operation

4.2.1 EVM GUI Global Settings for ADC Control

Although the EVM GUI does not allow direct access to the levels and timing configuration of the ADC digital interface, the EVM GUI does give users high-level control over many other functions of the ADS1285, including: internal clock dividers, oversampling ratio (OSR), and number of samples to be captured. Figure 4-2 identifies the input parameters of the GUI (as well as their default values) through which the various functions of the ADS1285 can be exercised.

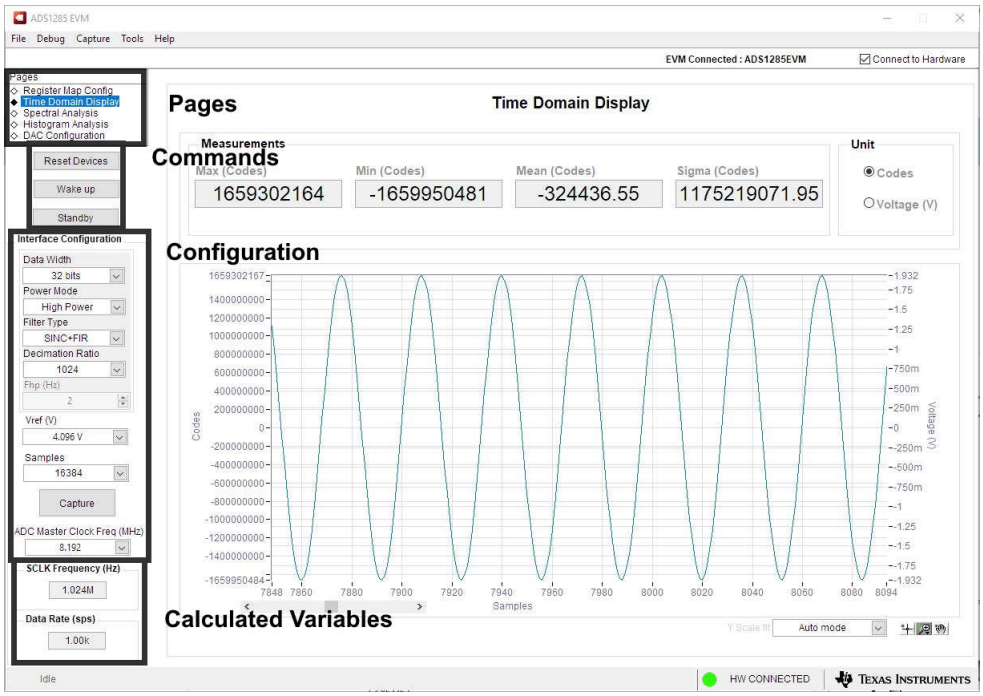


Figure 4-2. EVM GUI Global Input Parameters

There are four pages available in the ADS1285EVM-PDK GUI. The information area displays the results of each of the pages. Each of these pages display a different control or measurement of the device. The *Register Map Config* page reads and writes the registers of the device. The *Time Domain Display* page collects a set of data from the device and displays the result. The *Spectral Analysis* page can compute the FFT of the collected data, and the *Histogram Analysis* page shows a histogram of the collected data and displays basic statistics of the result.

The *Single Commands* section allows for direct control of the device for three basic functions. First, the **Reset** button sends a signal to the RESET pin to reset the device. The **Standby** button puts the device into a low-power state where all channels are disabled, and the reference and other non-essential circuitry are powered down. The **Wakeup** button exits standby mode.

The *Interface Configuration* section also sets the data rate by setting the internal clock dividers and OSR in the ADC. Finally, this section can set the power modes in the registers. The ADS1285 has three power modes (low-power, mid-power, and high-power) that are configured in the CONFIG0 register (bits 7-6). This configuration is used in conjunction with the jumper settings of JP8 for the CLK pin, as outlined in Section 2.4.

The *Clock and Sampling Rate* section allows the user to specify a target SCLK frequency (in Hz) and the GUI tries to match this frequency as closely as possible by changing the PHI PLL settings, but the achievable frequency can differ from the target value entered. This section also displays the sampling rate of the ADC as controlled by the internal clock dividers and the OSR.

The GUI is switched between hardware mode and simulation mode by checking and unchecking the *Connected to Hardware* box in the top right area of the screen at any time.

4.2.2 Register Map Configuration Tool

The register map configuration tool allows the user to view and modify the registers of the ADS1285. This tool can be selected, as indicated in Figure 4-3, by clicking on the **Register Map Config** radio button at the *Pages* section of the left pane. On power-up, the values on this page correspond to the *Host Configuration Settings* that enable ADC sampling at the maximum sampling rate specified for the ADC. The register values can be edited by double-clicking the corresponding value field. If interface mode settings are affected by the change in register values, this change reflects on the left pane immediately.

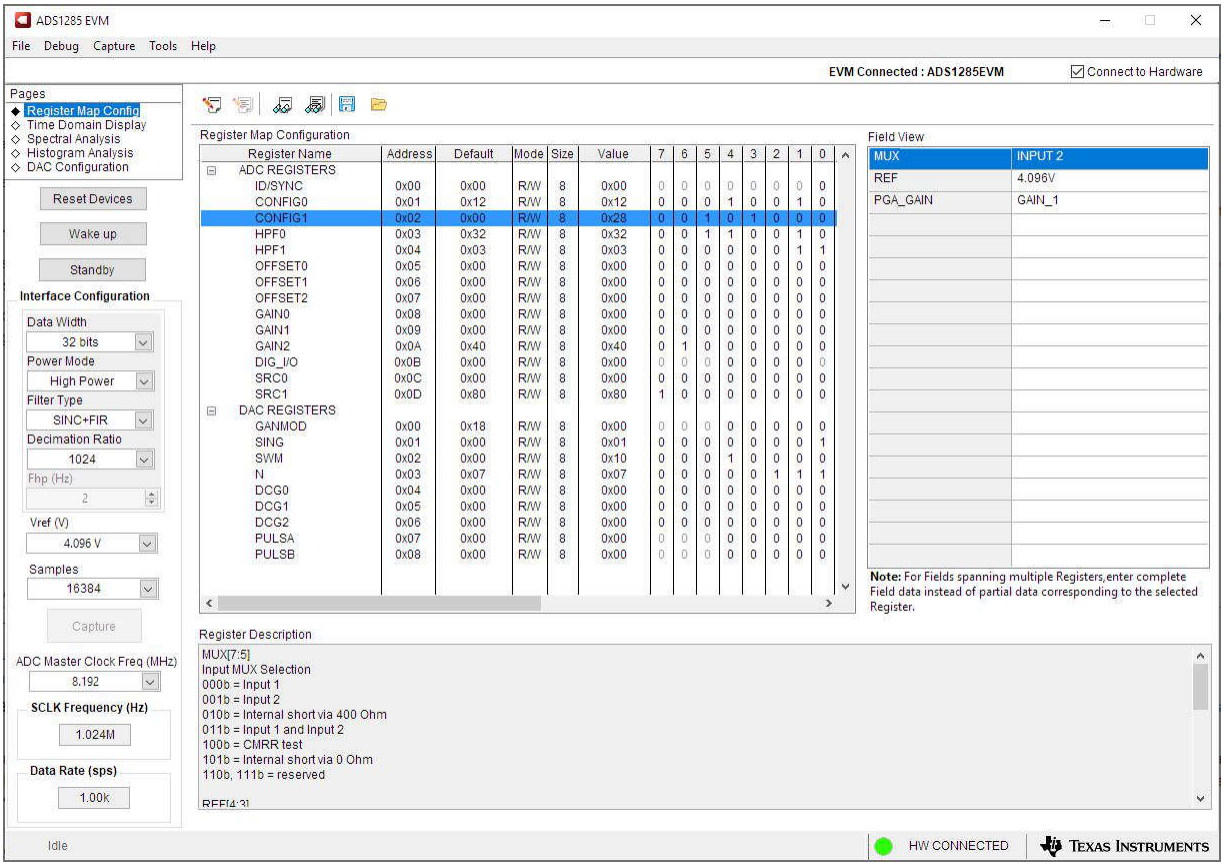


Figure 4-3. Register Map Configuration

Section 4.2.3 through Section 4.2.5 describe the data collection and analysis features of the ADS1285EVM-PDK GUI.

4.2.3 Time Domain Display Tool

The time domain display tool allows visualization of the ADC response to a given input signal. This tool is useful for both studying the behavior and debugging any gross problems with the ADC or drive circuits.

The user can trigger a capture of the data of the selected number of samples from the ADS1285EVM-PDK, as per the current interface mode settings indicated in Figure 4-4 by using the **Capture** button. The sample indices are on the x-axis and there are two y-axes showing the corresponding output codes as well as the equivalent analog voltages based on the specified reference voltage. Switching pages to any of the *Analysis* tools described in the subsequent sections causes calculations to be performed on the same set of data.

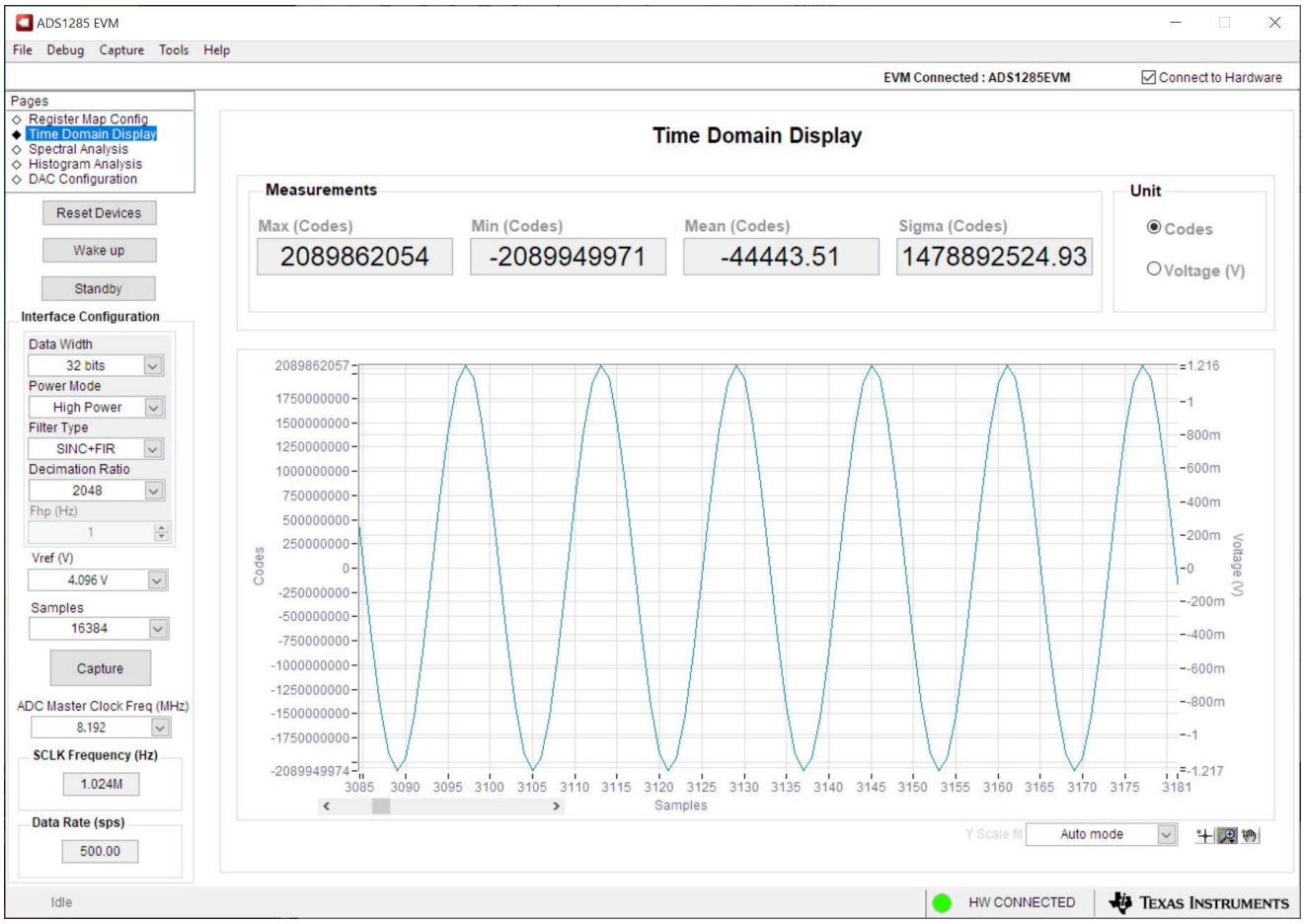


Figure 4-4. Time Domain Display Tool Options

4.2.4 Spectral Analysis Tool

The spectral analysis tool, shown in Figure 4-5, is intended to evaluate the dynamic performance (SNR, THD, SFDR, SINAD, and ENOB) of the ADS1285 ADC through single-tone sinusoidal signal FFT analysis using the *7-term Blackman-Harris* window setting.

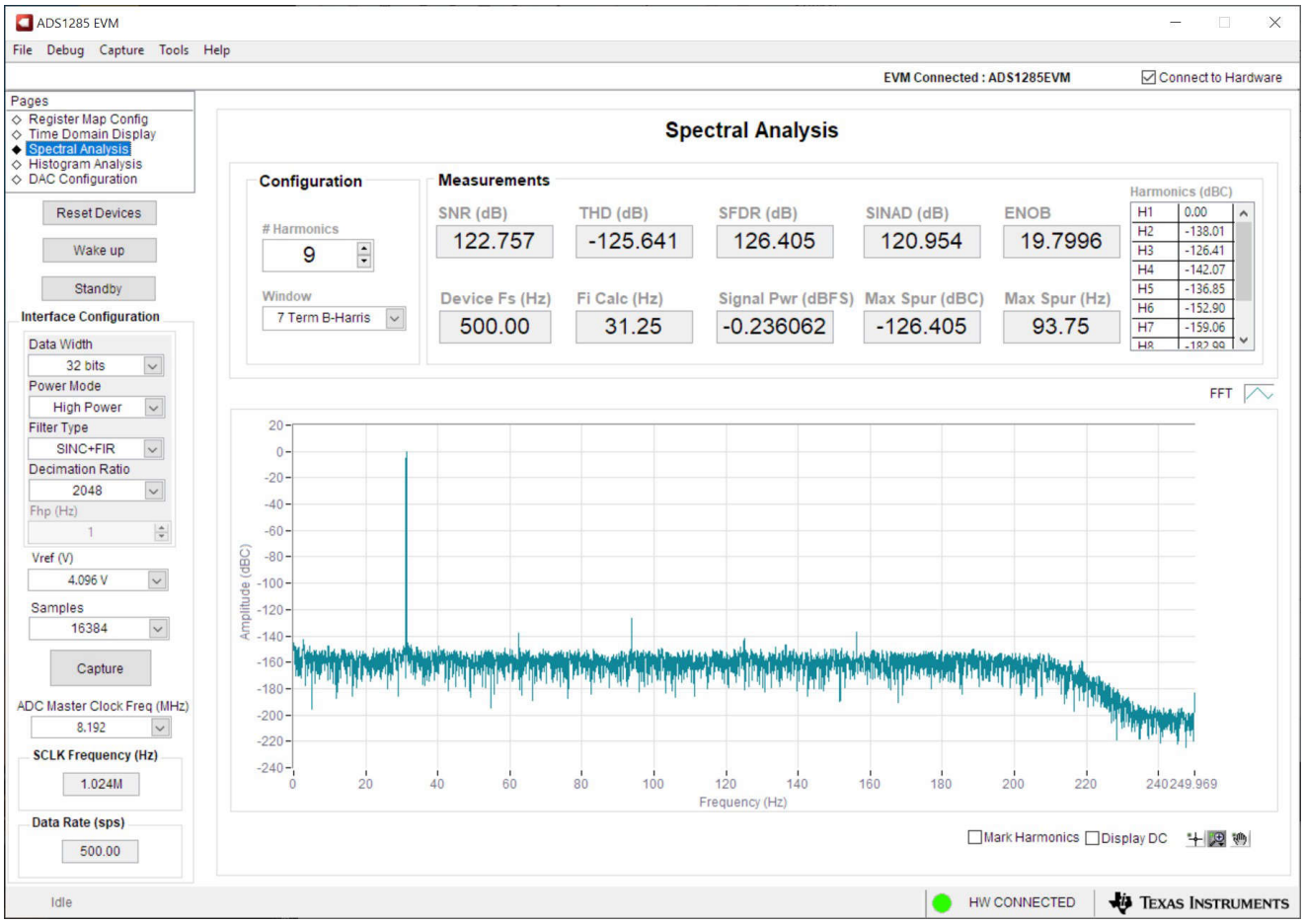


Figure 4-5. Spectral Analysis Tool

The FFT tool includes windowing options that are required to mitigate the effects of non-coherent sampling (this discussion is beyond the scope of this document). The *7-Term Blackman-Harris* window is the default option and has sufficient dynamic range to resolve the frequency components of up to a 24-bit ADC. The *None* option corresponds to not using a window (or using a rectangular window) and is not recommended.

4.2.5 Histogram Tool

Noise degrades ADC resolution and the histogram tool can be used to estimate effective resolution, which is an indicator of the number of bits of ADC resolution losses resulting from noise generated by the various sources connected to the ADC when measuring a DC signal. The cumulative effect of noise coupling to the ADC output from sources such as the input drive circuits, the reference drive circuit, the ADC power supply, and the ADC is reflected in the standard deviation of the ADC output code histogram that is obtained by performing multiple conversions of a DC input applied to a given channel.

As shown in Figure 4-6, the histogram corresponding to a DC input is displayed on clicking the **Capture** button.

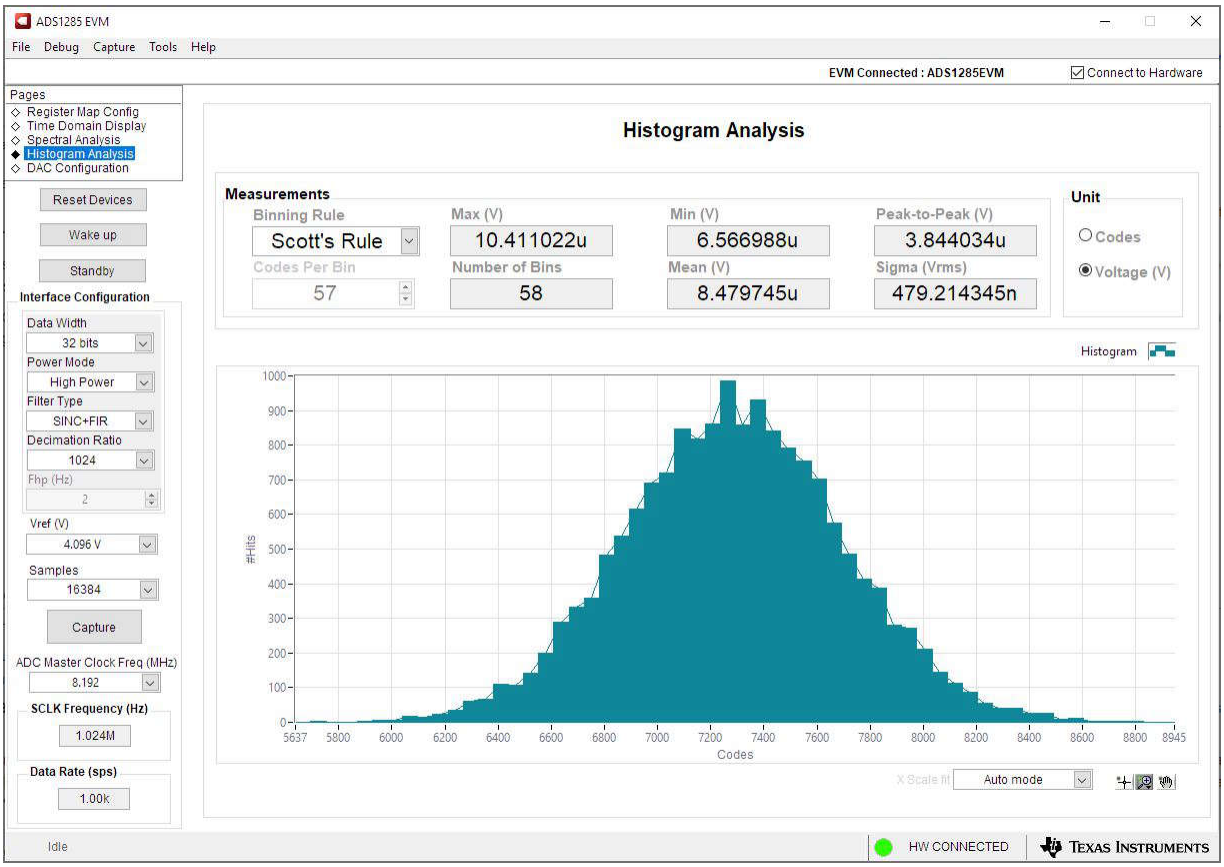


Figure 4-6. Histogram Analysis Tool

4.2.6 DAC Configuration Tool

The DAC configuration tool page shown in Figure 4-7 controls the onboard DAC1282, a test DAC specifically designed to work with the ADS128x family of devices. As previously discussed in Section 2.5, the DAC output frequency is programmable from 0.5Hz to 250Hz and the magnitude is scaled by both analog and digital control. The analog gain is adjustable in 6-dB steps and the digital gain in 0.5-dB steps. The analog gain settings match those of the ADS1285 for testing at all gains with high resolution. More information about each setting can be found in the DAC1282 data sheet.

In general, the most important DAC settings are the mode, output amplitude, and output frequency (if applicable). In the middle, the *Operation* box shows the Mode drop-down, which offers the following options: Sine, DC, digital pulse, and pulse.

The Sine option determines the amplitude by a combination of the analog gain and digital gain settings. In addition, the DAC page uses the Vref (V) drop-down menu to calculate the values in the gray boxes, although the DAC does not need to know the reference voltage to function. As a result, review the Sine AMP (Vp) calculation, in combination with the ADC gain on the register map page, to understand the output code and voltage of the ADC. The frequency is determined by typing a desired frequency into the *Desired Frequency (Hz)* text box. The GUI automatically displays the closest Freq, M, and N values to achieve the desired output frequency that are eventually written into the DAC registers. These options dynamically change when selecting DC, digital pulse, or pulse.

As mentioned in Section 2.1, the direct DAC output or the DAC integrated switches can be used. Assuming the correct hardware is changed to support the integrated switches, the state of the switches can be changed using the Switch Control drop-down.

The settings in Figure 4-7, in combination with selecting 2V/V for PGA_GAIN and Input 2 for MUX, create the time domain and spectral analysis plots in Figure 4-4 and Figure 4-5, respectively.

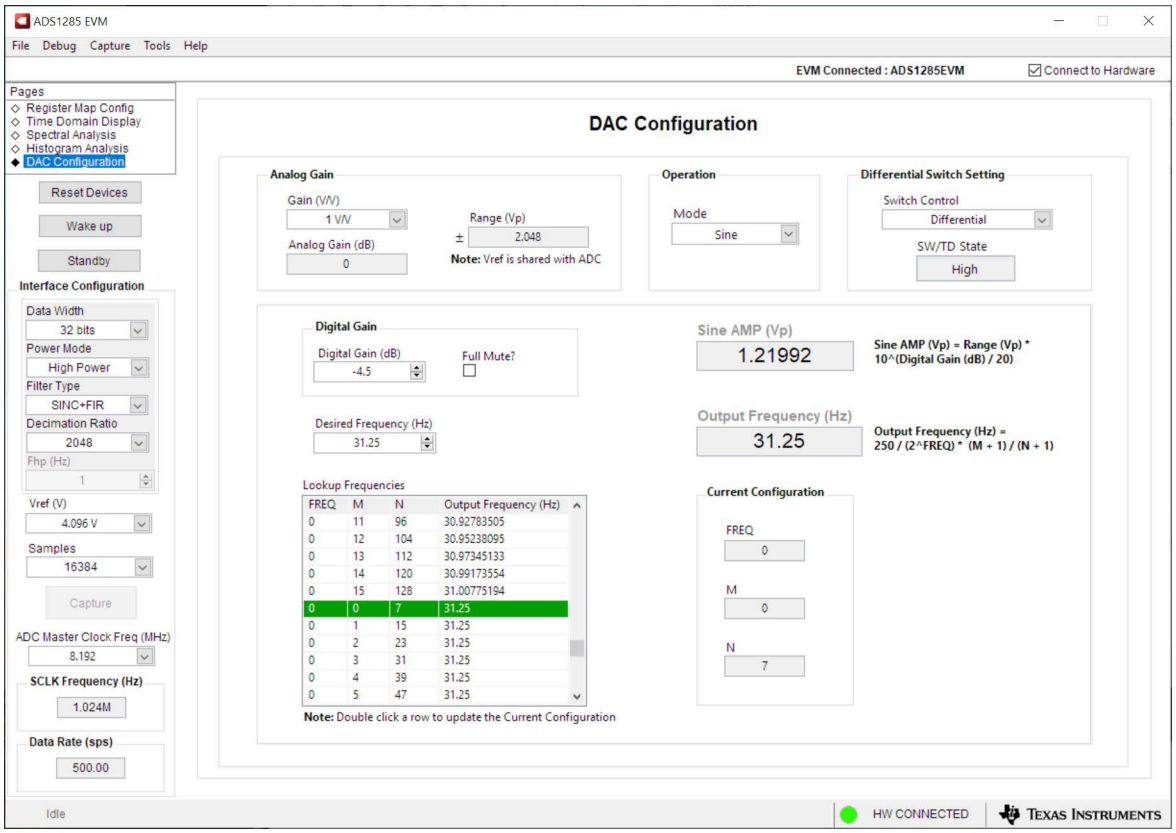


Figure 4-7. DAC Configuration Tool Page

5 Hardware Design Files

5.1 Schematics

Figure 5-1 shows a block diagram of the ADS1285EVM-PDK.

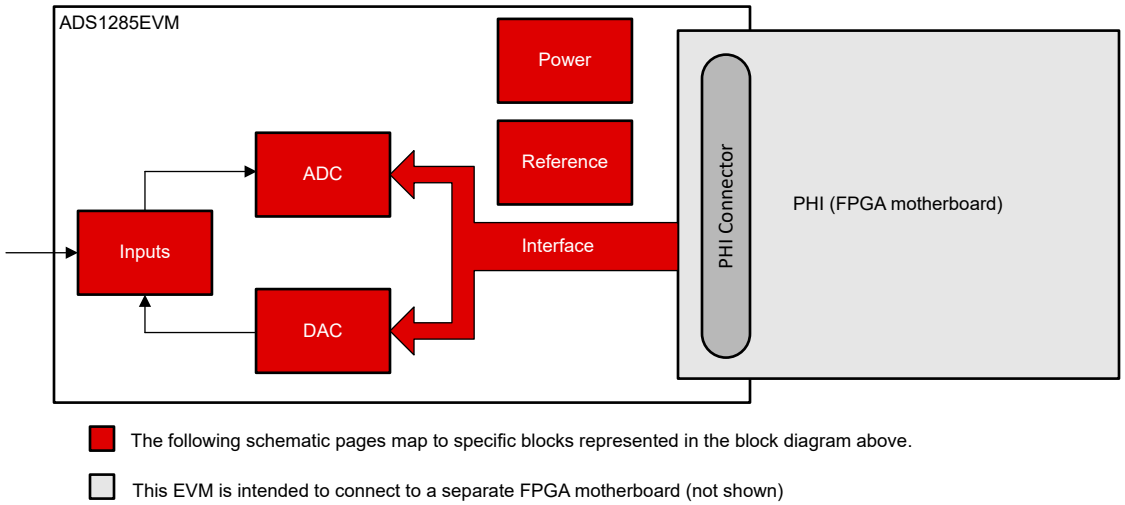
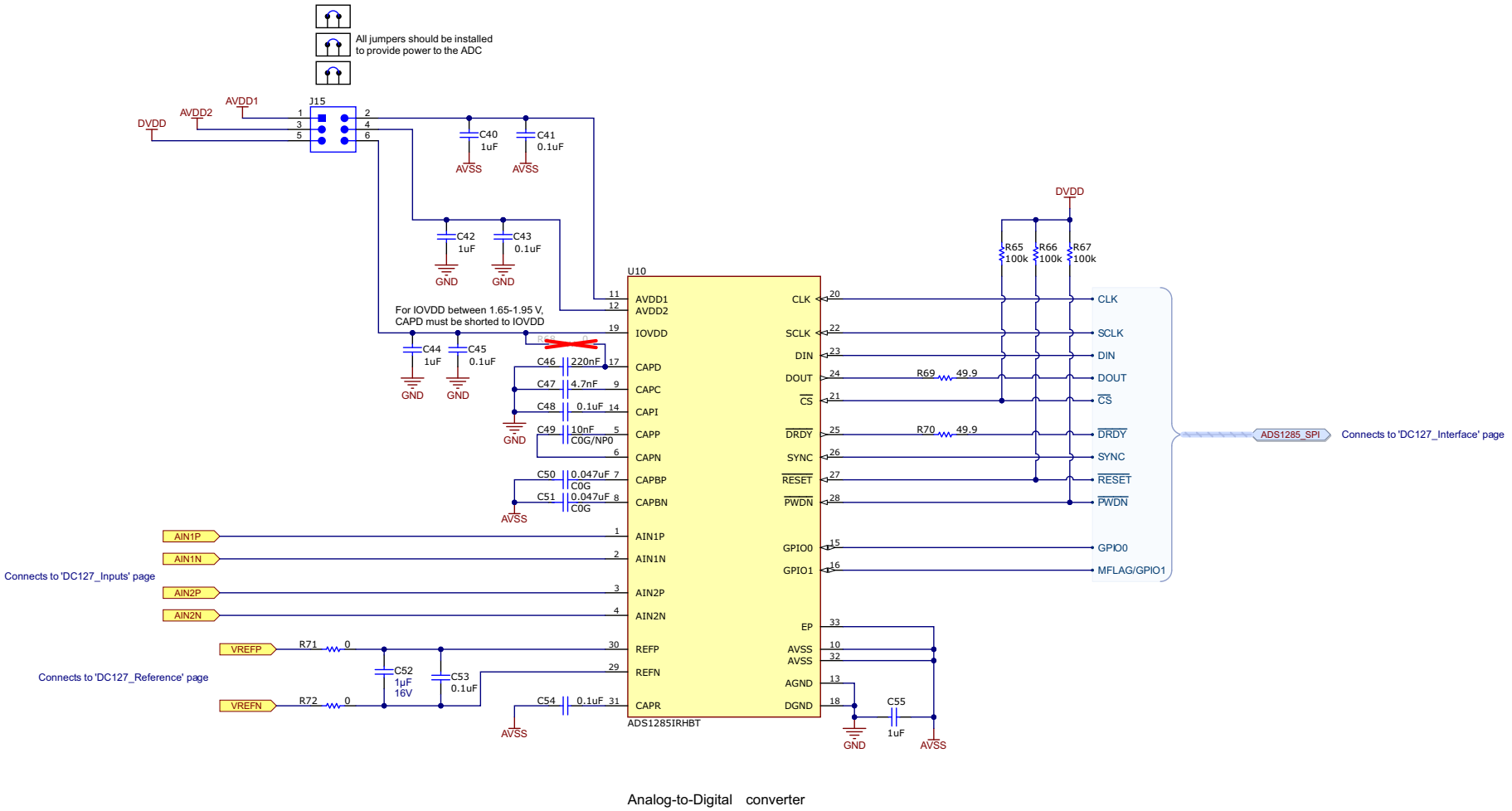


Figure 5-1. ADS1285EVM-PDK Block Diagram

Figure 5-2 through Figure 5-7 illustrate various schematics for the ADS1285EVM-PDK ADC.



Analog-to-Digital converter

Figure 5-2. ADS1285EVM-PDK ADC Schematic

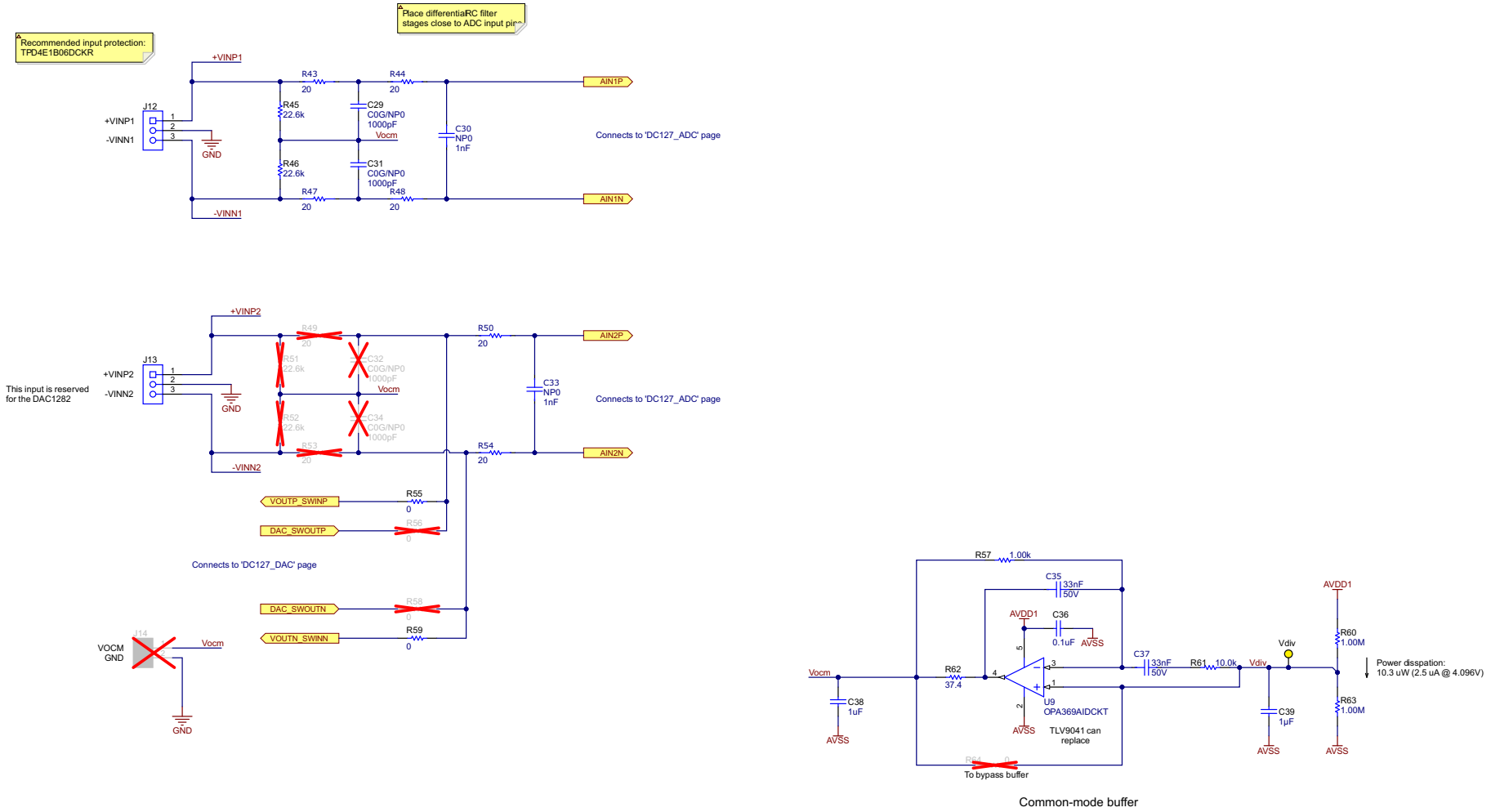


Figure 5-3. ADS1285EVM-PDK Analog Inputs and Common-Mode Buffer Schematic

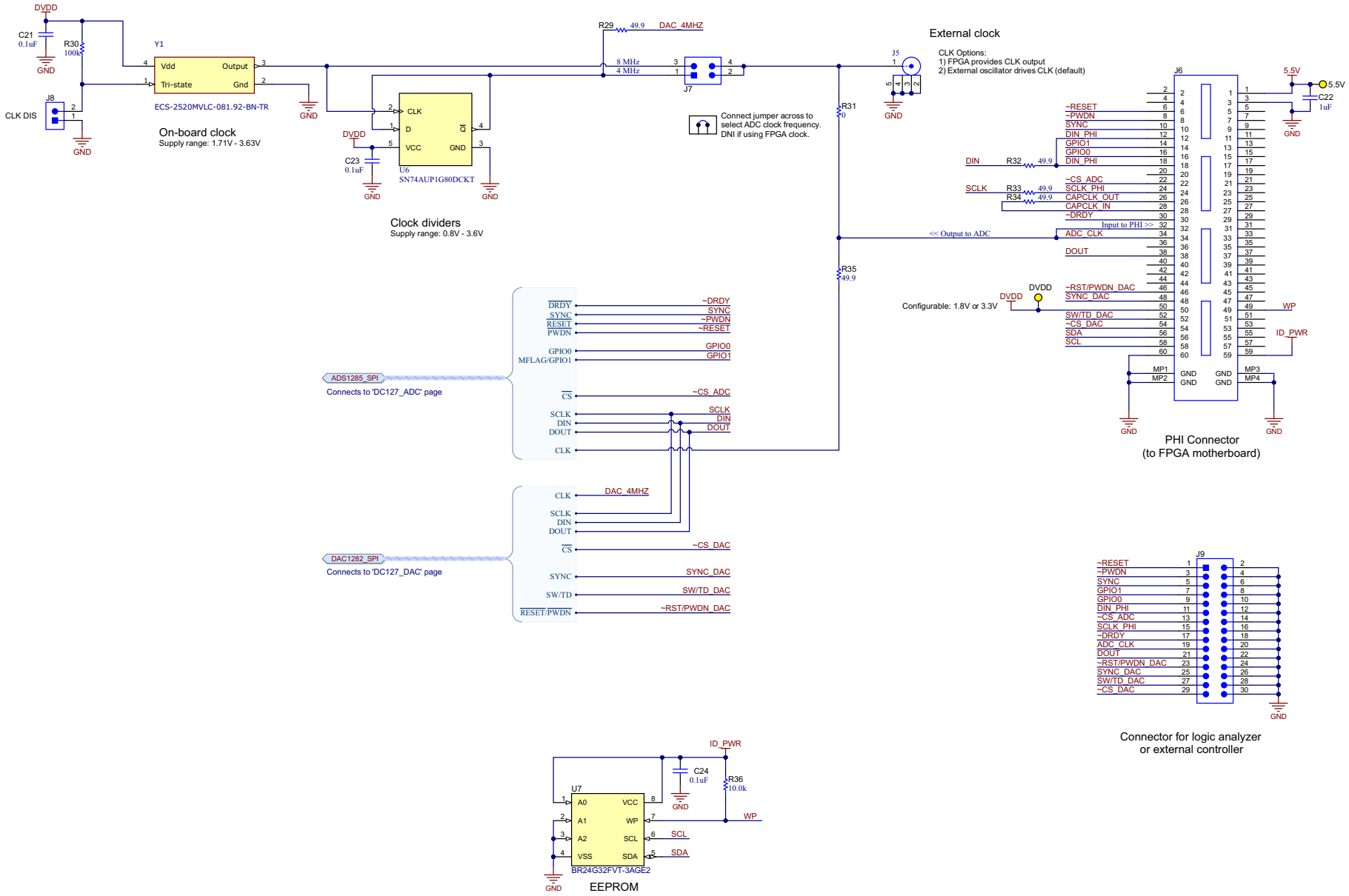
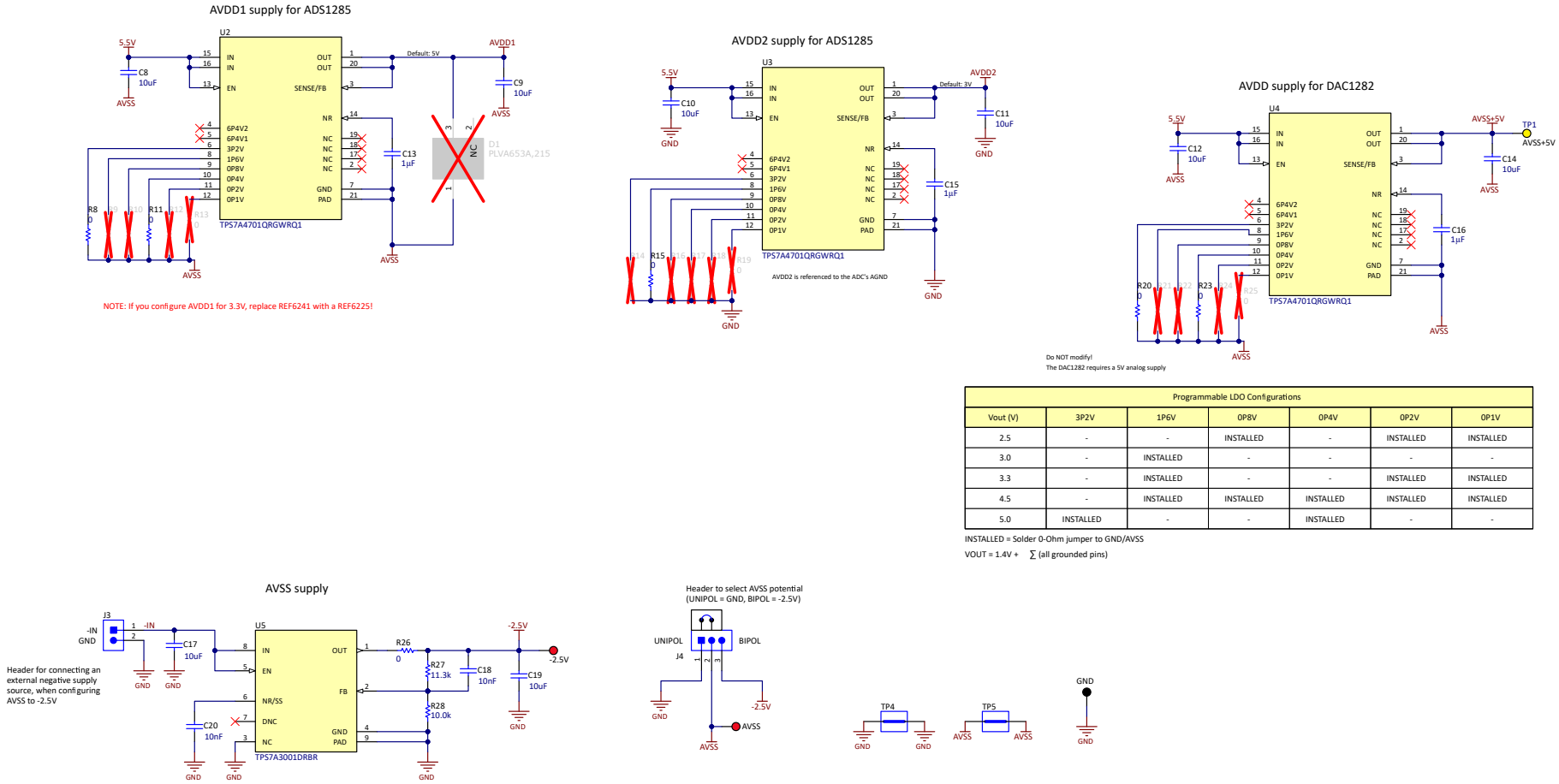


Figure 5-4. ADS1285EVM-PDK Clock and Interface Schematic



Programmable LDO Configurations						
Vout (V)	3P2V	1P6V	0P8V	0P4V	0P2V	0P1V
2.5	-	-	INSTALLED	-	INSTALLED	INSTALLED
3.0	-	INSTALLED	-	-	-	-
3.3	-	INSTALLED	-	-	INSTALLED	INSTALLED
4.5	-	INSTALLED	INSTALLED	INSTALLED	INSTALLED	INSTALLED
5.0	INSTALLED	-	-	INSTALLED	-	-

INSTALLED = Solder 0-Ohm jumper to GND/AVSS

VOUT = 1.4V + ∑ (all grounded pins)

Figure 5-5. ADS1285EVM-PDK Power-Supply Schematic

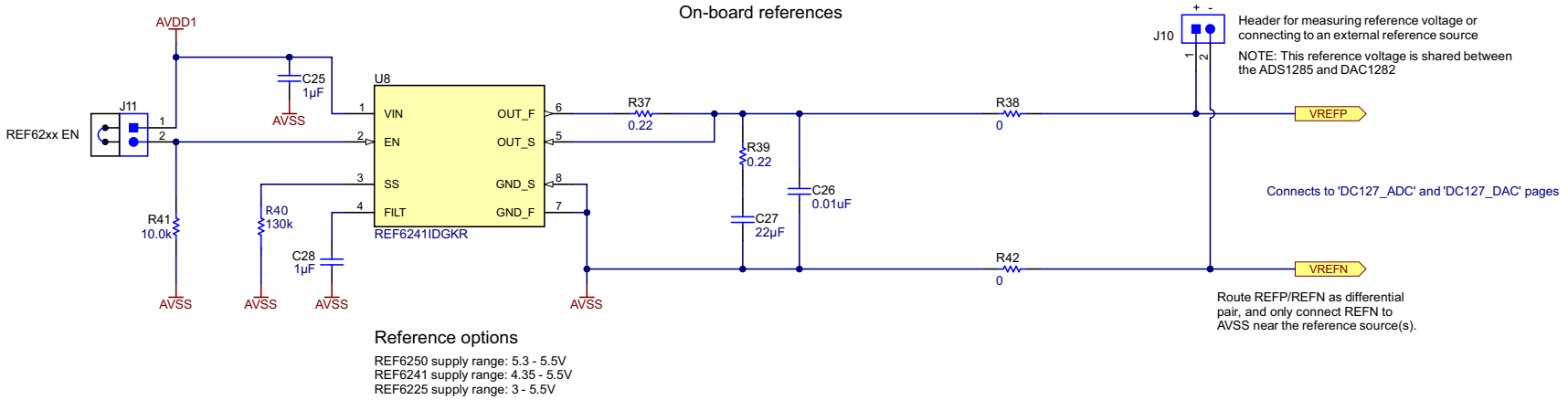


Figure 5-6. ADS1285EVM-PDK Reference Voltage Schematic

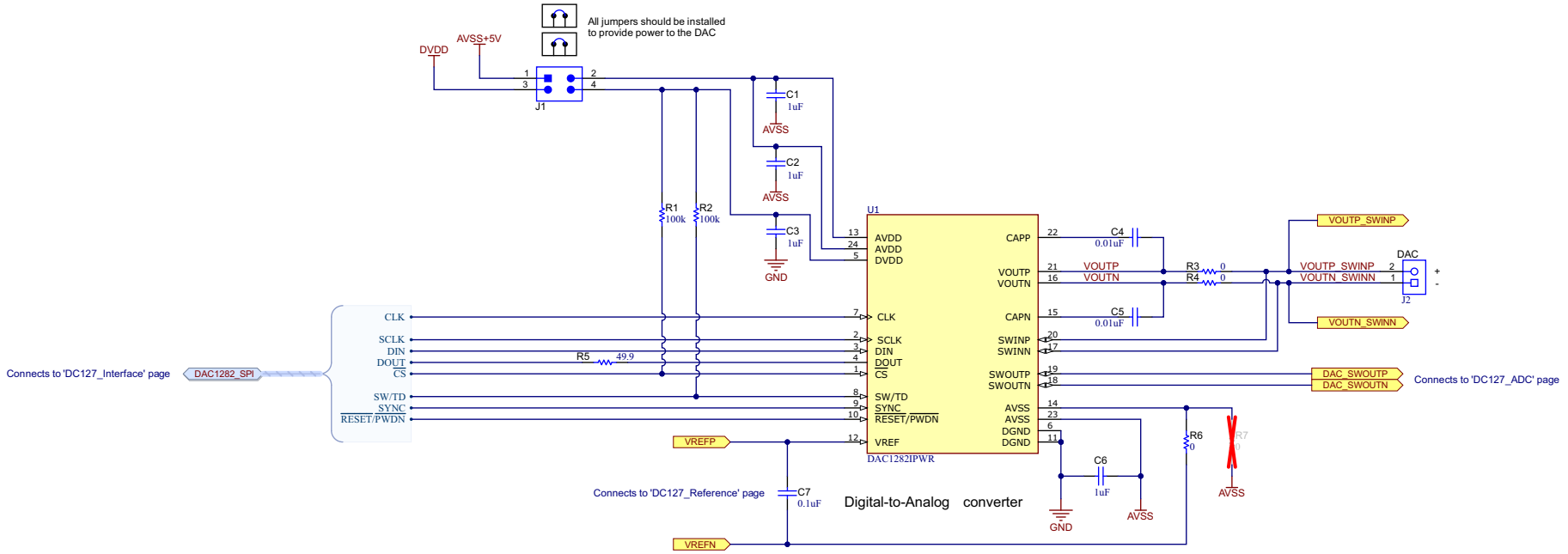


Figure 5-7. ADS1285EVM DAC Schematic

5.2 PCB Layout

Figure 5-8 through Figure 5-13 show the ADS1285EVM-PDK PCB layout.

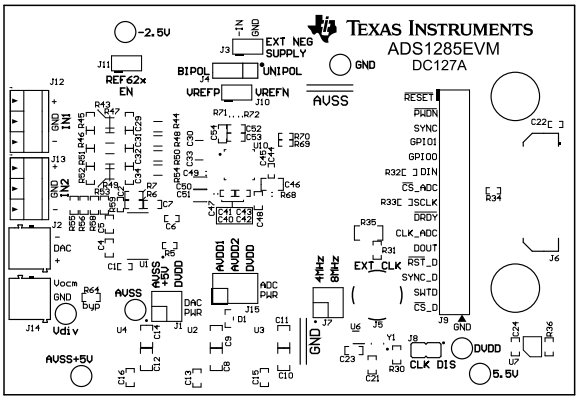


Figure 5-8. Top Silkscreen

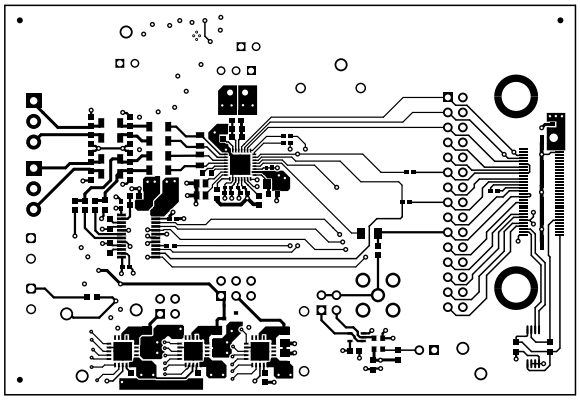


Figure 5-9. Top Layer

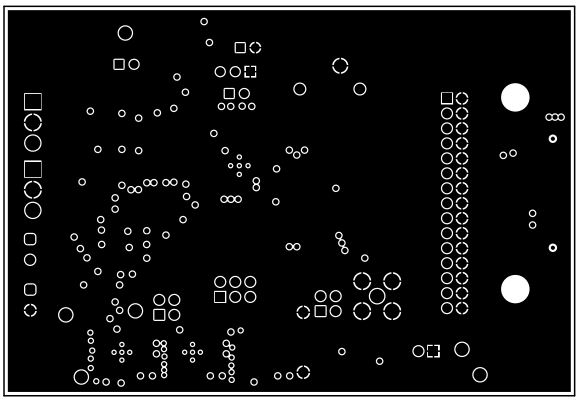


Figure 5-10. Ground Layer 1

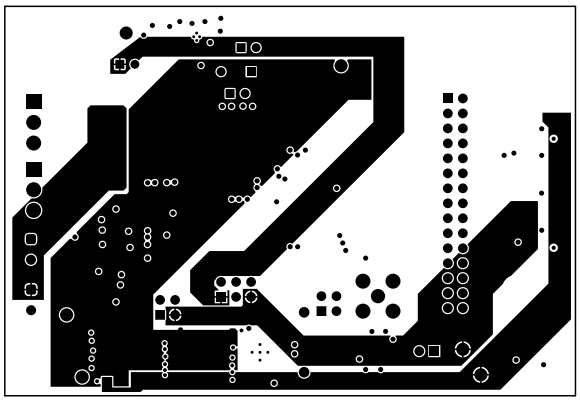


Figure 5-11. Power Layer

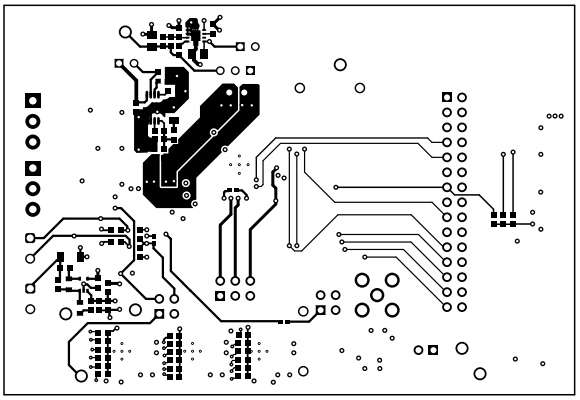


Figure 5-12. Bottom Layer

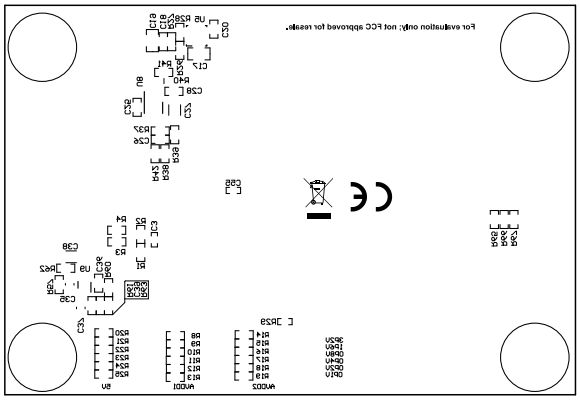


Figure 5-13. Bottom Silkscreen

5.3 Bill of Materials

Table 5-1 lists the ADS1285EVM-PDK bill of materials (BOM).

Table 5-1. ADS1285EVM-PDK BOM

Designator	Quantity	Value	Description	Package Reference	PartNumber	Manufacturer	Alternate PartNumber	Alternate Manufacturer
!PCB1	1		Printed Circuit Board		DC127	Any		
C1, C2, C3, C6, C22, C40, C42, C44, C55	9	1µF	CAP, CERM, 1µF, 35V, ±10%, X5R, 0402	402	C1005X5R1V105K050BC	TDK		
C4, C5, C26	3	0.01µF	CAP, CERM, 0.01µF, 25V, ±5%, C0G/NP0, AEC-Q200 Grade 1, 0603	603	C0603C103J3GECAUTO	Kemet		
C7, C48, C53, C54	4	0.1µF	CAP, CERM, 0.1uF, 50V, ±10%, X5R, 0603	603	C1608X5R1H104K080AA	TDK		
C8, C9, C10, C11, C12, C14, C17, C19	8	10µF	CAP, CERM, 10µF, 25V, ±10%, X5R, 0805	805	CL21A106KAFN3NE	Samsung Electro-Mechanics		
C13, C15, C16, C25, C28, C39	6	1µF	CAP, CERM, 1µF, 25V, ±10%, X7R, 0603	603	C0603C105K3RACTU	Kemet		
C18, C20	2	0.01µF	CAP, CERM, 0.01µF, 50V, ±10%, X7R, 0603	603	8.85012E+11	Wurth Elektronik		
C21, C23, C24, C36	4	0.1µF	CAP, CERM, 0.1µF, 50V, ±10%, X8R, AEC-Q200 Grade 0, 0603	603	CGA3E3X8R1H104K080AB	TDK		
C27	1	22µF	CAP, CERM, 22µF, 16V, ±20%, X5R, AEC-Q200 Grade 3, 1206	1206	CL31A226MOHNNNE	Samsung Electro-Mechanics		
C29, C31	2	1000pF	CAP, CERM, 1000pF, 50V, ±5%, C0G/NP0, 0603	603	C0603C102J5GACTU	Kemet		
C30, C33	2	1nF	1000pF ±5% 50V Ceramic Capacitor C0G, NP0 0805 (2012 Metric)	805	CC0805JRNPO9BN102	Yageo		
C35, C37	2	33nF	Cap Ceramic 33nF 50V NP0 5% Pad SMD 0805 +150°C Automotive T/R	805	CGA4J2NP01H333J125AA	TDK Corporation		
C38	1	1µF	CAP, CERM, 1µF, 50V, ±10%, X7R, AEC-Q200 Grade 1, 1206	1206	CGA5L3X7R1H105K160AB	TDK		
C41, C43, C45	3	0.1µF	CAP, CERM, 0.1µF, 25V, ±10%, X7R, 0402	402	GRM155R71E104KE14D	MuRata		
C46	1	0.22µF	CAP, CERM, 0.22µF, 50V, ±10%, X7R, 0805	805	C0805C224K5RACTU	Kemet		
C47	1	4700pF	CAP, CERM, 4700pF, 50V, ±10%, X7R, 0603	603	C0603X472K5RACTU	Kemet		
C49	1	0.01µF	CAP, CERM, 0.01µF, 50V, ±5%, C0G/NP0, 0603	603	GRM1885C1H103JA01D	MuRata		
C50, C51	2	47nF	0.047µF ±1% 25V Ceramic Capacitor C0G, NP0 0805 (2012 Metric)	805	C0805C473F3GAC7800	KEMET		
C52	1	1µF	CAP, CERM, 1µF, 16V, ±10%, X7R, AEC-Q200 Grade 1, 0603	603	GCM188R71C105KA64J	MuRata		
FID1, FID2, FID3	3		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A		
H1, H2	2		Machine Screw Pan PHILLIPS M3		RM3X4MM 2701	APM HEXSEAL		
H3, H4, H5, H6	4		Bumpon, Hemisphere, 0.44X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M		
H7, H8	2		ROUND STANDOFF M3 STEEL 5MM	ROUND STANDOFF M3 STEEL 5MM	9774050360R	Wurth Elektronik		
J1, J7	2		Header, 100mil, 2x2, Gold, TH	2x2 Header	TSW-102-07-G-D	Samtec		
J2	1		Terminal Block, 3.5mm, 2x1, Tin, TH	Terminal Block, 3.5mm, 2x1, TH	1776275-2	TE Connectivity		
J3, J10, J11	3		Header, 100mil, 2x1, Tin, TH	Header, 2 PIN, 100mil, Tin	PEC02SAAN	Sullins Connector Solutions		
J4	1		Header, 100mil, 3x1, Tin, TH	Header, 3 PIN, 100mil, Tin	PEC03SAAN	Sullins Connector Solutions		
J5	1		Connector, SMA, TH	SMA	142-0701-231	Cinch Connectivity		

Table 5-1. ADS1285EVM-PDK BOM (continued)

Designator	Quantity	Value	Description	Package Reference	PartNumber	Manufacturer	Alternate PartNumber	Alternate Manufacturer
J6	1		Header(Shrouded), 19.7mil, 30x2, Gold, SMT	Header (Shrouded), 19.7mil, 30x2, SMT	QTH-030-01-L-D-A-K-TR	Samtec		
J8	1		Header, 100mil, 2x1, Gold, TH	Sullins 100mil, 1x2, 230mil above insulator	PBC02SAAN	Sullins Connector Solutions		
J9	1		Header, 100mil, 15x2, Gold, TH	15 x 2 Header	MTSW-115-22-G-D-315	Samtec		
J12, J13	2		Terminal Block, 3.5mm Pitch, 3x1, TH	10.5x8.2x6.5mm	ED555/3DS	On-Shore Technology		
J15	1		Header, 100mil, 3x2, Tin, TH	3x2 Header	PEC03DAAN	Sullins Connector Solutions		
R1, R2, R30, R65, R66, R67	6	100k	RES, 100k, 1%, 0.1W, 0603	603	RC0603FR-07100KL	Yageo		
R3, R4, R6, R8, R11, R15, R20, R23, R26, R31, R38, R42, R55, R59, R71, R72	17	0	RES, 0, 5%, 0.1W, 0603	603	RC0603JR-070RL	Yageo		
R5, R29, R32, R33, R34, R69, R70	7	49.9	RES, 49.9, 1%, 0.063W, 0402	402	RC0402FR-0749R9L	Yageo America		
R27	1	11.3k	RES, 11.3k, 1%, 0.1W, 0603	603	RC0603FR-0711K3L	Yageo		
R28, R36, R41, R61	4	10.0k	RES, 10.0k, 1%, 0.1W, 0603	603	RC0603FR-0710KL	Yageo		
R35	1	49.9	RES, 49.9, 1%, 0.25W, 1206	1206	RC1206FR-0749R9L	Yageo America		
R37, R39	2	0.22	RES, 0.22, 1%, 0.1W, AEC-Q200 Grade 0, 0603	603	ERJ-3RQFR22V	Panasonic		
R40	1	130k	130kOhms ±5% 0.1W, 1/10W Chip Resistor 0603 (1608 Metric) Moisture Resistant Thick Film	603	RC0603JR-07130KL	Yageo		
R43, R44, R47, R48, R50, R54	6	20	Res Thick Film 1206 20Ohm 1% 0.25W ±100ppm/°C Molded SMD Paper T/R	1206	RMCF1206FT20R0	Stackpole		
R45, R46	2	22.6k	RES, 22.6k, 1%, 0.1W, AEC-Q200 Grade 0, 0603	603	CRCW060322K6FKEA	Vishay-Dale		
R57	1	1.00k	RES, 1.00k, 1%, 0.1W, 0603	603	RC0603FR-071KL	Yageo		
R60, R63	2	1.00Meg	RES, 1.00M, 1%, 0.1W, 0603	603	RC0603FR-071ML	Yageo		
R62	1	37.4	RES, 37.4, 1%, 0.1W, 0603	603	RC0603FR-0737R4L	Yageo		
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8	8	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec	969102-0000-DA	3M
TP1, TP7, TP8, TP9	4		Test Point, Multipurpose, Yellow, TH	Yellow Multipurpose Testpoint	5014	Keystone Electronics		
TP2, TP6	2		Test Point, Multipurpose, Red, TH	Red Multipurpose Testpoint	5010	Keystone Electronics		
TP3	1		Test Point, Multipurpose, Black, TH	Black Multipurpose Testpoint	5011	Keystone Electronics		
TP4, TP5	2		1mm Uninsulated Shorting Plug, 10.16mm spacing, TH	Shorting Plug, 10.16mm spacing, TH	D3082-05	Harwin		
U1	1		Low Distortion Digital-to-Analog Converter for Seismic	TSSOP24	DAC1282IPWR	Texas Instruments		
U2, U3, U4	3		Automotive 35V, 1A, 4.2μVRMS, RF Low-Dropout (LDO) Voltage Regulator, RGW0020A (VQFN-20)	RGW0020A	TPS7A4701QRGWRQ1	Texas Instruments	TPS7A4701QRGWTQ1	Texas Instruments
U5	1		Vin -3V to -36V, -200mA, Ultra-Low-Noise, High-PSRR, Low-Dropout (LDO) Linear Regulator, DRB0008A (VSON-8)	DRB0008A	TPS7A3001DRBR	Texas Instruments	TPS7A3001DRBT	Texas Instruments

Table 5-1. ADS1285EVM-PDK BOM (continued)

Designator	Quantity	Value	Description	Package Reference	PartNumber	Manufacturer	Alternate PartNumber	Alternate Manufacturer
U6	1		Low-Power Single Postitive-Edge-Triggered D-Type Flip-Flop, DCK0005A, SMALL T&R	DCK0005A	SN74AUP1G80DCKT	Texas Instruments		
U7	1		I2C BUS EEPROM (2-Wire), TSSOP-B8	TSSOP-8	BR24G32FVT-3AGE2	Rohm		
U8	1		High-Precision Voltage Reference with Integrated High-Bandwidth Buffer, DGK0008A (VSSOP-8)	DGK0008A	REF6241IDGKR	Texas Instruments	REF6241IDGKT	Texas Instruments
U9	1		700nA, Zero-Crossover Rail-to-Rail I/O Operational Amplifier, 1.8 to 5.5V, -40° to 85°C, 5pin SOT23 (DCK5), Green (RoHS & no Sb/Br)	DCK0005A	OPA369AIDCKT	Texas Instruments		
U10	1		ADS1285 High Resolution, Delta-Sigma ADC for Seismic 4000sps 1 to 64 as Gain 3-5.25V	VQFN32	ADS1285IRHBT	Texas Instruments		None
Y1	1		8.192MHz XO (Standard) CMOS Oscillator 1.6V ~ 3.6V Enable/Disable 4-SMD, No Lead	SMT4_2MM5_2MM0	ECS-2520MVLC-081.92-BN-TR	ECS		
C32, C34	0	1000pF	CAP, CERM, 1000pF, 50V, ±5%, C0G/NP0, 0603	603	C0603C102J5GACTU	Kemet		
D1	0		Zener Diode Single 5V 4% 250Ω 250mW Automotive 3-Pin SOT-23 T/R	SOT23	PLVA653A,215	Nexperia		
J14	0		Terminal Block, 3.5mm, 2x1, Tin, TH	Terminal Block, 3.5mm, 2x1, TH	1776275-2	TE Connectivity		
R7, R9, R10, R12, R13, R14, R16, R17, R18, R19, R21, R22, R24, R25, R56, R58, R64, R68	0	0	RES, 0, 5%, 0.1W, 0603	603	RC0603JR-070RL	Yageo		
R49, R53	0	20	Res Thick Film 1206 20Ω 1% 0.25W ±100ppm/°C Molded SMD Paper T/R	1206	RMCF1206FT20R0	Stackpole		
R51, R52	0	22.6k	RES, 22.6k, 1%, 0.1W, AEC-Q200 Grade 0, 0603	603	CRCW060322K6FKEA	Vishay-Dale		

6 Additional Information

6.1 Trademarks

LabVIEW® is a registered trademark of National Instruments.
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7 References

- Texas Instruments, *DAC1282 Low Distortion Digital-to-Analog Converter for Seismic* data sheet
- Texas Instruments, *REF62xx High-Precision Voltage Reference With Integrated ADC Drive Buffer* data sheet

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2022) to Revision B (August 2025)	Page
• Updated LDO figure and text to reflect actual board component placement in Section 2.3	8
• Updated LDO figure to reflect the actual board component placement in Section 5.1	22

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

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   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

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4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

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