Application Note

AM625x/AM623x and AM62Lx Hardware Migration Guide

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ABSTRACT

This application note serves as a hardware migration guide overview for moving a design from the AM62x (AM625x, AM623x) family of TI Sitara™ processors to the AM62Lx family of TI Sitara™ processors, or moving a design from the AM62Lx family of processors to the AM62x family of processors. This highlights board-level design differences associated with power rails, IO voltages, peripheral interfaces, boot configurations, and package options.

The AM62x family of processors provides higher performance capabilities than the AM62Lx family of processors along with additional flexibility of powering the device from a single 0.85V core power domain or separate 0.75V and 0.85V core power domains. The single 0.85V core power domain option provides maximum performance, while the separate core power domain option provides lower power consumption with a slight reduction in performance and the additional cost of implementing another core power domain. These core power options provide the system designer with a trade-off between device performance and power consumption.

The AM62Lx family of processors has characteristics that enable a simpler, lower-cost design by only requiring a single 0.75V core power domain, supporting RTC Only and RTC + IO + DDR low-power states, and streamlining SD-card power path with an integrated LDO, SDIO_LDO, which simplifies the system design and enables a lower cost Bill of Material (BOM).

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1 Introduction

This application note serves as a guide for hardware compatibility between the AM62x and AM62Lx processors. The document focuses on board-level design changes for things like power rails, IO voltages, interfaces, boot pins, and package options. Highlighting the primary differences between the two processor families, which helps hardware board designers to understand the schematics and layout changes required to transition the system design.

This document is not a substitute for information provided in the respective device data sheets. The designer is still responsible for understanding the requirements of each device as defined in the respective data sheets, AM62x Sitara™ Processors data sheet, and AM62Lx Sitara™ Processors data sheet.

2 Overview of AM62x vs AM62Lx

The AM62Lx is a low-power, reduced feature variant of AM62x. The AM62Lx has fewer processor cores, no GPU or PRU, a smaller BGA package, simplified power and IO domains.

AM62x targets higher performance with more media and industrial features. This device has more processor cores, an optional GPU and PRU, dual display, and more options for power and IO domains.

Table 2-1 lists the high-level differences in processor cores and key peripherals.

Table 2-1. Feature Comparison – AM62x vs. AM62Lx

FEATURE OR PERIPHERAL	AM62x	AM62Lx
Main CPU Cores	• 4× Arm Cortex-A53 up to 1.4GHz • 32KB L1 DCache per core • 32KB L1 ICache per core • 512KB L2 shared cache	• 2× Arm Cortex-A53 up to 1.25GHz • 32KB L1 DCache per core • 32KB L1 ICache per core • 256KB L2 shared cache
Microcontroller Cores	• 1× Cortex-M4F up to 400MHz	• No microcontroller cores
On-Chip Memory	• Up to 816KB of On-Chip RAM – 64KB MAIN Domain OCSRAM – 256KB M4F Domain SRAM – 256KB SMS SRAM – 176KB SMS security SRAM – 64KB in Device/Power Manager Subsystem	• Up to 160KB of Shared On-Chip RAM – 96KB MAIN Domain – 64KB WKUP Domain
Graphics and Display	• 3D GPU (OpenGL ES 3.1/Vulkan)(1) • Dual display output (up to 1080p60 each) via 24-bit DPI(1) • Dual-link OLDI (LVDS)(1)	• No GPU • Single display output up to 1080p60 (either 24-bit DPI or 4-lane MIPI DSI) • No LVDS output
Camera Interface	• 1× MIPI CSI-2 receiver (4-lane) for camera input	• No CSI
PRUSS (Industrial IO)	• 1× PRUSS (dual PRU cores) for cycle accurate protocols	• No PRUSS
Gigabit Ethernet	• 2-port Gb Ethernet switch with IEEE 1588, RGMII/RMII; MDIO interface (3.3V capable) • Network boot via Ethernet is supported	• 2-port Gb Ethernet switch with IEEE 1588 (same functionality) but IO is 1.8V only. • Network boot via Ethernet is not supported
USB	• 2x USB 2.0 ports • Configurable as host, peripheral, or DRD • VBUS detection	
I^2C	• 5× I^2C + 1× MCU I^2C	• 5× I^2C
UART / CAN-FD	• 8× UART + 1× MCU UART • 3× CAN-FD	• 8× UART • 3× CAN-FD
SPI / McASP / ePWM	• 4× SPI + 2x MCU SPI • 3× McASP • 3× ePWM	• 4× SPI • 3× McASP • 3× ePWM
ADC (Analog Inputs)	• No on-chip ADC	• 4× Analog inputs integrated ADC

Table 2-1. Feature Comparison – AM62x vs. AM62Lx (continued)

FEATURE OR PERIPHERAL	AM62x	AM62Lx
Memory Interfaces	• DDR4/LPDDR4 is single or dual ranks • GPMC up to 4 chip selects; more address bits in some modes • OSPI/QSPI supports up to 1× device – 1.8V/3.3V • 3× MMC/SD/SDIO – 1× eMMC – 2× SD/SDIO – No internal LDO (needs external)	• DDR4/LPDDR4 is single rank only • GPMC up to 4 chip selects; reduced address bits in some modes • OSPI/QSPI supports up to 2× devices – Only 1.8V • 3× MMC/SD/SDIO – 1× eMMC – 2× SD/SDIO – Integrated LDO for 1.8V/3.3V
Boot Options	• UART • I^2C EEPROM • OSPI/QSPI Flash • GPMC NOR/NAND Flash • Serial NAND Flash • SD Card • eMMC • USB (host) • USB (device) • Ethernet	• Same boot options with the following changes: – I^2C EEPROM boot is removed – GPMC NOR Flash boot is removed – Ethernet boot is removed • AM62Lx supports reduced boot pin configuration; see Section 6, *Boot Configuration and Reset Changes*.
Core Power Domains / Operating Voltage	• VDD_CORE dual voltage options 0.75V/ 0.85V • VDDR_CORE single voltage 0.85V	• Single 0.75V
IO Power Domains / Operating Voltages	• 9× IO banks support a 1.8V or 3.3V operation – 6× LVCMOS fixed – 3× SDIO dynamic • All other IO banks only support a fixed 1.8V operation	• 5× IO banks support a 1.8V or 3.3V operation – 2× LVCMOS fixed – 3× SDIO dynamic • All other IO banks only support a fixed 1.8V operation
Security Features	• Cortex R5F boot core • Hardware-enforced Root-of-Trust (RoT) • Trusted Execution Environment (TEE) • HSM Core and security DMA/IPC • SAx_UL hardware crypto	• Cortex A53 boot core • Hardware-enforced Root-of-Trust (RoT) • Trusted Execution Environment (TEE) • HSM Core and security DMA/IPC • DTHEv2 hardware crypto – Enhanced engine with similar features
Package	See the *Package Variants Comparison* table	

1. Feature on select AM62x devices. For more details about different device features, refer to AM62x Sitara™ Processors data sheet, *Device Comparison* table.

3 Power Architecture and PMIC Considerations

One of the main differences in power architecture is that AM62Lx uses a single VDD_CORE 0.75V voltage domain and adds an always-on RTC domain to enable RTC-only low power mode. AM62Lx removes the VMON supply monitor pins and integrates an SDIO_LDO to switch SD card IO between 0V, 1.8V, and 3.3V for UHS-I.

AM62x supports VDD_CORE to run at 0.75V or 0.85V. AM62x includes VMON pins for supply monitoring and does not integrate an SDIO_LDO, so UHS-I SD card IO voltage switching is done with external circuitry.

For complete AM62Lx schematics, recommended power sequences, and low-power mode details, see the AM62L Power Supply Implementation application note, and the AM62Lx Processor Family Schematic Design Guidelines and Checklist *Power Architecture* section. These documents provide PMIC programming recommendation and sequencing diagrams for AM62Lx designs.

For the AM62x family, use the AM62x Processor Family Schematic, Design Guidelines and Review Checklist Processor *Power Architecture* section for schematic guidance and review, and the Powering the AM62x with the TPS65219 PMIC, for PDN rails, sequencing examples and PMIC settings.

Table 3-1. Power Supply Differences

POWER ASPECT	AM62x	AM62Lx	DESIGN NOTES
Core Voltage Rails	• VDD_CORE dual-voltage options 0.75V, or 0.85V • VDDR_CORE always 0.85V	• All core power rails operate at 0.75V • VDDR_CORE internally merged with VDD_CORE	Program AM62Lx PMIC to 0.75V. AM62Lx does not require dedicated supply for VDDR_CORE supply.
IO Supply Rails	• 6× LVCMOS IO banks that support a fixed 1.8V/3.3V operation • 3× SDIO IO banks that support dynamic operating voltage change between 0V, 1.8V, and 3.3V operation • All other IO banks only support a fixed 1.8V operation	• 2× LVCMOS IO banks that support a fixed 1.8V or 3.3V operation • 3× SDIO IO banks that support a dynamic operating voltage change between 0V, 1.8V, and 3.3V operation • All other IO banks only support a fixed 1.8V operation	AM62Lx power rails associated with SDIO IOs support dynamic voltage change between 1.8V/3.3V, while the AM62x requires external circuitry for the same functionality. See *Dual-Voltage vs. 1.8V-Only IO Banks* section for more information.
VMON Pins	• VMON_3P3_SOC • VMON_1P8_SOC • VMON_VSYS	• VMON pins not supported	If migrating to AM62Lx, remove any schematic connections or circuitry for VMON related pins; use PMIC power-good outputs or internal supervisors to monitor power supplies instead, as recommended in the AM62L Power Supply Implementation application note.
PMIC Low-Power Enable (PMIC_LPM_EN)	• Requires an external pull-up resistor to turn on PMIC	• No external pull-up needed due to built-in internal pull-up	If migrating to AM62Lx, drop external pull-up resistor; verify PMIC_LPM_EN0 net ties to the PMIC enable pin. For more information, see the AM62L Power Supply Implementation application note.
PMIC Recommendation	• TPS65219 (4× LDOs)	• TPS65214 (2× LDOs)	For AM62Lx, verify that power sequencing and voltages comply with the AM62Lx Schematic Checklist and AM62L Power Supply Implementatio application note. For AM62x, check AM62x Schematic Checklist and Powering the AM62x with the TPS65219 PMIC application note.

Table 3-1. Power Supply Differences (continued)

POWER ASPECT	AM62x	AM62Lx	DESIGN NOTES
Low-Power Modes	• Partial IO support for CAN/ GPIO/UART wakeup • DeepSleep • MCU Only • Standby • Dynamic frequency scaling for Cortex-A53 • Partial IO wake	• No support for Partial IO wake for CAN/GPIO/UART • DeepSleep • Standby • Dynamic frequency scaling • RTC Only • RTC Only + IO + DDR Self-refresh	Only dedicated wake pins (for example, EXT_WAKEUP0/1) can wake from lowest power states; check the *Boot Configuration and Reset Changes* section for more information.

4 IO Voltage Domains and Signal Levels

Migrating to AM62Lx requires a review of IO bank voltage configurations. AM62x offers broad flexibility with dual-voltage (1.8V/3.3V) IO banks, whereas AM62Lx has designated some banks for dual-voltage and made the rest 1.8V only. Moreover, AM62Lx introduces new buffer types (1.8V-specific) and there are changes in which signals are fail-safe. This section discusses a high-level overview of those differences.

4.1 Dual-Voltage vs. 1.8V-Only IO Banks

On AM62x, most IO (VDDSHVx rails) can either be 1.8V or 3.3V. AM62Lx splits the IO rails between five rails that are 1.8V or 3.3V selectable (some constraints on dynamic switching), and the remaining rails are fixed at 1.8V. The *IO Supply Voltage Domains* table shows how each voltage domain of the IO banks differ.

For detailed IO-bank mapping and voltage domain planning, see the respective AM62x Sitara™ Processors data sheet or AM62Lx Sitara™ Processors data sheet *Recommended Operating Conditions* section, and the SysConfig tool.

Table 4-1. IO Supply Voltage Domains

IO BANK (RAIL)	AM62x VOLTAGE OPTIONS	AM62Lx VOLTAGE OPTIONS	DESIGN NOTES
VDDSHV_CANUART	• 1.8V or 3.3V (dual)	• Not present	All CAN-FD and UART pins are in the main domain IO rails.
VDDSHV_MCU	• 1.8V or 3.3V (dual) • Powers MCU domains including wakeup, JTAG, I^2C, Clock Out	• Not present	There is no MCU domain on AM62Lx.
VDDSHVx	• VDDSHV0-3 IO power rails associated with LVCMOS buffer types supports a fixed 1.8V or 3.3V operation • VDDSHV4-6 IO power rails associated with SDIO buffer types support a dynamic operating voltage change between 0V, 1.8V, and 3.3V	• VDDSHV0-1 IO power rails associated with LVCMOS buffer types supports a fixed 1.8V or 3.3V operation • VDDSHV2-4 IO power rails associated with SDIO buffer types support a dynamic operating voltage change between 0V, 1.8V, and 3.3V	The SDIO buffer types support dynamically voltage change between 0V, 1.8V, and 3.3V, which is required for UHS-I SD Card support.
MMC IO Voltage	• MMC0 (VDDSHV4) – Dynamic but typically fixed 1.8V/3.3V per application • MMC1 (VDDSHV5) and MMC2 (VDDSHV6) – Dynamic 3.3V and 1.8V when used for UHS-I SD card operation – Requires discrete LDO or PMIC	• MMC0 (VDDSHV2) – Dynamic but typically fixed 1.8V/3.3V per application • MMC1 (VDDSHV3) – Dynamic 3.3V and 1.8V when used for UHS-I SD card operation – Integrated SDIO_LDO • MMC2 (VDDSHV4) – Dynamic 3.3V and 1.8V when used for UHS-I SD card operation – Requires discrete LDO or PMIC	Dynamic switching is only required for SD card (UHS-I) use cases; eMMC/embedded SDIO are typically fixed voltage. For more information, refer to AM62Lx Processor Family Schematic Design Guidelines and Checklist, *IO Power Supply* section. For AM62x, refer to AM62x Processor Family Schematic, Design Guidelines and Review Checklist, *IO Power Supply* section.
VDDS_WKUP	• Not present	• 1.8V only	AM62Lx VDDS_WKUP is a dedicated supply for certain always-on RTC domain signals (e.g., EXT_WAKEUP pins, RTC IO).
VDDS0/1	• Not present	• 1.8V only	VDDS rails introduced in AM62Lx for analog blocks (ADC, RTC).

Table 4-1. IO Supply Voltage Domains (continued)

IO BANK (RAIL)	AM62x VOLTAGE OPTIONS	AM62Lx VOLTAGE OPTIONS	DESIGN NOTES
VDDA_ADC	• Not present	• 1.8V only	This powers internal AM62Lx ADC. Even if ADC is unused, provide power and decoupling according to data sheet recommendations.
VDDS_DDR	• 1.1V operation only	• 1.1V or 1.2V operation	1.2V is to allow for DDR4, and 1.1V is for LPDDR4.
VDDS_DDR_C	• 1.1V or 1.2V operation only	• Not present	AM62Lx merged DDR clock voltage with VDDS_DDR.

4.2 Buffer Types and Fail-Safe IOs

AM62Lx introduces new IO buffer types to accommodate the 1.8V-only rails and always-on domain, and there are slight changes in fail-safe behavior. The *Fail-Safe Behavior Comparison* table compares a few important signals and the *IO Buffer Types Comparison* table highlights buffer changes between AM62x and AM62Lx.

For buffer-type definitions and recommended operating conditions, see the AM62x Sitara™ Processors data sheet or AM62Lx Sitara™ Processors data sheet *Electrical Characteristics* section.

Table 4-2. Fail-Safe Behavior Comparison

PIN/BUFFER TYPE	AM62x FAIL-SAFE?	AM62Lx FAIL-SAFE?	DESIGN NOTES
PORz, EXTINTn	Yes	Yes	N/A
MCU I2C0, WKUP I2C0	Yes	No	N/A
I2C2 SDA, I2C2 SCL	No	Yes	N/A
VMON (1P8/3P3/VSYS)	Yes	Not present	See the *Power Architecture and PMIC Considerations* section, to use PMIC power-good instead of VMON pins.

Table 4-3. IO Buffer Types Comparison

PIN/BUFFER TYPE	AM62x Present?	AM62Lx Present?	DESIGN NOTES
LVCMOS	Yes	Yes	N/A
1P8-LVCMOS	No	Yes	Standard 1.8V CMOS buffers; not fail-safe.
RTC-LVCMOS	No	Yes	RTC domain IO not fail-safe.

5 Peripheral Interface Changes

5.1 Memory Interfaces

Some memory subsystems' capabilities have been removed or changed in AM62Lx compared to AM62x. The *Memory Interface Differences* table goes the main changes in the memory interfaces.

For more information refer to the AM62x, AM62Lx DDR Board Design and Layout Guidelines for signal-integrity rules, and the respective AM62Lx Schematic Design Guidelines and Schematic Review Checklist or AM62x Schematic Design Guidelines and Review Checklist *Memory Interface* section.

Table 5-1. Memory Interface Differences

MEMORY INTERFACE	AM62x	AM62Lx	DESIGN NOTES
DDR4/LPDDR4 (16-bit)	• Dual-rank (8GB DDR4) • Inline ECC option	• Single rank only (4GB DDR4) • No ECC	For AM62Lx, design for one rank only; remove ECC lines and second chip select.
GPMC	• 8- / 16-bit Synchronous/ Asynchronous • 4× CS • More address bits – 23 bits in non-mux mode, A[22:0] – 27 bits in AD-mux mode, A[26:0] – 28 bits in AAD-mux mode, A[27:0]	• 8- / 16-bit Synchronous/ Asynchronous • 4× CS • Less address bits – 7 bits in non-mux mode, A[6:0] – 23 bits in AD-mux mode, A[22:0] – 28 bits in AAD-mux mode, A[27:0]	For more information on different register values check the TRM and data sheet for the respective processor.
OSPI/QSPI	• Only supports connecting a single OSPI/QSPI device	• Supports connecting up to two OSPI/QSPI devices, with specific connection topology exceptions and PCB layout requirements	AM62x EVM includes 1× CS while AM62Lx EVM includes dual CS; use 1.8V for AM62Lx.
eMMC or Embedded SDIO (MMC0)	• 1- / 4- / 8-bit • eMMC speeds up to HS200 – High-Speed DDR not supported • Embedded SDIO speeds up to High Speed or UHS-I SDR25	• 1- / 4- / 8-bit • eMMC speeds up to HS200 – High-Speed DDR is supported • Embedded SDIO speeds up to High Speed or UHS-I SDR25	N/A
SD Card or Embedded SDIO (MMC1/2)	• 1- / 4-bit • Up to UHS-I SDR104 for SD Card (needs external power) • Embedded SDIO speeds up to High Speed or UHS-I SDR25 • Needs an external 1.8V/3.3V IO power source	• 1- / 4-bit • Up to UHS-I SDR104 for SD Card • Embedded SDIO speeds up to High Speed or UHS-I SDR25 • Internal 1.8V/3.3V IO power source for MMC1	If moving to AM62x, make sure to add appropriate external shifter/regulator circuitry, and remove the circuitry if migrating to AM62Lx.

5.2 Connectivity

Most high-speed connectivity remains the same, but the voltage differences and some feature removals require changes. The *Connectivity Interface Differences* table highlights interface differences for networking and serial connectivity.

For more detailed information, see the respective AM62x Sitara™ Processors data sheet or AM62Lx Sitara™ Processors data sheet *Peripherals* section.

Table 5-2. Connectivity Interface Differences

INTERFACE	AM62x	AM62Lx	DESIGN NOTES
Ethernet (RGMII)	• 1.8V or 3.3V IO • Network boot	• 1.8V IO only • No network boot	For AM62Lx, use 1.8V-capable PHY; remove Ethernet-boot circuitry.

Table 5-2. Connectivity Interface Differences (continued)

INTERFACE	AM62x	AM62Lx	DESIGN NOTES
CAN-FD / UART	• Wake-capable • Connected VDDSHV_CANUART (1.8V/3.3V)	• No wake support • No VDDSHV_CANUART	Verify voltage domain alignment. For AM62Lx, EXT_WAKEUP/ EXTINTn for wake.
USB 2.0	• 2× ports • Configurable modes • Integrated PHY • VBUS monitoring		N/A
SPI / McASP	• 4× SPI • 3× McASP	• 4× SPI • 3× McASP	Verify voltage domain alignment.

5.3 Media and Display Interfaces

The multimedia features of the AM62Lx are reduced compared to AM62x. Some changes in display and camera interfaces, where audio remains the same. Table 5-3 lists the overview of what to change for the multimedia peripherals.

For more detailed information, see the respective AM62x Sitara™ Processors data sheet or AM62Lx Sitara™ Processors data sheet *Peripherals* section.

Table 5-3. Media and Display Interface Differences

INTERFACE	AM62x	AM62Lx	DESIGN NOTES
Graphics & Display	• 3D GPU (Open GL ES 3.1/ Vulkan 1.2) • Dual display output up to 1080p60 each • 24-bit DPI • Dual OLDI (LVDS)	• No GPU • Single display output up to 1080p60 • Either 24-bit DPI or 4-lane MIPI DSI • No OLDI/LVDS output	Due to clocking limitations, only one of the interfaces, either DSI or DPI, can be used at once.
Camera (CSI-2)	• 4-lane MIPI CSI-2 receiver	• No CSI	N/A
Audio (McASP)	• 3× McASP ports	• 3× McASP ports	Verify voltage domain alignment.

5.4 Analog and Other Interfaces

AM62Lx adds an on-chip ADC and simplifies some functions when compared to AM62x. The *Analog and Other Interfaces Comparison* table highlights the differences in ADC, temperature sensing, and PRU support.

For more detailed information see the respective AM62x Sitara™ Processors data sheet or AM62Lx Sitara™ Processors data sheet *Peripherals* section, and relevant E2E forums: [FAQ] AM62x/AM62Lx Voltage and Thermal Manager.

Table 5-4. Analog and Other Interfaces Comparison

FEATURE	AM62x	AM62Lx	DESIGN NOTES
ADC	• External only (no on-chip)	• 4× analog inputs (time multiplexed) • 12-bit (approximately 10 ENOB) • Up to 4MSPS	Provide VDDA_ADC 1.8V and decouple per AM62Lx data sheet.
Temp Sensor	• Temp Sensor 0: DDR controller • Temp Sensor 1: A53	• Temp Sensor 0: DDR/A53	Accuracy of internal temperature sensor is +/- 5 °C. Refer to the AM62Lx Sitara™ Processors data sheet *Temperature Sensor Characteristics* section.

Table 5-4. Analog and Other Interfaces Comparison (continued)

FEATURE	AM62x	AM62Lx	DESIGN NOTES
PRU-ICSS	• Present	• Not present	N/A

6 Boot Configuration and Reset Changes

AM62Lx streamlines the bootstrapping and reset structure compared to AM62x. The Table 6-1 table lists new bootstrap pin requirements, supported boot media, and other boot and reset-related changes.

For AM62Lx helpful FAQs and an overview on boot configuration, check the respective AM62Lx Schematic Design Guidelines and Schematic Review Checklist or AM62x Schematic Design Guidelines and Review Checklist *Configuration of Boot Modes for Processor* section.

For more detailed boot mode information and pin-mux settings, refer to the respective AM62Lx Sitara™ Processors data sheet or AM62x Sitara™ Processors data sheet *Pin Attributes* section, and the respective AM62L Technical Reference Manual or AM62x Technical Reference Manual *Boot Mode Pins* section.

Table 6-1. Boot and Reset Signal Changes

ASPECT	AM62x	AM62Lx	DESIGN NOTES
Bootstrap Pins Options	• 16 boot mode pins (BOOTMODE[15:0])	• Reduced Pincount: 4 bootstrap pins (BOOTMODE[15:12]) • Full Pincount: 16 bootstrap pins (BOOTMODE[15:0])	Boot pins must be pulled up or down and not floating. For more information, refer to the AM62L Technical Reference Manual *Boot Mode Pin Mapping Options* Section.
Boot Modes	• UART • I2C EEPROM • OSPI/QSPI Flash • GPMC NOR/NAND Flash • Serial NAND Flash • SD Card • eMMC • USB • Ethernet	• UART • No I2C EEPROM • OSPI/QSPI Flash • GPMC NAND (no NOR) Flash • No Serial NAND Flash • SD Card • eMMC • USB • No Ethernet	For AM62Lx, remove old boot circuitry to reduce BOM and simplify design. See AM62x Sitara™ Processors data sheet, and AM62Lx Sitara™ Processors data sheet for supported options.
Reset Inputs	• MCU_PORz • MCU_RESETz • RESET_REQz	• PORz • RESETz • RTC_PORz • No MCU_PORz	N/A
Reset Outputs	• PORz_OUT • RESETSTATz • MCU_RESETSTATz	• RESETSTATz • No MCU_RESETSTATz	N/A
Wake Pins	• EXTINTn • partial CAN/UART on MCU domain	• EXTINTn • EXT_WAKEUP0/1 • No CAN/UART wake (no MCU)	For AM62Lx, if not connected to a wake source, connect EXT_WAKEUP0/1 to corresponding power supply through external pull-resistor.

7 Package and Layout Considerations

7.1 BGA Package Options

The *Package Variants Comparison* table summarizes the overall package size, ball count, and ball pitch differences of the various package options. The AM62x family of processors offers two package options. The smaller of the two package options has a 0.5mm ball pitch and is only available in the non-Q1 qualified devices. The larger of the two package options has a 0.8mm ball pitch and is only available in the Q1 qualified devices. Each of the two AM62x package options are larger and have more balls than the AM62Lx package option, which also has a 0.5mm ball pitch. Note that AM62Lx processors do not currently offer Q1 qualified variants.

For full mechanical drawings and valid device orderable part numbers, refer to the *Mechanical, Packaging, and Orderable Information* section in the respective AM62x Sitara™ Processors and AM62Lx Sitara™ Processors data sheet. Design recommendations can be found in the AM62Lx Schematic Design Guidelines and Schematic Review Checklist.

Table 7-1. Package Variants Comparison

PARAMETER	AM62x ALW Package • AM625x • AM623x	AM62x AMC Package • AM625-Q1 • AM620-Q1	AM62Lx ANB Package • AM62Lx
Package Size	13mm × 13mm	17.2mm × 17.2mm	11.9mm × 11.9mm
Ball Pitch	0.5mm	0.8mm	0.5mm
Ball Count	425-ball, FCCSP BGA	441-ball, FCBGA	373-ball, FCCSP BGA

7.2 Thermal and Power Dissipation

Thermal and power behavior depends on device configuration and package selection. In general, AM62x can draw more power at peak performance due to the quad cores and optional GPU, while AM62Lx typically draws less due to fewer cores and no GPU. Package choice also affects thermal resistance; see Table 7-2. Always validate with workload-based power estimation and system-level thermal testing.

For junction-to-ambient thermal data and via-in-pad guidance, see the *Thermal, Resistance Characteristics* section in the respective AM62x Sitara™ Processors and AM62Lx Sitara™ Processors data sheet, and relevant E2E forums: [FAQ] AM62x/AM62Lx Voltage and Thermal Manager.

Table 7-2. Thermal and Power Dissipation Comparison

METRIC	AM62x	AM62Lx	DESIGN NOTES
Active Cores	• Up to 4× Cortex-A53, M4, GPU on some packages	• Up to 2× Cortex-A53 (No MCU/GPU)	For more information on device power consumption, see the AM62x Power Estimation Tool application note.
Core Voltage	• VDD_CORE dual-voltage (0.75V/0.85V) • VDDR_CORE fixed 0.85V	• Single 0.75V rail	
Junction-to-Case (°C/W)	• ALW package: 3.7 • AMC package: 1.2	• ANB package: 5.2	Verify cooling with thermal simulation or testing; check *Thermal Resistance Characteristics* section in the relevant processor data sheet for more information.
Junction-to-Air (°C/W, Still Air)	• ALW package: 22.3 • AMC package:13.3	• ANB package: 22.2	

8 Summary

This document summarizes the migration between AM62x and AM62Lx. Choose the device based on performance or features, versus power or BOM targets, then confirm package, pinout, power and thermal implications using the contents of this document and references.

If migrating from AM62x to AM62Lx, expect lower BOM and power. Plan for fewer A53 cores and no GPU, potential changes to display and graphics options, and differences in peripheral counts and boot modes. Validate the single 0.75V core rail, IO bank voltages, and any pinout and package differences. Designers must account for different pinouts, package sizes, and thermal characteristics, and use the AM62Lx Schematic Design Guidelines and Schematic Review Checklist to verify a correct implementation in the updated design.

If migrating from AM62Lx to AM62x, expect higher compute with up to 4× A53 cores, and optional GPU, with broader display and peripheral options. Plan for higher power and thermal budget, possible split core domains (selectable 0.75V/0.85V VDD_CORE with fixed 0.85V VDDR_CORE), and verify package pin availability for DDR, display, and high-speed IO. Designers must account for different pinouts, package sizes, and thermal characteristics, and use the AM62x Schematic Design Guidelines and Review Checklist to verify a correct implementation in the updated design.

9 Terminology and Acronyms

- AAD-mux: Address-Address/Data multiplexed mode
- ADC: Analog-to-Digital Converter
- ALW: Package code for 13 × 13mm AM62x
- AMC: Package code for 17.2 × 17.2mm AM62x
- ANB: Package code for 11.9 × 11.9mm AM62Lx
- BOM: Bill of Materials
- BGA: Ball Grid Array
- BSP: Board Support Package
- CAN-FD: Controller Area Network with Flexible Data rate
- °C/W: Degrees Celsius per Watt
- CPU: Central Processing Unit
- CS: Chip Select
- DDR: Double Data Rate
- DDR4: Fourth-generation Double Data Rate
- DPI: Display Parallel Interface
- DRD: Dual-Role Device
- E2E: Engineer-to-Engineer (Texas Instruments support forum)
- EEPROM: Electrically Erasable Programmable Read-Only Memory
- ENOB: Effective Number of Bits
- eFuse: Electronic Fuse
- eMMC: Embedded MultimediaCard
- EVM: Evaluation Module
- EXTINTn: External Interrupt Pin
- EXT_WAKEUP: External Wake-Up Pin
- FAQ: Frequently Asked Question
- FCBGA: Flip-Chip Ball Grid Array
- GPMC: General Purpose Memory Controller
- GPU: Graphics Processing Unit
- GPIO: General Purpose Input/Output
- HS200: High Speed 200 MB/s (for eMMC)
- I2C: Inter-Integrated Circuit
- ICSS: Industrial Communication Subsystem
- IEEE: Institute of Electrical and Electronics Engineers
- IO: Input/Output
- JTAG: Joint Test Action Group
- L1: Level 1 (cache)
- L2: Level 2 (cache)
- LDO: Low Drop-Out regulator
- LPDDR4: Low Power Double Data Rate 4^{th} generation
- LVDS: Low Voltage Differential Signaling
- MCU: Microcontroller Unit
- McASP: Multi-Channel Audio Serial Port
- MDIO: Management Data Input/Output
- Processor Interface
- MSPS: Million Samples Per Second
- OLDI: Open LVDS Display Interface
- OTP: One-Time Programmable
- OSPI: Octal Serial Peripheral Interface
- PMIC: Power Management Integrated Circuit
- PORz: Power-On Reset
- PRU: Programmable Realtime Unit
- PRUSS: Programmable Real-time Unit Subsystem
- PWM: Pulse Width Modulation
- QSPI: Quad Serial Peripheral Interface

- RGMII: Reduced Gigabit Media Independent Interface
- RMII: Reduced Media Independent Interface
- RTC: Real-Time Clock
- SD: Secure Digital
- SDIO: Secure Digital Input/Output
- SMS: Security Management System
- SoC: System on Chip
- SPL: Secondary Program Loader
- TRM: Technical Reference Manual
- Tx: Transmit
- UHS-I: Ultra High-Speed Phase I (SD bus mode)
- UART: Universal Asynchronous Receiver/Transmitter
- U-Boot: Universal Boot
- USB: Universal Serial Bus
- VBUS: Voltage Bus
- VTM: Voltage and Thermal Manager
- WKUP: Wakeup

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