Application Note

TDP0604 HDMI1.4/2.0 Electrical Compliance Test Tuning Guide

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ABSTRACT

HDMI 2.0 supports up to 18Gbps total bandwidth (6Gbps per channel, with three TMDS data links). The insertion loss budget is usually calculated for the entire transmission path (including the loss of the motherboard PCB trace, vias, connectors, cables, and the equalization capability of the receiving end.) During the design, if the total insertion loss exceeds the HDMI source and receiver compensation capability then consider adding designs such as a redriver pr a retimer. Between them, the redriver is more popular in economical design projects because of the cost advantage. This application note introduces and uses the latest HDMI 2.0 redriver (TDP0604) to discuss and share how to make correct adjustments when executing the HDMI compliance test to achieve a passing result.

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Trademarks

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1 Introduction

This application note discusses how to perform the HDMI electrical compliance test and adjusts several TDP0604 registers such as equalization (EQ), differential output voltage (VoD), and slew rate to obtain different and ultimately passing results. The application note also provides a TDP0604 I2C control script example.

2 Test Setup

2.1 Block Diagram

The DUT is a motherboard (MB) with TDP0604 and the Aardvark I2C/SPI controller is used as the I2C host to config TDP0604, the MB HDMI port connects to a test fixture. The fixture breaks out the HDMI three TMDS data lane, one clock lane, and the DDC bus. The three TMDS data and the clock lane are connected to an oscilloscope for the electrical compliance testing. The DDC bus is connected to an EDID emulator that acts as a HDMI sink to let the MB detecting as a monitor and send the display signal out.

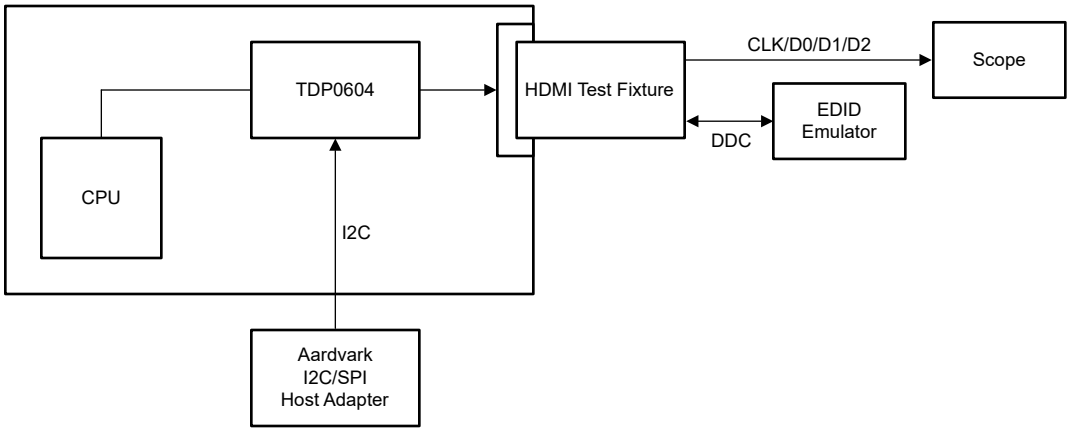

Figure 2-1. Block Diagram of the Test Platform

2.2 Aardvark I2C and SPI Controller

The proper software must be downloaded from the Total Phase on a personal laptop that includes Total Phase Control Center v4.5.0 and the Aardvark I2C and SPI Host Adapter.

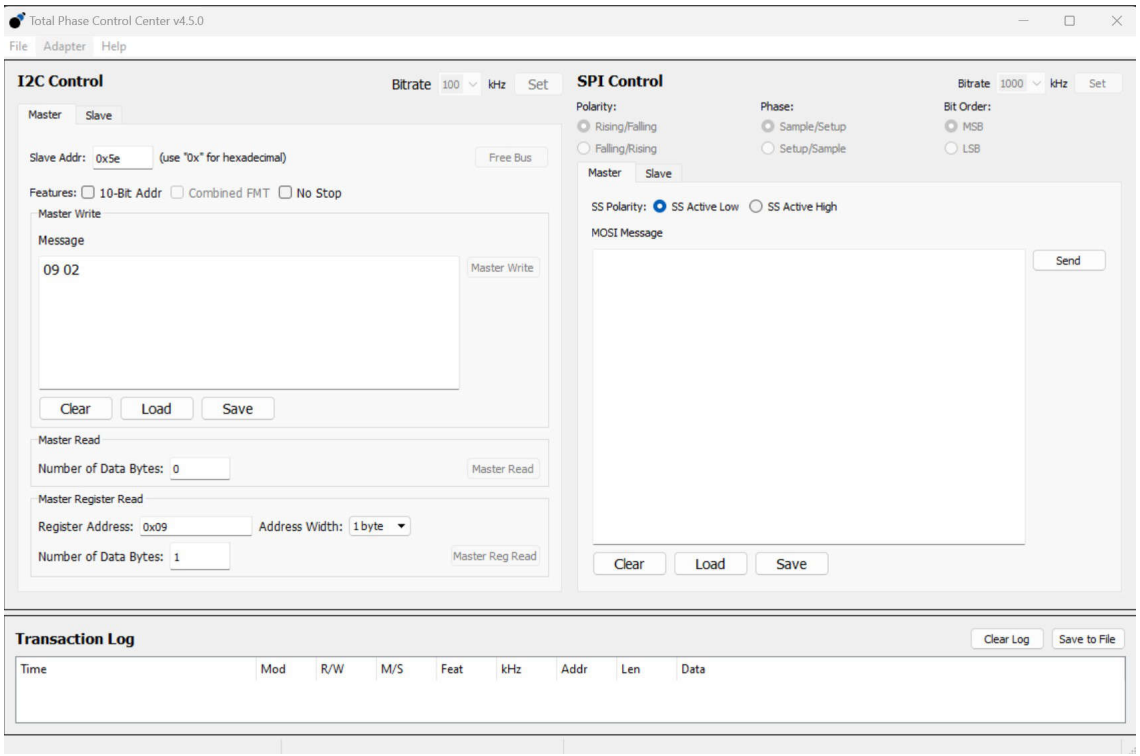

Figure 2-2. Total Phase Control Center App Screenshot

Total Phase Control Center provides a *batch mode* which allows the user to load a series of commands that are executed in sequence.

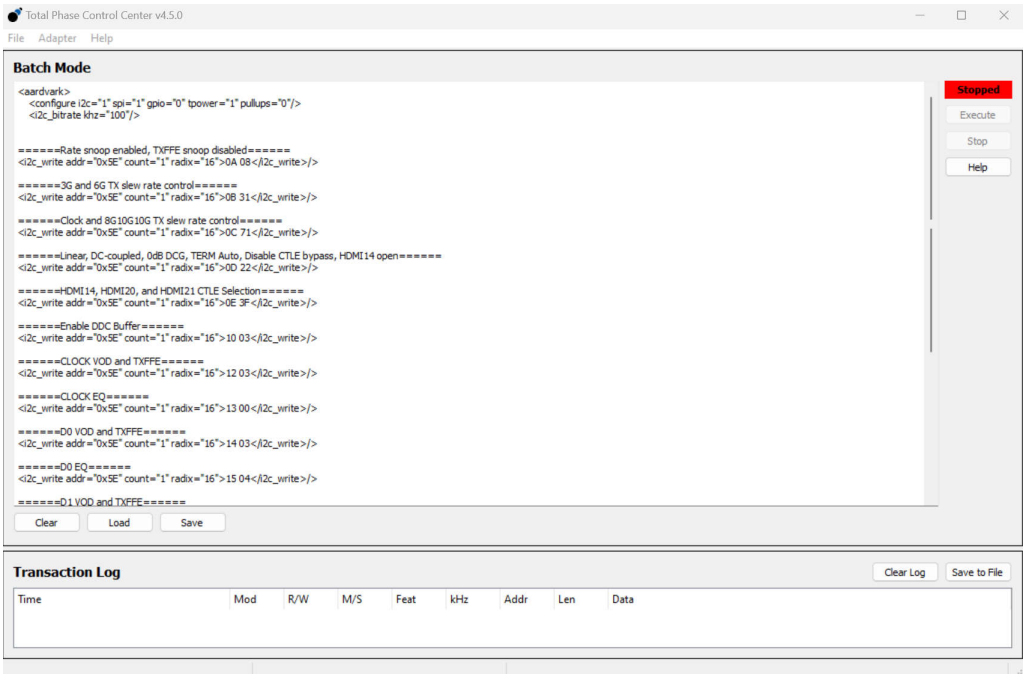

Figure 2-3. Total Phase Control Center Batch Mode

An example batch script for TDP0604 [follower address = 5Eh(7bit)] is shown here:

```
<aardvark>

<configure i2c="1" spi="1" gpio="0" tpower="1" pullups="0"/>
<i2c_bitrate khz="100"/>

======Rate snoop enabled, TXFFE snoop enabled. Enable SWAP======
<i2c_write addr="0x5E" count="1" radix="16">0A 08</i2c_write>/>

======3G and 6G TX slew rate control======
<i2c_write addr="0x5E" count="1" radix="16">0B 31</i2c_write>/>

======Clock and 8G10G10G TX slew rate control======
<i2c_write addr="0x5E" count="1" radix="16">0C 71</i2c_write>/>

======Linear, DC-coupled, 0dB DCG, TERM Auto, Disable CTLE bypass. HDMI14 open======
<i2c_write addr="0x5E" count="1" radix="16">0D 22</i2c_write>/>

======HDMI14, HDMI20, and HDMI21 CTLE Selection======
<i2c_write addr="0x5E" count="1" radix="16">0E 3F</i2c_write>/>

======Enable DDC Buffer======
<i2c_write addr="0x5E" count="1" radix="16">10 03</i2c_write>/>

======Lane enable HDMI1P4_2P0_VOD enable======
<i2c_write addr="0x5E" count="1" radix="16">11 5F</i2c_write>/>

======CLOCK VOD and TXFFE======
<i2c_write addr="0x5E" count="1" radix="16">12 03</i2c_write>/>

======CLOCK EQ======
<i2c_write addr="0x5E" count="1" radix="16">13 00</i2c_write>/>

======D0 VOD and TXFFE======
<i2c_write addr="0x5E" count="1" radix="16">14 03</i2c_write>/>

======D0 EQ======
<i2c_write addr="0x5E" count="1" radix="16">15 04</i2c_write>/>

======D1 VOD and TXFFE======
<i2c_write addr="0x5E" count="1" radix="16">16 03</i2c_write>/>

======D1 EQ======
<i2c_write addr="0x5E" count="1" radix="16">17 04</i2c_write>/>

======D2 VOD and TXFFE======
<i2c_write addr="0x5E" count="1" radix="16">18 03</i2c_write>/>

======D2 EQ======
<i2c_write addr="0x5E" count="1" radix="16">19 04</i2c_write>/>

======Read 0x20 to know HDMI1P4_2P0 TMDS_CLK_RATIO ======
<i2c_write addr="0x5E" count="1" radix="16">20</i2c_write>/>
<i2c_read addr="0x5E" count="1"/>

======Take out of Power down mode. HPD_OUT is asserted high if HPD_IN is high======
<i2c_write addr="0x5E" count="1" radix="16">09 02</i2c_write>/>

<aardvark>
```

2.3 EDID Emulator

The EDID emulator acts as an HDMI sink and provides appropriate EDID and SCDC registers so the HDMI source can be configured into different resolutions. For example, to perform HDMI2.0 electrical compliance testing, the EDID emulator emulates a 4K (4096 × 2160 at 60Hz) resolution, so that the system can identify this EDID and output a 4K resolution display signal for testing.

2.4 Enable TDP0604 in I2C Mode and Set Target I2C Address

This application note uses Aardvark as an I2C master to configure the TDP0604 register setting. As a result, the register setting requires TDP0604 in I2C mode. The TDP0604 has 4-level inputs pins that control the receiver equalization gain, transmitter voltage swing, and pre-emphasis, and places TDP0604 into different modes of operation. Use Table 2-1 and set the MODE pin for *F* level input which floats the pin in HW.

Table 2-1. Level Control Pin Settings

Level	Settings
0	Tie 1kΩ 5% to GND
R	Tie 20kΩ 5% to GND
F	Float (leave pin open)
1	Tie 1kΩ 5% to V_{CC}

Table 2-2. Mode Pin Functions

Mode Pin Function	Description
0	Pin strap with DDC buffer enabled
R	Pin strap with DDC buffer disabled
F	I2C mode
1	Reserved

Besides the I2C mode enable, the TDP0604 on the I2C bus also requires a target I2C address. TDP0604 has a ADDR/EQ0 pin to represent the address bit for I2C programming when TDP0604 is configured for I2C mode. So in this application note, there is an example to config this pin with 1kΩ to GND to set level *0*. Level *0* listed in Table 2-3 results in target I2C address 0xBCh(Read/8bit)/BDh(Write/8bit) or equal to 0x5E (7bit).

Table 2-3. TDP0604 I2C Device Address Description

ADDR/EQ0 Pin	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (W/R)	HEX
0	1	0	1	1	1	1	0	0/1	BC/BD
R	1	0	1	1	1	0	1	0/1	BA/BB
F	1	0	1	1	1	0	0	0/1	B8/B9
1	1	0	1	1	0	1	1	0/1	B6/B7

3 TDP0604 Controls for HDMI Compliance Testing

This section shows several examples by adjusting different settings to get different results with different HDMI1.4 /2.0 resolutions. Different results are observed and the correct adjustment value is tuned to pass the test.

3.1 Data Eye Diagram in Different EQ

3.1.1 HDMI2.0 Test with Resolution 4096 × 2160_60p_8bit_444

3.1.1.1 D1 NegativeLane, EQ = 0

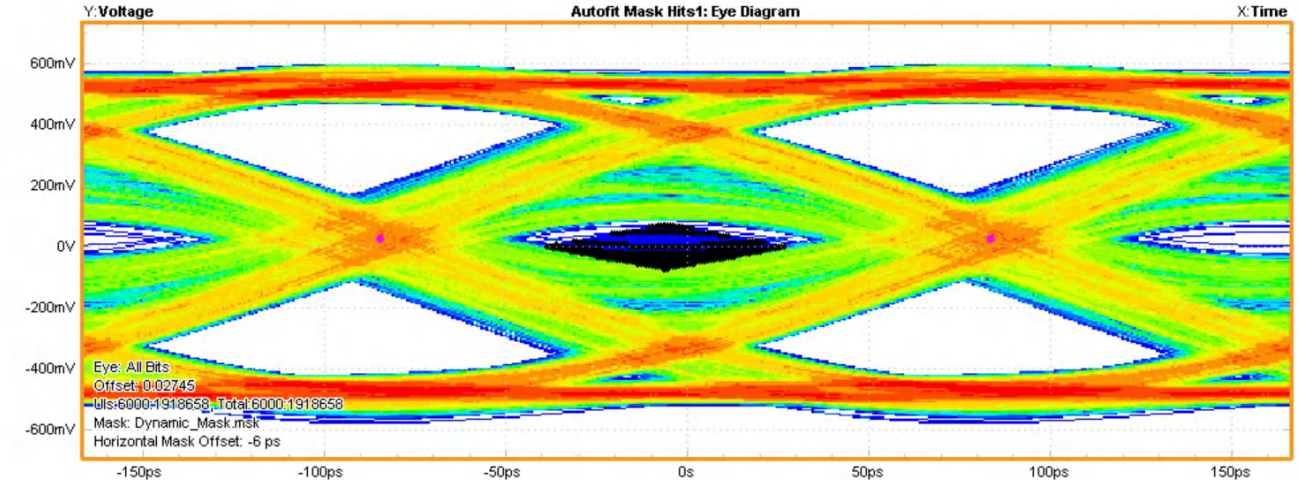

Figure 3-1. HDMI2.0_4K_60fps Test Eye Mask (EQ = 0)

3.1.1.2 D1 NegativeLane, EQ = 4

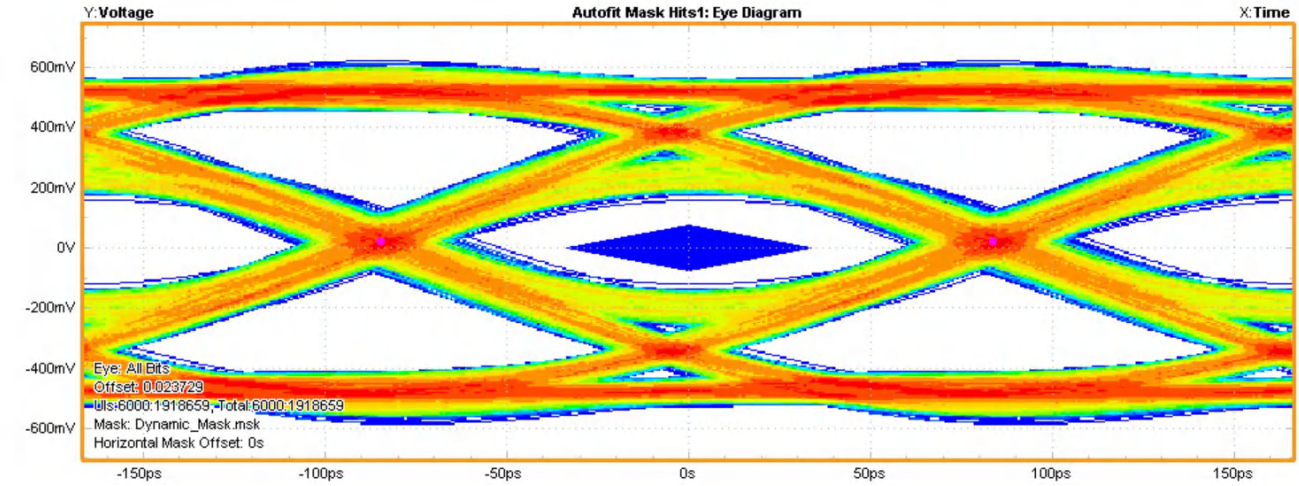

Figure 3-2. HDMI2.0_4K_60fps Test Eye Mask (EQ = 4)

3.1.1.3 D1 NegativeLane, EQ = F

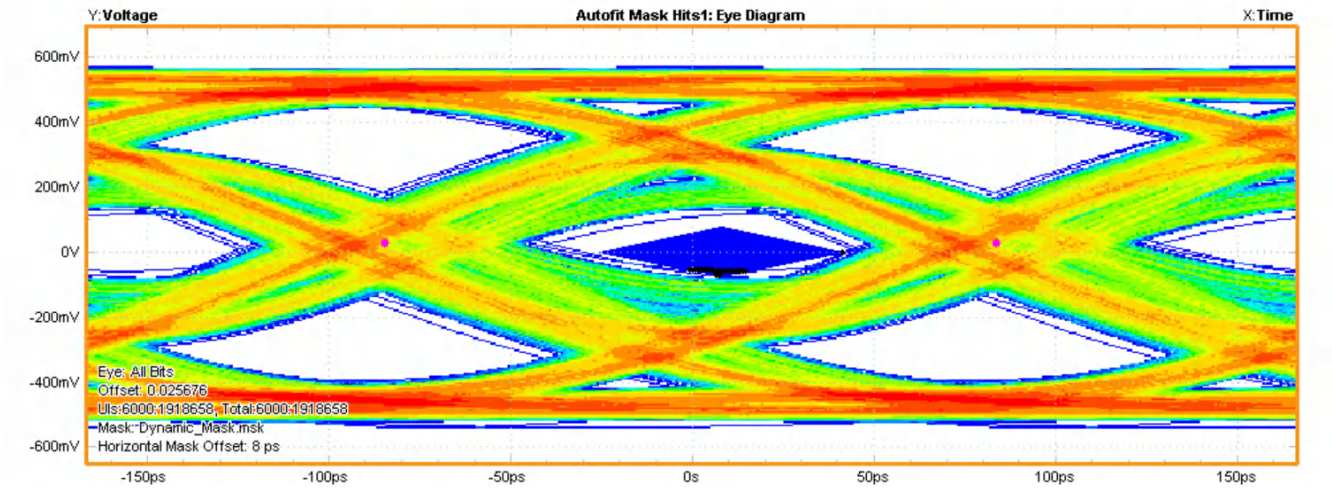

Figure 3-3. HDMI2.0_4K_60fps Test Eye Mask (EQ = F)

3.1.2 HDMI1.4 Test with Resolution 4096 × 2160_30p_8bit_444

3.1.2.1 Source Eye Diagram: CK - D1, EQ = 0

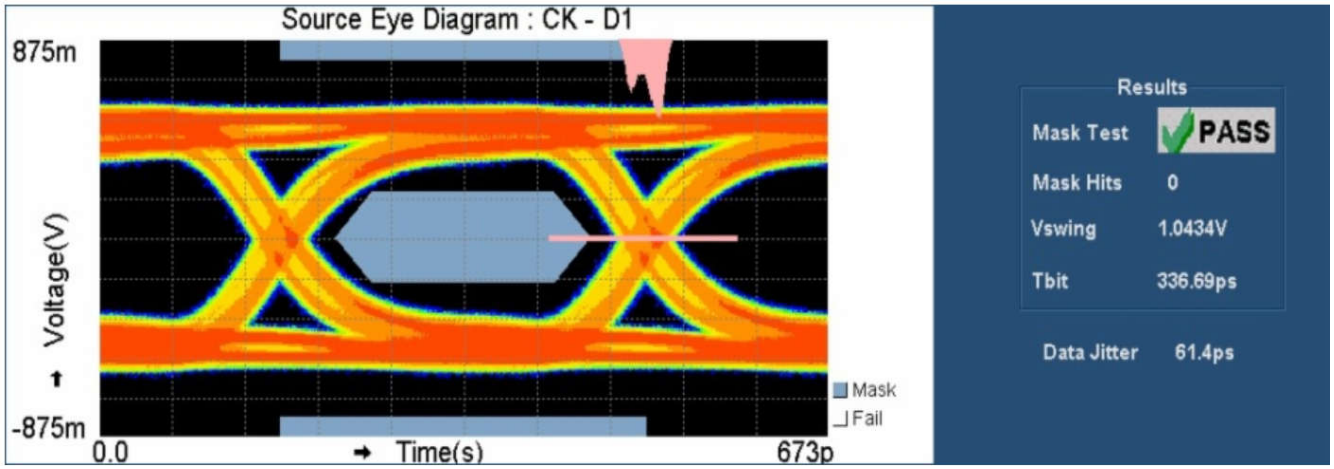

Figure 3-4. HDMI1.4_4K_30fps Test Eye Mask (EQ = 0)

3.1.2.2 Source Eye Diagram: CK - D1, EQ = 4

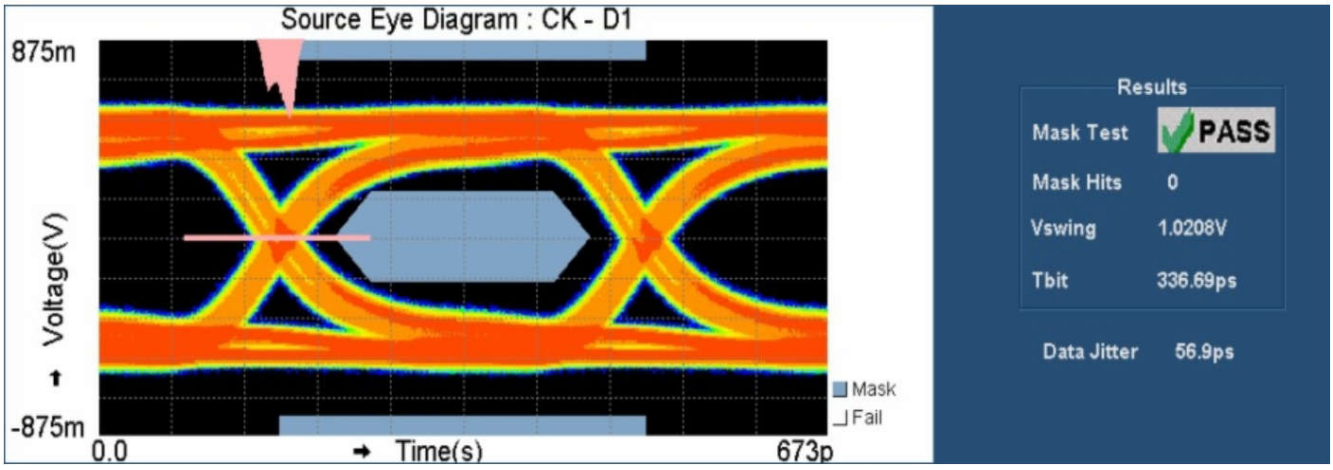

Figure 3-5. HDMI1.4_4K_30fps Test Eye Mask (EQ = 4)

3.1.2.3 Source Eye Diagram: CK - D1, EQ = F

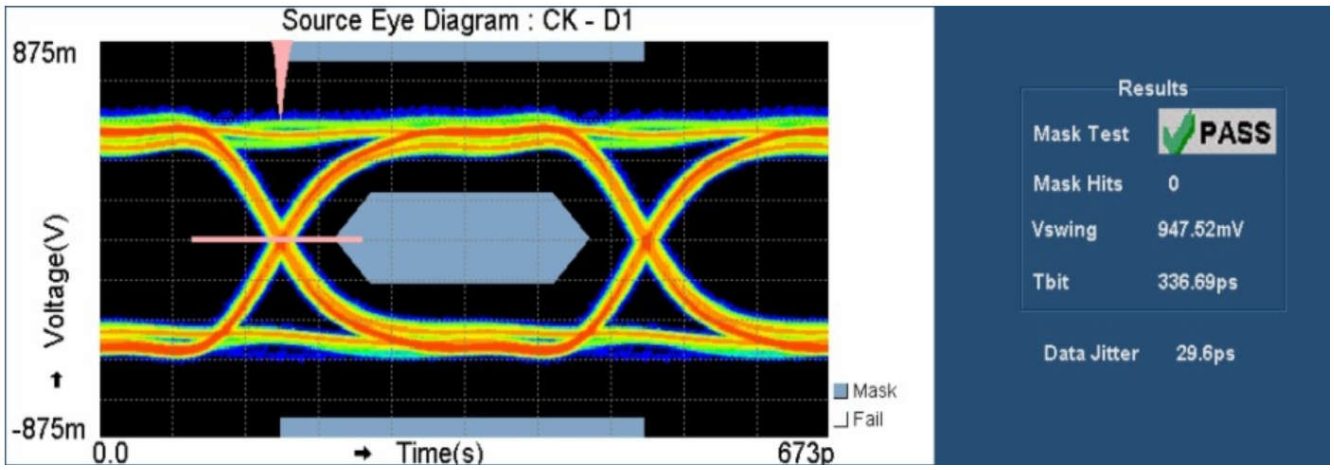

Figure 3-6. HDMI1.4_4K_30fps Test Eye Mask (EQ = F)

3.1.3 HDMI1.4 Test with Resolution 720 × 480_60p_8bit_444

3.1.3.1 Source Eye Diagram: CK - D1, EQ=0

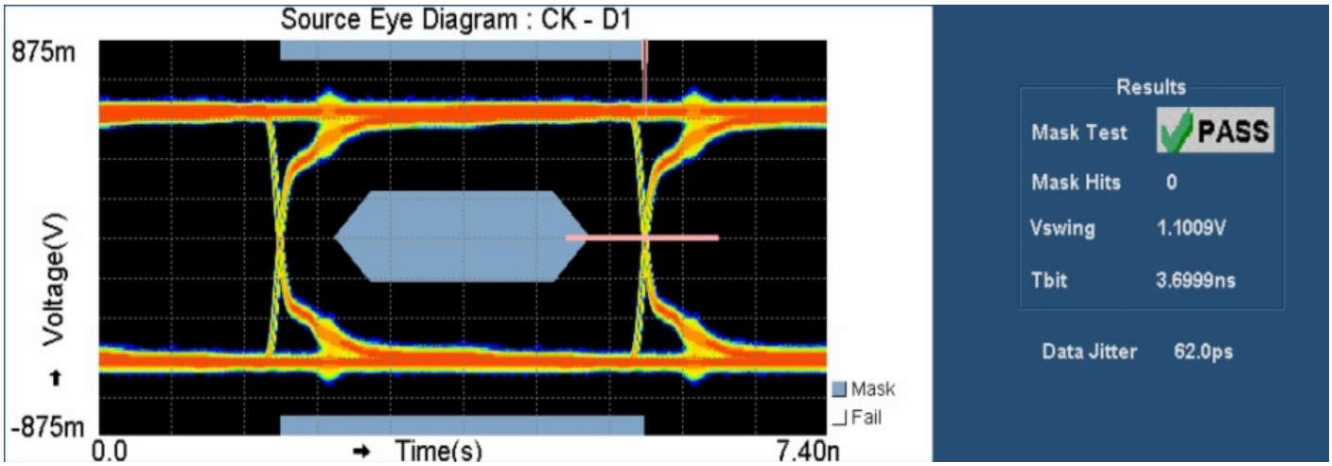

Figure 3-7. HDMI1.4_480p_60fps Test Eye Mask (EQ=0)

3.1.3.2 Source Eye Diagram: CK - D1, EQ = 4

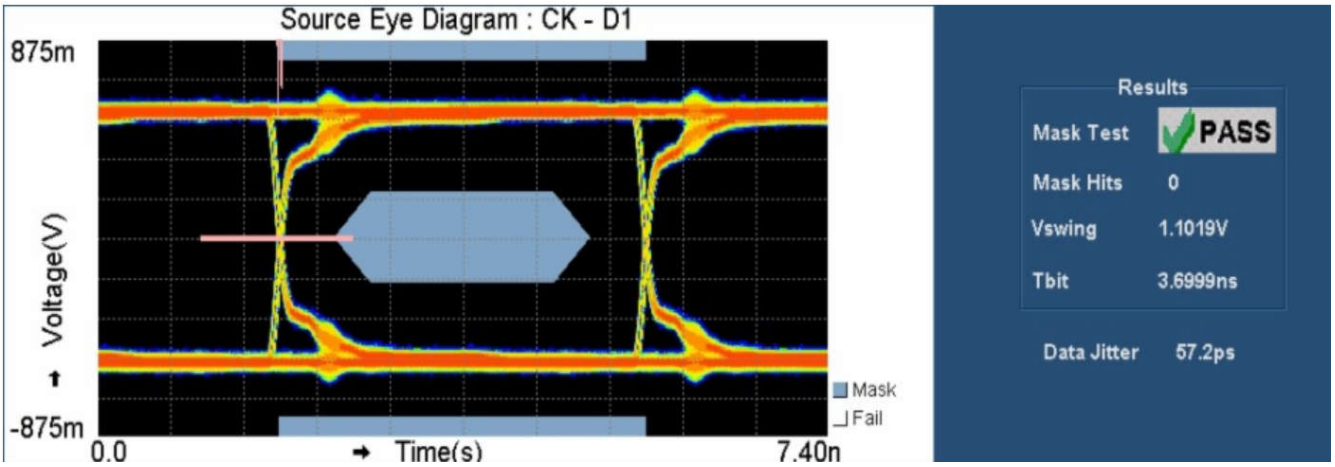

Figure 3-8. HDMI1.4_480p_60fps Test Eye Mask (EQ = 4)

3.1.3.3 Source Eye Diagram: CK - D1, EQ = F

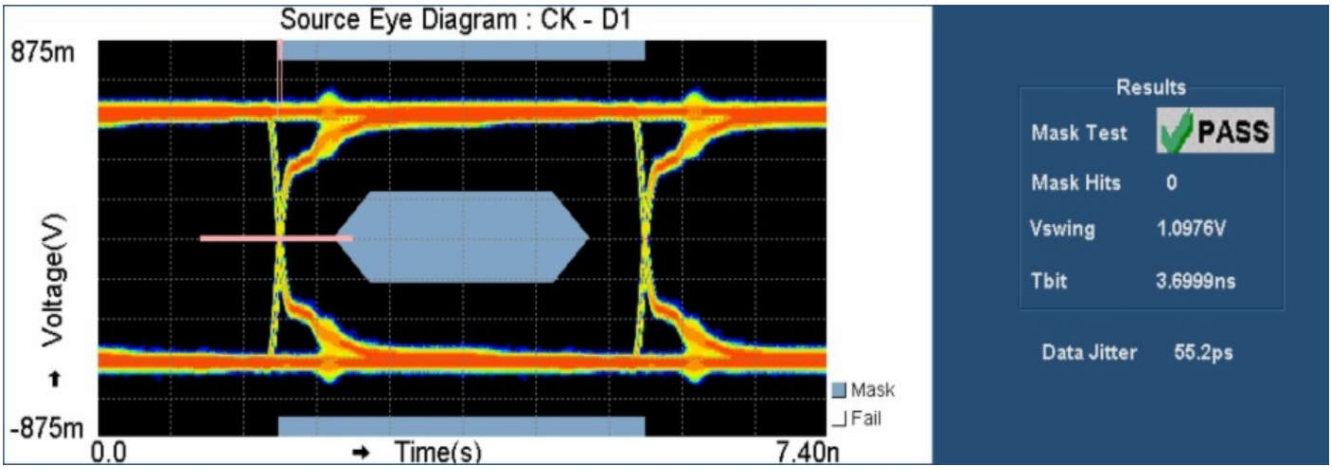

Figure 3-9. HDMI1.4_480p_60fps Test Eye Mask (EQ = F)

3.2 Rising and Falling Resulting in Different Slew Rates

3.2.1 HDMI2.0 Test with Resolution 4096 × 2160_60p_8bit_444

3.2.1.1 TRISE, TFALL when SLEW_3G =3h, SLEW_6G=0h, SLEW_CLK 0 =0h

HF1-2- TRISE, TFALL

Lane Name	Measurement Details	Measured Value	Units	TBit	Data Rate	Test Result	Margin	Low Limit	High Limit	Comments
Clock	Clock Rise Time	179.7593	ps	168.3460 ps	5.94 Gbps	Pass	104.7593	75.0000	-	
Clock	Clock Fall Time	179.6075	ps	168.3460 ps	5.94 Gbps	Pass	104.6075	75.0000	-	
D0	D0 Rise Time	80.6127	ps	168.3460 ps	5.94 Gbps	Pass	38.1127	42.5000	-	
D0	D0 Fall Time	79.8119	ps	168.3460 ps	5.94 Gbps	Pass	37.3119	42.5000	-	
D1	D1 Rise Time	77.4813	ps	168.3460 ps	5.94 Gbps	Pass	34.9813	42.5000	-	
D1	D1 Fall Time	76.8607	ps	168.3460 ps	5.94 Gbps	Pass	34.3607	42.5000	-	
D2	D2 Rise Time	82.4868	ps	168.3460 ps	5.94 Gbps	Pass	39.9868	42.5000	-	
D2	D2 Fall Time	82.8182	ps	168.3460 ps	5.94 Gbps	Pass	40.3182	42.5000	-	
COMMENTS										

Figure 3-10. HDMI2.0_4K_60fps Test Slew Rate (SLEW_3G = 3h, SLEW_6G = 0h, SLEW_CLK = 0h)

3.2.1.2 TRISE, TFALL when SLEW_3G =3h, SLEW_6G=1h, SLEW_CLK 0 =1h

HF1-2- TRISE, TFALL

Lane Name	Measurement Details	Measured Value	Units	TBit	Data Rate	Test Result	Margin	Low Limit	High Limit	Comments
Clock	Clock Rise Time	170.7983	ps	168.3458 ps	5.94 Gbps	Pass	95.7983	75.0000	-	
Clock	Clock Fall Time	171.7427	ps	168.3458 ps	5.94 Gbps	Pass	96.7427	75.0000	-	
D0	D0 Rise Time	80.2006	ps	168.3458 ps	5.94 Gbps	Pass	37.7006	42.5000	-	
D0	D0 Fall Time	78.9200	ps	168.3458 ps	5.94 Gbps	Pass	36.4200	42.5000	-	
D1	D1 Rise Time	77.9838	ps	168.3458 ps	5.94 Gbps	Pass	35.4838	42.5000	-	
D1	D1 Fall Time	77.0102	ps	168.3458 ps	5.94 Gbps	Pass	34.5102	42.5000	-	
D2	D2 Rise Time	86.0967	ps	168.3458 ps	5.94 Gbps	Pass	43.5967	42.5000	-	
D2	D2 Fall Time	86.0807	ps	168.3458 ps	5.94 Gbps	Pass	43.5807	42.5000	-	
COMMENTS										

Figure 3-11. HDMI2.0_4K_60fps Test Slew Rate (SLEW_3G = 3h, SLEW_6G = 1h, SLEW_CLK = 1h)

3.2.1.3 TRISE, TFALL when SLEW_3G =3h, SLEW_6G=7h, SLEW_CLK 0 =7h

HF1-2- TRISE, TFALL

Lane Name	Measurement Details	Measured Value	Units	TBit	Data Rate	Test Result	Margin	Low Limit	High Limit	Comments
Clock	Clock Rise Time	82.3938	ps	168.3460 ps	5.94 Gbps	Pass	7.3938	75.0000	-	
Clock	Clock Fall Time	76.7717	ps	168.3460 ps	5.94 Gbps	Pass	1.7717	75.0000	-	
D0	D0 Rise Time	57.2870	ps	168.3460 ps	5.94 Gbps	Pass	14.7870	42.5000	-	
D0	D0 Fall Time	55.0670	ps	168.3460 ps	5.94 Gbps	Pass	12.5670	42.5000	-	
D1	D1 Rise Time	58.0699	ps	168.3460 ps	5.94 Gbps	Pass	15.5699	42.5000	-	
D1	D1 Fall Time	57.2474	ps	168.3460 ps	5.94 Gbps	Pass	14.7474	42.5000	-	
D2	D2 Rise Time	58.4076	ps	168.3460 ps	5.94 Gbps	Pass	15.9076	42.5000	-	
D2	D2 Fall Time	57.5933	ps	168.3460 ps	5.94 Gbps	Pass	15.0933	42.5000	-	
COMMENTS										

Figure 3-12. HDMI2.0_4K_60fps Test Slew Rate (SLEW_3G = 3h, SLEW_6G = 7h, SLEW_CLK = 7h)

3.2.2 HDMI1.4 Test with Resolution 4096 × 2160_30p_8bit_444

3.2.3 TRISE, TFALL when SLEW_3G =0h, SLEW_6G=1h, SLEW_CLK 0 =0h

Table 3-1. HDMI1.4_4K_30fps Test Slew Rate (SLEW_3G =0h, SLEW_6G=1h, SLEW_CLK=0h)

Index	Test Name	Lanes	Spec Range	Meas Value	Result
1	7-4: Source Rise Time	CK	75.00ps < TRISE	177.27ps	Pass
2	7-4: Source Rise Time	D0	75.00ps < TRISE	184.82ps	Pass
3	7-4: Source Rise Time	D1	75.00ps < TRISE	176.23ps	Pass
4	7-4: Source Rise Time	D2	75.00ps < TRISE	167.89ps	Pass
5	7-4: Source Fall Time	CK	75.00ps < TFALL	180.77ps	Pass
6	7-4: Source Fall Time	D0	75.00ps < TFALL	181.37ps	Pass
7	7-4: Source Fall Time	D1	75.00ps < TFALL	170.22ps	Pass
8	7-4: Source Fall Time	D2	75.00ps < TFALL	176.58ps	Pass

3.2.4 TRISE, TFALL when SLEW_3G =3h, SLEW_6G=1h, SLEW_CLK 0 =1h

Table 3-2. HDMI1.4_4K_30fps Test Slew Rate (SLEW_3G =3h, SLEW_6G=1h, SLEW_CLK=1h)

Index	Test Name	Lanes	Spec Range	Meas Value	Result
8	7-4: Source Rise Time	CK	75.00ps < TRISE	162.29ps	Pass
9	7-4: Source Rise Time	D0	75.00ps < TRISE	129.76ps	Pass
10	7-4: Source Rise Time	D1	75.00ps < TRISE	128.04ps	Pass
11	7-4: Source Rise Time	D2	75.00ps < TRISE	125.23ps	Pass
12	7-4: Source Fall Time	CK	75.00ps < TFALL	167.05ps	Pass
13	7-4: Source Fall Time	D0	75.00ps < TFALL	126.26ps	Pass
14	7-4: Source Fall Time	D1	75.00ps < TFALL	126.12ps	Pass
15	7-4: Source Fall Time	D2	75.00ps < TFALL	126.50ps	Pass

3.2.5 TRISE, TFALL when SLEW_3G =7h, SLEW_6G=1h, SLEW_CLK 0 =7h

Table 3-3. HDMI1.4_4K_30fps Test Slew Rate (SLEW_3G =7h, SLEW_6G=1h, SLEW_CLK=7h)

Index	Test Name	Lanes	Spec Range	Meas Value	Result
1	7-4: Source Rise Time	CK	75.00 < TRISE;	123.10	Pass
2	7-4: Source Rise Time	D0	75.00 < TRISE;	114.85	Pass
3	7-4: Source Rise Time	D1	75.00 < TRISE;	109.25	Pass
4	7-4: Source Rise Time	D2	75.00 < TRISE;	105.19	Pass
5	7-4: Source Fall Time	CK	75.00 < TFALL;	123.90	Pass
6	7-4: Source Fall Time	D0	75.00 < TFALL;	112.03	Pass
7	7-4: Source Fall Time	D1	75.00 < TFALL;	104.05	Pass
8	7-4: Source Fall Time	D2	75.00 < TFALL;	103.77	Pass

3.2.6 HDMI1.4 Test with Resolution 720 × 480_60p_8bit_444

3.2.6.1 TRISE, TFALL when SLEW_3G = 0h, SLEW_6G = 1h, SLEW_CLK 0 = 0h

Table 3-4. HDMI1.4_480p_60fps Test Slew Rate (SLEW_3G =0h, SLEW_6G=1h, SLEW_CLK=0h)

Index	Test Names	Lanes	Specification Range	Meas Value	Result
1	7-4: Source Rise Time	CK	75.00ps < TRISE;	313.55ps	Pass
2	7-4: Source Rise Time	D0	75.00ps < TRISE;	348.17ps	Pass
3	7-4: Source Rise Time	D1	75.00ps < TRISE;	352.35ps	Pass
4	7-4: Source Rise Time	D2	75.00ps < TRISE;	288.24ps	Pass
5	7-4: Source Rise Time	CK	75.00ps < TFALL;	307.47ps	Pass
6	7-4: Source Rise Time	D0	75.00ps < TFALL;	332.91ps	Pass
7	7-4: Source Rise Time	D1	75.00ps < TFALL;	328.74ps	Pass
8	7-4: Source Rise Time	D2	75.00ps < TFALL;	301.89ps	Pass

3.2.6.2 TRISE, TFALL when SLEW_3G = 3h, SLEW_6G = 1h, SLEW_CLK 0 = 1h

Table 3-5. HDMI1.4_480p_60fps Test Slew Rate (SLEW_3G = 3h, SLEW_6G = 1h, SLEW_CLK = 1h)

Index	Test Names	Lanes	Specification Range	Meas Value	Results
8	7-4: Source Rise Time	CK	75.00ps < TRISE;	291.51	Pass
9	7-4: Source Rise Time	D0	75.00ps < TRISE;	281.89	Pass
10	7-4: Source Rise Time	D1	75.00ps < TRISE;	293.08	Pass
11	7-4: Source Rise Time	D2	75.00ps < TRISE;	188.39	Pass
12	7-4: Source Rise Time	CK	75.00ps < TFALL;	281.31	Pass
13	7-4: Source Rise Time	D0	75.00ps < TFALL;	255.71	Pass
14	7-4: Source Rise Time	D1	75.00ps < TFALL;	263.85	Pass
15	7-4: Source Rise Time	D2	75.00ps < TFALL;	218.30	Pass

3.2.6.3 TRISE, TFALL when SLEW_3G = 7h, SLEW_6G = 1h, SLEW_CLK 0 = 7h

Table 3-6. HDMI1.4_480p_60fps Test Slew Rate (SLEW_3G = 7h, SLEW_6G = 1h, SLEW_CLK = 7h)

Index	Test Name	Lanes	Spec Range	Meas Value	Result
1	7-4: Source Rise Time	CK	75.00ps < TRISE;	184.29	Pass
2	7-4: Source Rise Time	D0	75.00ps < TRISE;	262.69	Pass
3	7-4: Source Rise Time	D1	75.00ps < TRISE;	267.06	Pass
4	7-4: Source Rise Time	D2	75.00ps < TRISE;	132.94	Pass
5	7-4: Source Rise Time	CK	75.00ps < TFALL;	186.67	Pass
6	7-4: Source Rise Time	D0	75.00ps < TFALL;	249.81	Pass
7	7-4: Source Rise Time	D1	75.00ps < TFALL;	249.70	Pass
8	7-4: Source Rise Time	D2	75.00ps < TFALL;	131.29	Pass

3.3 VL and VSwing

3.3.1 HDMI2.0 Test with Resolution 4096 × 2160_60p_8bit_444

3.3.1.1 VL and VSwing with HDMI20_VOD =0h, HDMI14_VOD =0h

HF1-1- VL and VSwing

Lane Name	Measurement Details	Measured Value	Units	TBit	Data Rate	Test Result	Margin	Low Limit	High Limit	Comments
Clock	TMDS VLow for Clock+	2.6520	V	168.3460 ps	5.94 Gbps	Pass	0.3520 & 0.4480	2.3	3.1	
Clock	TMDS VLow for Clock-	2.6469	V	168.3460 ps	5.94 Gbps	Pass	0.3469 & 0.4531	2.3	3.1	
Clock	VSwing for Clock+	383.0958	mV	168.3460 ps	5.94 Gbps	Pass	183.0958 & 216.9042	200	600	
Clock	VSwing for Clock-	381.6901	mV	168.3460 ps	5.94 Gbps	Pass	181.6901 & 218.3099	200	600	
D0	TMDS VLow for D0+	2.5759	V	168.3460 ps	5.94 Gbps	Pass	0.2759 & 0.3241	2.3	2.9	
D0	TMDS VLow for D0-	2.5458	V	168.3460 ps	5.94 Gbps	Pass	0.2458 & 0.3542	2.3	2.9	
D0	VSwing for D0+	414.5904	mV	168.3460 ps	5.94 Gbps	Pass	14.5904 & 185.4096	400	600	
D0	VSwing for D0-	404.7286	mV	168.3460 ps	5.94 Gbps	Pass	4.7286 & 195.2714	400	600	
D1	TMDS VLow for D1+	2.5156	V	168.3460 ps	5.94 Gbps	Pass	0.2156 & 0.3844	2.3	2.9	
D1	TMDS VLow for D1-	2.5022	V	168.3460 ps	5.94 Gbps	Pass	0.2022 & 0.3978	2.3	2.9	
D1	VSwing for D1+	442.1562	mV	168.3460 ps	5.94 Gbps	Pass	42.1562 & 157.8438	400	600	
D1	VSwing for D1-	461.6746	mV	168.3460 ps	5.94 Gbps	Pass	61.6746 & 138.3254	400	600	
D2	TMDS VLow for D2+	2.5806	V	168.3460 ps	5.94 Gbps	Pass	0.2806 & 0.3194	2.3	2.9	
D2	TMDS VLow for D2-	2.5565	V	168.3460 ps	5.94 Gbps	Pass	0.2565 & 0.3435	2.3	2.9	
D2	VSwing for D2+	419.7817	mV	168.3460 ps	5.94 Gbps	Pass	19.7817 & 180.2183	400	600	
D2	VSwing for D2-	389.1233	mV	168.3460 ps	5.94 Gbps	Fail	-10.8767 & 210.8767	400	600	

Figure 3-13. HDMI2.0_4K_60fps Test VL and VSwing (HDMI20_VOD =0h, HDMI14_VOD =0h, CLK_VOD, D0_VOD, D1_VOD and D2_VOD = 0h)

3.3.1.2 VL and VSwing with HDMI20_VOD =1h (default 1000mV), HDMI14_VOD =1h (default 1000mV)

HF1-1- VL and VSwing										
Lane Name	Measurement Details	Measured Value	Units	TBit	Data Rate	Test Result	Margin	Low Limit	High Limit	Comments
Clock	TMDS VLow for Clock+	2.5862	V	168.3456 ps	5.94 Gbps	Pass	0.2862 & 0.5138	2.3	3.1	
Clock	TMDS VLow for Clock-	2.5866	V	168.3456 ps	5.94 Gbps	Pass	0.2866 & 0.5134	2.3	3.1	
Clock	VSwing for Clock+	414.4800	mV	168.3456 ps	5.94 Gbps	Pass	214.4800 & 185.5200	200	600	
Clock	VSwing for Clock-	419.2105	mV	168.3456 ps	5.94 Gbps	Pass	219.2105 & 180.7895	200	600	
D0	TMDS VLow for D0+	2.5000	V	168.3456 ps	5.94 Gbps	Pass	0.2000 & 0.4000	2.3	2.9	
D0	TMDS VLow for D0-	2.4717	V	168.3456 ps	5.94 Gbps	Pass	0.1717 & 0.4283	2.3	2.9	
D0	VSwing for D0+	468.3807	mV	168.3456 ps	5.94 Gbps	Pass	68.3807 & 131.6193	400	600	
D0	VSwing for D0-	445.6433	mV	168.3456 ps	5.94 Gbps	Pass	45.6433 & 154.3567	400	600	
D1	TMDS VLow for D1+	2.4409	V	168.3456 ps	5.94 Gbps	Pass	0.1409 & 0.4591	2.3	2.9	
D1	TMDS VLow for D1-	2.4206	V	168.3456 ps	5.94 Gbps	Pass	0.1206 & 0.4794	2.3	2.9	
D1	VSwing for D1+	480.8352	mV	168.3456 ps	5.94 Gbps	Pass	80.8352 & 119.1648	400	600	
D1	VSwing for D1-	511.8712	mV	168.3456 ps	5.94 Gbps	Pass	111.8712 & 88.1288	400	600	
D2	TMDS VLow for D2+	2.4943	V	168.3456 ps	5.94 Gbps	Pass	0.1943 & 0.4057	2.3	2.9	
D2	TMDS VLow for D2-	2.4844	V	168.3456 ps	5.94 Gbps	Pass	0.1844 & 0.4156	2.3	2.9	
D2	VSwing for D2+	474.6607	mV	168.3456 ps	5.94 Gbps	Pass	74.6607 & 125.3393	400	600	
D2	VSwing for D2-	436.2706	mV	168.3456 ps	5.94 Gbps	Pass	36.2706 & 163.7294	400	600	

Figure 3-14. HDMI2.0_4K_60fps Test VL and VSwing (HDMI20_VOD =1h, HDMI14_VOD =1h)

3.3.1.3 VL and VSwing with HDMI20_VOD =0h, HDMI14_VOD =0h

HF1-1- VL and VSwing										
Lane Name	Measurement Details	Measured Value	Units	TBit	Data Rate	Test Result	Margin	Low Limit	High Limit	Comments
Clock	TMDS VLow for Clock+	2.4915	V	168.3459 ps	5.94 Gbps	Pass	0.1915 & 0.6085	2.3	3.1	
Clock	TMDS VLow for Clock-	2.4899	V	168.3459 ps	5.94 Gbps	Pass	0.1899 & 0.6101	2.3	3.1	
Clock	VSwing for Clock+	482.8657	mV	168.3459 ps	5.94 Gbps	Pass	282.8657 & 117.1343	200	600	
Clock	VSwing for Clock-	488.1558	mV	168.3459 ps	5.94 Gbps	Pass	288.1558 & 111.8442	200	600	
D0	TMDS VLow for D0+	2.3917	V	168.3459 ps	5.94 Gbps	Pass	0.0917 & 0.5083	2.3	2.9	
D0	TMDS VLow for D0-	2.3681	V	168.3459 ps	5.94 Gbps	Pass	0.0681 & 0.5319	2.3	2.9	
D0	VSwing for D0+	532.3578	mV	168.3459 ps	5.94 Gbps	Pass	132.3578 & 67.6422	400	600	
D0	VSwing for D0-	512.2132	mV	168.3459 ps	5.94 Gbps	Pass	112.2132 & 87.7868	400	600	
D1	TMDS VLow for D1+	2.3357	V	168.3459 ps	5.94 Gbps	Pass	0.0357 & 0.5643	2.3	2.9	
D1	TMDS VLow for D1-	2.3060	V	168.3459 ps	5.94 Gbps	Pass	0.0060 & 0.5940	2.3	2.9	
D1	VSwing for D1+	563.9695	mV	168.3459 ps	5.94 Gbps	Pass	163.9695 & 36.0305	400	600	
D1	VSwing for D1-	595.9603	mV	168.3459 ps	5.94 Gbps	Pass	195.9603 & 4.0397	400	600	
D2	TMDS VLow for D2+	2.3966	V	168.3459 ps	5.94 Gbps	Pass	0.0966 & 0.5034	2.3	2.9	
D2	TMDS VLow for D2-	2.3826	V	168.3459 ps	5.94 Gbps	Pass	0.0826 & 0.5174	2.3	2.9	
D2	VSwing for D2+	536.1971	mV	168.3459 ps	5.94 Gbps	Pass	136.1971 & 63.8029	400	600	
D2	VSwing for D2-	502.7240	mV	168.3459 ps	5.94 Gbps	Pass	102.7240 & 97.2760	400	600	

Figure 3-15. HDMI2.0_4K_60fps Test VL and VSwing (HDMI20_VOD =0h, HDMI14_VOD =0h, CLK_VOD, D0_VOD, D1_VOD and D2_VOD = 7h)

3.3.2 HDMI1.4 Test with Resolution 4096 x 2160_30p_8bit_444

3.3.2.1 VL and VSwing with HDMI20_VOD =0h, HDMI14_VOD = 0h, Use Values in CLK_VOD, D0_VOD, D1_VOD and D2_VOD = 0h, Limited -15%

Table 3-7. HDMI1.4_4K_30fps Test VL and VSwing (HDMI20_VOD =0h, HDMI14_VOD =0h, CLK_VOD, D0_VOD, D1_VOD and D2_VOD = 0h)

Index	Test Name	Lanes	Specification Range	Meas Value	Result
1	7-2: Source Low Amplitude + (Supported Sink≤ 165MHz	D1+	2.700V < VL < 2.900V	2.7465V	Pass
2	7-2: Source Low Amplitude + (Supported Sink≤ 165MHz	D2+	2.700V < VL < 2.900V	2.7939V	Pass
3	7-2: Source Low Amplitude + (Supported Sink≤ 165MHz	D1-	2.700V < VL < 2.900V	2.7366V	Pass
4	7-2: Source Low Amplitude + (Supported Sink≤ 165MHz	D2-	2.700V < VL < 2.900V	2.8848V	Pass
5	7-2: Source Low Amplitude + (Supported Sink≤ 165MHz	D1+	2.600V < VL < 2.900V	2.7465V	Pass
6	7-2: Source Low Amplitude + (Supported Sink≤ 165MHz	D2+	2.600V < VL < 2.900V	2.7939V	Pass
7	7-2: Source Low Amplitude + (Supported Sink≤ 165MHz	D1-	2.600V < VL < 2.900V	2.7366V	Pass
8	7-2: Source Low Amplitude + (Supported Sink≤ 165MHz	D2-	2.600V < VL < 2.900V	2.8848V	Pass
9	7-2: Source Low Amplitude + (Supported Sink≤ 165MHz	CK+	2.700V < VL < 2.900V	2.7801V	Pass
10	7-2: Source Low Amplitude + (Supported Sink≤ 165MHz	D0+	2.700V < VL < 2.900V	2.7966V	Pass
11	7-2: Source Low Amplitude + (Supported Sink≤ 165MHz	CK-	2.700V < VL < 2.900V	2.7634V	Pass
12	7-2: Source Low Amplitude + (Supported Sink≤ 165MHz	D0-	2.700V < VL < 2.900V	2.7665V	Pass
13	7-2: Source Low Amplitude + (Supported Sink≤ 165MHz	CK+	2.600V < VL < 2.900V	2.7803V	Pass
14	7-2: Source Low Amplitude + (Supported Sink≤ 165MHz	D0+	2.600V < VL < 2.900V	2.7966V	Pass
15	7-2: Source Low Amplitude + (Supported Sink≤ 165MHz	CK-	2.600V < VL < 2.900V	2.7699V	Pass
16	7-2: Source Low Amplitude + (Supported Sink≤ 165MHz	D0-	2.600V < VL < 2.900V	2.7633V	Pass

3.3.2.2 VL and VSwing with HDMI20_VOD =1h (Default 1000mV), HDMI14_VOD =1h (Default 1000mV)

Table 3-8. HDMI1.4_4K_30fps Test VL and VSwing (HDMI20_VOD =1h, HDMI14_VOD =1h)

Index	Test Name	Lanes	Specification Range	Meas Value	Result
18	7-2: Source Low Amplitude + (Supported Sink ≤165MHz	D1+	2.700V < VL < 2900V	2.7395V	Pass
19	7-2: Source Low Amplitude + (Supported Sink ≤165MHz	D2+	2.700V < VL < 2900V	2.7613V	Pass
20	7-2: Source Low Amplitude + (Supported Sink ≤165MHz	D1-	2.700V < VL < 2900V	2.7055V	Pass
21	7-2: Source Low Amplitude + (Supported Sink ≤165MHz	D2-	2.700V < VL < 2900V	2.7587V	Pass
22	7-2: Source Low Amplitude + (Supported Sink > 165MHz	D1+	2.600V < VL < 2900V	2.7395V	Pass
23	7-2: Source Low Amplitude + (Supported Sink > 165MHz	D2+	2.600V < VL < 2900V	2.7649V	Pass
24	7-2: Source Low Amplitude + (Supported Sink > 165MHz	D1-	2.600V < VL < 2900V	2.7055V	Pass

Table 3-8. HDMI1.4_4K_30fps Test VL and VSwing (HDMI20_VOD =1h, HDMI14_VOD =1h) (continued)

Index	Test Name	Lanes	Specification Range	Meas Value	Result
25	7-2: Source Low Amplitude + (Supported Sink > 165MHz	D2-	2.600V < VL < 2900V	2.7587V	Pass
26	7-2: Source Low Amplitude + (Supported Sink ≤165MHz	CK+	2.600V < VL < 2900V	2.7237V	Pass
27	7-2: Source Low Amplitude + (Supported Sink ≤165MHz	D0+	2.700V < VL < 2900V	2.7372V	Pass
28	7-2: Source Low Amplitude + (Supported Sink ≤165MHz	CK-	2.700V < VL < 2900V	2.7075V	Pass
29	7-2: Source Low Amplitude + (Supported Sink ≤165MHz	D0-	2.700V < VL < 2900V	2.7155V	Pass
30	7-2: Source Low Amplitude + (Supported Sink > 165MHz	CK+	2.600V < VL < 2900V	2.7240V	Pass
31	7-2: Source Low Amplitude + (Supported Sink > 165MHz	D0+	2.600V < VL < 2900V	2.7372V	Pass
32	7-2: Source Low Amplitude + (Supported Sink > 165MHz	CK-	2.600V < VL < 2900V	2.7075V	Pass
33	7-2: Source Low Amplitude + (Supported Sink > 165MHz	D0-	2.600V < VL < 2900V	2.7155V	Pass

3.3.2.3 VL and VSwing with HDMI20_VOD =0h, HDMI14_VOD =0h, Use values in CLK_VOD, D0_VOD, D1_VOD and D2_VOD = 7h, Limited +20%)

Table 3-9. HDMI1.4_4K_30fps Test VL and VSwing (HDMI20_VOD =0h, HDMI14_VOD = 0h, CLK_VOD, D0_VOD, D1_VOD and D2_VOD = 7h)

Index	Test Name	Lanes	Specification Range	Meas Value	Result
1	7-2: Source Low Amplitude + (Supported Sink ≤ 165MHz	D1+	2.700V < VL < 2.900V	2.6334V	Fail
2	7-2: Source Low Amplitude + (Supported Sink ≤ 165MHz	D2+	2.700V < VL < 2.900V	2.6755V	Fail
3	7-2: Source Low Amplitude + (Supported Sink ≤ 165MHz	D1-	2.700V < VL < 2.900V	2.6125V	Fail
4	7-2: Source Low Amplitude + (Supported Sink ≤ 165MHz	D2-	2.700V < VL < 2.900V	2.6654V	Fail
5	7-2: Source Low Amplitude + (Supported Sink > 165MHz	D1+	2.600V < VL < 2.900V	2.6334V	Pass
6	7-2: Source Low Amplitude + (Supported Sink > 165MHz	D2+	2.600V < VL < 2.900V	2.6755V	Pass
7	7-2: Source Low Amplitude + (Supported Sink > 165MHz	D1-	2.600V < VL < 2.900V	2.6125V	Pass
8	7-2: Source Low Amplitude + (Supported Sink > 165MHz	D2-	2.600V < VL < 2.900V	2.6654V	Pass
9	7-2: Source Low Amplitude + (Supported Sink ≤ 165MHz	CK+	2.700V < VL < 2.900V	2.6500V	Fail
10	7-2: Source Low Amplitude + (Supported Sink ≤ 165MHz	D0+	2.700V < VL < 2.900V	2.6750V	Fail
11	7-2: Source Low Amplitude + (Supported Sink ≤ 165MHz	CK-	2.700V < VL < 2.900V	2.6328V	Fail

Table 3-9. HDMI1.4_4K_30fps Test VL and VSwing (HDMI20_VOD =0h, HDMI14_VOD = 0h, CLK_VOD, D0_VOD, D1_VOD and D2_VOD = 7h) (continued)

Index	Test Name	Lanes	Specification Range	Meas Value	Result
12	7-2: Source Low Amplitude + (Supported Sink ≤ 165MHz	D0-	2.700V < VL < 2.900V	2.6392V	Fail
13	7-2: Source Low Amplitude + (Supported Sink > 165MHz	CK+	2.600V < VL < 2.900V	2.6483V	Pass
14	7-2: Source Low Amplitude + (Supported Sink > 165MHz	D0+	2.600V < VL < 2.900V	2.6750V	Pass
15	7-2: Source Low Amplitude + (Supported Sink > 165MHz	CK-	2.600V < VL < 2.900V	2.6328V	Pass
16	7-2: Source Low Amplitude + (Supported Sink > 165MHz	D0-	2.600V < VL < 2.900V	2.6392V	Pass

3.3.3 HDMI1.4 Test with Resolution 720 x 480_60p_8bit_444

3.3.3.1 VL and VSwing with HDMI20_VOD =0h, HDMI14_VOD =0h,Use values in CLK_VOD, D0_VOD, D1_VOD and D2_VOD = 0h, Limited -15%)

Table 3-10. HDMI1.4_480p_60fps Test VL and VSwing (HDMI20_VOD =0h, HDMI14_VOD = 0h, CLK_VOD, D0_VOD, D1_VOD and D2_VOD = 0h

Index	Test Name	Lanes	Specifications Range	Meas Value	Result
1	7-2: Source Low Amplitude + (Supported Sink ≤ 165MHz)	D1+	2.700V < VL < 2.900V;	2.8169V	Pass
2	7-2: Source Low Amplitude + (Supported Sink ≤ 165MHz)	D2+	2.700V < VL < 2.900V;	2.8570V	Pass
3	7-2: Source Low Amplitude + (Supported Sink ≤ 165MHz)	D1-	2.700V < VL < 2.900V;	2.8077V	Pass
4	7-2: Source Low Amplitude + (Supported Sink ≤ 165MHz)	D2-	2.700V < VL < 2.900V;	2.8340V	Pass
5	7-2: Source Low Amplitude + (Supported Sink ≤ 165MHz)	CK+	2.700V < VL < 2.900V;	2.8318V	Pass
6	7-2: Source Low Amplitude + (Supported Sink ≤ 165MHz)	D0+	2.700V < VL < 2.900V;	2.8431V	Pass
7	7-2: Source Low Amplitude + (Supported Sink ≤ 165MHz)	CK-	2.700V < VL < 2.900V;	2.8260V	Pass
8	7-2: Source Low Amplitude + (Supported Sink ≤ 165MHz)	D0-	2.700V < VL < 2.900V;	2.8279	Pass

3.3.3.2 VL and VSwing with HDMI20_VOD =1h (default 1000mV), HDMI14_VOD =1h (default 1000mV)

Table 3-11. HDMI1.4_480p_60fps Test VL and VSwing (HDMI20_VOD =1h, HDMI14_VOD =1h)

Index	Test Name	Lanes	Specification Range	Meas Value	Result
18	7-2: Source Low Amplitude + (Supported Sink ≤165MHz	CK+	2.700V < VL < 2.900V	2.7825V	Pass
19	7-2: Source Low Amplitude + (Supported Sink ≤165MHz	D0+	2.700V < VL < 2.900V	2.7928V	Pass
20	7-2: Source Low Amplitude + (Supported Sink ≤165MHz	CK-	2.700V < VL < 2.900V	2.7701V	Pass

Table 3-11. HDMI1.4_480p_60fps Test VL and VSwing (HDMI20_VOD =1h, HDMI14_VOD =1h) (continued)

Index	Test Name	Lanes	Specification Range	Meas Value	Result
21	7-2: Source Low Amplitude + (Supported Sink ≤165MHz	D0-	2.700V < VL < 2.900V	2.7768V	Pass
22	7-2: Source Low Amplitude + (Supported Sink ≤165MHz	D1+	2.700V < VL < 2.900V	2.7574V	Pass
23	7-2: Source Low Amplitude + (Supported Sink ≤165MHz	D2+	2.700V < VL < 2.900V	2.8016V	Pass
24	7-2: Source Low Amplitude + (Supported Sink ≤165MHz	D1-	2.700V < VL < 2.900V	2.7452V	Pass
25	7-2: Source Low Amplitude + (Supported Sink ≤165MHz	D2-	2.700V < VL < 2.900V	2.7793V	Pass

3.3.3.3 VL and VSwing with HDMI20_VOD =0h, HDMI14_VOD =0h, use values in CLK_VOD, D0_VOD, D1_VOD and D2_VOD = 7h, Limited +20%)

Table 3-12. HDMI1.4_480p_60fps Test VL and VSwing (HDMI20_VOD =0h, HDMI14_VOD =0h, CLK_VOD, D0_VOD, D1_VOD and D2_VOD = 7h)

Index	Test Name	Lanes	Spec Range	Meas Value	Result
1	7-2: Source Low Amplitude + (Supported Sink ≤ 165MHz	D1+	2.700V < VL < 2.900V	2.6945V	Fail
2	7-2: Source Low Amplitude + (Supported Sink ≤ 165MHz	D2+	2.700V < VL < 2.900V	2.7438V	Pass
3	7-2: Source Low Amplitude + (Supported Sink ≤ 165MHz	D1-	2.700V < VL < 2.900V	2.6834V	Fail
4	7-2: Source Low Amplitude + (Supported Sink ≤ 165MHz	D2-	2.700V < VL < 2.900V	2.7200	Pass
5	7-2: Source Low Amplitude + (Supported Sink ≤ 165MHz	CK+	2.700V < VL < 2.900V	2.7054V	Pass
6	7-2: Source Low Amplitude + (Supported Sink ≤ 165MHz	D0+	2.700V < VL < 2.900V	2.7282V	Pass
7	7-2: Source Low Amplitude + (Supported Sink ≤ 165MHz	CK-	2.700V < VL < 2.900V	2.7028V	Pass
8	7-2: Source Low Amplitude + (Supported Sink ≤ 165MHz	D0-	2.700V < VL < 2.900V	2.7074V	Pass

Note: VL spec in different resolution was different in HDMI 1.4.

Single-ended low level output voltage, VL

If attached Sink support only <=165MHz : (AVcc-600mV)≤ VL ≤ (AVcc-400mV)

If attached Sink support only >165MHz : (AVcc-700mV) ≤ VL ≤ (AVcc-400mV)

3.4 HDMI1.4-2.0 Pass Compliance Test Pass Result

3.4.1 HDMI2.0 Test with Resolution 4096x2160_60p_8bit_444

Tektronix

TekExpress HDM

Source Test Report

Setup Information			
DUT ID	DUT001	Scope Model	DPO73304SX
Date/Time	2025-03-21 17:14:26	Scope Serial Number	B010266
Device Type	HDM Physical Layer Solution	SPC, FactoryCalibration	PASS;PASS
App Version	10.3.5.6	Scope F/W Version	10.14.1 Build 15
TekExpress Version	4.16.0.20	DPOJET Version	10.5.0.9
Spec Version	CTS 2.0	Ch1 Deskew Time (s)	0.000000
Overall Compliance Mode	Yes	Ch2 Deskew Time (s)	0.000000
Execution Mode	Live	Ch3 Deskew Time (s)	0.000000
Overall Execution Time	0:47:10	Ch4 Deskew Time (s)	0.000000
Overall Test Result	Pass	Probe1 Model	P7313SMA
		Probe1 Serial Number	B022547
		Probe2 Model	P7313SMA
		Probe2 Serial Number	B010379
		Probe3 Model	P7313SMA
		Probe3 Serial Number	B022271
		Probe4 Model	P7313SMA
		Probe4 Serial Number	B022549
DUT COMMENT:	General Comment – HDM2.0 Source		

Test Name Summary Table		
Test Name	Result	Execution Time
HF1-2- TRISE, TFALL	Pass	0:09:19
HF1-5- Differential Voltage	Pass	0:06:20
HF1-6- Clock Duty Cycle and Clock Rate	Pass	0:02:01
HF1-3- Inter-Pair Skew	Pass	0:31:18
HF1-7- Clock Jitter	Pass	0:01:02
HF1-1- VL and VSwing	Pass	0:18:20
HF1-4- Intra-Pair Skew	Pass	0:12:57
HF1-8- Data Eye Diagram	Pass	0:15:46

Figure 3-16. HDMI2.0_4K_60fps Overall Pass Result

3.4.2 HDMI1.4 Test With Resolution 4096 × 2160_30p_8bit_444

Fri Mar 28 08:52:14 GMT 2025

Source Tests Report

Configuration

Setup Configuration

Oscilloscope Info	DPO73304S - 10.14.1 Build 15
TDSHT3 Version	5.4.0 Build 8

Device Configuration

Device Details	HDMI Device
Clock Frequency(Mhz)	297.077
Resolution	4096x2160
Refresh Rate	30Hz

Compliance Summary

Total Tests Supported	9
Tests Completed	37
Pass	37
Fail	0

Figure 3-17. HDMI1.4_4K_30fps Overall Pass Result

3.4.3 HDMI1.4 Test with Resolution 720 x 480_60p_8bit_444

Wed Apr 02 07:23:26 GMT 2025

Source Tests Report

Configuration

Setup Configuration

Oscilloscope Info	DPO73304S - 10.14.1 Build 15
TDSHT3 Version	5.4.0 Build 8

Device Configuration

Device Details	HDMI Device
Clock Frequency(Mhz)	27.0288
Resolution	720x480p
Refresh Rate	60Hz

Compliance Summary

Total Tests Supported	9
Tests Completed	29
Pass	29
Fail	0

Figure 3-18. HDMI1.4_480p_60fps Overall Pass Result

4 Tips

TDP0604 reads the last value snooped through DDC read/write or I2C write. Use I2C host to read the TMDS_CLK_RATIO [1] bit in SCDC_TMDS_CONFIG Register (Offset = 20h) to find the correct TMDS clock period ratio.

Table 4-1. TMDS_CLK_Ratio Bit

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	Reserved
1	TMDS_CLK_RATIO	RH/W	0h	TMDS Bit Period to TMDS Clock Period Ratio. Reads last value snooped through DC read/write or I2C write
0	RESERVED	R	0h	Reserved

When reading is HDMI2.0 clock ratio:

Figure 4-1. TMDS_CLK_RATIO = 1

When reading back is HDMI1.4 clock ratio:

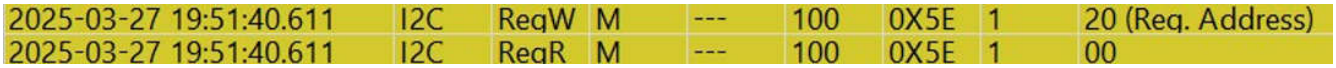

Figure 4-2. TMDS_CLK_RATIO = 0

5 Summary

The TDP0604 is a hybrid redriver supporting both source and sink applications. A hybrid redriver can operate either in a linear or limited redriver function. The device also has rich and flexible adjust capabilities that can be fine-tuned for each high speed LANE and different data rate (HDMI1.4 or 2.0), including EQ and rising and falling slew rate and VL and VSwing, and so on.

This article uses actual adjustments to show what results and impacts are produced by different parameter adjustments during testing, to helps readers understand what parameters can or must be adjusted when encountering test failures to pass the certification test.

6 References

1. Texas Instruments, *TDP0604 6-Gbps DC or AC-Coupled to HDMI 2.0 Level Shifter Hybrid Redriver*, data sheet.

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