Application Note

Pairing Isolated Amplifiers With SAR AD Converters

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ABSTRACT

Isolated amplifiers, such as the AMC0311 or AMC0330, are frequently paired with successive approximation register (SAR) analog-to-digital converters (ADCs). Many high-voltage systems use a multiplexed ADC to quickly scan through multiple channels and pass this information to the controller. This imposes stringent timing requirements and reduces the time allowed for each channel conversion. This application note provides examples of how operational amplifier selection affects the DC and AC characteristics of the signal chain and what happens when timing requirements are violated.

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1 Introduction

Isolated amplifiers are essential building blocks in systems that require galvanic isolation for electrical isolation of two parts of a circuit. Good examples of systems that require galvanic isolation are high-voltage DC/DC converters, motor drives, hybrid electric vehicle (HEV) and electric vehicles (EV) traction inverters. Most commonly, isolated amplifiers sense current or voltage and transfer this information to the controller across the galvanic isolation barrier. Isolated amplifiers are similar to delta-sigma modulators in function; however, the output of the isolated amplifier is analog, whereas the output of the modulator is a digital signal. Many systems and engineers benefit from the analog output, as the system implementation and testing are generally better understood and do not require assistance from a microcontroller (MCU).

Typically, the output of the isolated amplifier interfaces with a SAR ADC.

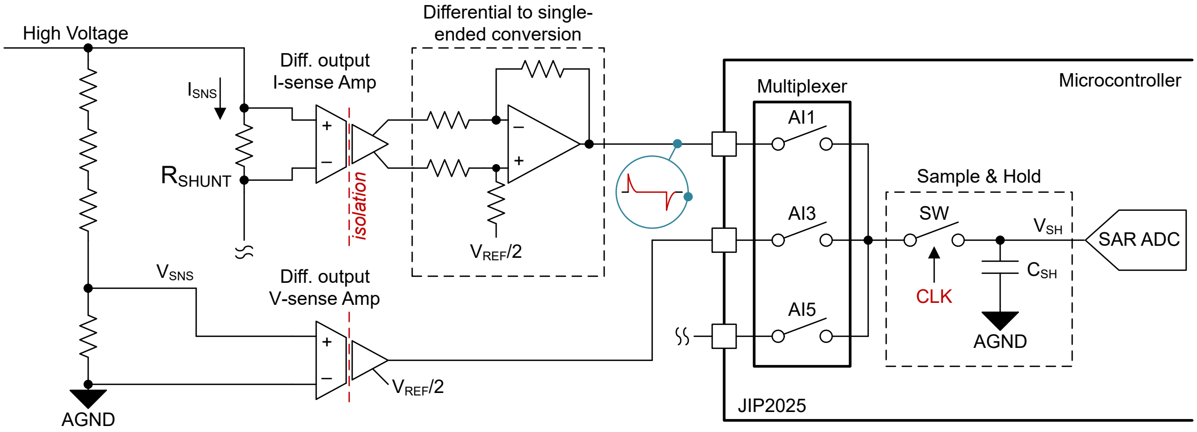

Figure 1-1. Isolated Amplifiers Interfacing With a SAR ADC

The SAR ADC is the most common type present in MCUs. The resolution ranges from 10-b for low-cost to 16-b for high-end microcontrollers. A critical aspect of this implementation is that the SAR ADC's sample-and-hold (S/H) circuit momentarily disrupts the analog signal chain during data acquisition. MCUs have multiple analog inputs but only one, two, or three ADC blocks. For this reason, analog inputs share the ADC through the analog multiplexer. The multiplexed system makes things more difficult because the C_{SH} capacitor is typically not reset and therefore remembers the state of the previous channel. Figure 1-1 shows a simplified diagram as an example.

Analog amplifiers have two possible output types.

Differential output (Figure 1-2) is a preferred choice for systems where the physical distance between the isolated amplifier and the ADC is long or passes through connectors. The information carried to the controller is the voltage difference between two complementary outputs, not the absolute value with regard to the common ground. For this reason, this output effectively suppresses common-mode noise that can intrude the circuit between the ADC and the isolated amplifier. The drawback is that many ADCs cannot work directly with the differential signaling. In this case there is a differential-to-single-ended conversion in close proximity to the ADC. The difference amplifier converts the signal for the ADC but introduces additional measurement errors and increases the system complexity.

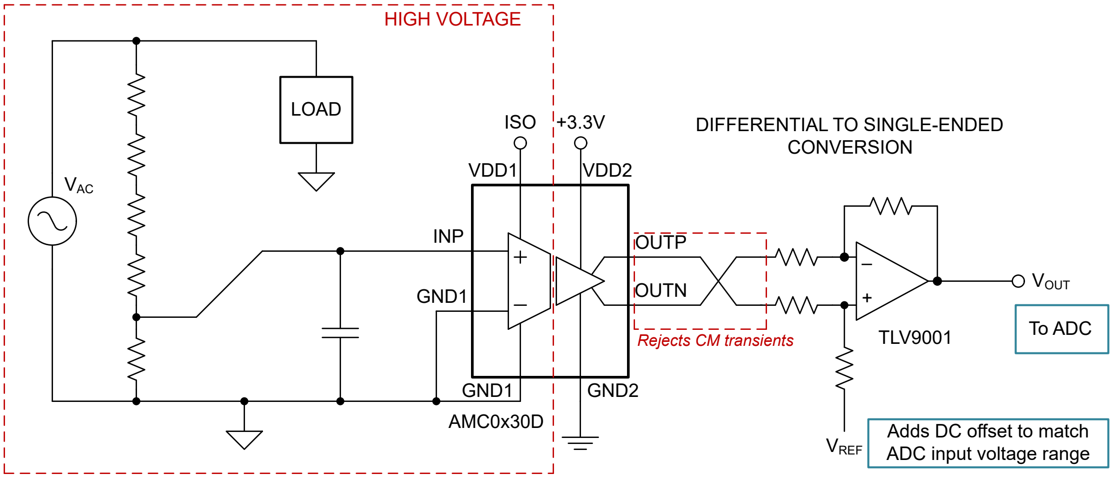

Figure 1-2. Differential Output Isolation Amplifier

Single-ended output (Figure 1-3) interfaces directly with the ADC and does not require a difference amplifier. Typically, this device has a reference voltage input (REFIN) to add an offset to the output (OUT) or set the gain. This is easier to implement but this configuration cannot reject the common-mode noise. For this reason, this type of output is a preferred design for situations where the distance between the ADC and the isolated amplifier is relatively short (<10cm), or performance degradation due to the common mode noise is acceptable.

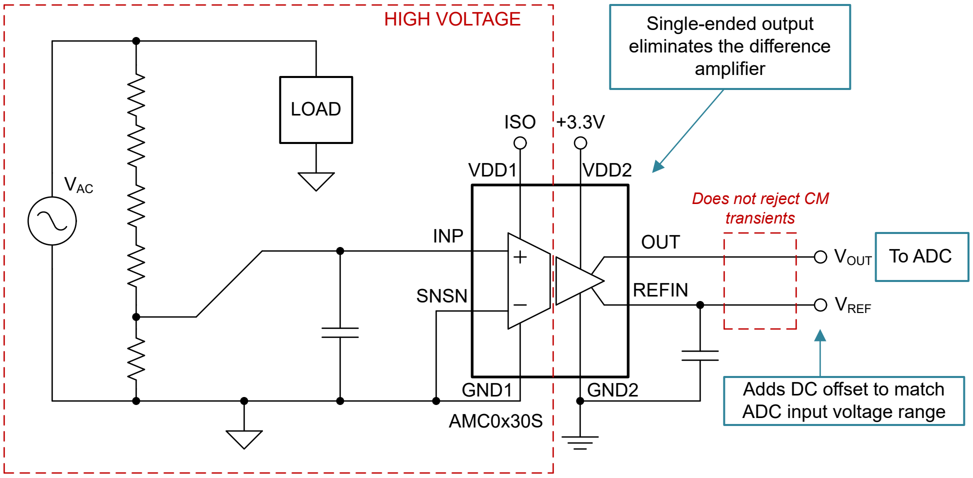

Figure 1-3. Single-Ended Output Isolation Amplifier

For both types, the engineer must understand very well how the sampling process works to avoid AC and DC signal chain performance loss.

2 Signal Chain

2.1 Inside the Multiplexed SAR ADC

Figure 2-1 shows a simplified diagram of the SAR ADC converter with the input multiplexer. In this example, the sampling order starts with the channel AI1, continues through AI3, and ends with AI5. Then, the process repeats.

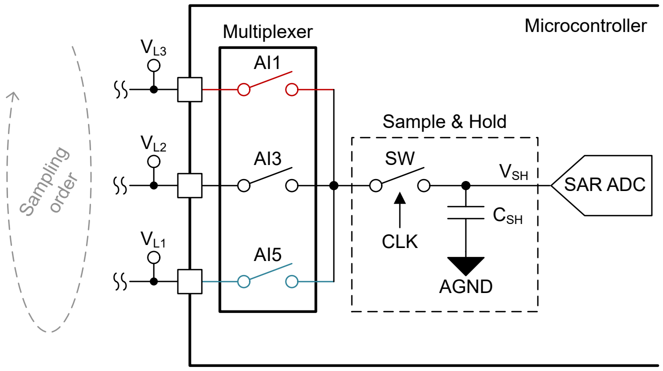

Figure 2-1. Example of SAR ADC Functional Block Diagram

For each channel, the multiplexer first closes the respective switch AIx, then the ADC closes the switch SW for duration called the sample or acquisition time t_{SMPL}. After the sample time the switch SW opens again and the AD conversion starts. After the end of conversion, the ADC proceeds to the next channel as Figure 2-2 shows.

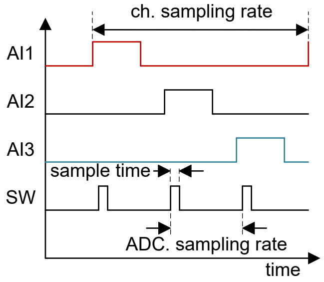

Figure 2-2. Timing Diagram of Repetitive Sampling With Multiplexed ADC

2.2 Driving ADC With an Amplifier

Figure 2-3 shows the scenario when an operational amplifier, or output of a single-ended isolation amplifier, drives the analog input of the ADC. The analog amplifier exhibits a transient on the output as the sample and hold switch SW connects the sample and hold capacitor C_{SH} to the output.

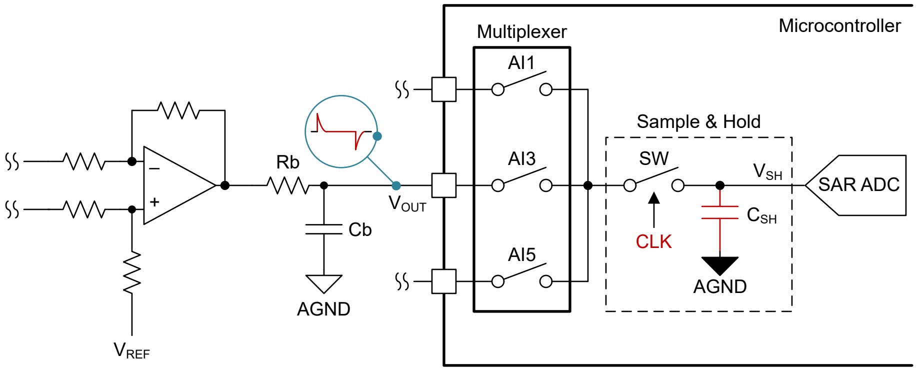

Figure 2-3. Operational Amplifier Driving the Multiplexed ADC Input

During the sample and hold process, the amplifier must swiftly recharge the sample and hold capacitor C_{SH} to the desired level V_{OUT}. However, this process is not fully deterministic. Most (but not all) ADCs do not reset the sample and hold capacitor between each conversion. This means that the capacitor holds residual voltage (charge) V_{SH} as a result of the previous channel conversion. For this reason, there are three scenarios that can occur:

1. $V_{SH} > V_{OUT}$ results in overshoot as the external amplifier has to discharge C_{SH} to lower voltage
2. $V_{SH} = V_{OUT}$ does not cause any transient as voltage are same
3. $V_{SH} < V_{OUT}$ results in undershoot as the external amplifier has to charge C_{SH} to higher voltage

Adding a charge-bucket filter (Rb, Cb) partly helps controlling the output transient. However, the filter cannot improve settling speed of the amplifier. This only allows tuning the compromise between the settling time and the overshoot/undershoot magnitude.

3 Experimental Results

Figure 3-1 shows the experimental board used for obtaining the test data. The experimental board has three isolated amplifiers with different output type (single-ended fixed gain, single-ended ratiometric output and differential output). Additionally, the board contains a modulator device that is not a subject of this application note.

Figure 3-2 and Figure 3-3 show the performance of two different operational amplifiers in the identical setup using the TMS320F28P650 microcontroller with 16-bit 1-MSPS multiplexed ADC. The sample and hold time is t_{SMPL}=425ns.

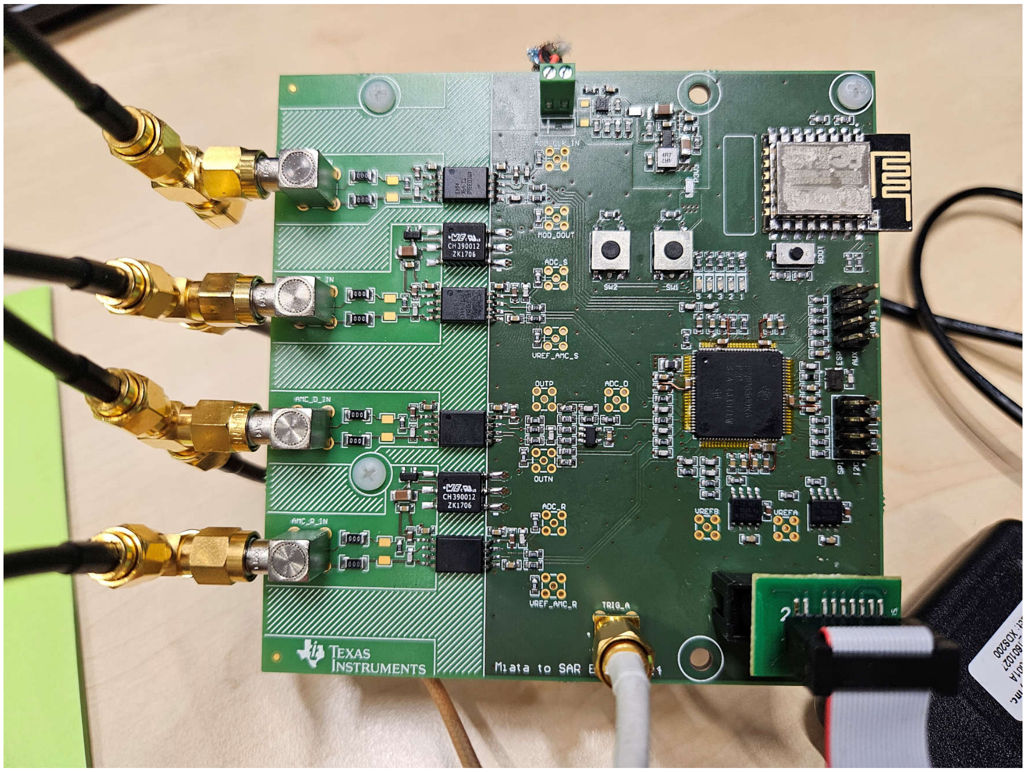

Figure 3-1. Experimental Test Setup

Waveforms in Figure 3-2 represent the OPA365. A high-performance, high-bandwidth (50MHz), rail-to-rail operational amplifier. This is visible during the three scenarios described previously, the operational amplifier output settles in less than 150ns. Waveforms in Figure 3-3 represent TLV9001, a low-cost, 1MHz bandwidth rail-to-rail operational amplifier. This is visible that the operational amplifier output requires more than 800ns to settle for the same three test conditions. As a consequence, the sample and hold switch opens before the input of the ADC has settled. This is visible especially for the undershoot scenario when $V_{SH}<V_{OUT}$. In this case the voltage used for AD conversion is 30mV higher than this needs to be. This is resulting in 1% reading error for a 3V voltage reference used in the system.

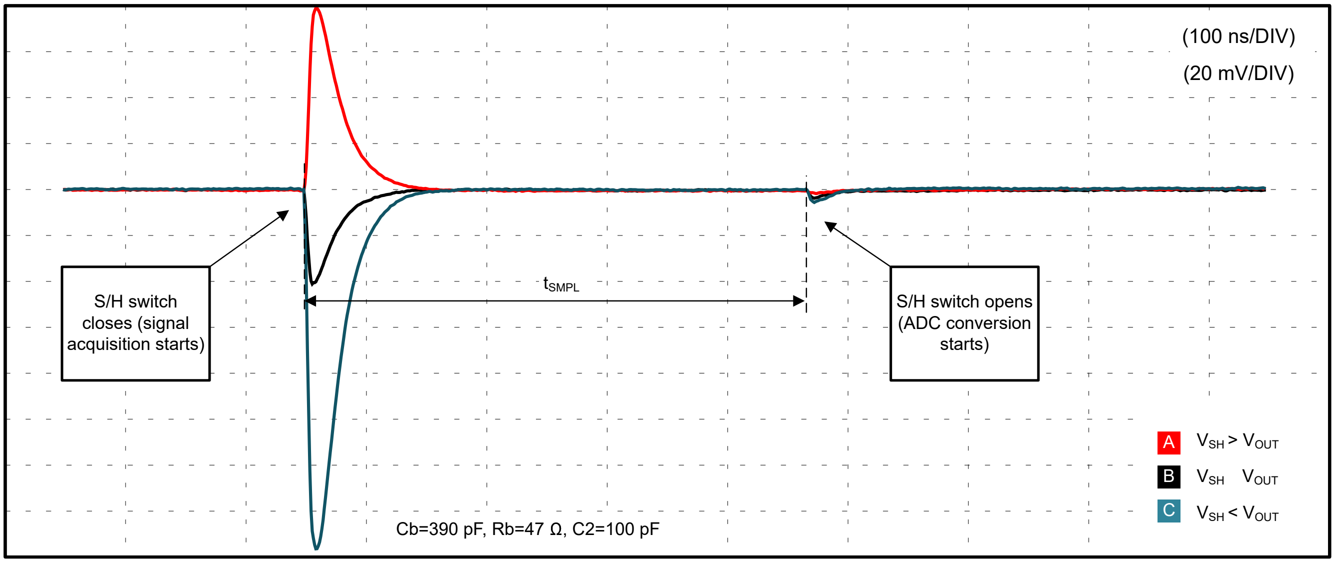

Figure 3-2. Output Settling With OPA365

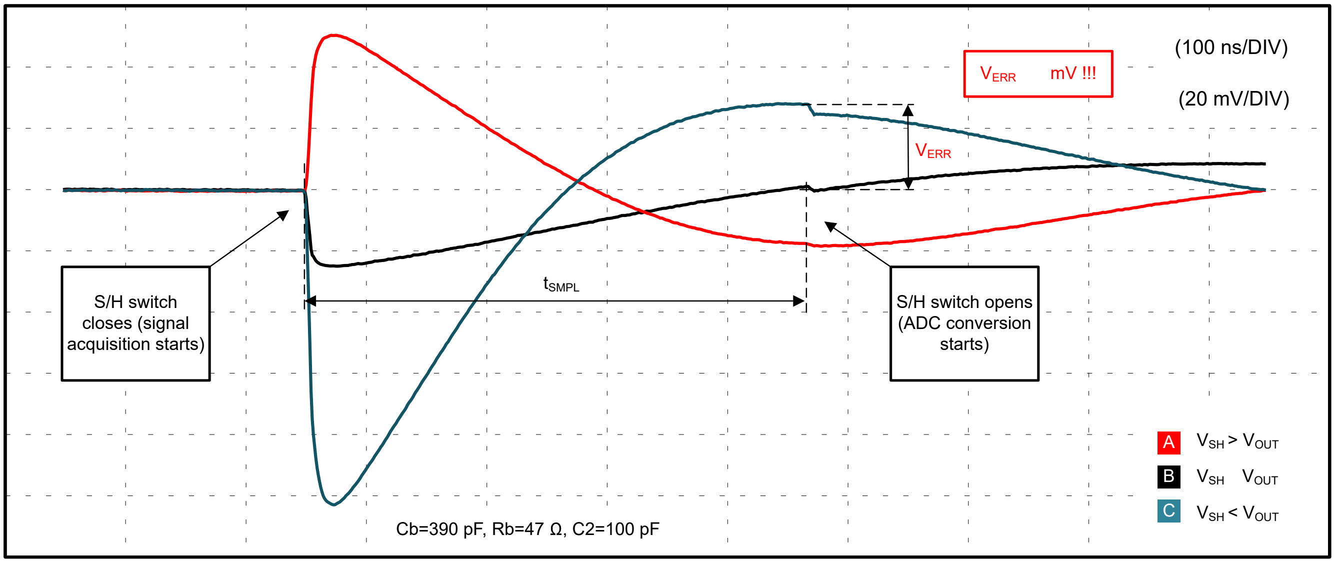

Figure 3-3. Output Settling With TLV9001

3.1 DC Characteristics

The error voltage V_{ERR} is not constant and varies with different operating conditions. Main contributor is the difference between the previous sampled voltage (V_{SH}) and the driving voltage V_{OUT}. Additionally, the input voltage, as well as temperature variations, component tolerances, and operation close to the voltage rails affect the error, making this difficult to calibrate.

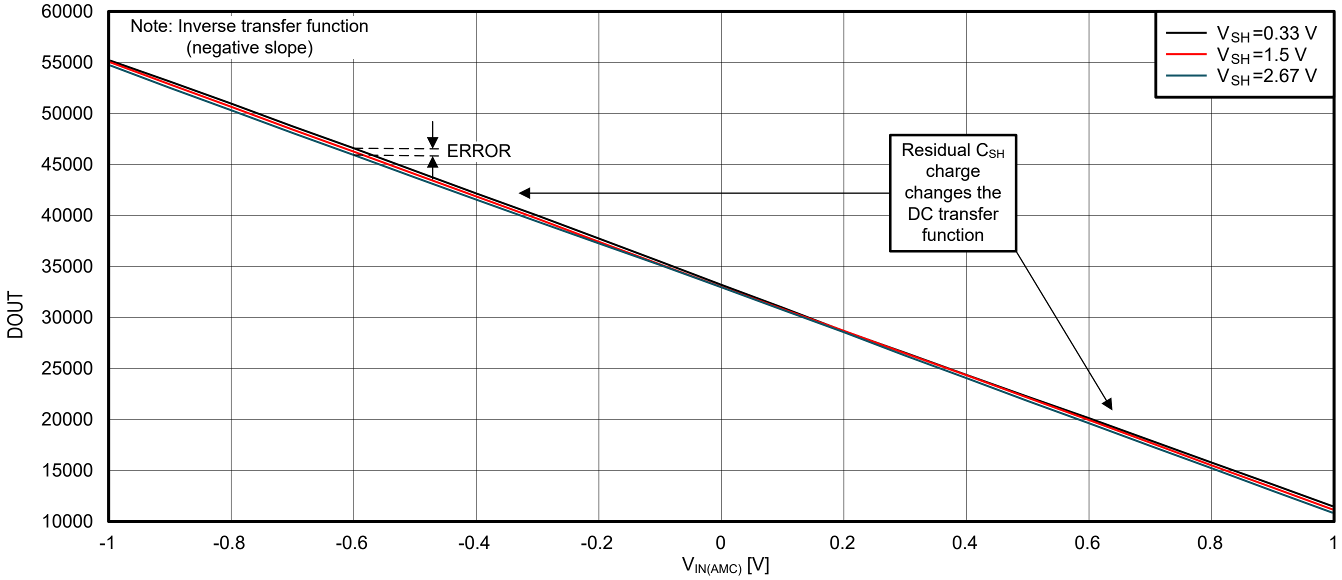

Figure 3-4. Transfer Function of the Signal Chain With AMC0330D and TLV9001, t_{SMPL}=425ns

Figure 3-4 shows the transfer function of the complete signal chain with AMC0330D and TLV9001-based difference amplifier. The X-axis represents the input voltage ($V_{IN(AMC)}$) entering the isolation amplifier. The Y-axis represents the digital output (DOUT) of the ADC. Three different conditions of V_{SH} are the values of the previously sampled channel. Graphically, the error is not significant and difficult to read from the plot. Figure 3-5 is a better plot that shows the negative effect of the V_{ERR}. The plot shows the system integral non-linearity (INL) over the analog input voltage range. Also, this is the error between the transfer function's best fit line and the real conversion reading. The plot reveals that the overall full-scale error varies up to 1.06% with regard to the residual voltage V_{SH}.

Figure 3-6 shows the very same analysis for the faster OPA365-based difference amplifier. The test uses the same hardware with only the OPA365 replacing the TLV9001 operational amplifier. In this case, the total full-scale error variation is less than 0.26% which is 4 times improvement over the circuit with the TLV9001.

For completeness, Figure 3-7 represents signal chain that uses the single-ended variant of the isolated amplifier (AMC0330S). The marginal improvement over AMC0330D with the OPA365-based difference amplifier comes from the full integration of the amplifier on-chip. The high integration removes other error contributors coming from the discrete implementation of the difference amplifier.

As can be seen, the settling time of the amplifier that drives the ADC input affects the DC transfer function and linearity of the signal chain. In cases where the settling time of the amplifier is longer than the sampling time of the ADC, significant error is introduced to the measurement.

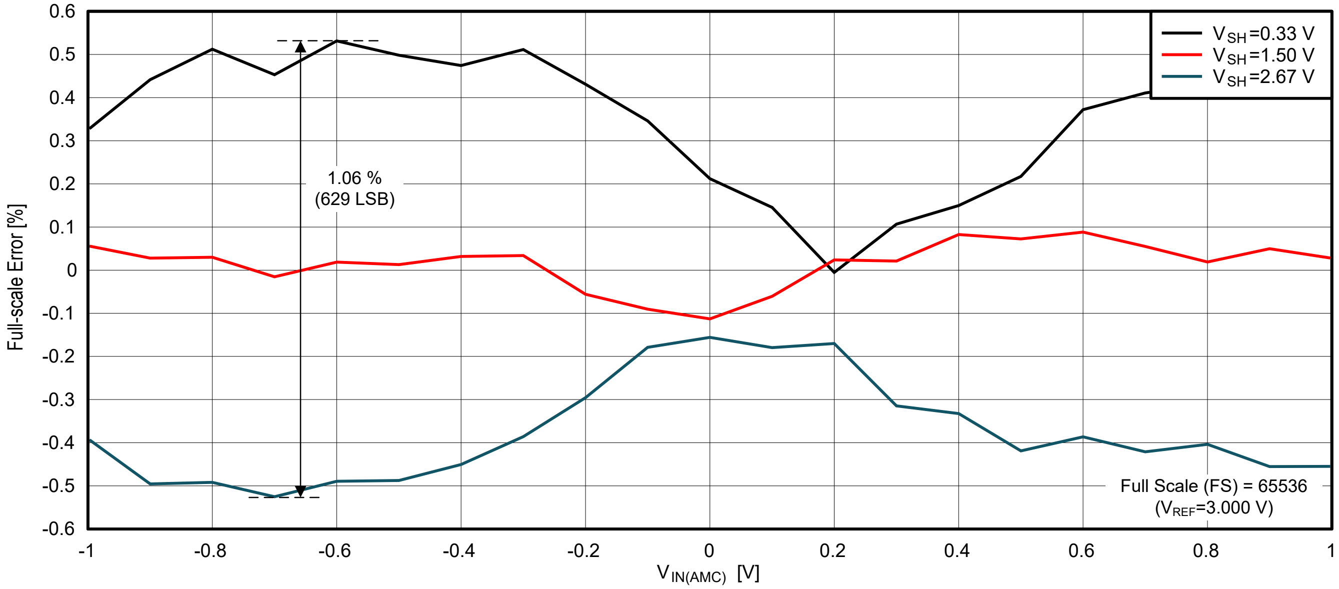

Figure 3-5. Integral Non-Linearity of the Signal Chain With AMC0330D and TLV9001, t_{SMPL}=425ns

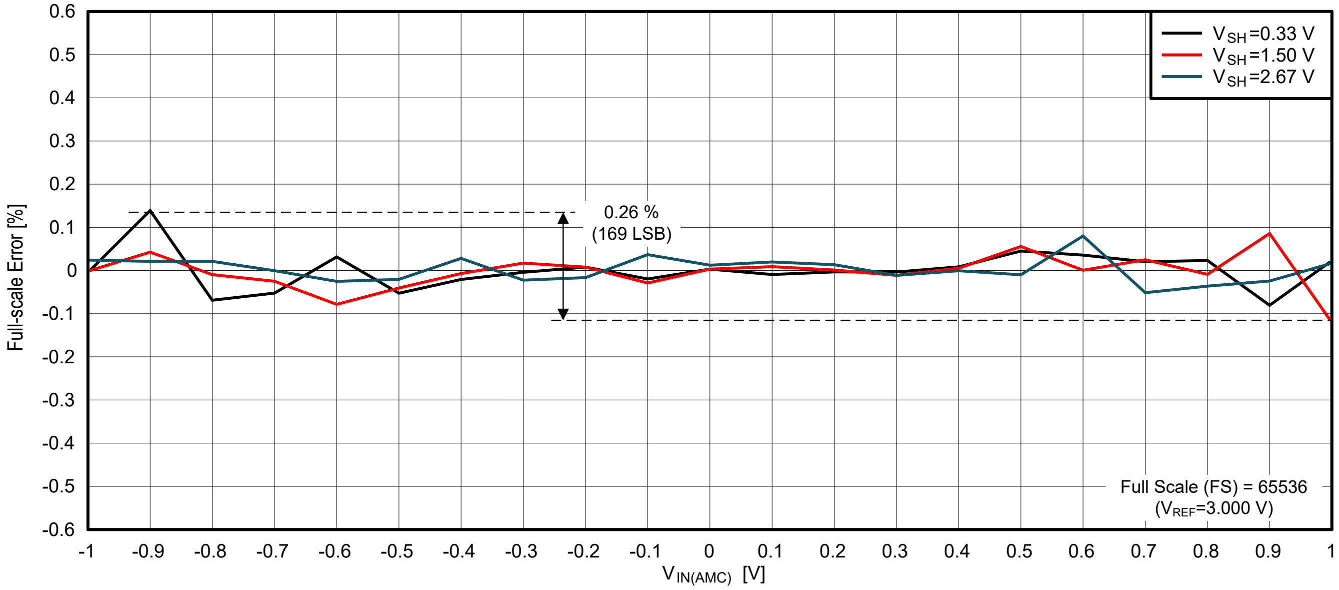

Figure 3-6. Integral Non-Linearity of the Signal Chain With AMC0330D and OPA365, t_{SMPL}=425ns

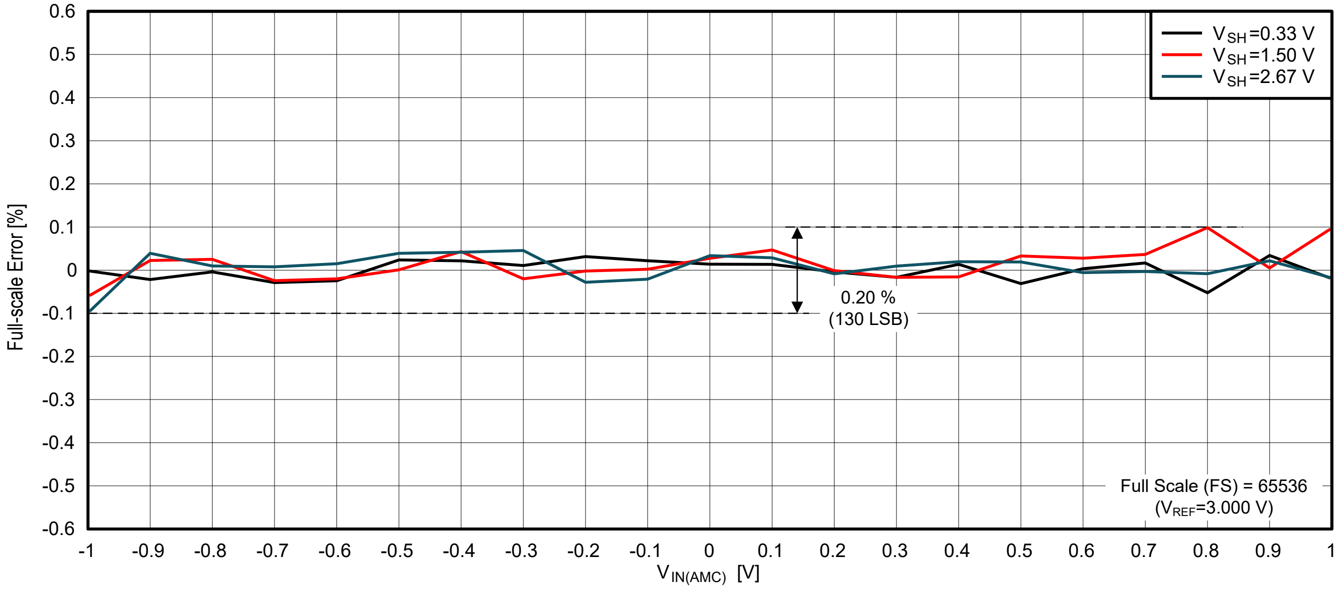

Figure 3-7. Integral Non-Linearity of the Signal Chain With Single-Ended Output AMC0330S Amplifier, t_{SMPL}=425ns

3.2 AC Characteristics

The non-linearity in the DC transfer function transforms into harmonic distortion in the AC characteristics.

Figure 3-5, Figure 3-6, and Figure 3-7 show fast Fourier transform (FFT) of 8192 data samples. The effective sampling frequency is 312.5kHz, with a 16-bit resolution, and the sampling time remains unchanged from the DC discussion (t_{SMPL}=425ns). The input signal (carrier) is a 10kHz sinewave with amplitude of 1V. The FFT uses Hanning window to suppress spectral leakage.

The negative effect we observe in the DC characteristic is visible in the AC domain as well. The TLV9001-based difference amplifier introduces unwanted harmonics as multiples of the carrier frequency. At least ten harmonics are visible before disappearing into the noise level. The systems with OPA365 or AMC0330S perform significantly better.

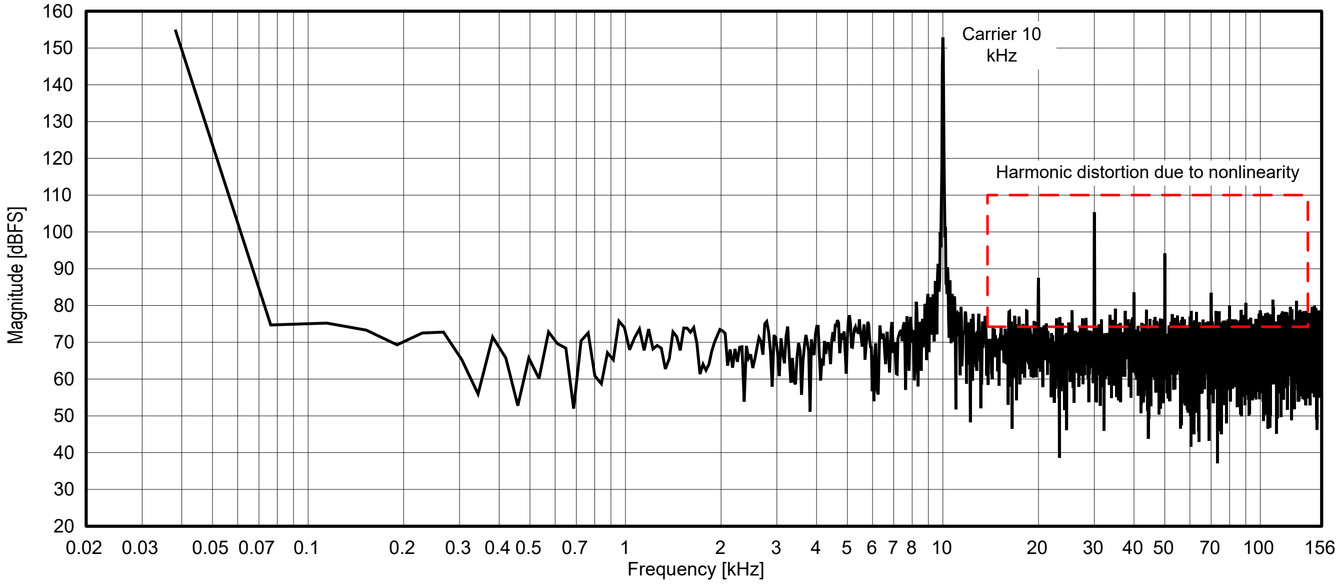

Figure 3-8. Output Spectrum of the Signal Chain With AMC0330D and TLV9001

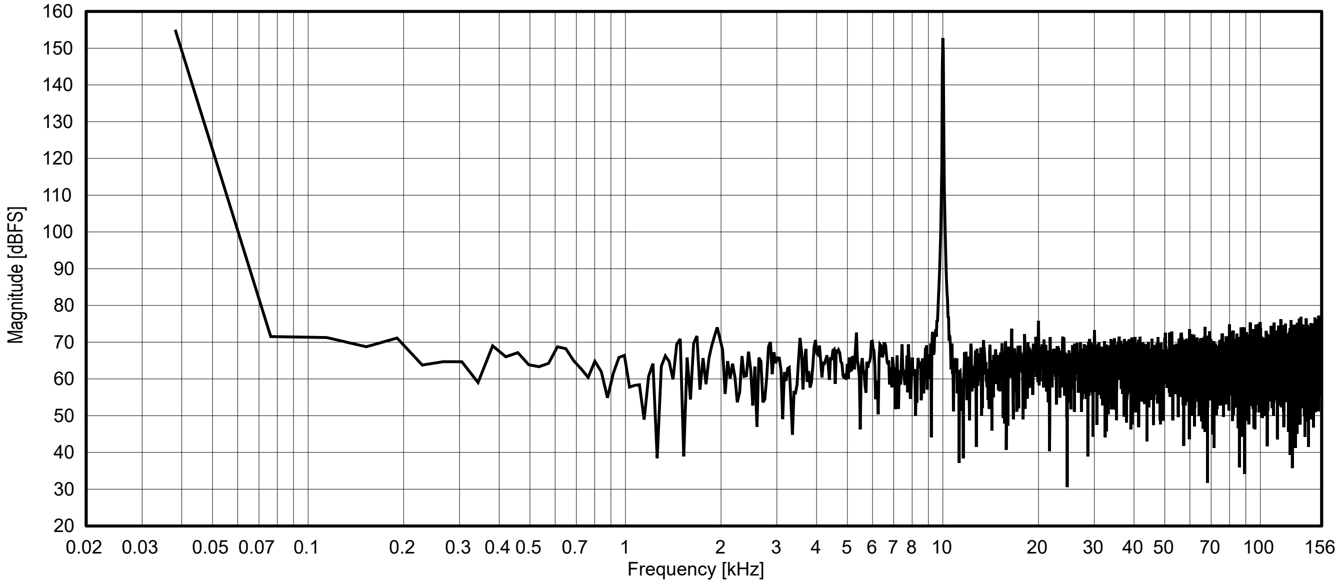

Figure 3-9. Output Spectrum of the Signal Chain With AMC0330D and OPA365

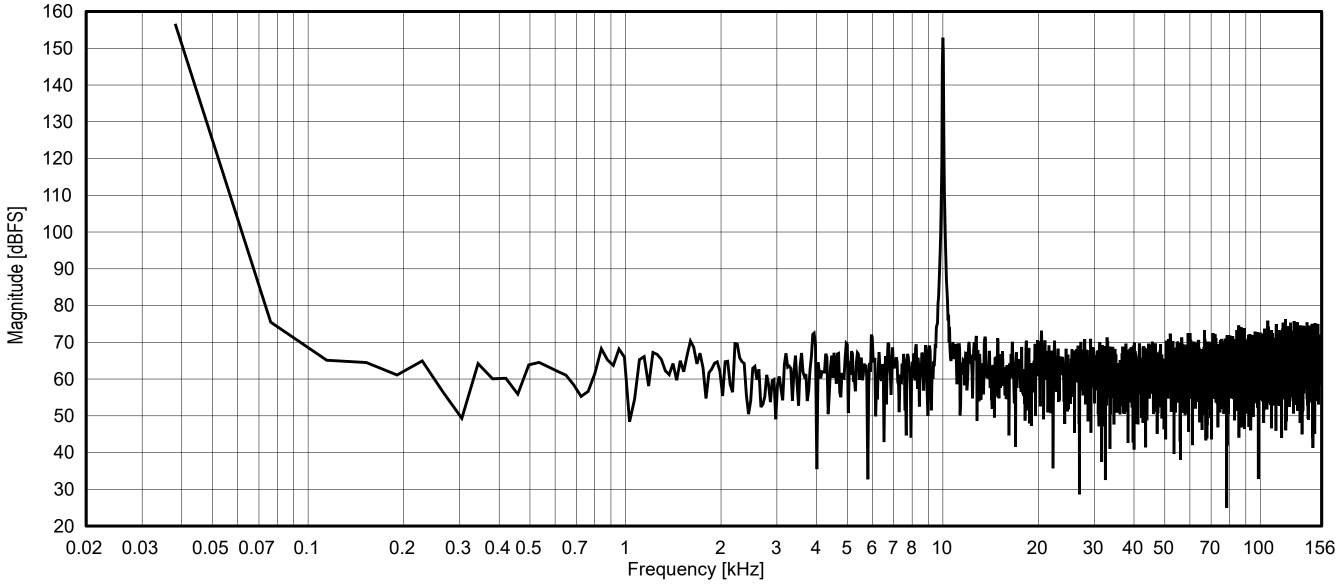

Figure 3-10. Output Spectrum of the Signal Chain with Single-Ended AMC0330S

4 Summary

Table 4-1 lists summary of the measurements. The spurious-free dynamic range (SFDR) is more relevant in the communication industry, but this is also a practical indicator that can be clearly seen in the frequency domain. The difference in performance between the TLV9001- and OPA365-based difference amplifier comes from the timing specification of the test board. The TLV9001 operational amplifier is a valid choice in systems that can work with longer sampling times, allowing the difference amplifier to fully settle before the sample and hold switch (SW) opens. However, this slows down the conversion rate, as other channels have to wait for the slowest one. Alternatively, split *slow* and *fast* channels between two ADCs if present in the MCU.

Table 4-1. Measurements Summary

Parameter	TLV9001	OPA365	AMC0330S	Unit
SFDR	48	76	81	dB
INL	0.53	0.14	0.1	%
INL	346	91	65	LSB

Systems that require faster ADC sampling benefit from higher-bandwidth operational amplifiers, such as the OPA365 or TLV365. The most economical choice is a single-ended output isolated amplifier, such as the AMC0330S or AMC0330R, in cases where the distance between the isolation amplifier and the ADC is short.

A list of recommendations when designing and validating an isolated signal chain interfacing with a SAR ADC is provided below:

- Use the single-ended output isolated amplifier (AMC0330R, AMC0330S) when the common-mode noise is not a concern
- Always use a charge bucket filter in front of the ADC input
- Measure the transient response of the amplifier during sampling for different conditions on the previously sampled signal
- Investigate the sampled signal in both the time and frequency domains (using FFT)
- Work closely with firmware implementers to make sure that the sampling order and timing do not change during development
- Use operational amplifiers that are capable of settling the input within the sampling time of the ADC (e.g. OPA365, TLV365)
- Keep in mind that operational amplifier's AC characteristics can affect the DC accuracy
- Simulate the sampling in a tool like pSpice to optimize the performance and charge-bucket filter
- Retest the behavior when changing the operational amplifier even if the family name remains same

Table 4-2 lists good-performing component values for the system with TMS320F28P650 MCU and the ADC running in single-ended mode with 16-bit resolution.

Table 4-2. Component Values Used in the Experimental Board With TMS320F28P650

Sample and hold switch resistance R_{SW} = 425Ω **Sample and hold capacitance C_{SH}=42.5pF**				
Parameter	**TLV9001**	**OPA365**	**AMC0330(R/S)**	**Unit**
Rb	47	47	47	Ω
Cb	1000	390	2200	pF
Settling time	2	0.1	0.4	us

5 References

1. Texas Instruments, *AMC0x30S Precision, ±1V Input, Basic and Reinforced Isolated Amplifiers With Fixed-Gain, Single-Ended Output*, data sheet.
2. Texas Instruments, *AMC0x30D Precision, ±1V Input, Basic and Reinforced Isolated Amplifiers With Fixed-Gain Differential Output*, data sheet.
3. Texas Instruments, *TLV900x Low-Power, RRIO, 1-MHz Operational Amplifier for Cost-Sensitive Systems*, data sheet.
4. Texas Instruments, *OPAx365 50-MHz, Zerø-Crossover, Low-Distortion, High-CMRR, RRI/O, Single-Supply Operational Amplifiers*, data sheet.

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