Application Note

Design Voltage Margining Circuit for UCD91xxx Power Sequencer and System Manager

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ABSTRACT

The UCD91xxx power sequencer and system manager provides margining function to trim output voltage of analog point-of-load converters. This application report discusses design considerations and provides a design procedure of the margining circuit.

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1 Introduction

The UCD91xxx power sequencer and system manager provides margining function to trim output voltage of analog point-of-load converters. This function can be used to facilitate voltage corner testing, which verifies the robustness of a product, as well as to actively trim output voltages in normal operation mode.

The UCD91xxx devices use digital pulse width modulator (DPWM) to implement the margining function. Figure 1-1 shows a closed-loop margining circuit. The UCD91xxx device outputs a pulse width modulation (PWM) signal, which is filtered by an RC filter formed by R4 and C1. The DC component of C1 voltage is controlled by the PWM duty cycle. The voltage on C1 sources or sinks current from the FB node through R3 and, as a result, changes the output voltage. The UCD91xxx compares the rail voltage and the targeted value and slowly adjusts the duty cycle. The margin control loop is so slow that it does not affect the power or feedback loop of the converter.

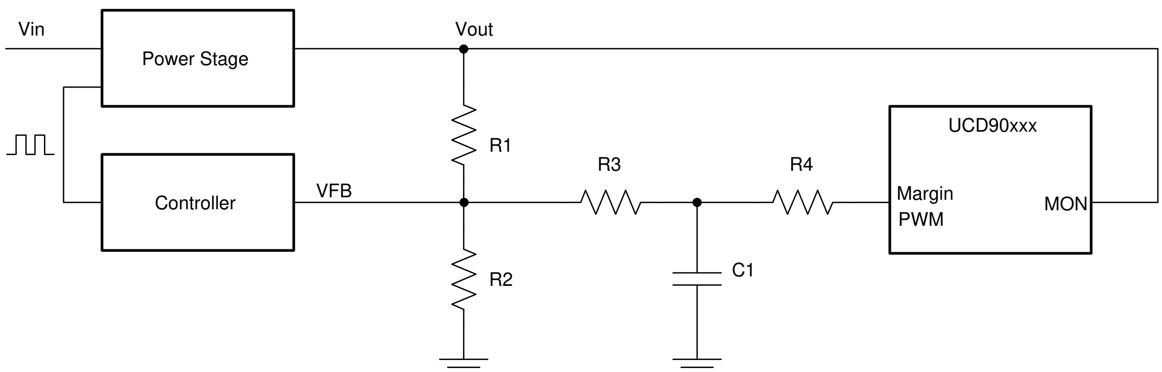

Figure 1-1. Closed-Loop Margining Circuit

This application report discusses the selection of the margin DPWM frequency, initial duty cycle, and component values of R3, R4, and C1.

2 Design Considerations

2.1 Resistor Values and Regulation Range

The maximum and minimum V_{out} occurs when the margin PWM duty cycle is 0 and 100%, respectively. Figure 2-1 shows the equivalent circuit. The minimum and maximum output voltages with margining circuit are derived in Equation 2 and Equation 3, respectively.

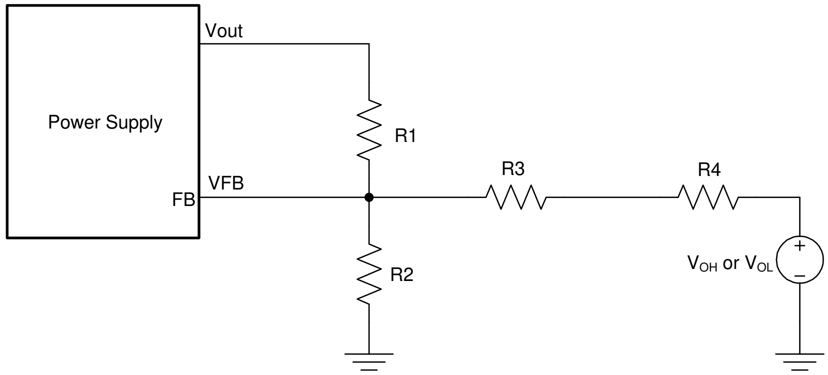

Figure 2-1. Equivalent Circuit at Maximum and Minimum V_{out}

$$V_{out,nom} = V_{ref} \times \frac{R_1 + R_2}{R_2} \tag{1}$$

$$V_{out,min} = V_{out,nom} + R_1 \times \left(\frac{V_{ref} - V_{OH}}{R_3 + R_4} \right) \tag{2}$$

$$V_{out,max} = V_{out,nom} + R_1 \times \left(\frac{V_{ref} - V_{OL}}{R_3 + R_4} \right) \tag{3}$$

where

- $V_{out,nom}$ is the nominal output voltage determined by resistor divider values
- V_{OH} is the PWM high-level output voltage
- V_{OL} is the PWM low-level output voltage
- V_{ref} is the reference voltage of the power supply

Based on Equation 2 and Equation 3, the sum of R3 and R4 is determined by the desired margin low or margin high values, whichever results in a smaller R3+R4 value. Equation 4 and Equation 5 can be used to calculate R3+R4 value for margin low and margin high scenarios, respectively.

$$R_3 + R_4 = \frac{R_1 \left(V_{OH} - V_{ref} \right)}{V_{out,nom} - V_{out,low}} \tag{4}$$

$$R_3 + R_4 = \frac{R_1 \left(V_{ref} - V_{OL} \right)}{V_{out,high} - V_{out,nom}} \tag{5}$$

The above equations still hold true when R2 is not present in some applications.

2.2 DPWM Frequency and V_{out} Resolution

The DPWM signals are generated from an internal clock. The number of quantization steps in each DPWM period is inversely proportional to the DPWM frequency. Equation 6 shows this relationship.

$$n = \frac{F_{CLK}}{F_{PWM}} \tag{6}$$

where

- n is the number of quantization steps in a DPWM period
- F_{CLK} is the internal clock frequency
- F_{PWM} is the DPWM frequency

The DPWM duty cycle can only have an integer number of quantization steps. As a result, the V_{out} controlled by the margin DPWM has finite resolution. The V_{out} step size equals the full voltage margining range divided by the number of quantization steps in a period, as shown in Equation 7.

$$V_{out,step} = \frac{V_{out,max} - V_{out,min}}{n} = \frac{V_{out,max} - V_{out,min}}{F_{CLK}} F_{PWM} \tag{7}$$

Apparently, the V_{out} step size is proportional to the V_{out} margining range and the DPWM frequency.

In margin mode and Active Trim mode, the UCD91xxx controls V_{out} with a very slow feedback loop. The loop is executed approximately once every 500µs. If the sampled V_{out} is unequal to the target value, the DPWM duty cycle changes by one quantization step towards the direction to minimize the error. Because V_{out} has voltage ripple and the analog-to-digital converter (ADC) has sampling noise, it can be expected that the DPWM duty cycle fluctuates by ±1 least significant bit (LSB) during margining and Active Trim operations, which causes V_{out} to slightly fluctuate around the targeted margin or trim value.

To minimize the voltage fluctuation, V_{out} step size should be reduced in order for the V_{out} fluctuation, due to the ±1 LSB duty cycle fluctuation, is acceptable. According to Equation 7, the DPWM frequency can be reduced to achieve this goal. The DPWM frequency is calculated by making $V_{out,step}$ an acceptable value then deriving the switching frequency accordingly. For example, $V_{out,step}$ can be arbitrarily set to 1mV, then the margin DPWM frequency can be determined by Equation 8.

$$F_{PWM} = \frac{V_{out,step} F_{CLK}}{V_{out,max} - V_{out,min}} \tag{8}$$

2.3 Margin DPWM Output Filtering

The square-wave signal from the margin DPWM must be sufficiently filtered so only the DC component shows effect on V_{out}.

There are two filtering mechanisms:

1. RC filter in the margining circuit
2. Loop response of the power supply

2.3.1 Attenuation by RC Filter

As shown in Figure 1-1, the RC filter is formed by R4 and C1. The voltage of C1 is connected to FB node through R3. Assuming the error amplifier is ideal, the FB node voltage is a DC voltage equal to the reference voltage. For AC analysis, the equivalent circuit of the RC filter can be drawn as in Figure 2-2.

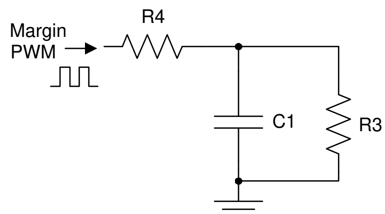

Figure 2-2. Equivalent Circuit of RC Filter

The amplitude of the AC voltage on C1 can be estimated by Equation 9. The lower case v denotes AC voltage component.

$$V_{C1} = \left| \frac{V_{PWM,1} R_3 Z_{C1}}{R_3 R_4 + (R_3 + R_4) Z_{C1}} \right| \quad (9)$$

where

- Z_{C1} is the C1 impedance at the DPWM frequency
- $v_{PWM,1}$ is the amplitude of the fundamental harmonic of the DPWM square-wave output

Only the fundamental harmonic is considered for simplicity. As shown in Equation 10, higher-order harmonics have more attenuation by the loop response of the power supply and are, thus, negligible. The $v_{PWM,1}$ is determined by Fourier series:

$$V_{PWM,1} = \frac{2\left(V_{OH} - V_{OL}\right)\sin\left(\pi D\right)}{\pi} \tag{10}$$

where

- D is the duty cycle of the margin DPWM

The biggest $v_{PWM,1}$ value occurs at D=0.5.

2.3.2 Attenuation by Loop Response

The voltage ripple on C1 is further attenuated by the loop response of the power supply. The following analysis shows how to estimate the attenuation.

First, consider a power supply without the margining circuit. If there is a break in the loop at point A, the compensated open-loop transfer function, G(s), is defined in Figure 2-3 and Equation 11.

$$G\left(s\right) = \frac{\hat{v}_{out}\left(s\right)}{\hat{v}_{A}\left(s\right)} \tag{11}$$

G(s) includes both power stage and compensator transfer functions, which can be obtained from modeling or circuit measurement. G(s) must be available information to power supply designers.

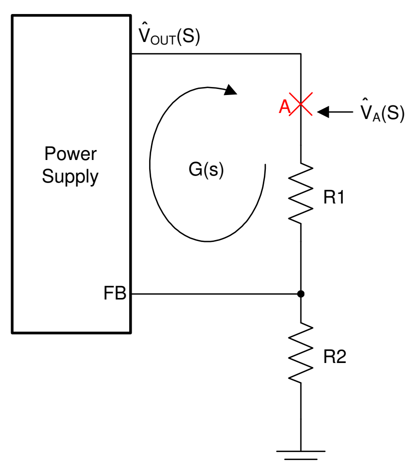

Figure 2-3. Block Diagram Without Margining Circuit

Next consider a power supply with the margining circuit, as shown in Figure 2-4. The transfer function of the power supply from V_{C1} to V_{out} is in Equation 12.

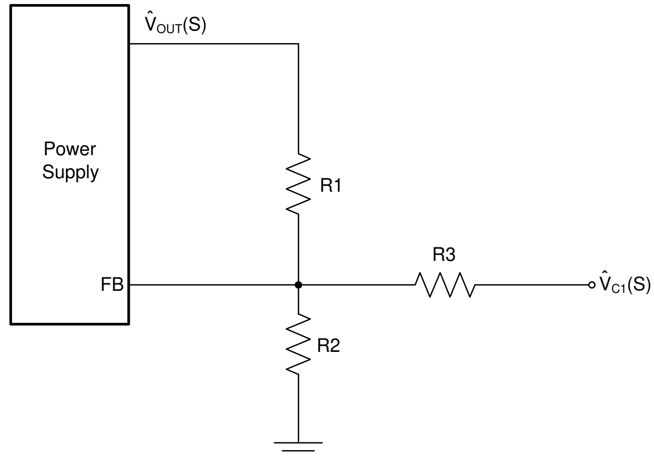

Figure 2-4. Block Diagram With Margining Circuit

$$T(s) = \frac{\hat{v}_{out}(s)}{\hat{v}_{C1}(s)} = \frac{R_1}{R_3}\frac{G(s)}{1-G(s)} \tag{12}$$

Based on Equation 12, it can be predicted that when R1=R3, the transfer function from V_{C1} to V_{out} is identical to the closed-loop transfer function of the original power supply. Figure 2-5 provides simulation results to verify the above conclusion supply: below the cross-over frequency, the closed-loop gain is 0dB, and above the cross-over frequency, the closed-loop gain is equal to open-loop gain.

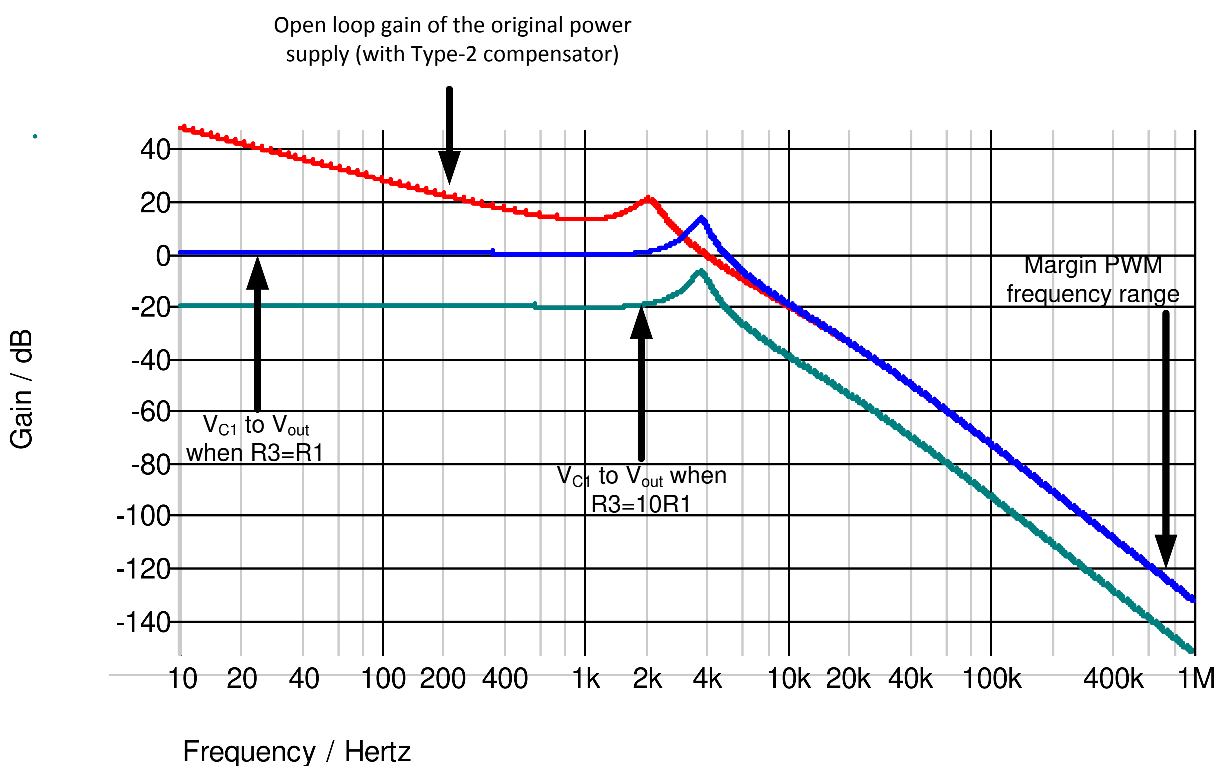

Figure 2-5. Example of V_{C1} to V_{out} Attenuation by Loop Response (Type-2)

The loop gain of the power supply at the margin DPWM frequency can be observed on the Bode plot, estimated from cross-over frequency, or calculated from the mathematical model. The voltage gain from V_{C1} to V_{out} at the margin DPWM frequency can be calculated from Equation 13.

$$\frac{\hat{v}_{out}\left(2\pi F_{PWM}\right)}{\hat{v}_{C1}\left(2\pi F_{PWM}\right)} = \frac{R_1}{R_3}\frac{G\left(2\pi F_{PWM}\right)}{1-G\left(2\pi F_{PWM}\right)} \tag{13}$$

For the Type-3 compensator, there is an R-C network in parallel with R1. In this case, Z1 must be used to replace R1 as shown in Figure 2-6 and Equation 14.

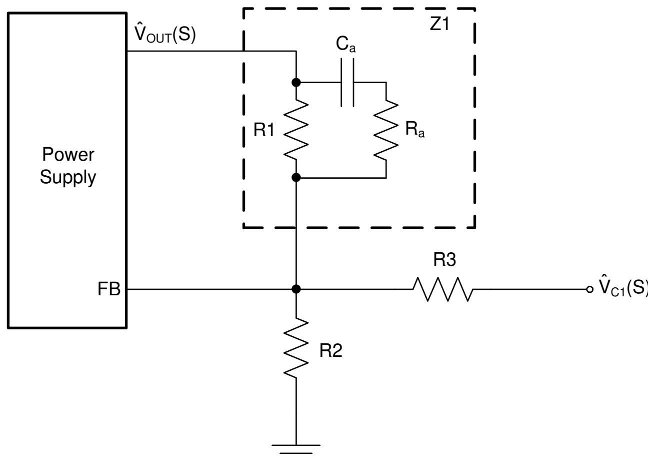

Figure 2-6. Block Diagram With Margining Circuit (Type-3 Compensator)

$$\frac{\hat{v}_{out}\left(2\pi F_{PWM}\right)}{\hat{v}_{C1}\left(2\pi F_{PWM}\right)} = \frac{\left|Z_1\left(2\pi F_{PWM}\right)\right|}{R_3}\frac{G\left(2\pi F_{PWM}\right)}{1-G\left(2\pi F_{PWM}\right)}$$

$$Z_1\left(2\pi F_{PWM}\right) = \frac{R_1\left(R_a + \frac{1}{j2\pi F_{PWM}C_a}\right)}{R_1 + R_a + \frac{1}{j2\pi F_{PWM}C_a}} \tag{14}$$

For simplicity, the Type-3 compensator can also use Equation 13 instead of Equation 14.

In conclusion, if the margin DPWM frequency is above the loop cross-over frequency, which is usually the case, the compensator provides significant attenuation. A large R3 value compared to R1 (or Z1) also provides attenuation. The C1 value must be selected to provide additional attenuation in order to eliminate V_{out} voltage ripple at the margin DPWM frequency.

For switch mode power supply only (not applicable to LDO), an additional frequency component that requires attenuation is the alias generated by the power supply switching frequency (Fsw) and the margin DPWM frequency (F_{PWM}). Due to the sampling nature of the PWM, the V_{C1} ripple is injected into compensated error signal, which is then sampled at the PWM fall edges. If the V_{C1} ripple frequency is greater than ½ Fsw, alias frequencies occur at output.

The alias frequencies can be calculated by Equation 15.

$$F_{alias} = \left| \pm k \times F_{SW} \pm F_{PWM} \right|, k = 1, 2, 3... \quad (15)$$

The lowest alias frequency (Fa) occurs in the first Nyquist zone (≤ ½ Fsw), which is the most difficult to filter. Fa frequency can be calculated by Equation 16.

$$m = \text{floor}\left(\frac{F_{PWM}}{F_{SW}} \right)$$
$$F_a = \min\left(\left| F_{PWM} - m \times F_{SW} \right|, \left| F_{PWM} - (m+1) \times F_{SW} \right| \right) \quad (16)$$

The margin DPWM frequency must be selected such that Fa is at the highest possible value (½ Fsw).

$$F_{PWM} = \left(m + \frac{1}{2} \right) \times F_{SW}, m = 0, 1, 2... \quad (17)$$

2.4 Impact on Power Supply Normal Operation

When not in margin or Active Trim mode, the margin DPWM pin is in high-impedance state. The branch formed by R3 and C1 is in parallel with R2, as shown in Figure 2-7.

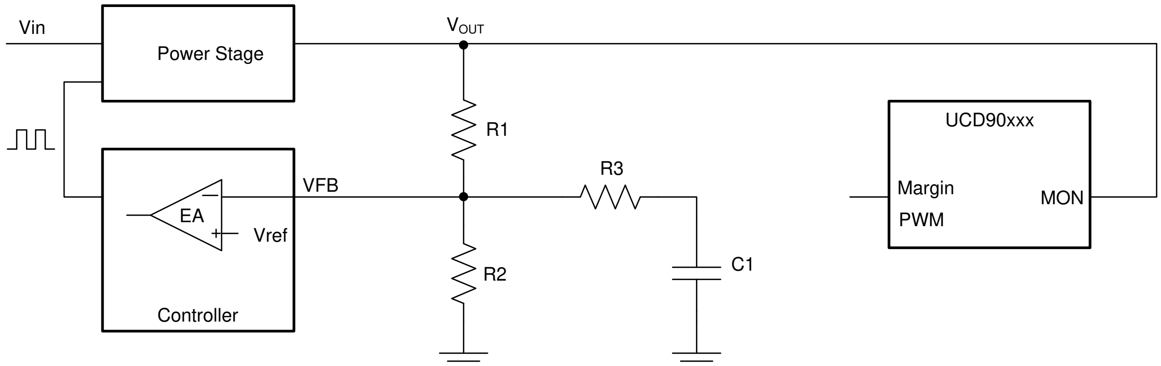

Figure 2-7. Equivalent Circuit in Normal Operation

Assuming the error amplifier in the controller is an ideal op-amp, the VFB is a DC voltage equal to the reference voltage. In this case, there is no small-signal current flowing through the R3-C1 branch, as a result, it has no impact to the loop transfer of the power supply function.

Real-world error amplifier has limited gain-bandwidth product, but the op-amp gain at the cross-over frequency must be still greater than 100. Consider the case where there is a voltage disturbance on V_{out} at the cross-over frequency. Because the closed-loop gain is 1 at cross-over frequency and the error amplifier still has a gain of 100, the voltage disturbance on VFB is about 1/100 of that on V_{out}. Assuming R3=10·R1, the small-signal current flowing through R3 is only 0.1% of that flowing through R1. Therefore, the impact of the R3-C1 branch on the transfer function of the power supply is negligible.

2.5 Impact on Power Supply Soft Start

During closed-loop soft start, the FB node voltage ramps up with the reference voltage. C1 voltage is initially zero. Current must flow from FB node to C1 to charge the capacitor. The additional charge current to C1 is from V_{out} flowing through R1. Therefore, when C1 is charging, V_{out} is higher than the reference voltage determined value. At the end of the soft start ramp, there is a possibility to overshoot.

In reality, the actual V_{out} ramp lags VFB ramp because the system has a steady state error for a slope input. At the end of VFB ramp, the V_{out} lag cancels the overshoot. The VFB ramp is often flattened near the end of the ramp, which reduces the current in R3 and thus reduces the overshoot. Therefore, the actual overshoot is often invisible. The following simplified math model is for sanity check and for reference only.

Assuming the soft start ramp is strictly linear, the VFB can be expressed as a function of time.

$$V_{FB}(t) = \frac{V_{ref}}{t_{rise}} \times t \tag{18}$$

where

- t_{rise} is the soft start rise time

If the ramp is infinitely long, the R3 current achieves a steady state.

$$I_{R3}(\infty) = \frac{V_{ref}}{t_{rise}} \times C_1 \tag{19}$$

The R3 current as a function of time can then be derived as:

$$I_{R3}(t) = I_{R3}(\infty) \times \left(1 - e^{\frac{-t}{R3xC1}}\right) \tag{20}$$

At the end of soft start ramp, the voltage overshoot caused by C1 charging is:

$$\Delta V_{out} = I_{R3}(t_{rise}) \times R_1 = \frac{V_{ref}}{t_{rise}} \times R_1 \times C_1 \times \left(1 - e^{\frac{-t_{rise}}{R3 \times C1}}\right) \tag{21}$$

Equation 21 can be used to check overshoot voltage at the end of soft start ramp. The actual overshoot amount is often approximately 50mV smaller than predicted because the soft start ramp is often flattened and gradually merges into steady state near the end. This calculation is for information only. If the overshoot is too large, the C1 value must be decreased.

To minimize C1 value needed:

1. Make R3=R4 (R3+R4 is fixed, which is discussed in Section 2.1).
2. Reduce the Margin High/Low range so that the larger R3+R4 value can be used.
3. Increase the R1 value so that larger R3+R4 value can be used.
4. Allow a higher ripple at V_{out}.

Alternately, increasing soft start rise time can also reduce overshoot.

2.6 Initial Duty Cycle

The UCD91xxx adjusts the margin DPWM duty cycle by one LSB every 500µs. If the initial duty cycle setting is far from the steady state value, this causes sudden V_{out} change when margining and Active Trim function is activated.

The suggested initial duty cycle is calculated by Equation 22. The initial DC output voltage of the margin DPWM's is equal to the reference voltage, which allows the UCD91xxx to gradually bring V_{out} to the targeted Margin High/Low level.

$$D_{init} = \frac{V_{ref} - V_{OL}}{V_{OH} - V_{OL}} \tag{22}$$

3 Design Procedure

Step 1: Use Equation 23 to calculate nominal output voltage. V_{ref} is the reference voltage of the power supply controller.

$$V_{out,nom} = V_{ref} \times \frac{R_1 + R_2}{R_2} \tag{23}$$

Step 2: Use Equation 24 to calculate initial margin DPWM duty cycle. V_{OH} and V_{OL} are output high and output low voltage levels of DPWM pins. Typical values are V_{OH} = 3.2V and V_{OL} = 0 V.

$$D_{init} = \frac{V_{ref} - V_{OL}}{V_{OH} - V_{OL}} \tag{24}$$

Step 3: Use Equation 25 and Equation 26 to estimate the margin DPWM pin current. $V_{out,low}$ is the margin-low output voltage, which must be less than $V_{out,nom}$. $V_{out,high}$ is the margin-high output voltage, which must be greater than $V_{out,nom}$.
If the higher current value of the two is greater than 1mA, increase the R1 and R2 values. In general, larger R1 and R2 values are preferred to reduce the current of the margin DPWM pin.

$$I_{DPWM} = \frac{V_{out,high} - V_{out,nom}}{R_1} \tag{25}$$

$$I_{DPWM} = \frac{V_{out,nom} - V_{out,low}}{R_1} \tag{26}$$

Step 4: Use Equation 27 and Equation 28 to calculate R3 and R4 values. The smaller value of the two must be selected. The actual resistor value must be equal to or less than the calculated value.

$$R_3 = R_4 = \frac{R_1 \left(V_{OH} - V_{ref}\right)}{2\left(V_{out,nom} - V_{out,low}\right)} \tag{27}$$

$$R_3 = R_4 = \frac{R_1 \left(V_{ref} - V_{OL}\right)}{2\left(V_{out,high} - V_{out,nom}\right)} \tag{28}$$

Step 5: Use Equation 29 to calculate maximum margin DPWM frequency that provides sufficient V_{out} resolution.

$$F_{PWM,max} = \frac{V_{out,step} F_{CLK}}{V_{out,max} - V_{out,min}} \tag{29}$$

$V_{out,step}$ is the allowed V_{out} fluctuation in margining and Active Trim mode. Larger $V_{out,step}$ allows for higher margin DPWM frequency. A good starting point is $V_{out,step}$ = 0.1% $V_{out,nom}$.

$V_{out,min}$ and $V_{out,max}$ are the output voltage levels when margin DPWM is at 100% and 0% duty cycle, respectively. The voltage levels can be calculated from Equation 30 and Equation 31.

$$V_{out,min} = V_{out,nom} + R_1 \times \left(\frac{V_{ref} - V_{OH}}{R_3 + R_4} \right) \tag{30}$$

$$V_{out,max} = V_{out,nom} + R_1 \times \left(\frac{V_{ref} - V_{OL}}{R_3 + R_4} \right) \tag{31}$$

F_{CLK} is the internal clock frequency of UCD91xxx devices:

1. Use 80MHz for UCD91320 and UCD91160 Margin pins.

Step 6: Use Equation 32 to calculate optimal margin DPWM frequency, F_{PWM}. F_{SW} is power supply's switching frequency.

$$\begin{gathered} m = \max\left(1, \mathrm{round}\left(\frac{F_{PWM,max}}{F_{SW}}\right)\right) \\ F_{PWM} = \min\left(F_{PWM,max}, \left(m - \frac{1}{2}\right) \times F_{SW}\right) \end{gathered} \tag{32}$$

Step 7: Use Equation 33 to calculate the lowest alias frequency, Fa.

$$\begin{gathered} n = \mathrm{floor}\left(\frac{F_{PWM}}{F_{SW}}\right) \\ F_a = \min\left(\left|F_{PWM} - n \times F_{SW}\right|, \left|F_{PWM} - (n+1) \times F_{SW}\right|\right) \end{gathered} \tag{33}$$

Step 8: Use Equation 34 to estimate switch mode power supply's open loop gain at frequency Fa, assuming:

1. The loop bandwidth is approximately 20% of switching frequency.
2. The gain slope is -20dB/decade between crossover frequency and Fa.

$$\mathrm{Gain}_{OL}(2\pi F_a) = \frac{0.2 F_{SW}}{F_a} \tag{34}$$

This value can be also obtained from experimental result.

For the margining LDO output, use 1 for this value.

Step 9: Use Equation 35 to estimate closed-loop gain from V_{C1} ripple to V_{out}.

$$\mathrm{Gain}_{VC1\_to\_Vout}(2\pi F_a) = \min\left(\frac{R_1}{R_3}, \mathrm{Gain}_{OL}(2\pi F_a)\frac{R_1}{R_3}\right) \tag{35}$$

(Optional for Type-3 compensator)

$$\mathrm{Gain}_{\mathrm{VC1\_to\_Vout}}\left(2\pi F_a\right)=\min\left(\frac{\left|Z_1\left(2\pi F_a\right)\right|}{R_3},\mathrm{Gain}_{\mathrm{OL}}\left(2\pi F_a\right)\frac{\left|Z_1\left(2\pi F_a\right)\right|}{R_3}\right) \tag{36}$$

where

- Z1 is defined in Figure 2-6

$$\left|Z_1\left(2\pi F_a\right)\right|=R_1\sqrt{\frac{4C_a^2F_a^2\pi^2R_a^2+1}{4C_a^2F_a^2\pi^2\left(R_1+R_a\right)^2+1}} \tag{37}$$

For simplicity, Equation 35 can be used for Type-3 compensator.

Step 10: Use Equation 38 to calculate the required total gain so the margin DPWM square-wave signal is attenuated to an acceptable V_{out} ripple, that is, $V_{out,step}$ defined in Step 5. This step takes into account the worst case scenario where the margin DPWM duty cycle is 50%.

$$\mathrm{Gain}_{\mathrm{total}}=V_{\mathrm{out,step}}\times\frac{\pi}{2\left(V_{\mathrm{OH}}-V_{\mathrm{OL}}\right)} \tag{38}$$

Step 11: Use Equation 39 to calculate the gain required to attenuate the margin DPWM square wave to the required V_{C1} ripple.

$$\mathrm{Gain}_{\mathrm{RC}}=\frac{\mathrm{Gain}_{\mathrm{total}}}{\mathrm{Gain}_{\mathrm{VC1\_to\_Vout}}\left(2\pi F_a\right)} \tag{39}$$

Step 12: Use Equation 40 to calculate the C1 value. If Gain_{RC} is greater than R4/(R3+R4), C1 is not needed.

$$C_1=\frac{\sqrt{R_3^2-\mathrm{Gain}_{\mathrm{RC}}^2\left(R_3+R_4\right)^2}}{2\pi F_{\mathrm{PWM}}\,\mathrm{Gain}_{\mathrm{RC}}\,R_3\,R_4} \tag{40}$$

Use Equation 41 to predict overshoot at the end of soft start ramp. t_{rise} is the soft start rise time.

The actual overshoot is often approximately 50mV smaller than predicted because the soft start ramp is often flattened and gradually merges into steady state near the end. This calculation is for information only.

If the overshoot is too large, the following measures can be used:

1. Reduce unnecessarily wide Margin High/Low range to reduce the C1 value.
2. Increase the allowed V_{out} ripple so as to increase DPWM frequency and, thus, decreases the C1 value.
3. Increase the soft start rise time to reduce overshoot directly.
4. Increase the R1 value to reduce C1 value needed for filtering.

$$\Delta V_{out} = \frac{V_{ref}}{t_{rise}} \times R_1 \times C_1 \times \left(1 - e^{\frac{-t_{rise}}{R3 \times C1}}\right) \tag{41}$$

4 Summary

The UCD91xxx devices provide functions to closed-loop margining and trim power supply output voltage with high accuracy. This application report discussed design considerations and provided a design procedure to achieve optimal design.

5 References

Texas Instruments, *UCD91320 32-Rail PMBus™ Power Sequencer and System Manager* , data sheet.

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