Application Note

Selecting the Optimized MOSFET for TPS61287

Nathan Ding, Lisa Gao

ABSTRACT

Selecting the appropriate power switch, typically a MOSFET, is critical for the performance, efficiency, and reliability of a boost converter. An improper selection can lead to poor efficiency and even failures such as shoot-through. This application note provides basic guidelines that aim to aid engineers in the power MOSFET selection. The impact of different MOSFET parameters on converter operation and introduce a dedicated calculation tool is explained. A case study demonstrates the application of these selection guidelines and the calculation tool.

Table of Contents

Trademarks

All trademarks are the property of their respective owners.

Copyright © 2026 Texas Instruments Incorporated

1 Introduction

The TPS61287 is a high-power density, synchronous boost converter that integrates the high side synchronous rectifier MOSFET and uses an external low side MOSFET to provide a high efficiency and small size design. The TPS61287 has a wide input voltage range from 2V to 23V and the output voltage covers up to 25V with 20A switching valley current capability. The TPS61287 uses an adaptive constant on-time valley current control topology to regulate the output voltage. Under moderate to heavy load condition, the TPS61287 operates in pulse width modulation (PWM) mode. There are two optional modes in light load by configuring the MODE pin: Auto PFM mode to improve light-load efficiency and Forced PWM to avoid audible noise and other problems caused by low switching frequency. The switching frequency in the PWM mode is 320kHz. The TPS61287 provides 27V output overvoltage protection, cycle-by-cycle overcurrent protection, and thermal shutdown protection.

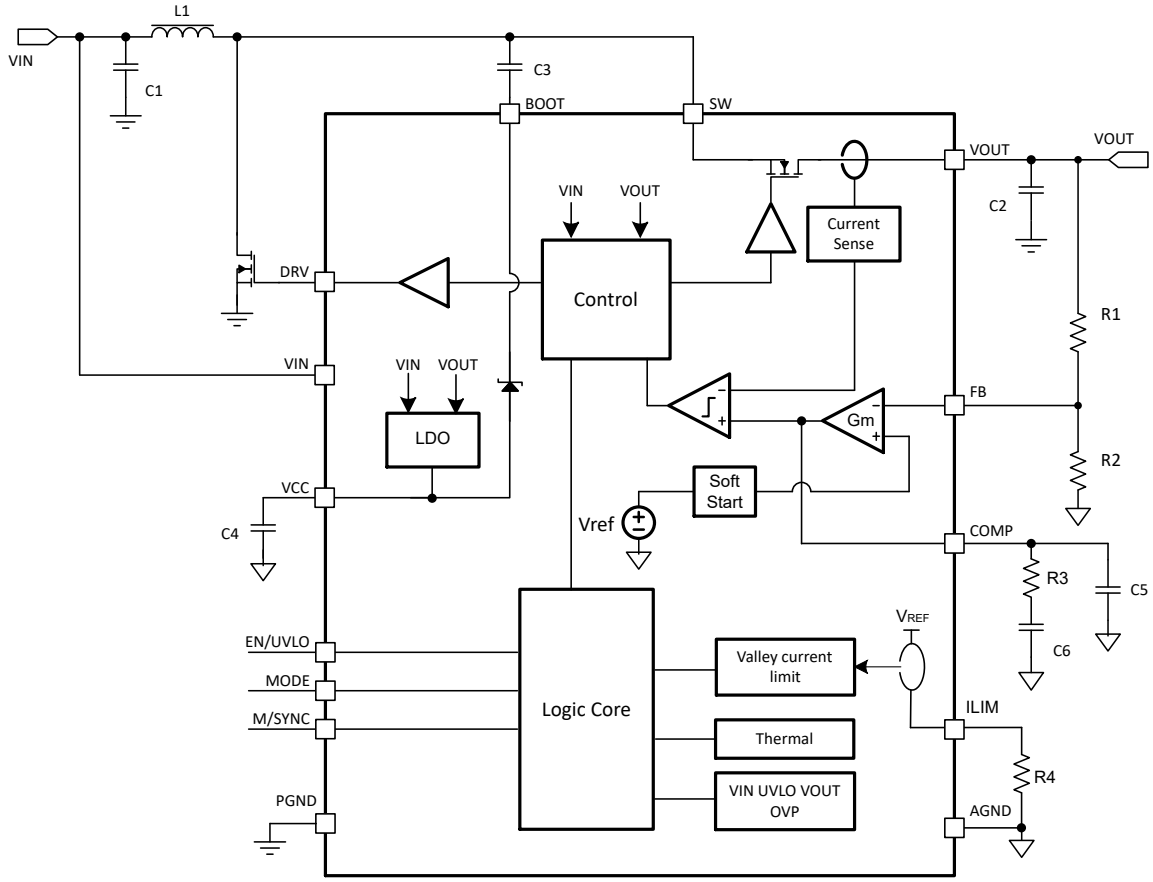

Figure 1-1. TPS61287 Functional Block Diagram

This application note is a guide for the selection of the external MOSFETs used in combination with the boost device TPS61287.

Copyright © 2026 Texas Instruments Incorporated

2 Key Parameters for Power MOSFET Selection

2.1 Static Characteristics

Static parameters usually define the absolute maximum ratings and on-state performance of the switch.

- Drain-Source Voltage (V_{DSS}): This must be rated higher than the maximum voltage seen by the MOSFET. For a boost converter, this is at least the maximum output voltage (V_{OUT}). A safety margin of 30-50% is recommended to account for voltage spikes caused by parasitic inductance.
- Continuous Drain Current (I_D): The MOSFET must handle the RMS and average input current. The RMS current in a boost converter is approximately equal to the input current (I_{IN}).
- On-Resistance ($R_{DS(on)}$): This parameter directly determines the conduction losses ($P_{cond} = I_{RMS}{}^2 \times R_{DS(on)}$). A lower $R_{DS(on)}$ is desirable but often trades off with higher gate charge.
- Gate threshold voltage ($V_{GS(th)}$) and gate plateau voltage ($V_{plateau}$) or miller voltage (V_{miller}): these two voltages must be smaller than the MOSFET gate driving voltage so than the MOSFET can be fully turned on.

2.2 Dynamic Characteristics

Dynamic parameters are related to the switching speed and the energy required to gate driver.

The intrinsic capacitances of a MOSFET (C_{iss}, C_{oss}, C_{rss}) decide the switching behavior. Figure 2-1 shows the switching process of a usual Boost device low-side MOSFET and then the role of these capacitances is explained.

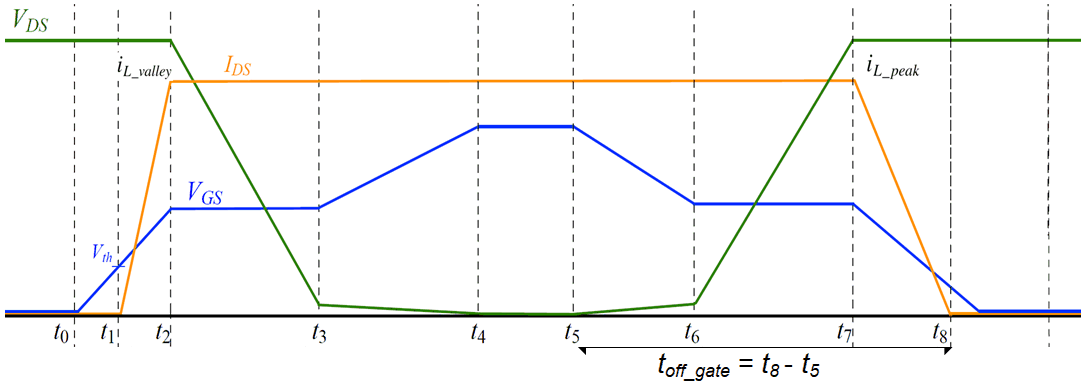

Figure 2-1. MOSFET Switching Waveforms

How capacitances affect switching speed: when the MOSFET is turning on, the gate driver must charge C_{iss} (input capacitance) to turn the MOSFET on first (from t_0 to t_2). As V_{GS} reaches the plateau voltage, the driver current is consumed to discharge C_{rss}, which falls down the V_{DS} (from t_2 to t_3). A larger total gate charge (Q_g) and capacitance require more drive current and time to switch.

Usually there are two negative impacts with larger capacitance:

1. Increased switching losses: slower switching transitions increase the time during which high voltage and high current overlap (t_1 to t_3 and t_6 to t_8 in Figure 2-1), leading to high switching losses (P_{sw}) and low efficiency.
2. Risk of shoot-through: if the switch turns off too slowly, there is not be enough time to prevent both the high-side and low-side switches from being on simultaneously. This shoot-through condition creates a short circuit across the output voltage rail, and there is a high risk of destroying the MOSFET and the Boost controller.

For controllers with adjustable dead time, the dead time must be set longer than the sum of the turn-off delay of the switch and fall time to avoid shooting-through. While for controllers with fixed dead time like TPS61287, the selected MOSFET must have a sufficiently low Q_g or junction capacitance to verify the switching time is shorter than the fixed dead time.

Copyright © 2026 Texas Instruments Incorporated

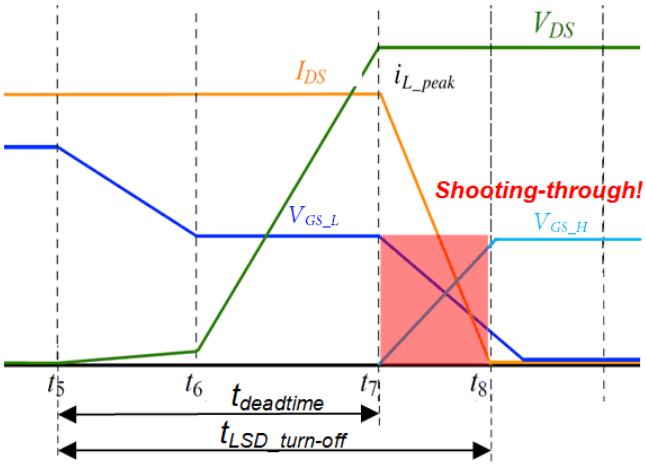

Figure 2-2. Switching Behavior with Poor Dynamic Characteristic

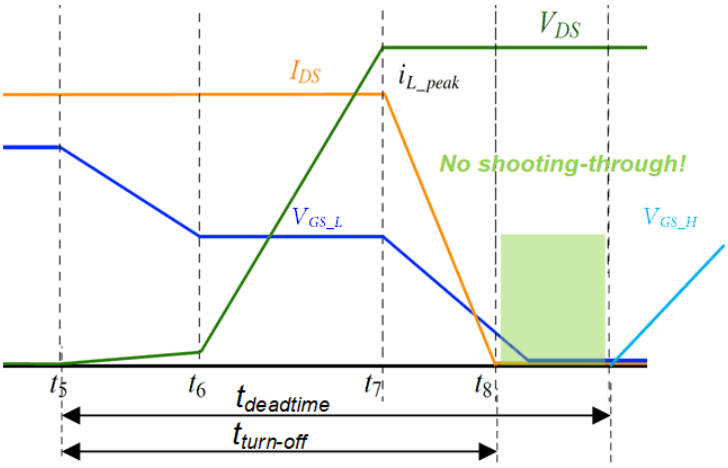

Figure 2-3. Switching Behavior with Good Dynamic Characteristics

Figure 2-2 and Figure 2-3 clearly demonstrates the negative impact of high dynamic parameters on switching speed and the risk of shooting-through.

However, the MOSFET junction capacitance is not as small as possible. Too small a junction capacitance can cause the switching speed to be too fast, increasing the SW voltage spikes (transient voltage at nanosecond level), causing the MOSFET and chip overvoltage stress. For safety of TPS61287, TI recommends that engineers control the voltage spike of the SW below 36V.

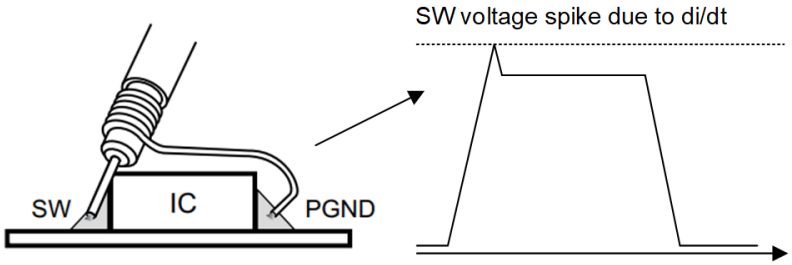

Figure 2-4. SW Voltage Spike Measurement with Low-Inductance Probe

If the SW voltage spike is too high due to the selection of a MOSFET with a very small junction capacitance, TI recommends series a drive resistor (RDRV) at the gate of the MOSFET to slow the drive speed and thus reduce the SW voltage spike.

Copyright © 2026 Texas Instruments Incorporated

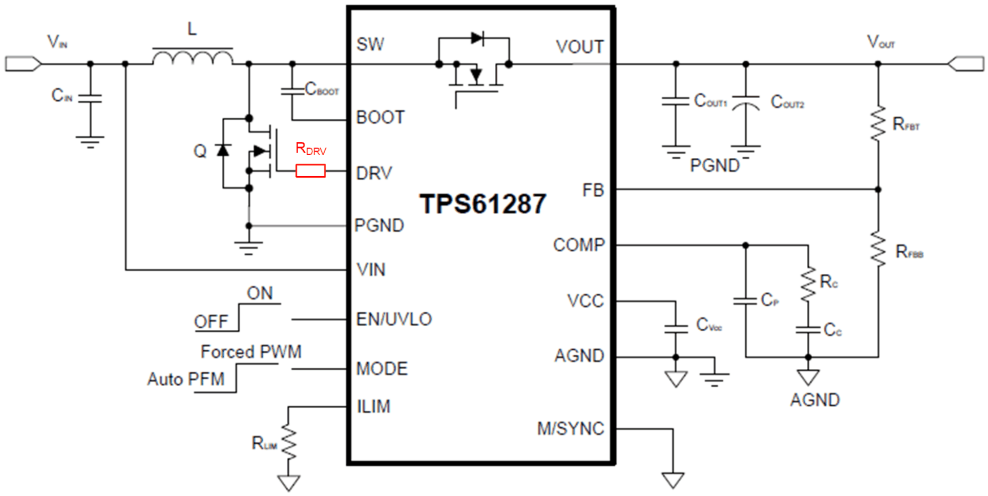

Figure 2-5. Gate Drive Resistor to Slow the Drive Speed and Reduce the SW Voltage Spike

2.3 Thermal Parameters

Thermal management verifies the switch operates within the safe operating area (SOA).

- Junction-to-Ambient Thermal Resistance ($R_{\theta JA}$): This defines the temperature rise from the junction to the ambient air for a given power dissipation. A lower $R_{\theta JA}$ (achieved through better packages or heatsinking) is critical for heat dissipation.
- Total Power Dissipation (P_D): The sum of conduction and switching losses. The junction temperature can be calculated as: $T_J = T_A + (P_D \times R_{\theta JA})$, where T_A is the ambient temperature. T_J must always remain below the maximum rating (typically 150°C or 175°C).

Copyright © 2026 Texas Instruments Incorporated

3 Introduction to the MOSFET Selection Tool

To simplify the selection process for our TPS61287 Boost controller family. An excel-based calculation tool is developed. The calculator can also take user inputs about the operating conditions, BOM, and system requirements to estimate power loss and efficiency. Note that the calculator does not consider power loss from other sources such as reverse recovery loss. The efficiency calculator is best used to compare one FET to another FET.

The calculator includes a low-side MOSFET selection section to estimate the turn-off time; the section can be used to select a MOSFET with proper dynamic characteristics.

3.1 Input MOSFET Parameters to Calculation Tool

This section aims to guide engineers on how to get the input parameters in calculation tool to select a proper MOSFET.

First input the application specifications, entering parameters such as V_{IN}(min/max), V_{OUT}, I_{OUT}, switching frequency and the LC parameters. Then choose a candidate MOSFET and manually enter the key parameters as shown in Figure 3-1.

Step 7: Low-Side MOSFET Selection		
On-State resistance, $R_{DS(on)}$	7	mΩ
Total gate charge, Q_G	9	nC
Gate resistance, R_G	0.8	Ω
External gate resistance on PCB, R_{G_PCB}	0	Ω
Input capacitance at Vds=0V, Ciss_0V	2000	pF
Input capacitance at Vds=Vout, Ciss_Vout	1800	pF
Output capacitance at Vds=0V, Coss_0V	2200	pF
Output capacitance at Vds=Vout, Coss_Vout	500	pF
Reverse transfer capacitance at Vds=0V, Crss_0V	450	pF
Reverse transfer capacitance at Vds=Vout, Crss_Vout	40	pF
Low side FET gate driving voltage, V_{LS_gate}	5.1	V
Gate-Source Threshold Voltage, $V_{GS(TH)}$	1.2	V
Gate plateau voltage / miller voltage, $V_{plateau}$	2.5	V
LS-GATE off to HS-GATE on deadtime, t_{DLH}	30.0	ns
Calculated low side gate turn off time, t_{off_gate} (should be smaller than deadtime t_{DLH})	19.2	ns

Figure 3-1. Input MOSFET Parameters in Calculation Tool

The first parameter in the design calculator is the on-state resistance (RDS(on)). The calculator asks for $R_{DS(on)}$ at 5.1V driving voltage. $R_{DS(on)}$ is typically given in the data sheet either in the electrical characteristics section or in a graph that plots the V_{gs} versus $R_{DS(on)}$.

The total gate charge (Q_G) refers to the charge (in coulombs) necessary to charge the gate capacitance to turn on the MOSFET so that the actual gate voltage of the MOSFET matches the driving voltage. This is different from the switching charge. Q_G is typically given in the MOSFET data sheet.

The internal gate resistance R_G can be modeled by a resistor in series with the MOSFET gate, while RG_PCB is the external gate resistance introduced by PCB copper trace or external resistor.

The C_{iss}, C_{rss}, C_{oss} is the input, reverse and output junction capacitance. Noted that the dynamic characteristic of a MOSFET mainly varies with the drain-source voltage V_{DS}, Figure 3-2 shows the dependency of C_{iss}, C_{rss}, C_{oss} on V_{DS}. The junction capacitance is typically given in a graph that plots the V_{DS} versus capacitance.

Copyright © 2026 Texas Instruments Incorporated

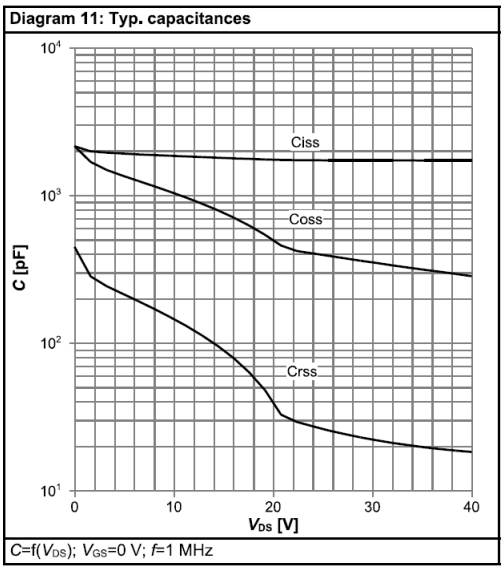

Figure 3-2. MOSFET C_{iss}, C_{rss}, C_{oss} versus V_{DS}

The gate-source threshold voltage V_{GSTH}, is the threshold voltage that the MOSFET is turned on, while the gate plateau voltage or miller voltage is the voltage that the C_{rss} is charged. These two voltages are typically given in the MOSFET data sheet.

3.2 Review the Results

The tool automatically calculates:

- The recommended BOM for provided conditions.
- A warning if the estimated low side turn-off time approaches the fixed dead time of the controller.
- The estimated bold plot, phase margin and gain margin to evaluate stability.
- The estimated low-side MOSFET power loss, total power dissipation, predicted junction temperature and efficiency.

Noted that the results in the tool are the calculation results by theory, doesn't consider some impact from non-linear circuits and components. The calculation tool is best used to compare different BOMs or quickly get a start point for system parameters design.

Copyright © 2026 Texas Instruments Incorporated

4 Calculator Tool MOSFET Selection Example and Bench Evaluation

This section gives an example of how to use the calculation tool for the design of TPS61287. For this example, the following operating conditions are used.

The other input parameters are left as the default.

Table 4-1. Operating Conditions for Design Calculator Example

Parameter	Value	Unit
V_{IN} (minimum)	3.0	V
V_{IN} (nominal)	3.6	V
V_{IN} (maximum)	4.2	V
V_{OUT}	18	V
I_{OUT} (maximum)	2	A
I_{LIM}	20	A
T_A	25	°C

There are two MOSFET candidates, option A and option B, with same $R_{DS(on)}$ while option A has larger junction capacitance than option B.

After the yellow cell are filled in, the calculator can get the low side MOSFET turn-off time, power loss, temperature rise and total efficiency.

Step 7: Low-Side MOSFET Selection

On-State resistance, $R_{DS(on)}$	7	mΩ
Total gate charge, Q_G	34	nC
Gate resistance, R_G	0.9	Ω
External gate resistance on PCB, R_{G_PCB}	0	Ω
Input capacitance at Vds=0V, Ciss_0V	5000	pF
Input capacitance at Vds=Vout, Ciss_Vout	3527	pF
Output capacitance at Vds=0V, Coss_0V	2000	pF
Output capacitance at Vds=Vout, Coss_Vout	257	pF
Reverse transfer capacitance at Vds=0V, Crss_0V	1500	pF
Reverse transfer capacitance at Vds=Vout, Crss_Vout	215	pF
Low side FET gate driving voltage, V_{LS_gate}	5.1	V
Gate-Source Threshold Voltage, $V_{GS(TH)}$	2	V
Gate plateau voltage / miller voltage, $V_{plateau}$	3	V
LS-GATE off to HS-GATE on deadtime, t_{DSH}	30.0	ns
Calculated low side gate turn off time, t_{off_gate} (should be smaller than deadtime t_{DSH})	34.3	ns

Step 8: Efficiency Analyzer

Default EVM Inductor DC loss, $P_{loss\_inductor\_DC}$	931	mW
Actually used inductor DC loss, $P_{loss\_act\_inductor\_DC}$		mW
Default EVM Inductor AC loss, $P_{loss\_inductor\_AC}$	59	mW
Actually used inductor AC loss, $P_{loss\_act\_inductor\_AC}$		mW
Low-side MOSFET power loss, $P_{loss\_LS\_FET}$	1746	mW
IC power loss, P_{loss_IC}	1631	mW
Low-side MOSFET Junction-to-ambient thermal resistance, $R_{\theta JA\_FET}$	53	°C/W
Low-side MOSFET junction temperature rise	92.5	°C
IC Junction-to-ambient thermal resistance, $R_{\theta JA\_IC}$	36.6	°C/W
IC junction temperature rise	59.7	°C
Calculated efficiency on PWM@V_{IN_nom}, V_{OUT}, I_{OUT_MAX}, $\eta_{@}$	89.2	%

Figure 4-1. Option A Calculated Results

Copyright © 2026 Texas Instruments Incorporated

Step 7: Low-Side MOSFET Selection		
On-State resistance, $R_{DS(on)}$	7	mΩ
Total gate charge, Q_G	9	nC
Gate resistance, R_G	0.8	Ω
External gate resistance on PCB, R_{G_PCB}	0	Ω
Input capacitance at Vds=0V, Ciss_0V	2000	pF
Input capacitance at Vds=Vout, Ciss_Vout	1800	pF
Output capacitance at Vds=0V, Coss_0V	2200	pF
Output capacitance at Vds=Vout, Coss_Vout	500	pF
Reverse transfer capacitance at Vds=0V, Crss_0V	450	pF
Reverse transfer capacitance at Vds=Vout, Crss_Vout	40	pF
Low side FET gate driving voltage, V_{LS_gate}	5.1	V
Gate-Source Threshold Voltage, $V_{GS(TH)}$	1.2	V
Gate plateau voltage / miller voltage, $V_{plateau}$	2.5	V
LS-GATE off to HS-GATE on deadtime, t_{DLH}	30.0	ns
Calculated low side gate turn off time, t_{off_gate} (should be smaller than deadtime t_{DLH})	19.2	ns

Step 8: Efficiency Analyzer		
Default EVM Inductor DC loss, $P_{loss\_inductor\_DC}$	931	mW
Actually used inductor DC loss, $P_{loss\_act\_inductor\_DC}$		mW
Default EVM Inductor AC loss, $P_{loss\_inductor\_AC}$	59	mW
Actually used inductor AC loss, $P_{loss\_act\_inductor\_AC}$		mW
Low-side MOSFET power loss, $P_{loss\_LS\_FET}$	1023	mW
IC power loss, P_{loss_IC}	1383	mW
Low-side MOSFET Junction-to-ambient thermal resistance, $R_{\theta JA}$_FET	60	°C/W
Low-side MOSFET junction temperature rise	61.4	°C
IC Junction-to-ambient thermal resistance, $R_{\theta JA\_IC}$	36.6	°C/W
IC junction temperature rise	50.6	°C
Calculated efficiency on PWM@V_{IN_nom}, V_{OUT}, I_{OUT_MAX}, η_{cal}	91.4	%

Figure 4-2. Option B Calculated Results

Option A has worse dynamic characteristics than option B, which led to significantly higher power loss (1746mW with option A while 1023mW with option B), higher temperature (92.5°C with option A while 61.4°C with option B) and poorer efficiency (89.2% with option A while 91.4% with option B).

More importantly, the turn-off time of option A is calculated as 34.3ns, which is longer than the LS-GATE off to HS-GATE on deadtime (30ns). A warning is listed here considering the risk of shoot-through. The turn-off time is 19.2ns with option B, which is much shorter than deadtime.

So, option B was chosen as option B provided lower power loss, meeting both the dynamic performance and thermal requirements. Figure 4-3 shows the efficiency curve on bench with the option B MOSFET.

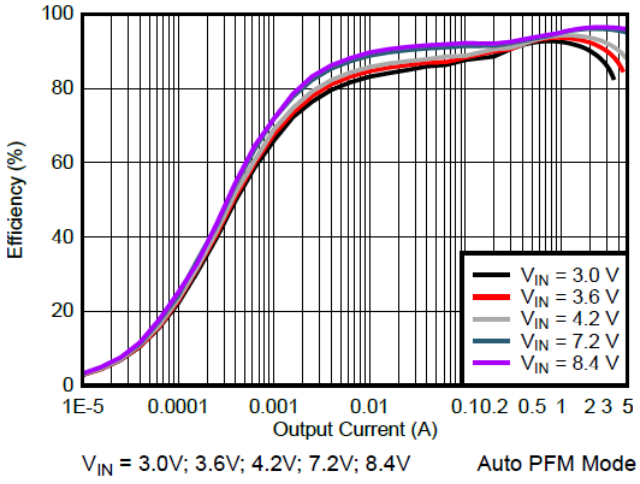

Figure 4-3. Efficiency Curve of TPS61287 With Option B MOSFET

Copyright © 2026 Texas Instruments Incorporated

5 Summary

TPS61287 device can be used to create efficient Boost converter systems for many kinds of applications. The efficiency of these systems can vary based on the operating conditions of the system and BOM selection, especially the MOSFET selection. The data sheet parameters of the MOSFET need to be reviewed and considered carefully. Engineers must ensure the voltage of the MOSFET and current ratings exceed the application requirements with sufficient margin. Crucially, the dynamic parameters, particularly gate charge and capacitances, must be compatible with the gate drive strength of the controller and dead time to minimize switching losses and prevent shoot-through. Thermal calculations are mandatory to validate the reliability of the design. Utilizing the calculation tool for our TPS61287 devices streamlines this process, enabling a swift and preferred MOSFET choice, leading to efficient and robust boost designs.

6 References

1. Texas Instruments, *TPS61287 23V VIN, 25V VOUT 20A Synchronous Boost Converter with Stackable Multiphase Function*, data sheet.
2. Texas Instruments, *MOSFET Selection Guide for BQ2575x Family*, application note.
3. Texas Instruments, *MOSFET Support and Training Tools*, application note.
4. Texas Instruments, *Understanding the Absolute Maximum Ratings of the SW Node*, application note.

Copyright © 2026 Texas Instruments Incorporated

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025