Application Brief

Up and Down Translation in TI's Programmable Logic Devices (TPLD)

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Introduction to Voltage-Level Translation

Modern electronics typically have many components operating at different voltage levels. This can be due to incorporating components from different generations, or to optimize performance or power consumption. A processor, for example, can operate at a lower 1.8V supply voltage, compared to a sensor's 3.3V supply voltage. This can lead to difficulty communicating between the two systems.

Voltage translators, also known as level shifters, are designed to have inputs of one voltage level and outputs of another. This allows for communication between devices operating at different voltages. Without a level shifter, a device outputting at 3.3V sending a signal to a processor operating at 1.8V can damage the processor, or, if the processor were to send a signal to the other device, it may not be able to reach the other device's threshold to register a high input. Up translation is when a device shifts a lower voltage input to a higher voltage output, and down translation is when a device shifts a higher voltage input to a lower voltage output.

Because logic devices are already often used in communication between different devices as buffers or to combine signals, there is a natural push to incorporate level shifting into logic devices. The TTL voltage threshold, for example, is an industry standard communication level designed to allow compatibility between devices operating at a 5V supply voltage and devices operating at a 3.3V supply voltage. For down-translation specifically, some devices are designed with overvoltage tolerant inputs that can accept voltages higher than the supply voltage. For down translation, open-drain outputs allow users to supply a separate, lower supply voltage for the output from the supply voltage of the device.

For more information about voltage translation, see this comprehensive introduction: Basics of Voltage-Level Translation

TI's Programmable Logic Devices (TPLD) support both up and down translation to maximize the ease of use and potential for integration for designers.

Up Translation in TPLD

To allow for up translation, all TPLD devices have an optional low voltage digital input mode for the input pins. This mode dramatically reduces the high- and low-level input threshold values for the pin, allowing for compatibility with as low as a 1.8V logic threshold device across the voltage range of the TPLD, while the TPLD would continue to output with the voltage level expected of its supply voltage.

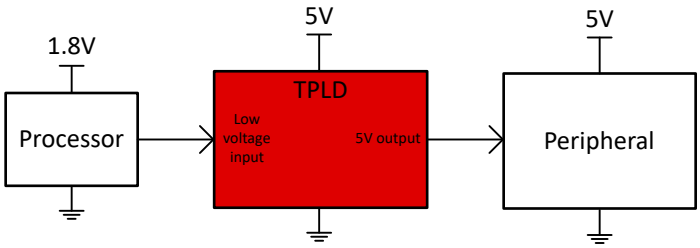

Figure 1. Up Translation Using TPLD

To put a pin into low voltage digital input mode in InterConnect Studio, select the input pin, click the Input Mode dropdown, and select *Low voltage digital input*, as shown in Figure 2.

Figure 2. ICS Pin Settings Showing Low Voltage Digital Inputs

Down Translation in TPLD

To allow for down translation in TPLD, the output pins of all TPLD have an optional open-drain NMOS output mode. This allows for a separate voltage source, lower than VCC, to be connected to that output line through a pull-up resistor. The pin either drives low, forcing the output line low, or is high impedance, causing the output line to be pulled up to the separate voltage source. This way, an arbitrary voltage can be output from the line. This output type supports slower speeds than a typical push-pull output, as the rail must be pulled up through the resistor instead of being driven high by the TPLD.

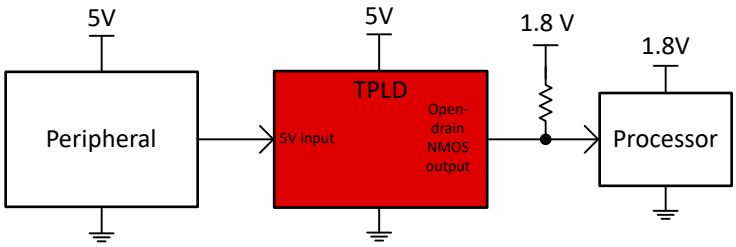

Figure 3. Down Translation Using TPLD

To put an output pin into open-drain NMOS mode in ICS, select the output pin, click the *Output Mode* dropdown, and select *Open Drain NMOS*, as shown in Figure 4.

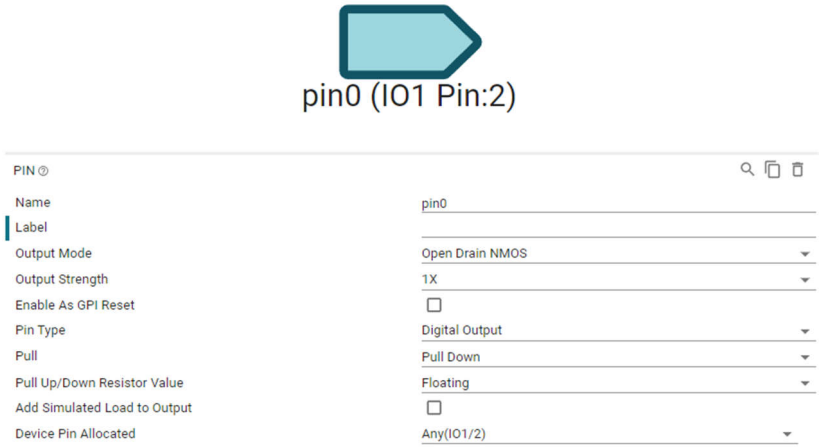

Figure 4. ICS Pin with Open Drain Outputs

As more industries trend towards lower voltages, TPLD devices allow designers to design-in and integrate the logic and level translators into a single device, simplifying the BOM and reducing solution size. For more information on TPLD, visit the TPLD product page or ask our engineers a question on the TI E2E™ Logic Support Forum.

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