Functional Safety Information

TPS2HB16-Q1
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for TPS2HB16-Q1 (HTSSOP package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

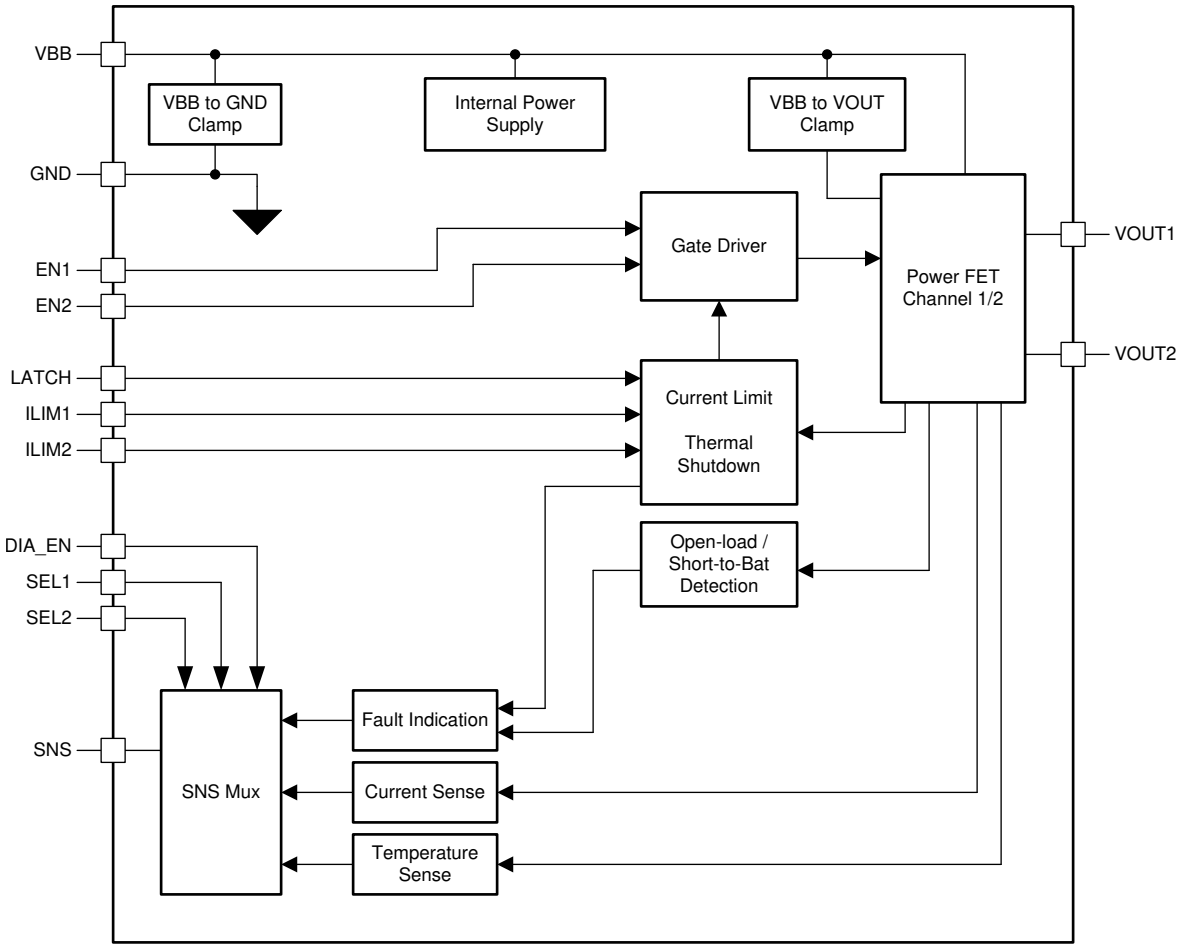

Figure 1-1. Functional Block Diagram

TPS2HB16-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for TPS2HB16-Q1 based on industry-wide used reliability standard:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	22
Die FIT rate	12
Package FIT rate	10

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 750mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17 or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS2HB16-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT open (Hi-Z)	20
VOUT stuck on (VBB)	10
VOUT functional, not in specification – voltage or timing	45
Diagnostics not in specification	10
Protect functions fail to trip	10
Pin to pin short any two pins	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS2HB16-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 and Figure 4-2 shows the TPS2HB16-Q1 pin diagrams. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS2HB16-Q1 datasheet.

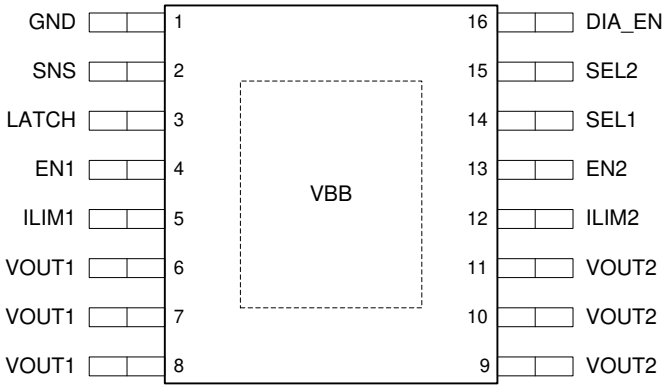

Figure 4-1. Pin Diagram Version A and B

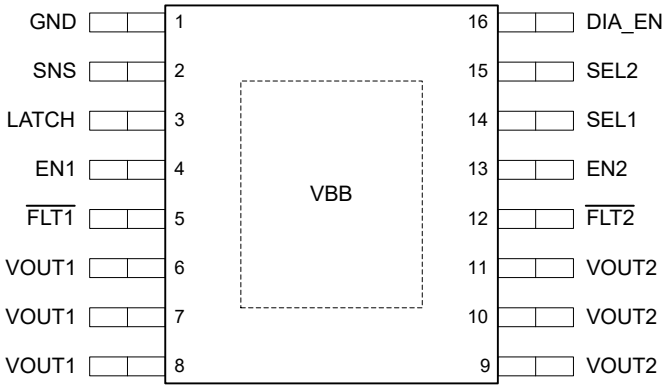

Figure 4-2. Pin Diagram Version F

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Follow the datasheet recommendations for operating conditions, external component selection, and PCB layout

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	1	The resistor or diode network is bypassed if present.	B
SNS	2	The SNS current diagnostic is not available.	B
LATCH	3	The device operates as normal with the device in automatic retry mode.	B
EN1	4	The device operates as normal with channel 1 output off (FET turned off).	B
ILIM1	5	The current limit for channel 1 defaults to the internal limit.	C
$\overline{\text{FLT1}}$	5	For Version F only: The open drain fault diagnostics of channel 1 cannot be reported.	B
VOUT1	6, 7, 8	Short to GND protection engages to protect the device.	B
VOUT2	9, 10, 11	Short to GND protection engages to protect the device.	B
ILIM2	12	The current limit for channel 2 defaults to the internal limit.	C
$\overline{\text{FLT2}}$	12	For Version F only: The open drain fault diagnostics of channel 2 cannot be reported.	B
EN2	13	The device operates as normal with the channel 2 output off (FET turned off).	B
SEL1	14	The device operates as normal with diagnostics corresponding to SEL1 = LOW.	B
SEL2	15	The device operates as normal with diagnostics corresponding to SEL2 = LOW.	B
DIAG_EN	16	The device operates as normal with the diagnostics function disabled.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	1	The output is off with the FET turned off.	B
SNS	2	The SNS current diagnostic is not available.	B
LATCH	3	The device operates as normal with the device in automatic retry mode. The internal pulldown resistor pull the pin to GND.	B
EN1	4	The device operates as normal with the channel 1 output off (FET turned off). The internal pulldown resistor pull the pin to GND.	B
ILIM1	5	The current limit for channel 1 defaults to the internal limit.	C
$\overline{\text{FLT1}}$	5	For Version F only: The open drain fault diagnostics of channel 1 cannot be reported.	B
VOUT1	6, 7, 8	The channel 1 output is off. Open load detection is triggered in off-state while in the diagnostics state.	B
VOUT2	9, 10, 11	The channel 2 output is off. Open load detection is triggered in off-state while in the diagnostics state.	
ILIM2	12	The current limit for channel 2 defaults to the internal limit.	C
$\overline{\text{FLT2}}$	12	For Version F only: The open drain fault diagnostics of channel 2 cannot be reported.	B
EN2	13	The device operates as normal with the channel 2 output off (FET turned off). The internal pulldown resistor pulls the pin to GND.	B
SEL1	14	The device operates as normal with diagnostics corresponding to SEL1 = LOW. The internal pulldown resistor pulls the pin to GND.	B
SEL2	15	The device operates as normal with diagnostics corresponding to SEL2 = LOW. The internal pulldown resistor pulls the pin to GND.	B
DIAG_EN	16	The device operates as normal with the diagnostics function disabled. The internal pulldown resistor pulls the pin to GND.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
GND	1	2 (SNS)	The SNS current diagnostic is not available.	B
SNS	2	3 (LATCH)	The behavior of the device is undefined, and depends on the voltage of the pin. The sense output is potentially incorrect. The latch function is potentially enabled if the pin voltage > VIH. The latch function is potentially disabled if the pin voltage < VIL.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
LATCH	3	4 (EN)	The behavior of the device depends on the voltage of the pin. The latch function is potentially enabled if the pin voltage > VIH. The latch function is potentially disabled if the pin voltage < VIL.	B
EN1	4	5 (ILIM1)	The behavior of the device is undefined. The channel is potentially enabled if the pin voltage > VIH. The channel is potentially disabled if the pin voltage < VIL. The current limit threshold of channel 1 is incorrect.	B
EN1	4	5 ($\overline{\text{FLT1}}$)	For Version F only: The behavior of the device is undefined. The channel is potentially enabled if the pin voltage > VIH. The channel is potentially disabled if the pin voltage < VIL. The open drain fault diagnostics of channel 1 cannot be reported.	B
ILIM1	5	6 (VOUT1)	The behavior of the device is undefined. The current limit threshold (channel 1) is not correct or short circuit or overload protection potentially does not function. The VOUT behavior of channel 1 is potentially incorrect.	B
$\overline{\text{FLT1}}$	5	6 (VOUT1)	For Version F only: The open drain fault diagnostics of channel 1 cannot be reported. The VOUT behavior of channel 1 is potentially incorrect.	B
VOUT1	6, 7, 8	5 (ILIM1)	The behavior of the device is undefined. The current limit threshold (channel 1) is not correct or short circuit or overload protection potentially does not function. The VOUT behavior of channel 1 is potentially incorrect.	A
VOUT1	6, 7, 8	5 ($\overline{\text{FLT1}}$)	For Version F only: The open drain fault diagnostics of channel 1 cannot be reported. The VOUT behavior of channel 1 is potentially incorrect.	B
VOUT2	9, 10, 11	12 (ILIM2)	The behavior of the device is undefined. The current limit threshold (channel 2) is not correct or short circuit or overload protection potentially does not function. The VOUT behavior of channel 2 is potentially incorrect.	A
VOUT2	9, 10, 11	12 ($\overline{\text{FLT2}}$)	For Version F only: The behavior of the device is undefined. The open drain fault diagnostics of channel 1 cannot be reported. The VOUT behavior of channel 2 is potentially incorrect.	B
ILIM2	12	13 (EN2)	The behavior of the device is undefined. The channel is potentially enabled if the pin voltage > VIH. The channel is potentially disabled if the pin voltage < VIL. The current limit threshold of channel 2 is incorrect.	B
$\overline{\text{FLT2}}$	12	13 (EN2)	For Version F only: The behavior of the device is undefined. The channel is potentially enabled if the pin voltage > VIH. The channel is potentially disabled if the pin voltage < VIL. The open drain fault diagnostics of channel 1 cannot be reported.	B
EN2	13	14 (SEL1)	The behavior of the device is undefined. Channel 2 is potentially enabled if the pin voltage > VIH. Channel 2 is potentially disabled if the pin voltage < VIL.	B
SEL1	14	15 (SEL2)	The behavior of the device depends on the voltage of the adjacent pin affecting the diagnostic output.	B
SEL2	15	16 (DIAG_EN)	The behavior of the device depends on the voltage of the adjacent pin affecting the diagnostic output. The diagnostic function is potentially enabled if the pin voltage > VIH. The diagnostic function is potentially disabled if the pin voltage < VIL.	B
DIAG_EN	16	15 (SEL2)	The behavior of the device depends on the voltage of the adjacent pin affecting the diagnostic output. The diagnostic function is potentially enabled if the pin voltage > VIH. The diagnostic function is potentially disabled if the pin voltage < VIL.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	1	The supply power is bypassed, and the device does not turn on.	B
SNS	2	The behavior of the device is undefined; and potentially causes damage to the device due to voltage breakdown on the ESD circuit.	A
LATCH	3	If the voltage of the pin exceeds the voltage range for the pin in the datasheet, the exceedance potentially causes damage to the device due to voltage breakdown on the ESD circuit. The behavior of the device depends on the supply voltage.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
EN1	4	The behavior of the device is undefined. If the voltage of the pin exceeds the voltage range for the pin in the datasheet, the exceedance potentially causes damage to the device due to voltage breakdown on the ESD circuit.	A
ILIM1	5	The device operates as normal, but with channel 1 higher current limit is programmed with an internal reference. There is no damage to the device.	C
$\overline{\text{FLT1}}$	5	For Version F only: The open drain fault diagnostics of channel 1 cannot be reported.	B
VOUT	6, 7, 8, 9, 10, 11	Output 1 is stuck on to supply. Open load detection is triggered in off-state in the diagnostics state.	C
VOUT2	9, 10, 11	Output 2 is stuck on to supply. Open load detection is triggered in off-state in the diagnostics state.	C
ILIM2	12	The device operates as normal, but with channel 2 higher current limit is programmed with an internal reference.	C
$\overline{\text{FLT2}}$	12	For Version F only: The open drain fault diagnostics of channel 2 cannot be reported.	B
EN2	13	The behavior of the device is undefined. If the voltage of the pin exceeds the voltage range for the pin in the datasheet, the exceedance potentially causes damage to the device due to voltage breakdown on the ESD circuit.	A
SEL1	14	The behavior of the device is undefined. If the voltage of the pin exceeds the voltage range for the pin in the datasheet, the exceedance potentially causes damage to the device due to voltage breakdown on the ESD circuit.	A
SEL2	15	The behavior of the device is undefined. If the voltage of the pin exceeds the voltage range for the pin in the datasheet, the exceedance potentially causes damage to the device due to voltage breakdown on the ESD circuit.	A
DIAG_EN	16	The behavior of the device is undefined. If the voltage of the pin exceeds the voltage range for the pin in the datasheet, the exceedance potentially causes damage to the device due to voltage breakdown on the ESD circuit.	A

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from January 11, 2021 to July 13, 2026 (from Revision * (January 2021) to Revision A (July 2026)) **Page**

- Updated document to the latest template and TI branding.....2
- Added information for the *Component Failure Rates per Siemens Norm SN 29500-2* table.....3

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