Functional Safety Information

ADS131M02-Q1
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for the ADS131M02-Q1 (TSSOP package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

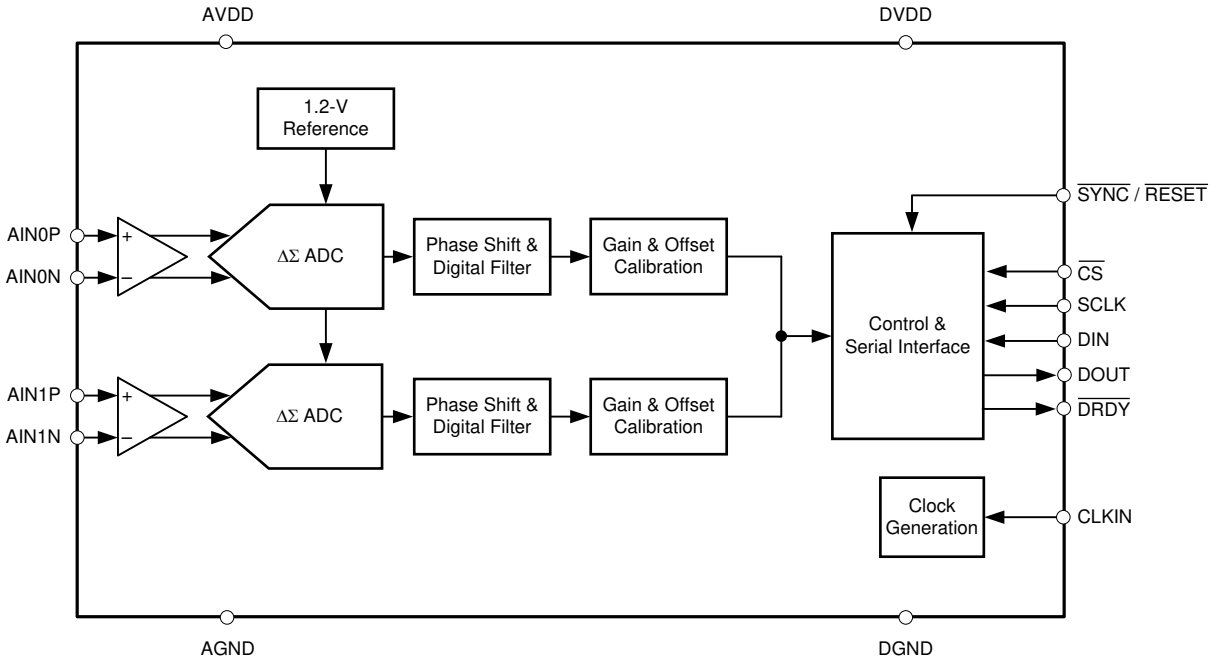

Figure 1-1. Functional Block Diagram

The ADS131M02-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the ADS131M02-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	13
Die FIT rate	2
Package FIT rate	11

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 7.5 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	60 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the ADS131M02-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Incorrect conversion result of an individual ADC(1) (for example, if the ADC output code is at positive or negative full scale, 0 V, undetermined, or otherwise incorrect).	35%
SPI communication error	15%
Register bit error leading to an incorrect device configuration (device behavior depends on which user or internal register bit is affected).	10%
Gain error of an individual ADC out of specification(1)	10%
Offset error of an individual ADC out of specification(1)	5%
Noise of the conversion result of an individual ADC out of specification(1)	5%
INL of an individual ADC out of specification(1)	5%
Gain error, INL, or noise of conversion results of all four ADCs out of specification because of common circuitry (common circuitry includes the internal supplies, voltage reference, bias current generator, and clock).	5%
The ADC output code bit is stuck-at	5%
Device behavior is undetermined	5%

(1) The failure mode percentage provided is for the sum of all four ADCs. For a single ADC, divide the failure mode percentage by 2x.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the ADS131M02-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the ADS131M02-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the ADS131M02-Q1 data sheet.

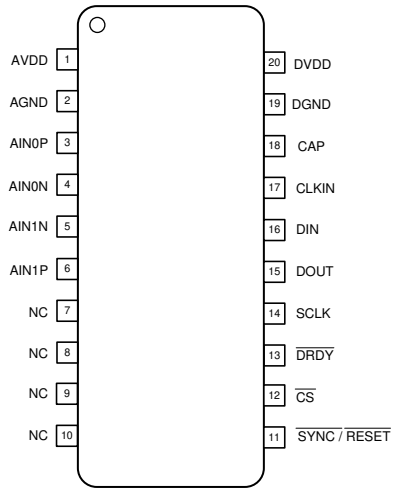

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- AVDD and DVDD use the same 3.3-V supply voltage.
- *Short-circuit to supply* means short AVDD to DVDD.
- *Short-circuit to ground* means short AGND to DGND.
- Differential RC filters on every ADC channel.
  Series resistors are sized to limit the input currents into the analog inputs to <10 mA in all circumstances (for example, if the device is unpowered and an input signal is applied).
- The device is the only peripheral on the SPI bus.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
AVDD	1	The device is unpowered and not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
AGND	2	No effect. Normal operation.	D
AIN0P	3	AIN0P is stuck low. $V_{IN0} = V_{AIN0P} – V_{AIN0N}$ = AGND – V_{AIN0N}. The conversion results of ADC0 are incorrect.	B
AIN0N	4	AIN0N is stuck low. $V_{IN0} = V_{AIN0P} – V_{AIN0N} = V_{AIN0P}$ – AGND. The conversion results of ADC0 are incorrect.	B
AIN1N	5	AIN1N is stuck low. $V_{IN1} = V_{AIN1P} – V_{AIN1N} = V_{AIN1P}$ – AGND. The conversion results of ADC1 are incorrect.	B
AIN1P	6	AIN1P is stuck low. $V_{IN1} = V_{AIN1P} – V_{AIN1N}$ = AGND – V_{AIN1N}. The conversion results of ADC1 are incorrect.	B
NC	7	No effect. Normal operation.	D
NC	8	No effect. Normal operation.	D
NC	9	No effect. Normal operation.	D
NC	10	No effect. Normal operation.	D
$\overline{\text{SYNC/RESET}}$	11	$\overline{\text{SYNC/RESET}}$ is stuck low. The device is held in reset.	B
$\overline{\text{CS}}$	12	$\overline{\text{CS}}$ is stuck low. Normal operation when trying to communicate with the ADS131M02-Q1.	B
$\overline{\text{DRDY}}$	13	$\overline{\text{DRDY}}$ is stuck low. No data-ready indication through the $\overline{\text{DRDY}}$ pin to the host is possible. An increase in supply current occurs when $\overline{\text{DRDY}}$ tries to drive high if the DRDY_HiZ bit = 0b. Device damage is plausible if $\overline{\text{DRDY}}$ drives high for an extended period of time.	A
SCLK	14	SCLK is stuck low. No SPI communication with the device is possible.	B
DOUT	15	DOUT is stuck low. No SPI communication back to the host is possible. An increase in supply current occurs when DOUT tries to drive high. Device damage plausible if DOUT drives high for an extended period of time.	A
DIN	16	DIN is stuck low. No SPI communication with the device is possible.	B
CLKIN	17	CLKIN is stuck low. No clock is provided to the device. The device is not functional, but SPI communication with the device is possible.	B
CAP	18	The device is unpowered and not functional.	B
DGND	19	No effect. Normal operation.	D
DVDD	20	The device is unpowered and not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
AVDD	1	Device functionality is undetermined. The device is unpowered and not functional if all external analog pins are held low. The device can power up through the internal ESD diodes to AVDD if voltages above the device power-on reset threshold are present on any of the analog pins.	B
AGND	2	Device functionality is undetermined. The device can be unpowered or connected to ground internally through an alternate pin ESD diode and power up.	B
AIN0P	3	The state of the AIN0P input is undetermined. The conversion results of ADC0 are undetermined.	B
AIN0N	4	The state of the AIN0N input is undetermined. The conversion results of ADC0 are undetermined.	B
AIN1N	5	The state of the AIN1N input is undetermined. The conversion results of ADC1 are undetermined.	B
AIN1P	6	The state of the AIN1P input is undetermined. The conversion results of ADC1 are undetermined.	B
NC	7	No effect. Normal operation.	D
NC	8	No effect. Normal operation.	D
NC	9	No effect. Normal operation.	D
NC	10	No effect. Normal operation.	D
$\overline{\text{SYNC/RESET}}$	11	The state of the $\overline{\text{SYNC/RESET}}$ input is undetermined. Device functionality is undetermined. The device can operate normally or be held in reset.	B
$\overline{\text{CS}}$	12	The state of the $\overline{\text{CS}}$ input is undetermined. SPI communication is corrupted.	B
$\overline{\text{DRDY}}$	13	The state of the $\overline{\text{DRDY}}$ output is undetermined. No data-ready indication through the $\overline{\text{DRDY}}$ pin to the host is possible.	B
SCLK	14	The state of the SCLK input is undetermined. No SPI communication with the device is possible.	B
DOUT	15	The state of the DOUT output is undetermined. No SPI communication back to the host is possible.	B
DIN	16	The state of the DIN input is undetermined. No SPI communication with the device is possible.	B
CLKIN	17	The state of the CLKIN input is undetermined. No clock is provided to the device. The device is not functional, but SPI communication with the device is possible.	B
CAP	18	The internal digital LDO is unstable. Device functionality is undetermined.	B
DGND	19	Device functionality is undetermined. The device can be unpowered or connected to ground internally through an alternate pin ESD diode and power up.	B
DVDD	20	Device functionality is undetermined. The device is unpowered and not functional if all external digital pins are held low. The device can power up through the internal ESD diodes to DVDD if voltages above the device power-on reset threshold are present on any of the digital pins.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
AVDD	1	AGND	The device is unpowered and not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
AGND	2	AIN0P	AIN0P is stuck low. $V_{IN0} = V_{AIN0P} – V_{AIN0N} = AGND – V_{AIN0N}$. The conversion results of ADC0 are incorrect.	B
AIN0P	3	AIN0N	$V_{IN0} = V_{AIN0P} – V_{AIN0N} = 0$ V. The conversion results of ADC0 are approximately 0 V.	B
AIN0N	4	AIN1N	The conversion results of ADC0 and ADC1 are undetermined.	B
AIN1N	5	AIN1P	$V_{IN1} = V_{AIN1P} – V_{AIN1N} = 0$ V. The conversion results of ADC1 are approximately 0 V.	B
AIN1P	6	NC	No effect. Normal operation.	D
NC	7	NC	No effect. Normal operation.	D
NC	8	NC	No effect. Normal operation.	D
NC	9	NC	No effect. Normal operation.	D
NC	10	$\overline{\text{SYNC}}/\overline{\text{RESET}}$	Not considered. Corner pin.	D
$\overline{\text{SYNC}}/\overline{\text{RESET}}$	11	$\overline{\text{CS}}$	The device behavior is dependent on the drive strength of the control signals driving the $\overline{\text{CS}}$ and $\overline{\text{SYNC}}/\overline{\text{RESET}}$ pins. If the $\overline{\text{SYNC}}/\overline{\text{RESET}}$ control signal can overdrive the $\overline{\text{CS}}$ control signal, then $\overline{\text{CS}}$ is stuck high or SPI communication is corrupted. No SPI communication with the device is possible. If the $\overline{\text{CS}}$ control signal can overdrive the $\overline{\text{SYNC}}/\overline{\text{RESET}}$ control signal, then the device synchronizes conversions every time $\overline{\text{CS}}$ transitions high. Conversion results are valid, but data ready is indicated outside the expected time window. If the $\overline{\text{SYNC}}/\overline{\text{RESET}}$ pin is held low for longer than the reset time period, a device reset occurs.	B
$\overline{\text{CS}}$	12	$\overline{\text{DRDY}}$	SPI communication is corrupted. No SPI communication with the device is possible. An increase in supply current is possible when $\overline{\text{DRDY}}$ tries to drive low when $\overline{\text{CS}}$ is driven high and vice versa. Device damage plausible if this condition exists for an extended period of time.	A
$\overline{\text{DRDY}}$	13	SCLK	SPI communication is corrupted. No SPI communication with the device is possible. An increase in supply current is possible when $\overline{\text{DRDY}}$ tries to drive low when SCLK is driven high and vice versa. Device damage plausible if this condition exists for an extended period of time.	A
SCLK	14	DOUT	SPI communication is corrupted. No SPI communication with the device is possible. An increase in supply current is possible when DOUT tries to drive low when SCLK is driven high and vice versa. Device damage plausible if this condition exists for an extended period of time.	A
DOUT	15	DIN	SPI communication is corrupted. No SPI communication with the device is possible. An increase in supply current is possible when DOUT tries to drive low when DIN is driven high and vice versa. Device damage plausible if this condition exists for an extended period of time.	A
DIN	16	CLKIN	SPI communication is corrupted. No SPI communication with the device is possible. The CLKIN signal is corrupted. Device behavior is undetermined.	B
CLKIN	17	CAP	Device behavior is undetermined. Device damage is plausible when the CLKIN pin drives the digital core LDO output on the CAP pin to >1.8 V.	A
CAP	18	DGND	The device is unpowered and not functional.	B
DGND	19	DVDD	The device is unpowered and not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
DVDD	20	AVDD	Not considered. Corner pin.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
AVDD	1	No effect. Normal operation.	D
AGND	2	The device is unpowered and not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
AIN0P	3	AIN0P is stuck high. $V_{IN0} = V_{AIN0P} – V_{AIN0N} = AVDD – V_{AIN0N}$. The conversion results of ADC0 are incorrect.	B
AIN0N	4	AIN0N is stuck high. $V_{IN0} = V_{AIN0P} – V_{AIN0N} = V_{AIN0P} – AVDD$. The conversion results of ADC0 are incorrect.	B
AIN1N	5	AIN1N is stuck high. $V_{IN1} = V_{AIN1P} – V_{AIN1N} = V_{AIN1P} – AVDD$. The conversion results of ADC1 are incorrect.	B
AIN1P	6	AIN1P is stuck high. $V_{IN1} = V_{AIN1P} – V_{AIN1N} = AVDD – V_{AIN1N}$. The conversion results of ADC1 are incorrect.	B
NC	7	No effect. Normal operation.	D
NC	8	No effect. Normal operation.	D
NC	9	No effect. Normal operation.	D
NC	10	No effect. Normal operation.	D
$\overline{\text{SYNC/RESET}}$	11	No effect. Normal operation. The device cannot be reset or synchronized using the $\overline{\text{SYNC/RESET}}$ pin anymore.	B
$\overline{\text{CS}}$	12	$\overline{\text{CS}}$ is stuck high. No SPI communication with the device is possible.	B
$\overline{\text{DRDY}}$	13	$\overline{\text{DRDY}}$ is stuck high. No data-ready indication through the $\overline{\text{DRDY}}$ pin to the host is possible. An increase in supply current occurs when $\overline{\text{DRDY}}$ tries to drive low. Device damage plausible if $\overline{\text{DRDY}}$ drives low for an extended period of time.	A
SCLK	14	SCLK is stuck high. No SPI communication with the device is possible.	B
DOUT	15	DOUT is stuck high. No SPI communication back to the host is possible. An increase in supply current occurs when DOUT tries to drive low. Device damage plausible if DOUT drives low for an extended period of time.	A
DIN	16	DIN is stuck high. No SPI communication with the device is possible.	B
CLKIN	17	CLKIN is stuck high. No clock is provided to the device. The device is not functional, but SPI communication with the device is possible.	B
CAP	18	The device may operate normally, but permanent device damage within a short period of time is very plausible. The device is not functional anymore in case of damage.	A
DGND	19	The device is unpowered and not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
DVDD	20	No effect. Normal operation.	D

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