Functional Safety Information

TPS61381-Q1, TPS61382-Q1, TPS61383-Q1, and TPS61382A-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the TPS61381-Q1, TPS61382-Q1, TPS61383-Q1, and TPS61382A-Q1 (WQFN-RAV package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 and Figure 1-2 show the device functional block diagrams for reference.

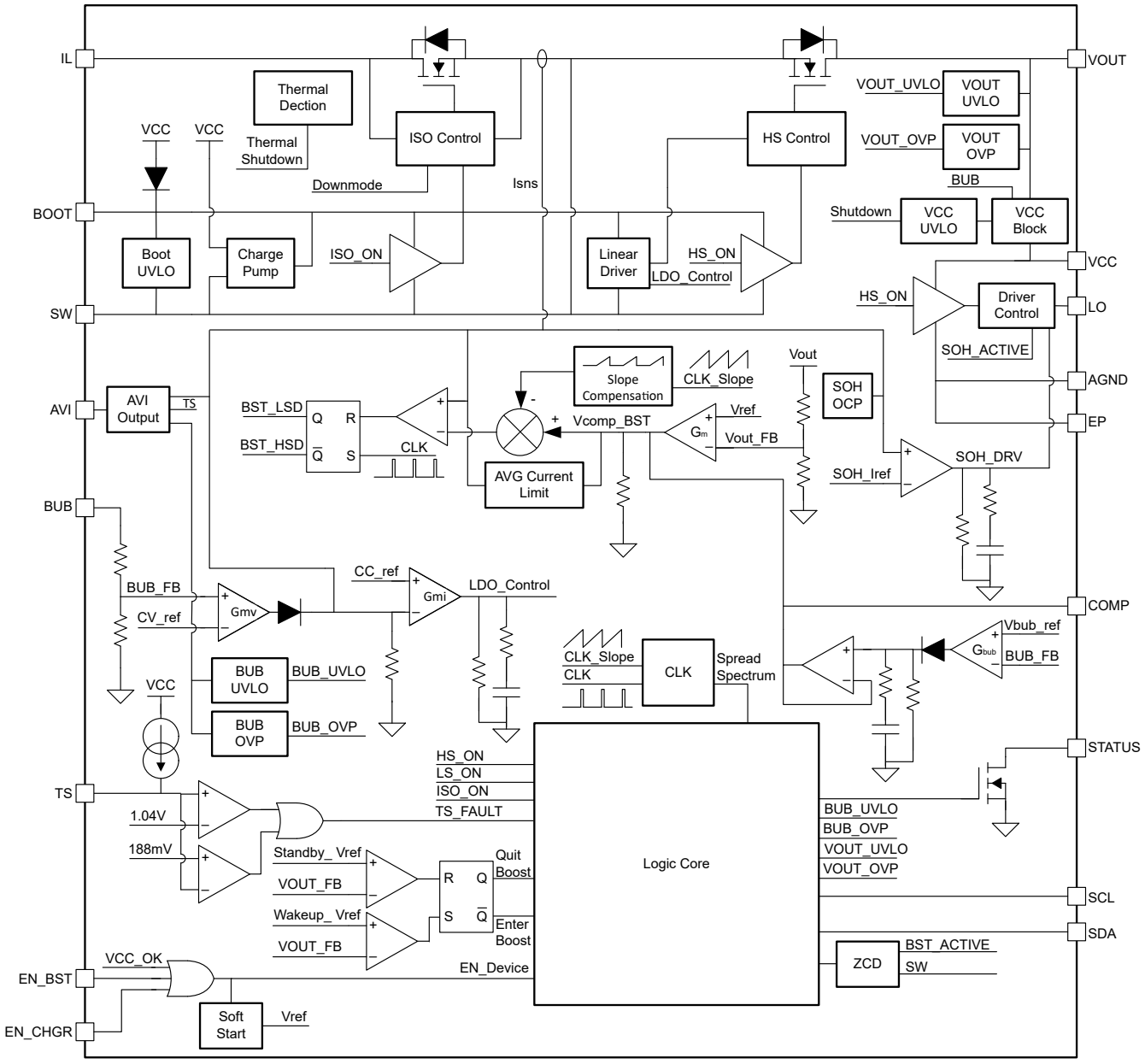

Figure 1-1. TPS61381-Q1 Functional Block Diagram

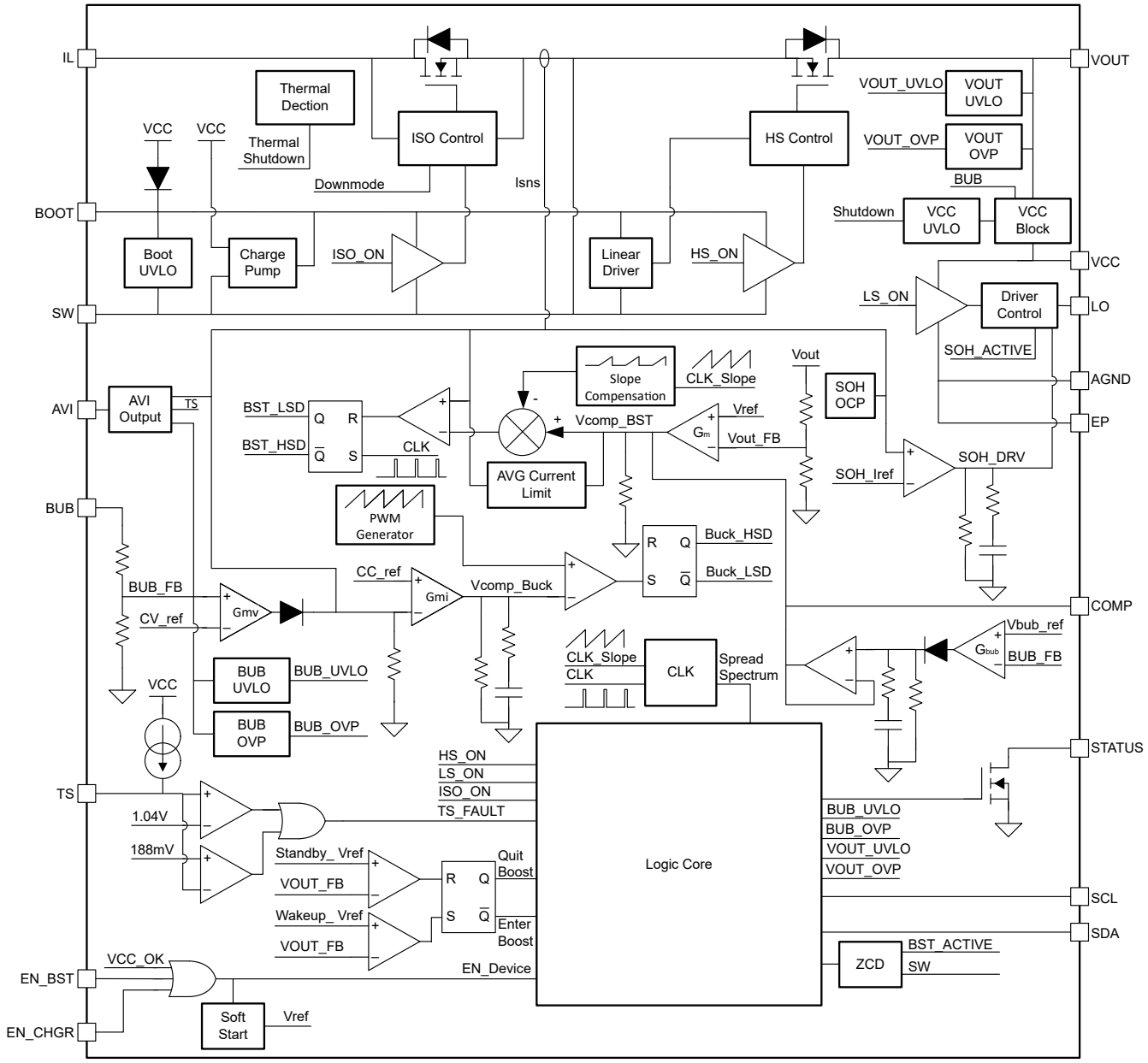

Figure 1-2. TPS61382-Q1, TPS61383-Q1 and TPS61382A-Q1 Functional Block Diagram

The TPS61381-Q1, TPS61382-Q1, TPS61383-Q1, and TPS61382A-Q1 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TPS61381-Q1, TPS61382-Q1, TPS61383-Q1, and TPS61382A-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	11
Die FIT rate	3
Package FIT rate	8

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 1500mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	60 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS61381-Q1, TPS61382-Q1, TPS61383-Q1, and TPS61382A-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VO not in specification voltage or timing	30.56
VO no output GND or Hi-Z	1.62
Software FETs stuck on	3.26
EN enable fails or false enable	13.54
Short circuit any two pins	51.03

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS61381-Q1, TPS61382-Q1, TPS61383-Q1, and TPS61382A-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TPS61381-Q1, TPS61382-Q1, TPS61383-Q1, and TPS61382A-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS61381-Q1, TPS61382-Q1, TPS61383-Q1, and TPS61382A-Q1 datasheets.

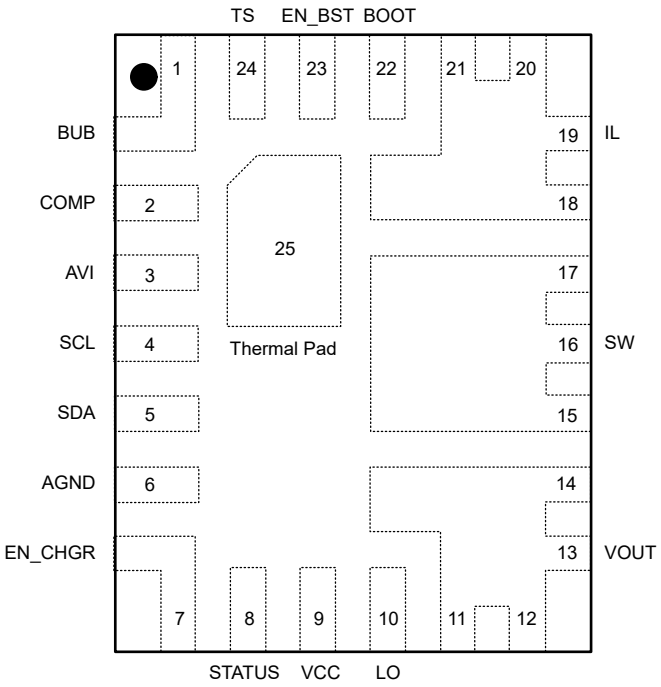

Figure 4-1. TPS61381-Q1, TPS61382-Q1, TPS61383-Q1, and TPS61382A-Q1 Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device is operated within the *Recommended Operating Conditions* and the *Absolute Maximum Ratings* in the TPS61381-Q1, TPS61382-Q1, TPS61383-Q1, and TPS61382A-Q1 datasheets.
- The device is configured as shown in the *Application and Implementation* section in the TPS61381-Q1, TPS61382-Q1, TPS61383-Q1, and TPS61382A-Q1 datasheets.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
BUB	1	The device stays in UVLO lockout.	B
COMP	2	Loop cannot regulate in boost mode. The VOUT pin drops below target.	B
AVI	3	There is no output signal for battery state-of-health (SOH) mode. The output of AVI pin is programmable by I2C interface. The device is damaged if the output of the AVI pin is programmed to *BUB voltage* and the output ratio is programmed to *ratio = 1*.	A
SCL	4	The device fails to connect the I2C registers.	B
SDA	5	The device fails to connect the I2C registers.	B
AGND	6	The layout parasitic inductance changes. Noise couples into the internal circuits.	C
EN_CHGR	7	The functions of the charger and SOH cannot be enabled.	B
STATUS	8	There is no STATUS indicator function.	B
VCC	9	The internal power supply of the device cannot be established. The device cannot operate.	B
LO	10	There is damage to the low-side driver.	A
VOUT	11	The device is damaged if the BST_SCP function of the I2C is not enabled.	A
VOUT	12	The device is damaged if the BST_SCP function of the I2C is not enabled.	A
VOUT	13	The device is damaged if the BST_SCP function of the I2C is not enabled.	A
VOUT	14	The device is damaged if the BST_SCP function of the I2C is not enabled.	A
SW	15	There is damage to the device.	A
SW	16	There is damage to the device.	A
SW	17	There is damage to the device.	A
IL	18	There is damage to the device.	A
IL	19	There is damage to the device.	A
IL	20	There is damage to the device.	A
IL	21	There is damage to the device.	A
BOOT	22	There is damage to the device.	A
EN_BST	23	The boost function cannot be enabled.	B
TS	24	TS_FAULT logic triggers, the device stops charging.	B
EP	25	The layout parasitic inductance changes. Noise couples into the internal circuits.	C

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
BUB	1	There is no output voltage in boost mode.	B
COMP	2	The boost output is unstable.	B
AVI	3	There is no output signal for SOH mode.	A
SCL	4	The device fails to connect the I2C registers.	B
SDA	5	The device fails to connect the I2C registers.	B
AGND	6	The layout parasitic inductance changes. Noise couples into the internal circuits.	C
EN_CHGR	7	The functions of the charger and SOH cannot be enabled.	B
STATUS	8	There is no STATUS indicator function.	B
VCC	9	The capacitance of the VCC pin is not enough. The VCC pin cannot support a heavy load.	B
LO	10	There is damage to the device.	A
VOUT	11	There is damage to the device.	A
VOUT	12	There is damage to the device.	A
VOUT	13	There is damage to the device.	A
VOUT	14	There is damage to the device.	A
SW	15	There is damage to the device.	A
SW	16	There is damage to the device.	A
SW	17	There is damage to the device.	A
IL	18	There is damage to the device.	A
IL	19	There is damage to the device.	A
IL	20	There is damage to the device.	A
IL	21	There is damage to the device.	A
BOOT	22	The VOUT pin is out of regulation.	A
EN_BST	23	The boost function cannot be enabled.	B
TS	24	There is no temperature sense function. The charger and SOH report a FAULT for the TS pin.	B
EP	25	The layout parasitic inductance changes. Noise couples into the internal circuits.	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
BUB	1	TS	There is damage to the device when BUB > 6V.	A
COMP	2	BUB	There is damage to the device when BUB > 6V.	A
AVI	3	COMP	The output voltage is out of regulation.	B
SCL	4	AVI	The device fails to connect the I2C registers.	B
SDA	5	SCL	The device fails to connect the I2C registers.	B
AGND	6	SDA	The device fails to connect the I2C registers.	B
EN_CHGR	7	AGND	The functions of the charger and SOH cannot be enabled.	B
STATUS	8	EN_CHGR	The charger can turn off abnormally.	B
VCC	9	STATUS	There is an increase in VOUT leakage.	B
LO	10	VCC	The boost leg is shooting through.	A
VOUT	11-14	LO	There is damage to the driver.	A
SW	15-17	VOUT	There is damage to the driver.	A
IL	18-21	SW	There is damage to the driver.	A
BOOT	22	IL	There is damage to the driver.	A
EN_BST	23	BOOT	There is damage to the driver.	A
TS	24	EN_BST	The TS_FAULT logic triggers, the device stops charging.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
EP	25	COMP	The device does not operate. The VCC pin is short.	B
EP	25	BUB	There is no output voltage in boost mode.	B
EP	25	AVI	There is no output signal for SOH mode. The device is damaged if the output of the AVI pin is programmed to *BUB voltage* and the output ratio is programmed to *ratio = 1*.	A
EP	25	SCL	The device fails to connect the I2C registers.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
BUB	1	There is damage to the device when the supply voltage is > 15V.	A
COMP	2	There is damage to the device when the supply voltage is > 6V.	A
AVI	3	There is damage to the device when the supply voltage is > 6V.	A
SCL	4	There is damage to the device when supply voltage > 6V.	B
SDA	5	There is damage to the device when the supply voltage is > 6V.	B
AGND	6	The device does not operate. The power supply is short.	C
EN_CHGR	7	There is damage to the device when the supply voltage is > 15V.	B
STATUS	8	There is damage to the device when the supply voltage is > 15V.	B
VCC	9	There is damage to the device when the supply voltage is > 6V.	B
LO	10	There is damage to the device when the supply voltage is > 6V.	A
VOUT	11	There is reverse current into the power supply in boost mode. There is no effect on the function of the device.	A
VOUT	12	There is reverse current into the power supply in boost mode. There is no effect on the function of the device.	A
VOUT	13	There is reverse current into the power supply in boost mode. There is no effect on the function of the device.	A
VOUT	14	There is reverse current into the power supply in boost mode. There is no effect on the function of the device.	A
SW	15	There is damage to the device.	A
SW	16	There is damage to the device.	A
SW	17	There is damage to the device.	A
IL	18	There is damage to the device.	A
IL	19	There is damage to the device.	A
IL	20	There is damage to the device.	A
IL	21	There is damage to the device.	A
BOOT	22	There is damage to the device when the supply voltage is > 6V in standby mode.	A
EN_BST	23	There is damage to the device when the supply voltage is > 15V.	B
TS	24	There is damage to the device when the supply voltage is > 6V.	B
EP	25	The device does not operate. The power supply is short.	C

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2025	*	Initial Release

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