Functional Safety Information

ISO6441
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for the ISO6441 (DW-16 Wide-SOIC, DFP-16 Wide-SSOP, and DBQ-16 SSOP packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

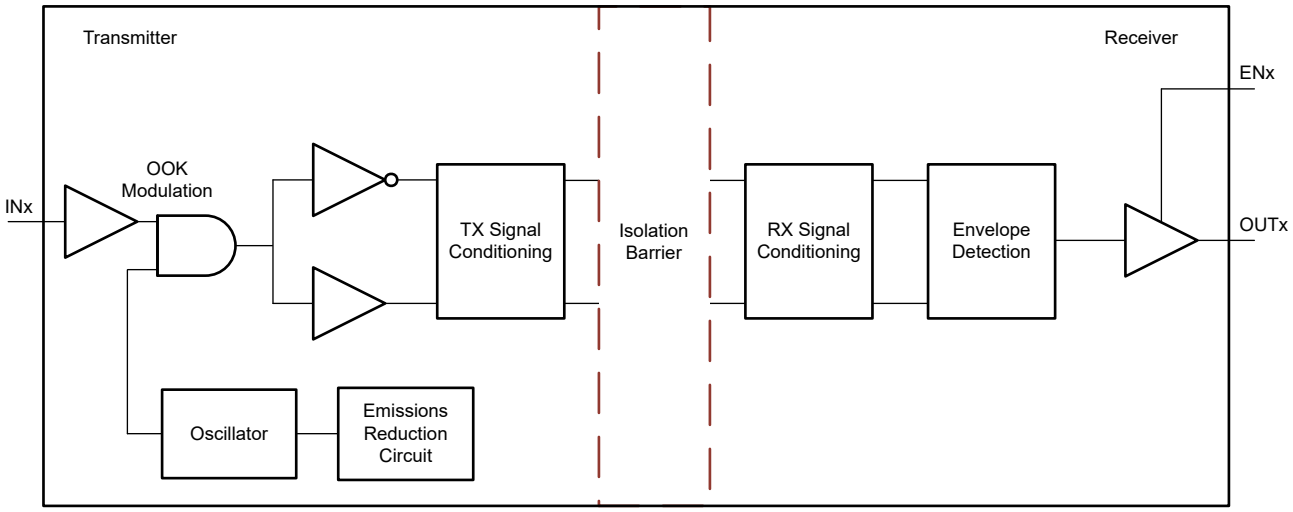

Figure 1-1. Functional Block Diagram

The ISO6441 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

ADVANCE INFORMATION for preproduction products; subject to change without notice.

2 Functional Safety Failure In Time (FIT) Rates

2.1 DW-16 Wide-SOIC Package

This section provides functional safety failure in time (FIT) rates for the DW-16 Wide-SOIC package of the ISO6441 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	38
Die FIT rate	4
Package FIT rate	34

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 262.2mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): From table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 DFP-16 Wide-SSOP Package

This section provides functional safety failure in time (FIT) rates for the DFP-16 Wide-SSOP package of the ISO6441 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	19
Die FIT rate	4
Package FIT rate	15

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 262.2mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): From table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.3 DBQ-16 SSOP Package

This section provides functional safety failure in time (FIT) rates for the DBQ-16 SSOP package of the ISO6441 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-5. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	13
Die FIT rate	4
Package FIT rate	9

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 262.2mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): From table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-6. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the ISO6441 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUTx state is undetermined	23
OUTx is stuck to default state	36
OUTx is stuck to non-default state	11
OUTx is not in timing or voltage specification	12
OUTx is stuck high	9
OUTx is stuck low	9

The FMD in the *Die Failure Modes and Distribution* table excludes short-circuit faults across the isolation barrier. Faults for short circuits across the isolation barrier can be excluded according to IEC 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a safety-separated extra low voltage (SELV) or protective extra low voltage (PELV) power supply is used, pollution degree 2 / OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the ISO6441 (DW-16 Wide-SOIC, DFP-16 Wide-SSOP, and DBQ-16 SSOP packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios, see Table 4-2 :

- Pin short-circuited to ground
- Pin open-circuited
- Pin short-circuited to an adjacent pin
- Pin short-circuited to supply

Table 4-2 also indicates how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- For short-to-ground analysis, the ground referenced for the short is the ground on that side of the isolation barrier.
- For short-to-supply analysis, the supply referenced for the short is the supply on that side of the isolation barrier.
- The default output levels for the outputs of OUTx are:
  - High for: ISO6441
  - Low for: ISO6441F

4.1 DW-16 Wide-SOIC, DFP-16 Wide-SSOP, and DBQ-16 SSOP Packages

Figure 4-1 shows the ISO6441 pin diagram for the DW-16 Wide-SOIC, DFP-16 Wide-SSOP, and DBQ-16 SSOP packages. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the ISO6441 datasheet.

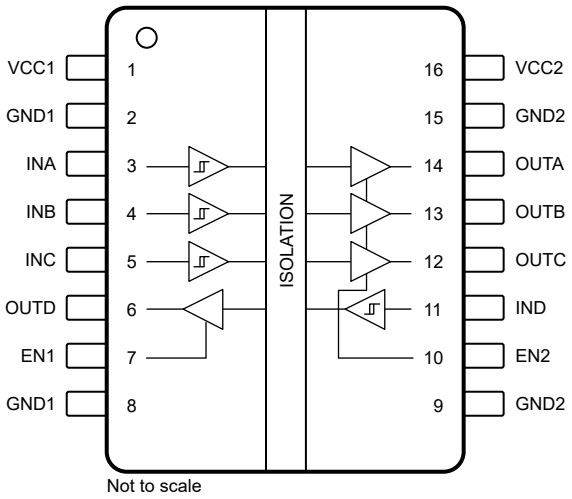

Figure 4-1. Pin Diagram (DW-16 Wide-SOIC, DFP-16 Wide-SSOP, and DBQ-16 SSOP Packages)

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground, Open-Circuited, Short-Circuited to Adjacent Pin, and Short-Circuited to Supply

Pin Name	Pin Number	Potential Failure Mode	Description of Potential Failure Effects	Failure Effect Class
VCC1	1	Short-Circuited to Ground (Side-1)	The device has no power on side-1 (the supply input is shorted to ground). The outputs of OUTA, OUTB, and OUTC are at the default logic state. The output state of OUTD is undetermined. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, damage to the device is possible. This short circuit potentially causes high current to flow between the two GND1 pins (pin2 and pin8); potentially damaging the device.	A
VCC1	1	Open-Circuited	The device has no power on side-1 (the supply input is open). The outputs of OUTA, OUTB, and OUTC are at the default logic state. The output state of OUTD is undetermined. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, damage to the device is possible.	A
VCC1	1	Short-Circuited to Pin2 (GND1)	The device has no power on side-1 (the supply input is shorted to ground). The outputs of OUTA, OUTB, and OUTC are at the default logic state. The output state of OUTD is undetermined. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, damage to the device is possible. This short circuit potentially causes high current to flow between the two GND1 pins (pin2 and pin8); potentially damaging the device.	A
VCC1	1	Short-Circuited to Supply (Side-1)	The device continues to function as expected. Normal operation.	D
GND1	2	Short-Circuited to Ground (Side-1)	The device continues to function as expected. Normal operation.	D
GND1	2	Open-Circuited	The device receives return ground through pin 8 (GND1). Normal operation.	D
GND1	2	Short-Circuited to Pin3 (INA)	The input signal is shorted to ground, so the output of OUTA is stuck low. Communication through channel A is corrupted.	B
GND1	2	Short-Circuited to Supply (Side-1)	The device has no power on side-1 (the supply input is shorted to ground). The outputs of OUTA, OUTB, and OUTC are at the default logic state. The output state of OUTD is undetermined. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, damage to the device is possible. This short circuit potentially causes high current to flow between the two GND1 pins (pin2 and pin8); potentially damaging device.	A
INA	3	Short-Circuited to Ground (Side-1)	The input signal is shorted to ground, so the output of OUTA is stuck low. Communication through channel A is corrupted.	B
INA	3	Open-Circuited	Communication through channel A is not possible. The output of OUTA is at the default state (weak internal pullup or pulldown to the default state).	B
INA	3	Short-Circuited to Pin4 (INB)	Communication is corrupted for either channel or both channels.	B
INA	3	Short-Circuited to Supply (Side-1)	The input signal is shorted to supply, so the output of OUTA is stuck high. Communication through channel A is corrupted.	B
INB	4	Short-Circuited to Ground (Side-1)	The input signal is shorted to ground, so the output of OUTB is stuck low. Communication through channel B is corrupted.	B
INB	4	Open-Circuited	Communication through channel B is not possible. The output of OUTB is at the default state (weak internal pullup or pulldown to the default state).	B
INB	4	Short-Circuited to Pin5 (INC)	Communication is corrupted for either or both channels.	B
INB	4	Short-Circuited to Supply (Side-1)	The input signal is shorted to supply, so the output of OUTB is stuck high. Communication through channel B is corrupted.	B
INC	5	Short-Circuited to Ground (Side-1)	The input signal is shorted to ground, so the output of OUTC is stuck low. Communication through channel C is corrupted.	B
INC	5	Open-Circuited	Communication through channel C is not possible. The output of OUTC is at the default state (weak internal pullup or pulldown to the default state).	B

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground, Open-Circuited, Short-Circuited to Adjacent Pin, and Short-Circuited to Supply (continued)

Pin Name	Pin Number	Potential Failure Mode	Description of Potential Failure Effects	Failure Effect Class
INC	5	Short-Circuited to Pin6 (OUTD)	Communication is corrupted for either channel or both channels. With an opposite logic state on both channels, high current can flow between the signals on INC, supply, and ground in OUTD and possibly cause damage to the device.	A
INC	5	Short-Circuited to Supply (Side-1)	The input signal is shorted to supply, so the output of OUTC is stuck high. Communication through channel C is corrupted.	B
OUTD	6	Short-Circuited to Ground (Side-1)	The output of OUTD is shorted to ground. Communication through channel D is corrupted. Damage to the device is possible if IND is driven high for an extended period of time.	A
OUTD	6	Open-Circuited	The output state of OUTD is undetermined. Communication through channel D is corrupted.	B
OUTD	6	Short-Circuited to Pin7 (EN1)	Data communication is corrupted on OUTD. If EN1 is pulled to the supply externally, damage to the device is possible when OUTD is driven low for an extended duration.	A
OUTD	6	Short-Circuited to Supply (Side-1)	OUTD is stuck high. Communication through channel D is corrupted. Damage to the device is possible if IND is driven low for an extended period of time.	A
EN1	7	Short-Circuited to Ground (Side-1)	EN1 is stuck low, so the output buffer for OUTD is not enabled. Communication is corrupted for channel D.	B
EN1	7	Open-Circuited	Control on the input of EN1 is lost. EN1 has a weak internal pullup to VCC1. Communication on channel D continues normally since the weak internal pullup to VCC1 on EN1 enables the output buffer for OUTD.	B
EN1	7	Short-Circuited to Pin8 (GND1)	EN1 is stuck low, so the output buffer for OUTD is not enabled. Communication is corrupted for channel D.	B
EN1	7	Short-Circuited to Supply (Side-1)	Control on the input of EN1 is lost since EN1 is shorted to a logic high. Communication on channel D continues normally since the high on EN1 enables the output buffer for OUTD.	B
GND1	8	Short-Circuited to Ground (Side-1)	The device continues to function as expected. Normal operation.	D
GND1	8	Open-Circuited	The device receives return ground through pin 2 (GND1). Normal operation.	D
GND1	8	Short-Circuited to Pin9 (N/A)	Not applicable (N/A), corner pin.	N/A
GND1	8	Short-Circuited to Supply (Side-1)	The device has no power on side-1 (the supply input is shorted to ground). The outputs of OUTA, OUTB, and OUTC are at the default logic state. The output state of OUTD is undetermined. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, damage to the device is possible. This short circuit potentially causes high current to flow between the two GND1 pins (pin2 and pin8); potentially damaging device.	A
GND2	9	Short-Circuited to Ground (Side-2)	The device continues to function as expected. Normal operation.	D
GND2	9	Open-Circuited	The device receives return ground through pin 15 (GND2). Normal operation.	D
GND2	9	Short-Circuited to Pin10 (EN2)	EN2 is stuck low, so the output buffers for OUTA, OUTB, and OUTC are not enabled. Communication is corrupted for channels A, B, and C.	B
GND2	9	Short-Circuited to Supply (Side-2)	The device has no power on side-2 (the supply input is shorted to ground). The output of OUTD is at the default logic state. The output states of OUTA, OUTB, and OUTC are undetermined. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, damage to the device is possible. This short circuit potentially causes high current to flow between the two GND2 pins (pin9 and pin15); potentially damaging the device.	A
EN2	10	Short-Circuited to Ground (Side-2)	EN2 is stuck low so the output buffers for OUTA, OUTB, and OUTC are not enabled. Communication is corrupted for channels A, B, and C.	B

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground, Open-Circuited, Short-Circuited to Adjacent Pin, and Short-Circuited to Supply (continued)

Pin Name	Pin Number	Potential Failure Mode	Description of Potential Failure Effects	Failure Effect Class
EN2	10	Open-Circuited	Control on the input of EN2 is lost. EN2 has a weak internal pullup to VCC2. Communication on channels A, B, and C continues normally since the weak internal pullup to VCC2 on EN2 enables the output buffers for OUTA, OUTB, and OUTC.	B
EN2	10	Short-Circuited to Pin11 (IND)	Communication is corrupted on all channels. The shorted external signals to EN2 and IND result in an unpredictable and non-deterministic level at the EN2 and IND inputs when the input level to EN2 and the input level to IND do not match. Thus, the enable status of the output buffers from EN2, which impacts channels A, B, and C, is unknown, as are the levels of OUTA, OUTB, and OUTC. The input level to IND is unknown, as is the output on OUTD.	B
EN2	10	Short-Circuited to Supply (Side-2)	Control on the input of EN2 is lost since EN2 is shorted to a logic high. Communication from the on channels A, B and C continues normally since the high on EN2 enables the output buffers for OUTA, OUTB, and OUTC.	B
IND	11	Short-Circuited to Ground (Side-2)	The input signal is shorted to ground, so the output of OUTD is stuck low. Communication through channel D is corrupted.	B
IND	11	Open-Circuited	Communication through channel D is not possible. The output of OUTD is at the default state (weak internal pullup or pulldown to the default state).	B
IND	11	Short-Circuited to Pin12 (OUTC)	Communication is corrupted for either channel or both channels. With an opposite logic state on both channels, high current can flow between the signals provided to the IND, supply, and ground through OUTC and possibly cause damage to the device.	A
IND	11	Short-Circuited to Supply (Side-2)	The input signal is shorted to supply, so the output of OUTD is stuck high. Communication through channel D is corrupted.	B
OUTC	12	Short-Circuited to Ground (Side-2)	The output of OUTC is shorted to ground. Communication through channel C is corrupted. Damage to the device is possible if INC is driven high for an extended period of time.	A
OUTC	12	Open-Circuited	The state of the OUTC output is undetermined. Communication through channel C is corrupted.	B
OUTC	12	Short-Circuited to Pin13 (OUTB)	Communication is corrupted for either channel or both channels. With an opposite logic state on both channels, high current can flow between the pins, supply, and ground and possibly cause damage to the device.	A
OUTC	12	Short-Circuited to Supply (Side-2)	The output of OUTC is stuck high. Communication through channel C is corrupted. Device damage is possible if INC is driven low for an extended period of time.	A
OUTB	13	Short-Circuited to Ground (Side-2)	The output of OUTB is shorted to ground. Communication through channel B is corrupted. Damage to the device is possible if INB is driven high for an extended period of time.	A
OUTB	13	Open-Circuited	The state of the OUTB output is undetermined. Communication through channel B is corrupted.	B
OUTB	13	Short-Circuited to Pin14 (OUTA)	Communication is corrupted for either channel or both channels. With an opposite logic state on both channels, high current can flow between the pins, supply, and ground and possibly cause damage to the device.	A
OUTB	13	Short-Circuited to Supply (Side-2)	The output of OUTB is stuck high. Communication through channel B is corrupted. Device damage is possible if INB is driven low for an extended period of time.	A
OUTA	14	Short-Circuited to Ground (Side-2)	The output of OUTA is shorted to ground. Communication through channel A is corrupted. Damage to the device is possible if INA is driven high for an extended period of time.	A
OUTA	14	Open-Circuited	The state of the OUTA output is undetermined. Communication through channel A is corrupted.	B
OUTA	14	Short-Circuited to Pin15 (GND2)	The output of OUTA is shorted to ground. Communication through channel A is corrupted. Damage to the device is possible if INA is driven high for an extended period of time.	A
OUTA	14	Short-Circuited to Supply (Side-2)	The output of OUTA is stuck high. Communication through channel A is corrupted. Device damage is possible if INA is driven low for an extended period of time.	A

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground, Open-Circuited, Short-Circuited to Adjacent Pin, and Short-Circuited to Supply (continued)

Pin Name	Pin Number	Potential Failure Mode	Description of Potential Failure Effects	Failure Effect Class
GND2	15	Short-Circuited to Ground (Side-2)	The device continues to function as expected. Normal operation.	D
GND2	15	Open-Circuited	The device receives return ground through pin 9 (GND2). Normal operation.	D
GND2	15	Short-Circuited to Pin16 (VCC2)	The device has no power on side-2 (the supply input is shorted to ground). The output of OUTD is at the default logic state. The output states of OUTA, OUTB, and OUTC are undetermined. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, damage to the device is possible. This short circuit potentially causes high current to flow between the two GND2 pins (pin9 and pin15); potentially damaging the device.	A
GND2	15	Short-Circuited to Supply (Side-2)	The device has no power on side-2 (the supply input is shorted to ground). The output of OUTD is at the default logic state. The output states of OUTA, OUTB, and OUTC are undetermined. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, damage to the device is possible. This short circuit potentially causes high current to flow between the two GND2 pins (pin9 and pin15); potentially damaging the device.	A
VCC2	16	Short-Circuited to Ground (Side-2)	The device has no power on side-2 (the supply input is shorted to ground). The output of OUTD is at the default logic state. The output states of OUTA, OUTB, and OUTC are undetermined. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, damage to the device is possible. This short circuit potentially causes high current to flow between the two GND2 pins (pin9 and pin15); potentially damaging the device.	A
VCC2	16	Open-Circuited	The device has no power on side-2 (the supply input is open). The output of OUTD is at the default logic state. The output states of OUTA, OUTB, and OUTC are undetermined. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, damage to the device is possible.	A
VCC2	16	Short-Circuited to Pin1 (N/A)	Not applicable (N/A), corner pin.	N/A
VCC2	16	Short-Circuited to Supply (Side-2)	The device continues to function as expected. Normal operation.	D

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2025	*	Initial Release

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025