Functional Safety Information

TPS2HC16-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for TPS2HC16-Q1 (VAH (QFN, 11) package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

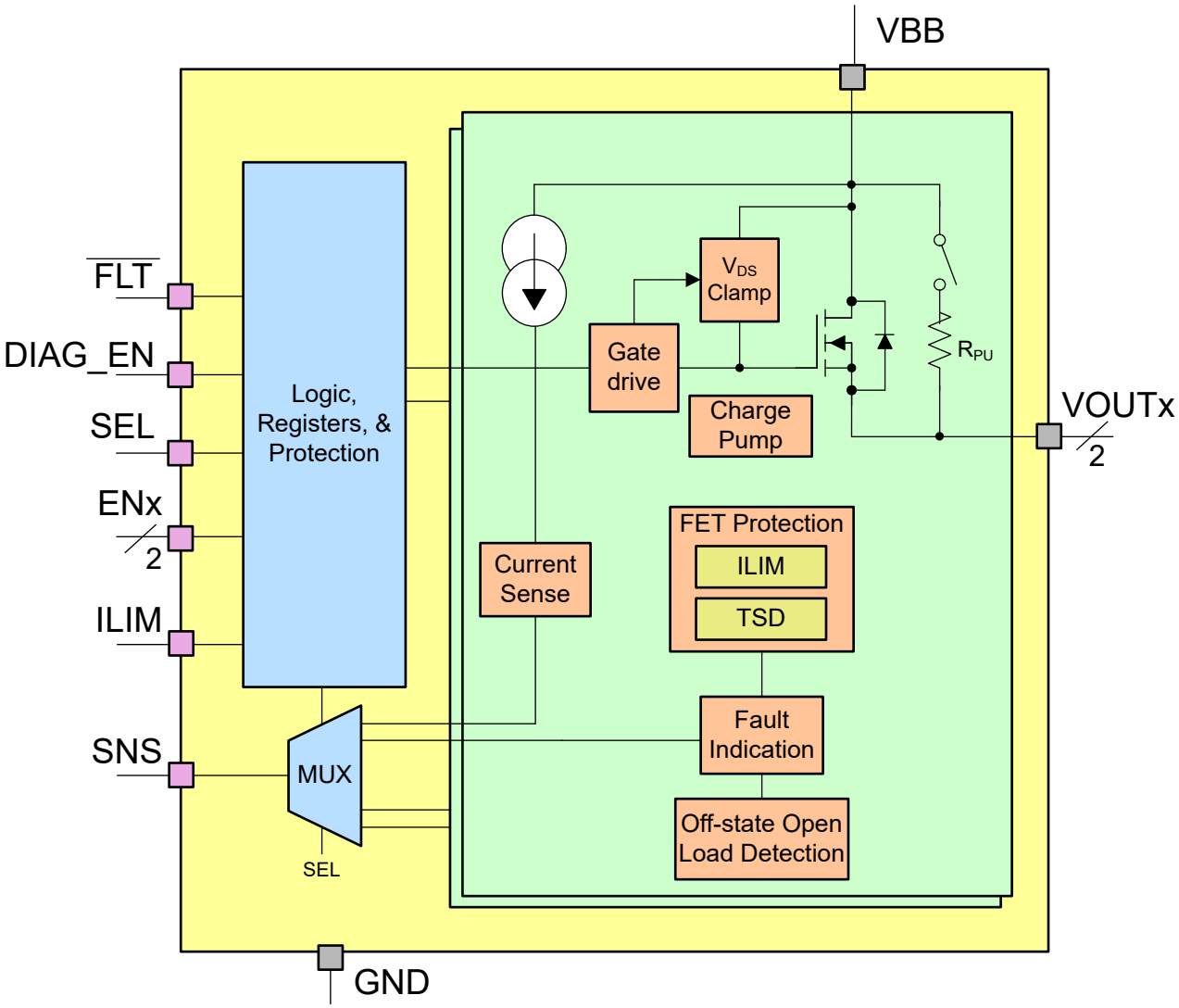

Figure 1-1. Functional Block Diagram

The TPS2HC16-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for TPS2HC16-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	13
Die FIT rate	7
Package FIT rate	6

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 750mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS2HC16-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUTx open (Hi-Z)	20
VOUTx stuck ON to VBB	10
VOUTx functional – not in specification voltage or timing	50
Diagnostics not in specification	10
Protection function fails to trip	10

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS2HC16-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VBB supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TPS2HC16-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS2HC16-Q1 datasheet.

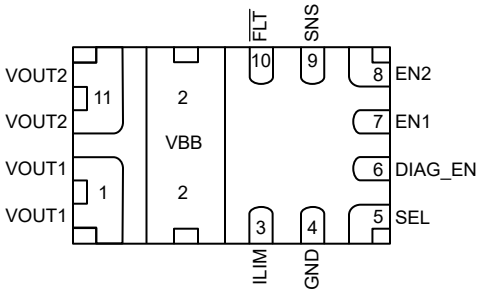

Figure 4-1. Pin Diagram for VAH (QFN, 11)

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device pins are connected per the recommendation in the datasheet, including pullup and pulldown resistors, as needed.
- The datasheet recommendations for operating conditions, external component selection, and PCB layout are followed.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VOUT1	1	The current limit of the device engages, and thermal protection turns off the FET of CH1.	B
VBB	2	The output stages are not powered, and the FET of both channels do not turn ON.	B
ILIM	3	The current limit is set at a maximum level, as per the data sheet.	C
GND	4	Any GND network, connected for protection, is bypassed.	B
SEL	5	The reported SNS current or fault status on the SNS pin is always of CH1 when the DIAG_EN pin is high.	B
DIAG_EN	6	The diagnostic features do not function, including current sense and fault reporting.	B
EN1	7	The FET of CH1 is turned off and an erroneous open-load fault reports for no-load conditions when the DIAG_EN pin is high.	B

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
EN2	8	The FET of CH2 is turned off and an erroneous open-load fault reports for no-load conditions when the DIAG_EN pin is high.	B
SNS	9	The reported SNS current or fault status on the SNS pin is erroneous.	B
$\overline{FLT}$	10	The reported fault status is potentially erroneous.	B
VOUT2	11	The current limit of the device engages, and thermal protection turns off the FET of CH2.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VOUT1	1	During the ON state of the device, CH1 is disconnected. During the OFF state of the device, if the DIAG_EN pin is high, an open-load fault reports.	B
VBB	2	The device is not powered and both the channels are kept OFF.	B
ILIM	3	The current limit is set at a minimum level, as per the data sheet.	C
GND	4	The loss of ground detection engages, and the device turns OFF.	B
SEL	5	The reported SNS current or fault status on the SNS pin is always of CH1 when the DIAG_EN pin is high. (internal pulldown).	B
DIAG_EN	6	The diagnostic features do not function, including current sense and fault reporting. (internal pulldown).	B
EN1	7	The FET of CH1 is turned off and an erroneous open-load fault reports for no-load conditions when the DIAG_EN pin is high (internal pulldown).	B
EN2	8	The FET of CH2 is turned off and an erroneous open-load fault reports for no-load conditions when the DIAG_EN pin is high (internal pulldown).	B
SNS	9	The current sense and fault at the SNS pin is not reported.	B
$\overline{FLT}$	10	The fault condition is not reported.	B
VOUT2	11	During the ON state of the device, CH2 is disconnected. During the OFF state of the device, if the DIAG_EN pin is high, an open-load fault reports.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
VOUT1	1	VOUT2	Loss of individual channel control. The current sensing and fault reported on the SNS and $\overline{FLT}$ pins are potentially erroneous.	B
VBB	2	VOUT1	The output of CH1 is pulled to the supply voltage. A short-to-battery detection triggers during the OFF state if the DIAG_EN pin is high.	B
ILIM	3	VBB	There is a loss of the current limit setting based on the RLIM resistor.	C
GND	4	ILIM	The current limit is set at a maximum level, as per the data sheet.	C
SEL	5	GND	There is a loss of control of the SEL pin and the reported current or fault status of the SNS pin is always of CH1 when the DIAG_EN pin is high.	B
DIAG_EN	6	SEL	There is a loss of control of the DIAG_EN and SEL pins and the current and fault reporting of the SNS pin is erroneous.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
EN1	7	DIAG_EN	There is a loss of enable control of CH1 and open-load fault detection is erroneous for CH1 when the DIAG_EN pin is high.	B
EN2	8	EN1	There is a loss of enable control for both channels (CH1 and CH2) and an erroneous fault is potentially reported at the SNS and $\overline{\text{FLT}}$ pins when the DIAG_EN pin is high.	B
SNS	9	EN2	The reported SNS current or fault status on the SNS pin is erroneous and there is a loss of enable control for CH2.	B
$\overline{\text{FLT}}$	10	SNS	The reported fault status and voltage of the SNS pin is potentially erroneous.	B
VBB	2	$\overline{\text{FLT}}$	The reported fault status is potentially erroneous.	B
VOUT2	11	VBB	The output of CH2 is pulled to the supply voltage. A short-to-battery detection triggers during the OFF state if the DIAG_EN pin is high.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to VBB Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VOUT1	1	The output of CH1 is pulled to the supply voltage. A short-to-battery detection triggers during the OFF state if the DIAG_EN pin is high.	B
VBB	2	No effect.	D
ILIM	3	There is a loss of the current limit setting based on the RLIM resistor.	C
GND	4	The supply power is bypassed, and the device stays OFF.	B
SEL	5	There is a potential violation of the absolute maximum rating for the pin and a possible breakdown of the ESD cell.	A
DIAG_EN	6	There is a potential violation of the absolute maximum rating for the pin and a possible breakdown of the ESD cell.	A
EN1	7	There is a potential violation of the absolute maximum rating for the pin and a possible breakdown of the ESD cell.	A
EN2	8	There is a potential violation of the absolute maximum rating for the pin and a possible breakdown of the ESD cell.	A
SNS	9	There is a potential violation of the absolute maximum rating for the pin and a possible breakdown of the ESD cell.	A
$\overline{\text{FLT}}$	10	The reported fault status is potentially erroneous.	B
VOUT2	11	The output of CH2 is pulled to the supply voltage. A short-to-battery detection triggers during the OFF state if the DIAG_EN pin is high.	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2025	*	Initial Release

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